Document Title

A7201 Data Sheet

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	2007/7/19	
0.1	Modify specifications	2007/9/21	
0.2	Modify title and Logo	2007/10/5	
0.3	Add circuit description	2007/11/26	
0.4	Modify register setting	2008/2/27	
0.5	Modify ordering information	2008/11/4	
	Add top marking info., reflow profile, Carry tape & reel dimensions		

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1. General Description

A7201 is a highly integrated CMOS RF receiver for sub 1GHz ISM band (315/434/868/915MHz). It futures both FSK and ASK capability.
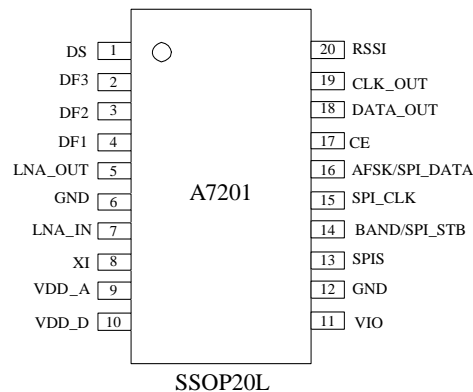
2. Typical Applications

- Remote Control.
- AMR (Auto Meter Reading).
- Security system.
- TPMS (Tire Pressure Measure System).

3. Features

- A7201A for 315/434MHz, A7201B for 868/ 915MHz.
- High sensitivity: -110dBm @ 434MHz band, IF bandwidth=100KHz.
- Very low current consumption: Typical 8.8mA
- Flexible control interface: Hardware pins or SPI.
- Support multi channels.
- High integration: VCO, PLL, LNA, Image Reject Mixer, IF Filter, Limiter, RSSI, Data Slicer, AFC, AGC…
- Very few external components: No need external filters (build in image reject mixer and IF channel filter).
- Build in image rejection mixer. Selectable IF band width (100, 200, 300 KHz).
- Wide operating range: VDD=2.2~3.3V (IO 2.0~4.2V). T=-40~+85/125℃.
- Auto ramp-up sequence control to optimize power consumption. Xtal→Auto Calibration→PLL→ RX.
- One receiver for different systems: Switching between ASK/FSK is possible.
- Auto calibration to compensate for process/temperature/voltage variation.
- Support typical 4/12/13.56/16MHz low cost crystal.

4. Pin Configuration

|				
DS	1		20	RSSI
DF3	2		19	CLK_OUT
DF2	3		18	DATA_OUT
DF1	4		17	CE
LNA_OUT	5	A7201	16	AFSK/SPI_DATA
GND	6		15	SPI_CLK
LNA_IN	7		14	BAND/SPI_STB
XI	8		13	SPIS
VDD_A	9		12	GND
VDD_D	10		11	VIO

SSOP20L

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Preliminary

5. Pin Description

Pin No.	Pin Name	Description
1	DS	Data slicer bypass. Connect a capacitor to GND
2	DF3	Data filter capacitors.
3	DF2	
4	DF1	
5	LNA_OUT	LNA output matching.
6	GND	Connect to PCB ground.
7	LNA_IN	LNA input matching.
8	XI	Crystal oscillator input.
9	VDD_A	Analog power input.
10	VDD_D	Digital power input.
11	VIO	Digital I/O voltage. For internal level shift VDD.
12	GND	Connect to PCB ground.
13	SPIS	SPI selection. Low→ disable SPI. Pin 14 will be configured as BAND and Pin 16 as AFSK. Pin 15 has to be tied to Low. High→ enable SPI. Pin 14 will be configured as SPI_STB and Pin 16 as SPI_DATA.
14	BAND	RF frequency band selection. Low→315MHz. High→ 434MHz.
	SPI_STB	SPI latch strobe.
15	SPI_CLK	SPI clock input. Tied to Low when SPIS is Low.
16	AFSK	Modulation selection. Low → FSK. High → ASK.
	SPI_DATA	SPI data input.
17	CE	Chip enable. Low→OFF mode. High→Active mode.
18	DATA_OUT	Received data output.
19	CLK_OUT	Clock output for micro controller. $F_{CLK\_OUT}=F_{xtal}/4$ or 16. Can be selected by SPI.
20	RSSI	Analog RSSI output. Connect a capacitor to GND.

Notes: Please refer to page 4 "**Circuit Description**" for detail definitions.

6. Block Diagram
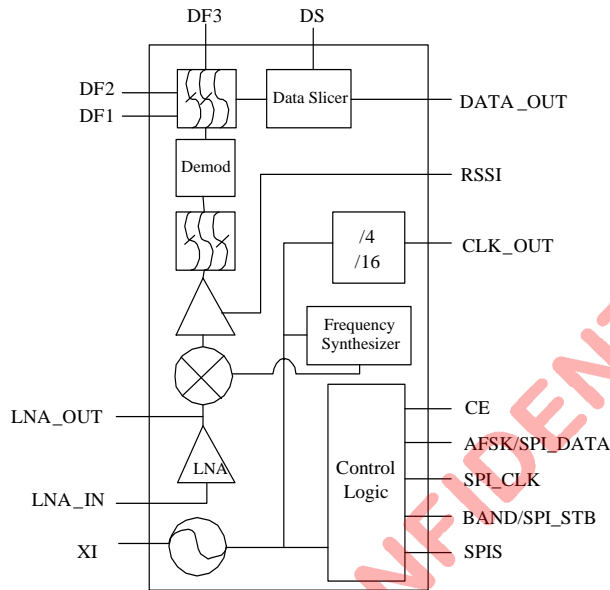
7. Specification

General Test Condition: Ta =25ºC, Fin=434MHz, VDD=3.0V, Crystal=13.56MHz

Parameter	Description		Min.	Typ.	Max.	Unit
General						
Operating temperature			-40		85/125	°C
Supply voltage	VDD_A, VDD_D		2.2	2.8	3.3	V
Current consumption	Sleep mode (all circuit off)		0.1	0.5		uA
	Rx mode			8.8		mA
Sensitivity	434MHz	FSK Bit rate=20K, Fdev=12KHz, BER<1E-3. IFBW=100KHz	-111	-109	-106	dBm
		ASK Bit rate=20K, BER<1E-3, IFBW=300KHz		-105	-102	
	314.8MHz	FSK Bit rate=20K, Fdev=12KHz, BER<1E-3. IFBW=100KHz		-108	-105	
		ASK Bit rate=20K, BER<1E-3, IFBW=300KHz		-105	-102	
	868.2MHz	FSK Bit rate=20K, Fdev=12KHz, BER<1E-3. IFBW=100KHz		-106	-103	
		ASK Bit rate=20K, BER<1E-3, IFBW=300KHz		-103	-101	
	915MHz	FSK Bit rate=20K, Fdev=12KHz, BER<1E-3. IFBW=100KHz		-105	-102	
		ASK Bit rate=20K, BER<1E-3, IFBW=300KHz		-102	-100	
IF bandwidth[1]	FSK	IFB[1:0]=[11]	90	100		KHz
		IFB[1:0]=[10]	135	150		

		IFB[1:0]=[0X]	180	200		
	ASK	IFB[1:0]=[11]	135	150		
		IFB[1:0]=[10]	225	250		
		IFB[1:0]=[0X]	315	350		
IF frequency	Reference frequency =13.56MHz			423.75		KHz
	Reference frequency =4/12/16MHz			400		
Max input	Enable AGC, ASK			-20		dBm
	Enable AGC, FSK			0		
Image rejection	434MHz			20		dB
RSSI	Dynamic range			85		dB
	Lower level			-120		dBm
	Upper level			-35		dBm
Outband blocking	+/- 1.5MHz			45		dBc
	+/- 2MHz			45		
	+/- 3MHz			50		
	+/- 10MHz			55		
	+/- 20MHz			60		

1) Different IF bandwidth setting results in different sensitivity. In general, better sensitivity can be obtained using narrower IF bandwidth, at the expense of tighter crystal tolerance.

8. Maximum Ratings

Characteristic	Pin name/symbol	Rating	Unit
Power supply voltage	All VDD	5.5	V
Input pin voltage		5	V
Storage temperature range	T_{stg}	-55~150	°C

9. Circuit Description

   The A7201 is a highly integrated ASK/FSK receiver featuring very low power consumption, flexible user interface and compact SSOP20 package. A built-in control sequence automatically brings A7201 into operation after a few settings, making this chip easy to use and power saving.

   The receiving part features a low-IF architecture with high receiving sensitivity and few external components. The received signal is amplified and down-converted to the intermediate frequency. Signal is demodulated by demodulator and then low pass filtered for the decision circuit. The output data can be accessed on the DATA_OUT pin.

9.1 Control Interface:

   A7201A (434/315MHz band) supports both SPI and hardware-pin controlled interface. A7201B (868/915MHz band) supports SPI only.

   9.1.1 Hardware-pin interface:

   For general-purpose 13.56MHz crystal-based applications, user can only set hardware pins to configure chip as Fig 9.1.1. In this mode, the receiver is in low-side band operation, auto gain control (AGC) is enabled, pin 19 CLK_OUT outputs crystal frequency/16, and IF bandwidth is max.
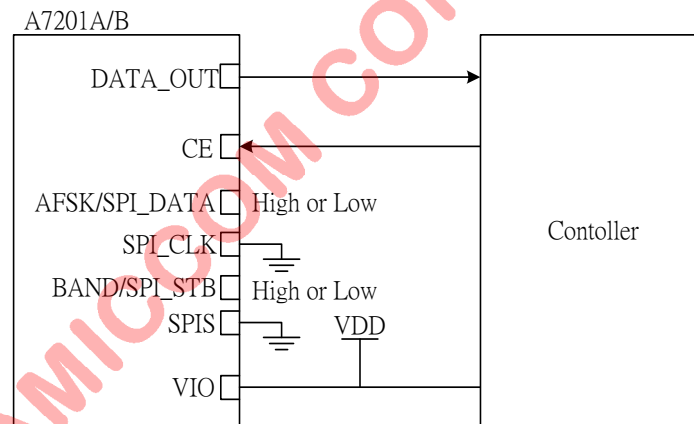

Fig 9.1.1

Pin No	Pin Name	Setting	Description
13	SPIS	0	Set to logic 0 to disable SPI
14	BAND/SPI_STB	0	RF band select to 315MHz band.
		1	RF band select to 434MHz band.
15	SPI_CLK	0	Set to logic 0 for normal operation.
16	AFSK/SPI_DATA	0	Active mode select to FSK
		1	Active mode select to ASK
17	CE	0	Chip will into OFF mode.

			1	Chip will into Active mode.

Table 9.1.1 Hardware pins setting

9.1.2 SPI interface:

 User can control this chip through SPI to get more flexible configuration, such as multi RF channel, 4/12/16MHz crystal, IF bandwidth… The total procedure only two steps:

Step 1: Write in RF and Crystal frequency to Register0.

Step 2: Write in Command (CEb, FASK, IFBW…) to Register1.
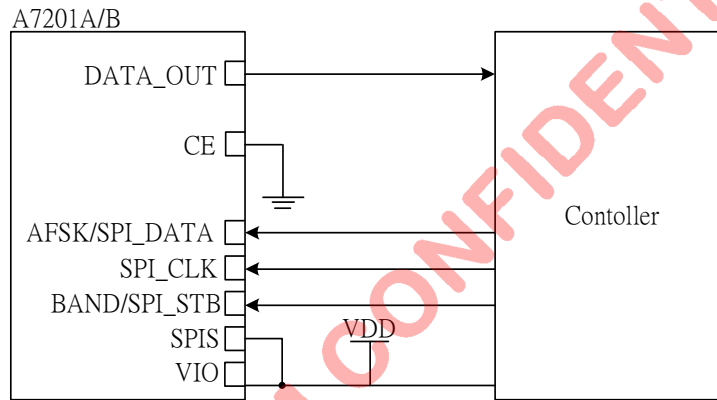
Please refer to section 9.2 SPI for full details.

Fig 9.1.2

9.2 SPI

9.2.1 Registers

Register 0

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	R1	R0	NB7	NB6	NB5	NB4	NB3	NB2	NB1	NB0	NA3	NA2	NA1	NA0	1	1
Reset	0	1	1	0	1	1	1	1	0	0	0	0	1	0		

← Write in direction (D0 first)

Note: (1) D[1:0] are address bits.
(2) All bits will be reset to default value after VIO powered on.
(3) Address D[1:0]=[10] is reserved for internal test. Do not use for normal operation.

Register 0: Used for RF/Crystal frequency setting. $F_{RF} = F_{crystal} \times N / 2R$,

  R[1:0]: Crystal reference frequency selection.

    [11]: R=5 for 4MHz crystal.

    [10]: R=15 for 12MHz crystal.

    [01]: R=16 for 13.56MHz crystal.

    [00]: R=20 for 16MHz crystal.

NB, NA: Binary format of PLL N counter. Used for RF frequency channel control.

For A7103A, N=(16XNB)+NA, NA=0~15; for A7103B, N=8X(NB+256)+NA, NA=0~7. Please refer to section 9.4 for detail calculation.

Note: Write in data (NA, NB) in 1's complement. For example, NA=15, NB=63.

Binary format NA=1111, NB=00111110.

Write in data should be 1's complement NA[3:0]=0000, NB[7:0]=11000001.

Register 1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	EAGC	TXP1	TXP0	ULS	CKS	ECK	X	IFB1	IFB0	BAND	FASK	CEb	RTX	CTLS	0	1
Reset	1	1	0	0	0	1	1	0	1	1	0	1	1	1		

Register 1: Used for comment and parameters setting.

EAGC: Auto gain control (AGC) selection. 0: enable AGC, 1: disable AGC.

TXP[1:0]: Set to default value for normal operation.

ULS: Receiver Up/Low side band selection. Used for TX/RX FDD application.

0: up side band .1:low side band.

CKS: Output clock (pin 19 CLK_OUT) divider ratio selection. 0: crystal frequency /4, 1: crystal frequency /16.

ECK: Output clock (pin 19 CLK_OUT) ON/OFF selection. 0: ON, 1: OFF.

X: Set to 1 for normal operation.

IFB[1:0]: IF filter band width selection.

[11]: Min bandwidth.

[10]: Medium bandwidth.

[0X]: Max bandwidth.

BANDb: RF band selection.

For A7201A, 0: 434MHz band. 1: 315MHz band.

For A7201B, 0: 915MHz band. 1: 868MHz band.

FASK: ASK_FSK selection. 0: ASK. 1: FSK.

CEb: Chip enable bar. 0: enable. 1: disable.

TRX: Set to 1 for normal operation.

CTLS: Control selection.

0: CE will be controlled by Register D4. IO pin 17 will be don't cared.

1: CE will be controlled by IO pin 17. Register1 D4 will be don't cared.

9.2.2 SPI timing

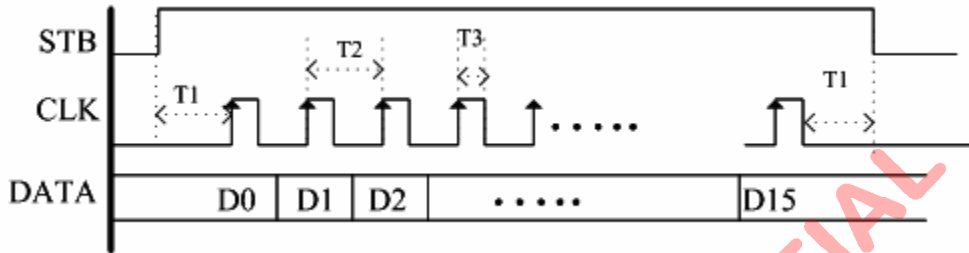After STB turns high, data can be written in at the rising edge of CLK.

Fig 9.2.2 SPI timing

Name	Description	Min	Unit
T1	STB go high to first CLK rising edge	200	
T2	CLK period	200	ns
T3	CLK high hold time	40	

9.3 Operation Modes

9.3.1 OFF Mode.

All circuits will be turned off in this mode.

Pin		Register 1		Operation Mode
13 SPIS	17 CE	D3 CTLS	D5 CEb	
0	0	X	X	OFF
1	0	1	X	
1	X	0	1	

Table 9.3.1 OFF mode setting

9.3.2 Active Mode.

The chip enters active mode from OFF mode as shown in Fig. 9.3.2.

SPI disabled. Set pin 13 SPIS =0. All register will be set to default values.

Pin	Operation Mode
17 CE	
0	OFF

	1			Active, RX

Table 9.3.2.1 Active mode setting by hardware pins

SPI enabled. Set pin 13 SPIS =1.

Pin	Register 1			Operation Mode
17 CE	D3 CTLS	D4 RTX	D5 CEb	
1	1	X		Active, RX
X	0	1	0	Active, RX

Table 9.3.2.2 Active mode setting by SPI
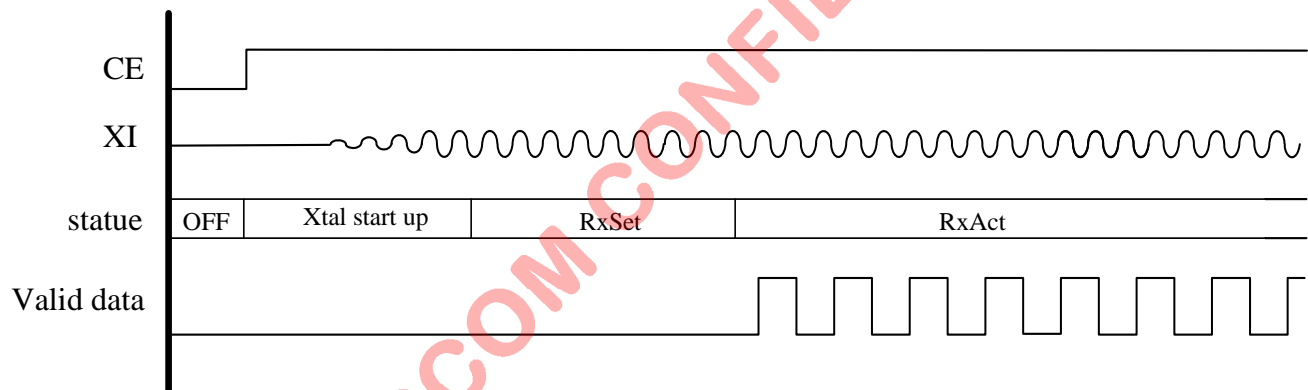
Fig 9.3.3 Start-up sequence

Name	Description	Time			Unit
		Mim	Typ	Max	
Xtal Start up[1]	From OFF to Xtal stable		0.8	1.2	ms
RxSet	From Xtal stable to Rx circuit ready		1	1.8	

Table 9.3.3.3 Timing description

9.3.4 Modulation and Band.

ASK/FSK modulation and 315/434MHz(A7201A), 868/915MHz(A7201B) frequency band can be set as following descriptions.

SPI disabled (pin 13 SPIS =0).

Pin		Operation Mode	Operation Mode
14 BAND/SPI_STB	16 AFSK/SPI_DATA	A7201A	A7201B

0	1	ASK, 315 band	ASK, 868 band
1	1	ASK, 434 band	ASK, 915 band
0	0	FSK, 315 band	FSK, 868 band
1	0	FSK, 434 band	FSK, 915 band

Table 9.3.4.1

SPI enabled (pin 13 SPIS =1).

Register 1		Operation Mode	Operation Mode
D6 BANDb	D5 FASK	A7201A	A7201B
1	0	ASK, 315 band	ASK, 868 band
0	0	ASK, 434 band	ASK, 915 band
1	1	FSK, 315 band	FSK, 868 band
0	1	FSK, 434 band	FSK, 915 band

Table 9.3.4.2

1) The stable time depends on the parallel capacitor (Ccomp) connected to XI, as shown in Fig 9.5.1. The time shown above assumes no parallel capacitor. For a 10pF capacitor, the stable time will be lengthened to 4ms typically.

9.4 RF and Reference Frequency Setting

A7201 support multi RF frequency and up to four crystal frequencies, which can be set by different approach.

9.4.1 SPI disabled (A7201A only): $F_{RF} = F_{crystal} \times N/32$, Recommended crystal frequency is around 13.56MHz.

	315MHz	434MHz
N	743	1023
F_{RF} (MHz)[1]	314.84625	433.49625

Table 9.4.1 RF channel frequency with SPI disabled

9.4.2 SPI be used: $F_{RF} = F_{crystal} \times N/(2XR)$, Recommend crystal can be 4[2]/12/13.56/16MHz.

R could be 5, 15, 16 or 20.

Used crystal	4MHz	12MHz	13.56MHz	16MHz
Recommended R value	5	15	16	20
SPI setting (R)	R[1:0]=[11]	R[1:0]=[10]	R[1:0]=[01]	R[1:0]=[00]

N could be 736~2319.

RF frequency band	315MHz	434MHz	868NHz	915MHz
Recommended N value	742~787	1022~1085	2171~2174	2256~2318
SPI setting (NA, NB)	N=(16XNB) + NA			

Table 9.4.2 RF channel frequency with SPI be enabled

For example:

  4MHz crystal, 434MHz BAND, set N=1084→ F_{RF}=4X1084/(2X5)=433.6MHz.

  12MHz crystal, 434MHz BAND, set N=1083→ F_{RF}=12X1083/(2X15)=433.2MHz.

  13.56MHz crystal, 315MHz BAND, set N=743→ F_{RF} =13.56X743/(2X16)=314.846MHz.

  16MHz crystal, 915MHz BAND, set N=2260→ F_{RF} =16X2260/(2X20)=904MHz.

1) F_{RF} is given for crystal=13.560000MHz.

2) 4MHz crystal has to be applied externally.

9.5 Reference Frequency Requirement

9.5.1 Crystal oscillator
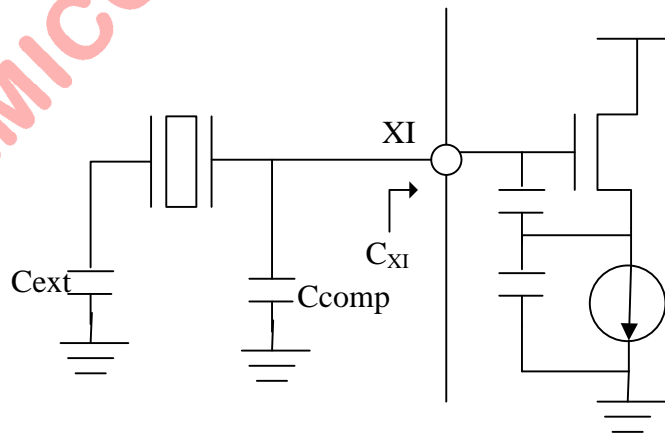
Fig 9.5.1

Crystal oscillator is Colpitts type oscillator with integrated feedback capacitors. Total input capacitance C_{XI} is about 10pF.

Cext is used to set the frequency align with transmitter for FSK application. It could be short to ground directly for ASK application.

Ccomp is an option used to compensate the load capacitance once the Cxi is too small for crystal default value.

9.5.2 Frequency tolerance

The crystal, RF, IF filter bandwidth and desired modulation signal bandwidth are all interrelated.

ΔRF_{TX} + ΔRF_{RX} < Min IF filter bandwidth – Max Signal bandwidth

ΔRF_{TX} is total RF frequency tolerant of transmitter. Usually equal to F_{RF} × TX crystal ppm.

ΔRF_{RX} is total RF frequency tolerant of receiver. Usually equal to F_{RF} × RX crystal ppm.

For example:

F_{RF}=433.496MHz. ΔRF_{TX}= 150KHz (+/- 75KHz). Max Signal bandwidth 50KHz (FSK data rate 20Kbps with deviation 12.5KHz). Max IF filter bandwidth=315KHz (ASK case).

Then ΔRF_{RX} < 315-50-150=115KHz. 115KHz/433.496MHz=265ppm (+/- 133ppm).

9.5.3 Sharing reference frequency with controller.

User can share RF and controller IC with one crystal as following two configurations. Reference clock can from RF side (divided by 4 or 16) to drive controller directly. Or from controller side send to RF through an AC coupled capacitor.
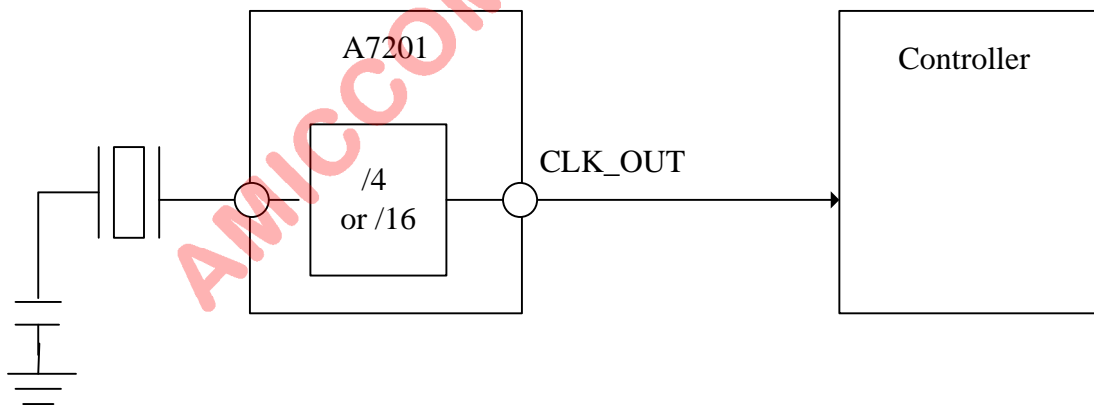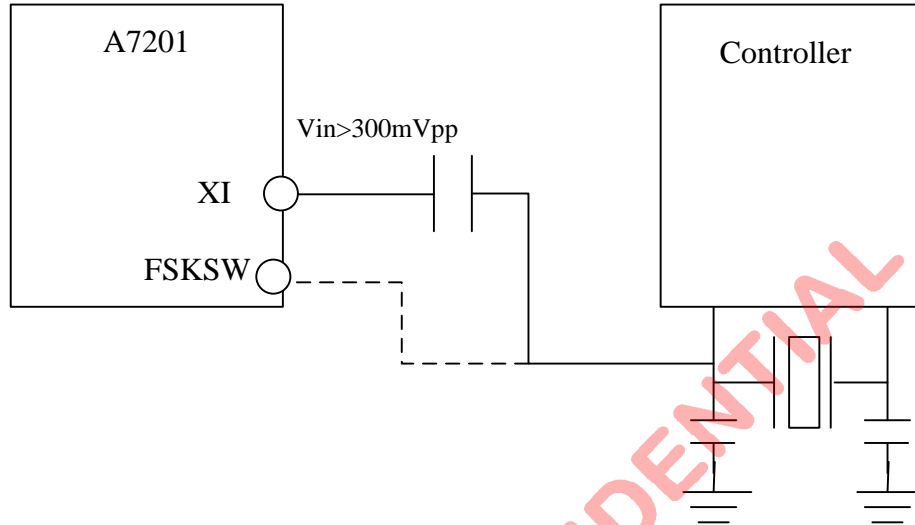

Fig 9.5.3.1 Crystal in RF side.

Fig 9.5.3.2 Crystal in controller side.

9.6 Data Filter

The data filter is composed of a second order multiple feedback low pass filter as shown in Fig 9.6. Two external capacitors can be adjusted for different data rates in order to obtain the best receiving sensitivity. Recommended component values are tabulated in Table 9.6 for 4.8, 9.6 and 20kbps application.
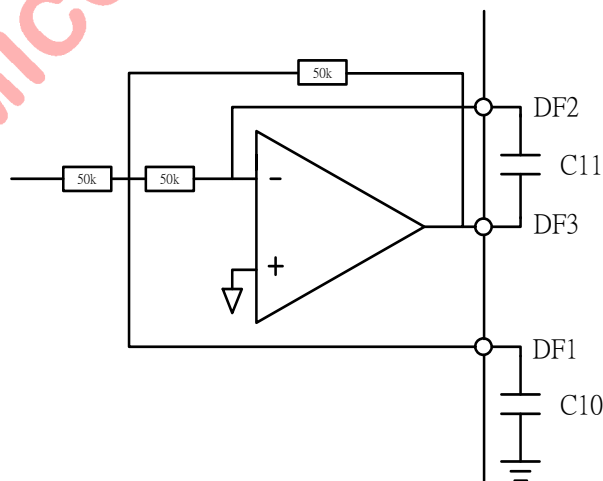

Fig 9.6

Data Rate (Kbps)	C10	C11
4.8	1nF	220pF
9.6	560pF	120pF
20	270pF	56pF

Table 9.6

Note: For other data rate, please contact AMICCOM's FAE for recommended values.

9.7 RSSI

Pin 20 is the analog RSSI output. The voltage is inverse proportional to the RF input power. The usable dynamic range is about -45 ~ -115 dBm. Due to AGC function action at RF input power about -70dBm, the curve exist a transition. Fig 9.7 show the typical curve of the RSSI for 433MHz RF input.
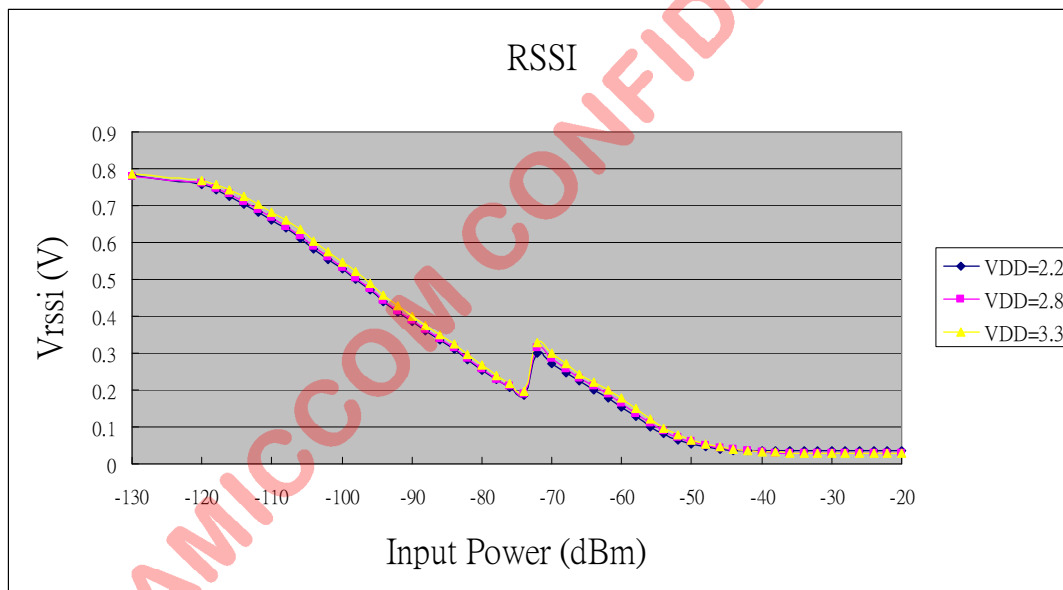
Fig 9.7 RSSI curve

9.8 Interference and Blocking

Build in image reject mixer and IF channel filters will provide better interference signal rejection without any external component needed. This will make system work stable even in the noisy ISM band environment. Three IF bandwidth can be selected for performance-cost optimization. Basically, narrower bandwidth can get better RX sensitivity and interference rejection. But need higher crystal accuracy.

As show in the Fig 9.8, over 45dBc rejection is available for interference frequency 1.5MHz away from signal. And over 60dBc rejection is available for interference 15MHz away.
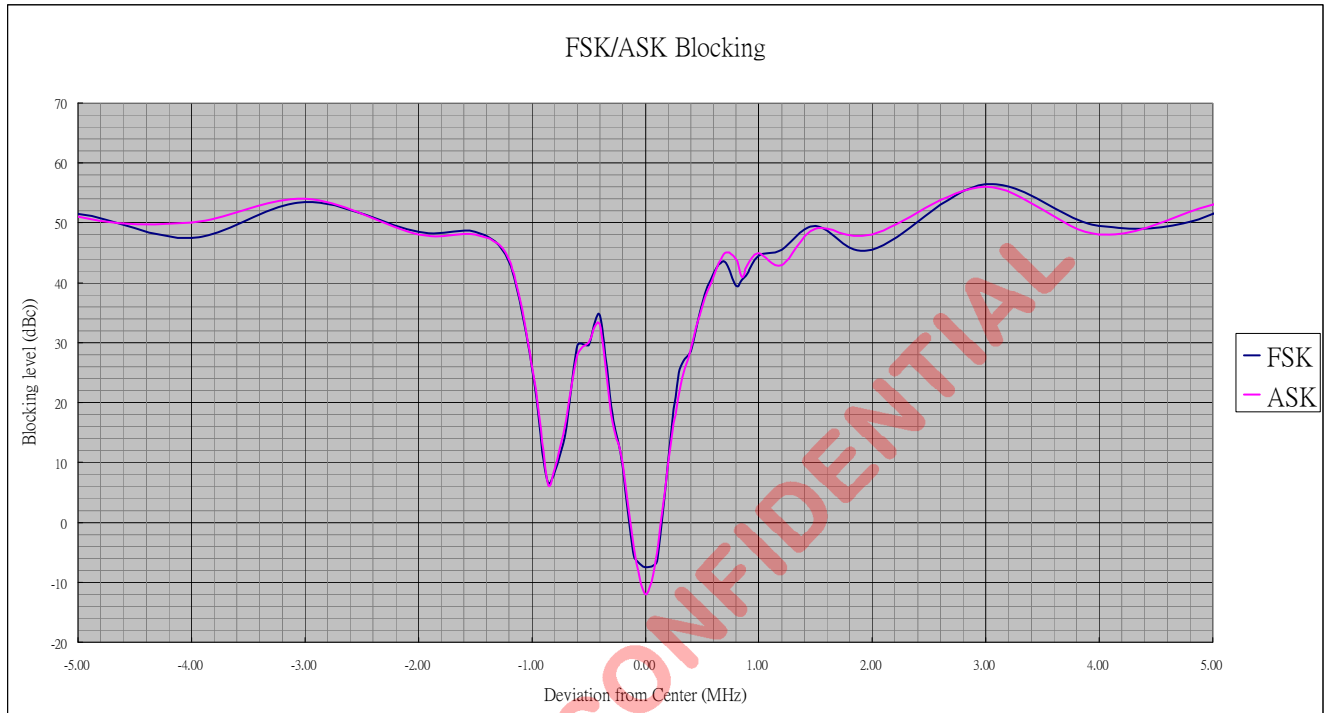
Fig 9.8 Blocking characteristics
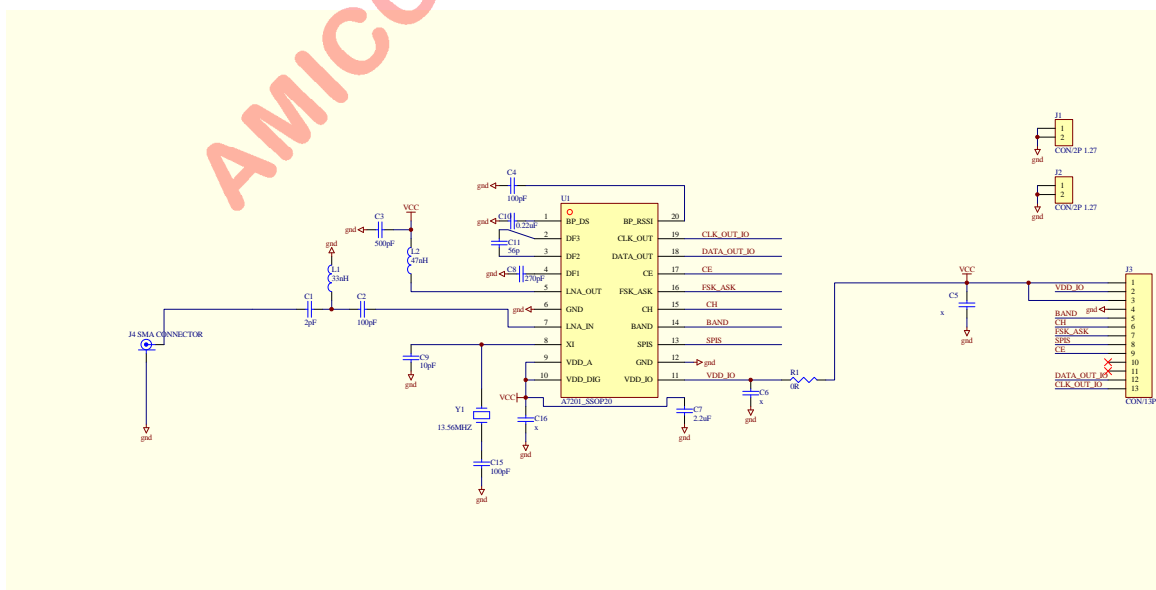
10. Application Circuit
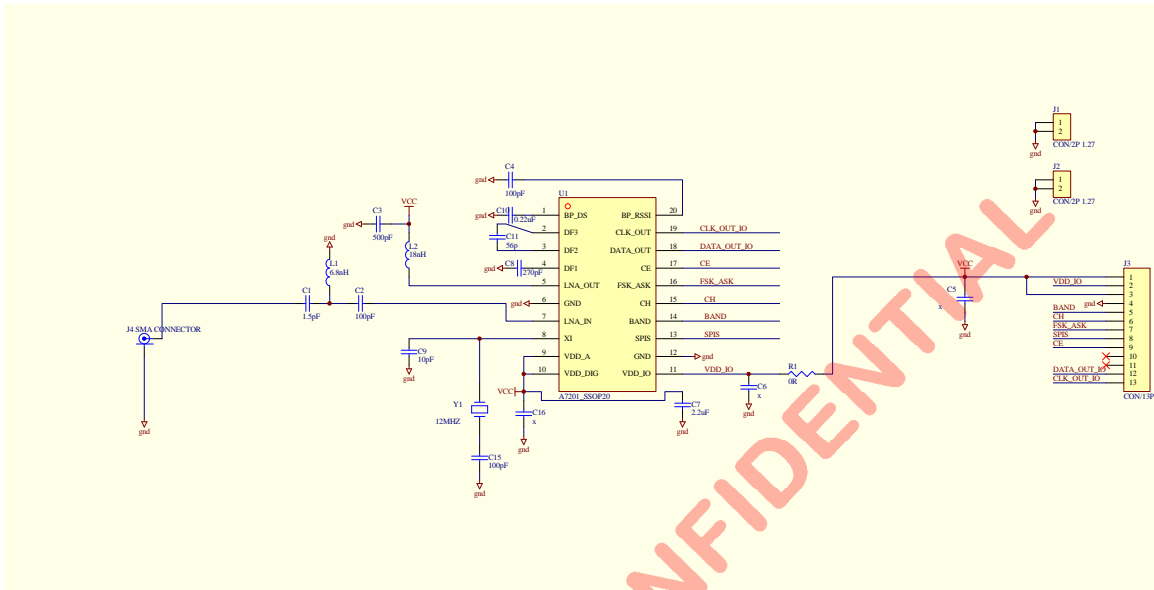

Fig 10.1 A7201A Application Circuit

Fig 10.2 A7201B Application Circuit

11. Ordering Information

Part No.	Package	Units Per Reel / Tube
A72C01AUF	SSOP 20L, Tube, Pb free, -40℃～85℃	56pcs
A72C01AUF/Q	SSOP 20L, Tape & Reel, Pb free, -40℃～85℃	3Kpcs
A72C01BUF	SSOP 20L, Tube, Pb free, -40℃～85℃	56pcs
A72C01BUF/Q	SSOP 20L, Tape & Reel, Pb free, -40℃～85℃	3Kpcs

12. Package Information

SSOP20 Outline Dimensions
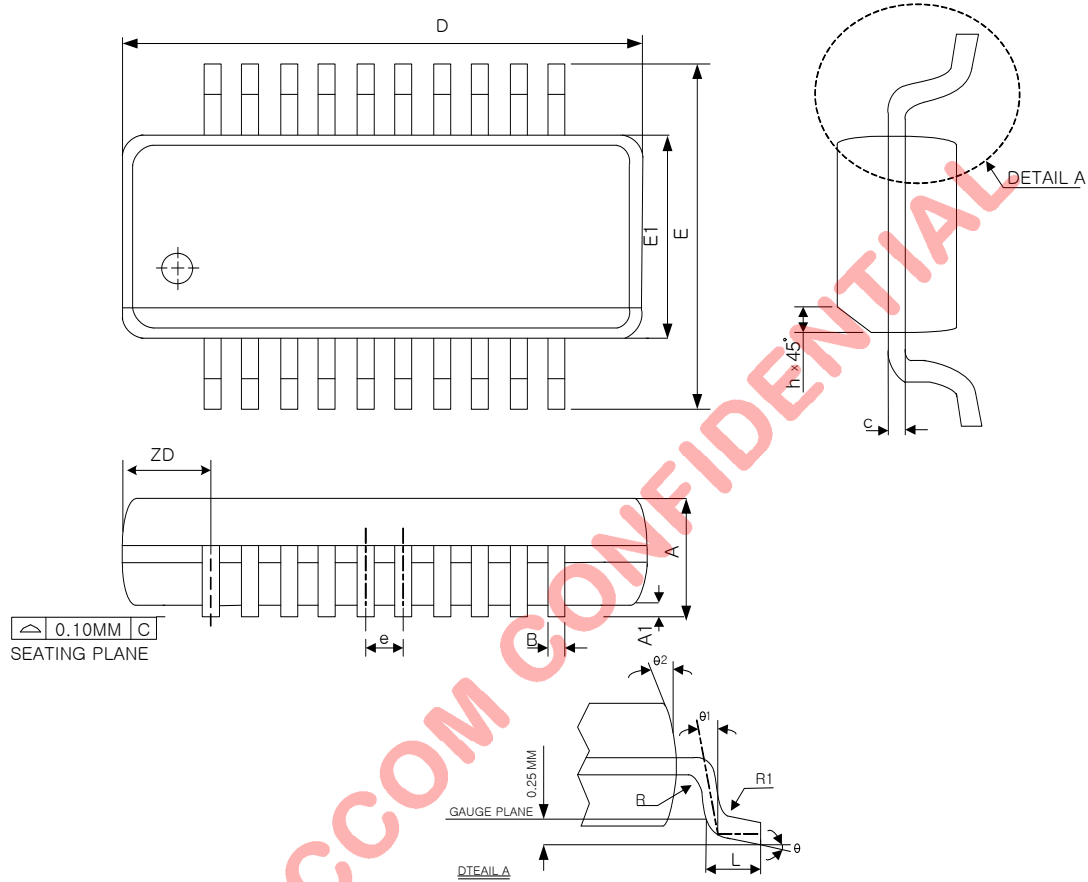
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NCM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	8.56	8.66	8.74	337	341	344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
ZD	1.4732 REF			0.058 REF.		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEOEC	M0-137 (AF)					

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13. Top Marking Information

A72C01AUF

- Part No.   : **A72C01AUF**
- Pin Count   : **20**
- Package Type : **QSOP**
- Dimension   : **150mil**
- Mark Method   : **Ink**
- Character Type : **Arial**
- Remark   : **Pb Free Type**

❖ CHARACTER SIZE : (Unit in mm)

A : 0.55
B : 0.36
C : 0.25
D : 0.03

I=J
K=L
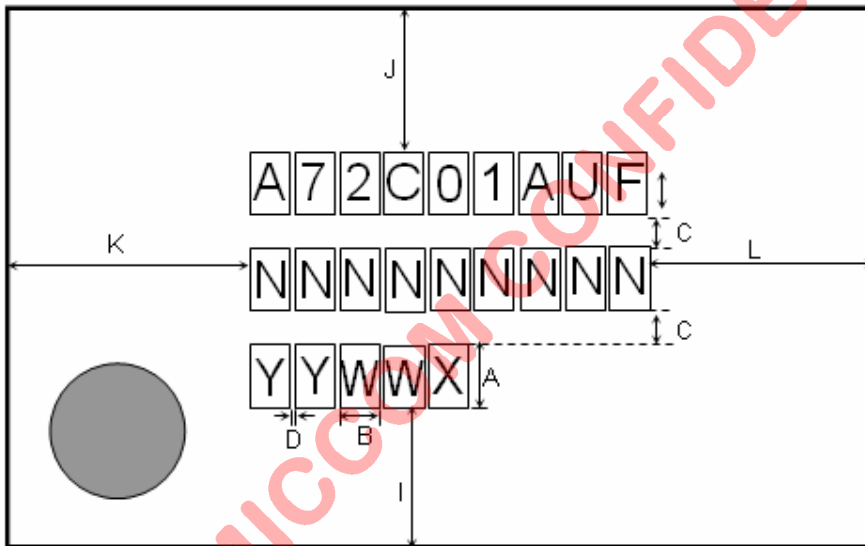
YYWW	: DATECODE
X	: PKG HOUSE ID
NNNNNNNNN	: LOT NO. (max. 9 characters)

A72C01BUF

- ■ Part No.   : **A72C01BUF**
- ■ Pin Count   : **20**
- ■ Package Type   : **QSOP**
- ■ Dimension   : **150mil**
- ■ Mark Method   : **Ink**
- ■ Character Type : **Arial**
- ■ Remark   : **Pb Free Type**

❖ CHARACTER SIZE : (Unit in mm)
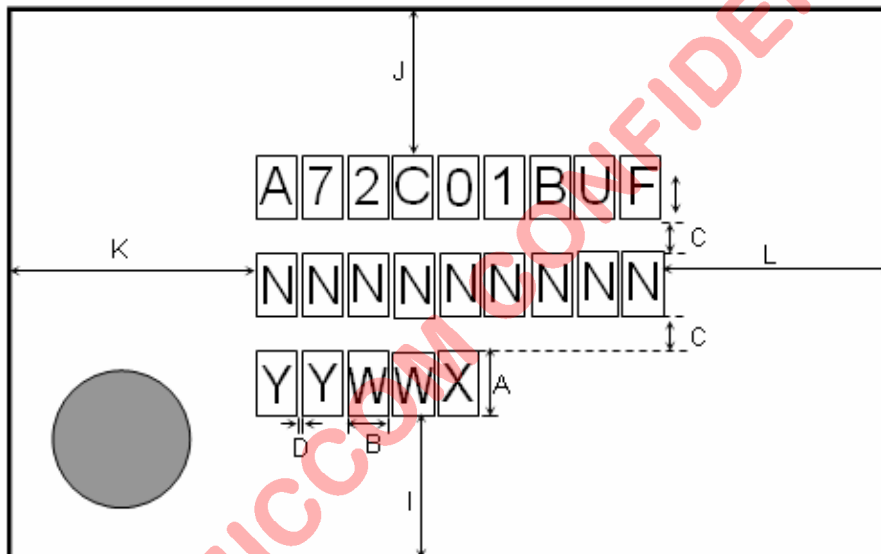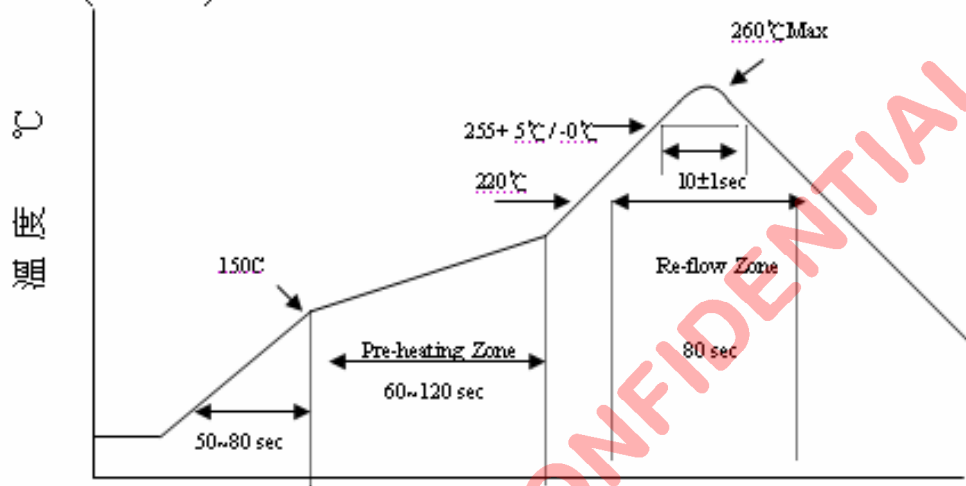
A : 0.55
B : 0.36
C : 0.25
D : 0.03

I=J
K=L

Y Y W W	: DATECODE
X	: PKG HOUSE ID
N N N N N N N N N	: LOT NO. (max. 9 characters)

14. Reflow Profile

LEAD FREE (GREEN) PROFILE :

15. Tape Reel Information

Cover / Carrier Tape Dimension
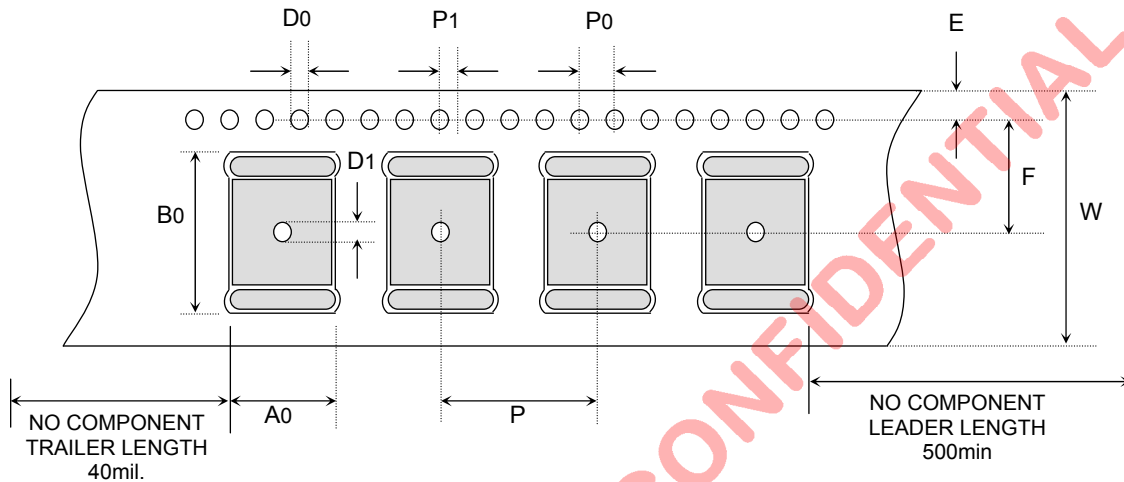
11 EA IC   **60cm±4cm**

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W
20 QFN 4*4	8	4.35	4.35	4.0	2.0	1.5	1.5	1.75	5.5	12
24 QFN 4*4	8	4.4	4.4	4.0	2.0	1.5	1.5	1.75	5.5	12
32 QFN 5*5	8	5.25	5.25	4.0	2.0	1.5	1.5	1.75	5.5	12
48 QFN 7*7	12	7.25	7.25	4.0	2.0	1.5	1.5	1.75	7.5	16
DFN-10	4	3.2	3.2	4.0	2.0	1.5	-	1.75	1.9	8
20 SSOP	12	8.2	7.5	4.0	2.0	1.5	1.5	1.75	7.5	16
24 SSOP	12	8.2	8.8	4.0	2.0	1.5	1.5	1.75	7.5	16
28 SSOP (150mil)	8	6	10	4.0	2.0	1.5	1.5	1.75	7.5	16
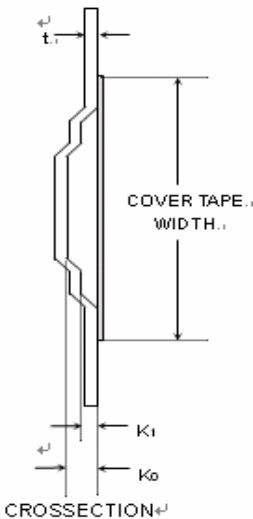
TYPE	K0	K1	t
20 QFN (4X4)	1.1	-	0.3
24 QFN (4X4)	1.4	-	0.3
32 QFN (5X5)	1.1	-	0.3
48 QFN (7X7)	1.1	-	0.3
DFN-10	0.75	-	0.25
20 SSOP	2.5	-	0.3
24 SSOP	2.1	-	0.3
28 SSOP (150mil)	2.5	-	0.3

COVER TAPE WIDTH
9.2
9.2
9.2
13.3
8
13.3
13.3
12.5

Unit : mm

REEL DIMENSIONS

UNIT IN mm

TYPE	G	N	T	M	D	K	L	R
20 QFN(4X4) 24 QFN(4X4) 32 QFN(5X5) DFN-10	12.8+0.6/-0.4	100 REF	18.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330＋0.00/-1.0	20.2
48 QFN(7X7)	16.8+0.6/-0.4	100 REF	22.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330＋0.00/-1.0	20.2
28 SSOP (150mil)	20.4+0.6/-0.4	100 REF	25(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330＋0.00/-1.0	20.2
20 SSOP 24 SSOP	16.4+2.0/-0.0	100 REF	22.4(MAX)	1.75±0.25	13.0+0.2/-0.2	1.9±0.4	330＋0.00/-1.0	20.2