DESCRIPTION

The A7220 is a current mode synchronous buck converter, and has a proprietary W-mode™® Gm curvature circuit that enables fast transient response, enables the device to adopt to both low ESR output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The A7220 operates from 4.3V to 18V V_{IN} input, and the output voltage can be programmed between 0.918V to 14V with 2A output current, and +/-1.5% high accuracy output voltage.

Due to 95mΩ (High side) and 90mΩ (Low side) integrated FETs, the A7220 works in high efficiency (up to 94% @12V Input, 3.3V output)

The A7220 is available in SOP8 Package.

ORDERING INFORMATION

Package Type	Part Number	
SOP8	M	A7220M8R
		A7220M8VR
Note	R: Tape & Reel V: Halogen free Package	
AiT provides all RoHS products Suffix " V " means Halogen free Package		

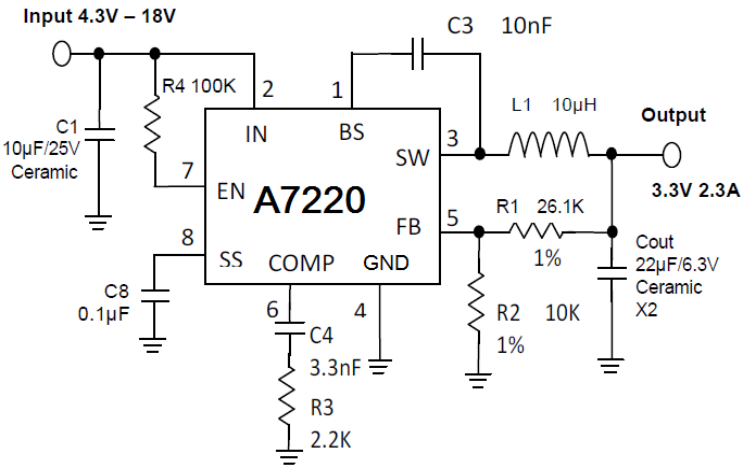
FEATURES

- 2A Output Current
- High Efficient Integrated FETs Optimized for portable application:
  95mΩ (High side) and 90mΩ (Low side)
- High Efficiency
  Up to 95% Efficiency @ 5V Input, 3.3V Output
  Up to 93% Efficiency @ 12V Input, 3.3V Output
- Wide Input Voltage Range: 4.3V to 18V @ 2A loading
- Wide Output Voltage Range: 0.918V to 14V @2A loading (32W output @max)
- Low Output Ripple and Allows Ceramic Output Capacitor
- Thermal Shutdown Protection
- 340KHz Switching Frequency(fsw)
- Cycle By Cycle Over Current Limit
- +/-1.5% High Accuracy Feedback Voltage
- Available in SOP8 and package

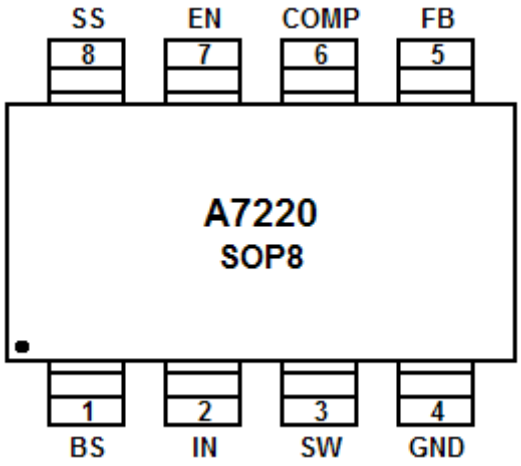
APPLICATION

- Wide Range of Applications for Low Voltage System
- Digital TV Power Supply
- High Definition Blu-ray Disc Players
- Networking Home Terminal
- Digital STB
- Ideal for Portable Applications

TYPICAL APPLICATION



PIN DESCRIPTION



Top View

Pin #	Symbol	Function
1	BS	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to SW pin. An internal PN diode is connected between V_{REG} to BS pin.
2	IN	Power input and connected to high side NFET drain
3	SW	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparators.
4	GND	Signal ground pin, also serve as ground returns for low-side NFET.
5	FB	Converter feedback input. Connect with feedback resistor divider.
6	COMP	Compensation Node. Used to compensate control loop. Connect a series RC network from COMP to G. In some cases, an additional capacitor is required
7	EN	Enable control input
8	SS	Soft-start control. A external capacitor should be connected to GND.

ABSOLUTE MAXIMUM RATINGS

IN	Voltage Range	-0.3V to 20V
BS		-0.3V to 25V
SW		-2V to 20V
SW (10 ns transient)		-2.5V to 21V
FB,SS,COMP		-0.3V to 5.5V
EN		-0.3V to 8V
T_J, Operation Junction		-40℃ to +150℃
T_{STG}, Storage temperature		-55℃ to +150℃

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range(unless otherwise noted) V_{IN}=12V, T_A=25℃

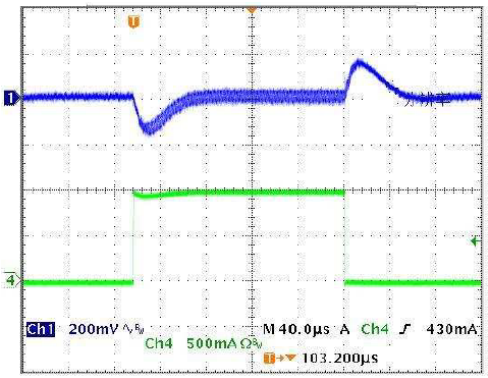
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Operating-non-switching supply current	I_{IN}	V_{IN} current, T_A=25℃, EN=1.8V,V_{FB}=1.0V	-	1.3	2.0	mA
Shut Down Supply Current	ISDN	V_{EN}=0V	-	2	4	μA
Feedback Voltage	V_{FB}	4.3V ≤V_{IN}≤18V	0.900	0.913	0.926	V
Feedback Overvoltage Threshold	OVP		-	1.1	-	V
Error Amplifier Voltage Gain	Aea		-	1000	-	V/V
Error Amplifier Transconductance	Gea	ΔIC=+/-10μA	-	900	-	μA/V
High Side Switch ON Resistance	$R_{DS(on)}$_1		-	95	-	mΩ
Low Side Switch ON Resistance	$R_{DS(on)}$_2		-	90	-	mΩ
High Side Switch Leakage Current	$I_{LEAKGAE}$	V_{EN}=0V, V_{SW}=0V	-	-	10	μA
High Side Switch Current Limit	I_{LM_H}	Minimum Duty Cycle	2.8	3.5	-	A
Low Side Switch Current Limit	I_{LM_L}	From Drain to Source	-	1.0	-	A
COMP Voltage to Current Sense Transconductance	Gcs		-	3.5	-	A/V
Switching Frequency	Fsw_1		-	340	-	KHz
Short Circuit Switching Frequency	Fsw_2	V_{FB}=0V	-	100	-	KHz
Maximum Duty Cycle	Dmax	V_{FB}=1.0V	-	90	-	%
Minimum ON Time	T_{ON_min}			220	-	ns
EN Threshold Voltage	V_{EN}_1	V_{EN} Rising	1.1	1.5	2.0	V
EN Threshold voltage's Hysteresis	V_{Hys}_1		-	100	-	mV
EN Lockout Threshold Voltage	V_{EN}_2		1.8	2.0	2.2	V
EN Lockout Hysteresis	V_{Hys}_2		-	210	-	mV
Input Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	3.0	3.6	4.2	V

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input Under Voltage Lockout Threshold Hysteresis	V_{Hys_3}			600		mV
Soft-Start Current	I_{SS}	V_{SS}=0V	4.25	4.40	4.55	μA
Setting Feedback Voltage by Using Soft-Start Voltage	V_{FB-SS}	Only when V_{SS} < 0.85V by adding resistor on SS pin V_{SS}= I_{SS}*R_{SS}=4.4μA*R_{SS}		V_{SS}+30 mV		mV
Soft-Start Period	T_{SS}	C_{SS}=0.1μF		15		ms
Thermal Shutdown	TSD			160		℃

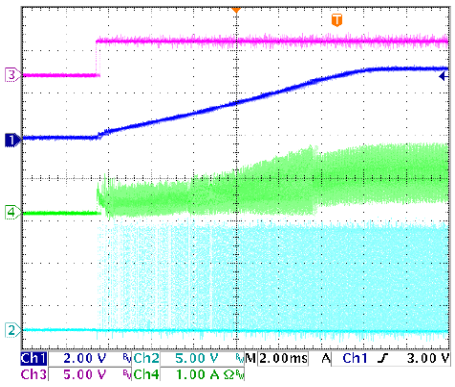
TEST CIRCUIT

V_{IN}=12V,V_{OUT}=3.3V, L=10μH, C_{IN}=10μF, C_{OUT}=22μF, T_A=+25℃

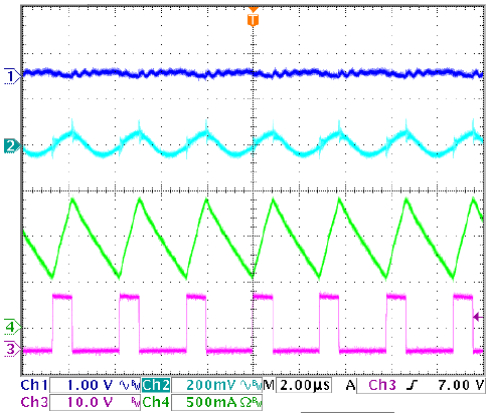
1. Fast Transient Response (20A/μs)



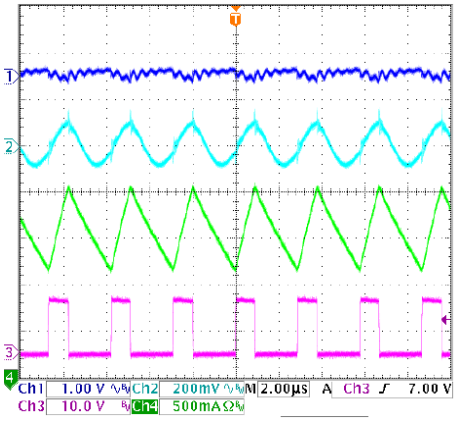
2. Startup through Enable



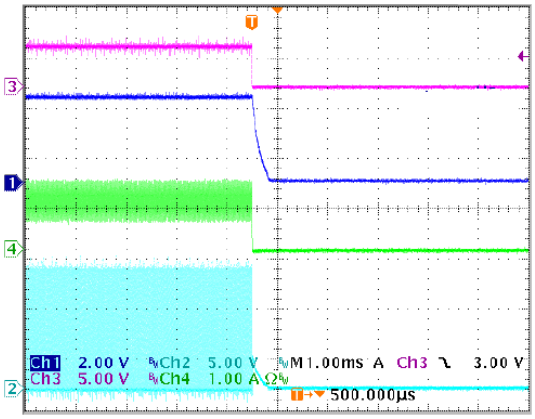
3. 1A Load Operation



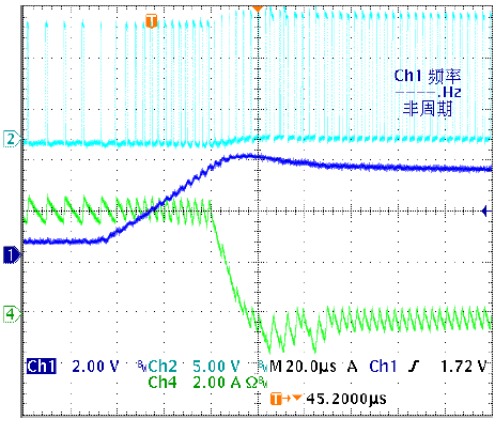
4. 2A Load Operation



5. Shutdown through Enable



6. Short Circuit Recovery



APPLICATION INFORMATION

APPLICATION SCHEMATIC (1)

With Electrolytic Capacitor

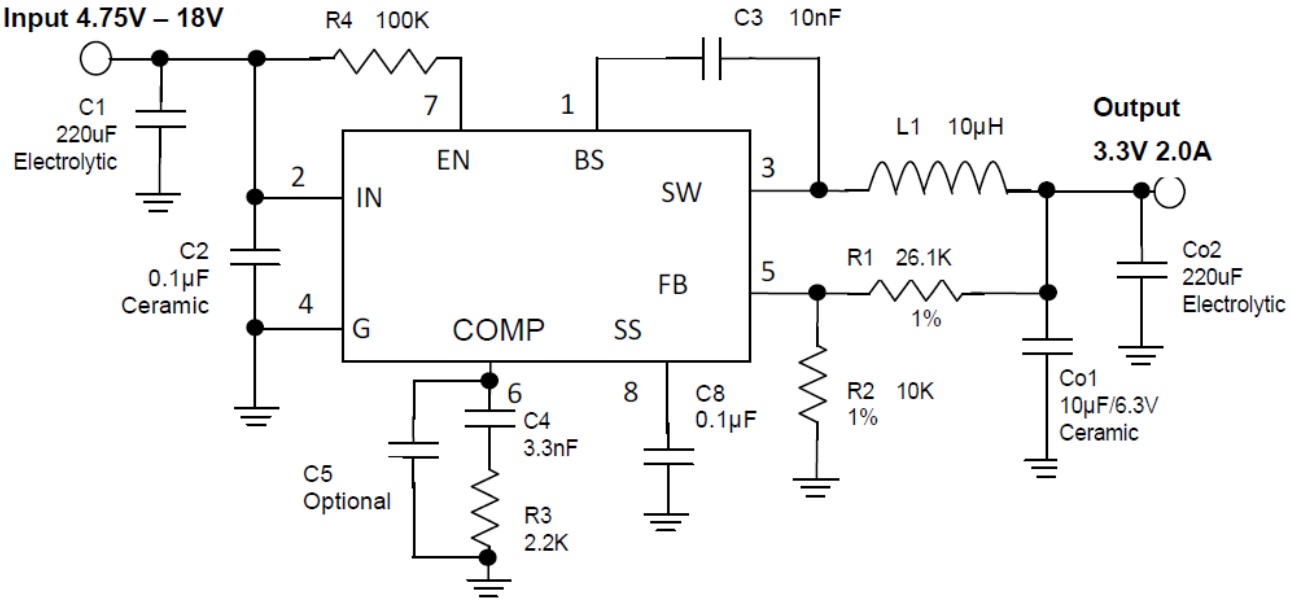


Figure 1

Compatible with main competitors without any external component change

RECOMMENDED COMPONENT SELECTION

V_{OUT}	C_{OUT}	R1	R2	R3(comp)	C4(comp)	C5(optional)	L(inductor)
1.0V	22Mf Ceramic X2	1.0K	10K	50Ω	10nF	OPEN	3.3µH
1.2V	22µF Ceramic X2	4.7K	15K	100Ω	10nF	OPEN	3.3µH
1.8V	22µF Ceramic X2	9.7K	10K	300Ω	3.3nF	OPEN	4.7µH
2.5V	22µF Ceramic X2	12.0K	6.8K	1.5KΩ	3.3nF	OPEN	6.8µH
3.3V	22µF Ceramic X2	26.1K	10K	2.2KΩ	3.3nF	OPEN	10µH
5.0V	22µF Ceramic X2	30.0K	6.8K	2.7KΩ	3.3nF	OPEN	22µH
1.0V	47µF SP Cap	1.0K	10K	50Ω	10nF	OPEN	3.3µH
1.2V	47µF SP Cap	4.7K	15K	100Ω	10nF	OPEN	3.3µH
1.8V	47µF SP Cap	9.7K	10K	300Ω	3.3nF	OPEN	4.7µH
2.5V	47µF SP Cap	12.0K	6.8K	1.5KΩ	3.3nF	OPEN	6.8µH
3.3V	47µF SP Cap	26.1K	10K	2.2KΩ	3.3nF	OPEN	10µH
5.0V	47µF SP Cap	30.0K	6.8K	2.7KΩ	3.3nF	OPEN	22µH

V_{OUT}	C_{OUT}	R1	R2	R3(comp)	C4(comp)	C5(optional)	L(inductor)
1.0V	470µF/6.3V/Electrolytic	1.0K	10K	50Ω	10nF	150pF	3.3µH
1.2V	470µF/6.3V/Electrolytic	4.7K	15K	100Ω	10nF	150pF	3.3µH
1.8V	470µF/6.3V/Electrolytic	9.7K	10K	300Ω	3.3nF	150pF	4.7µH
2.5V	470µF/6.3V/Electrolytic	12.0K	6.8K	1.5KΩ	3.3nF	150pF	6.8µH
3.3V	470µF/6.3V/Electrolytic	26.1K	10K	2.2KΩ	3.3nF	150pF	10µH
5.0V	470µF/10V/Electrolytic	30.0K	6.8K	2.7KΩ	3.3nF	150pF	22µH
12V	470µF/25V/Electrolytic	62.0K	5.1K	3.3KΩ	3.3nF	150pF	47µH

APPLICATION SCHEMATIC (2)

Fast Transient Response Without Electrolytic Capacitor

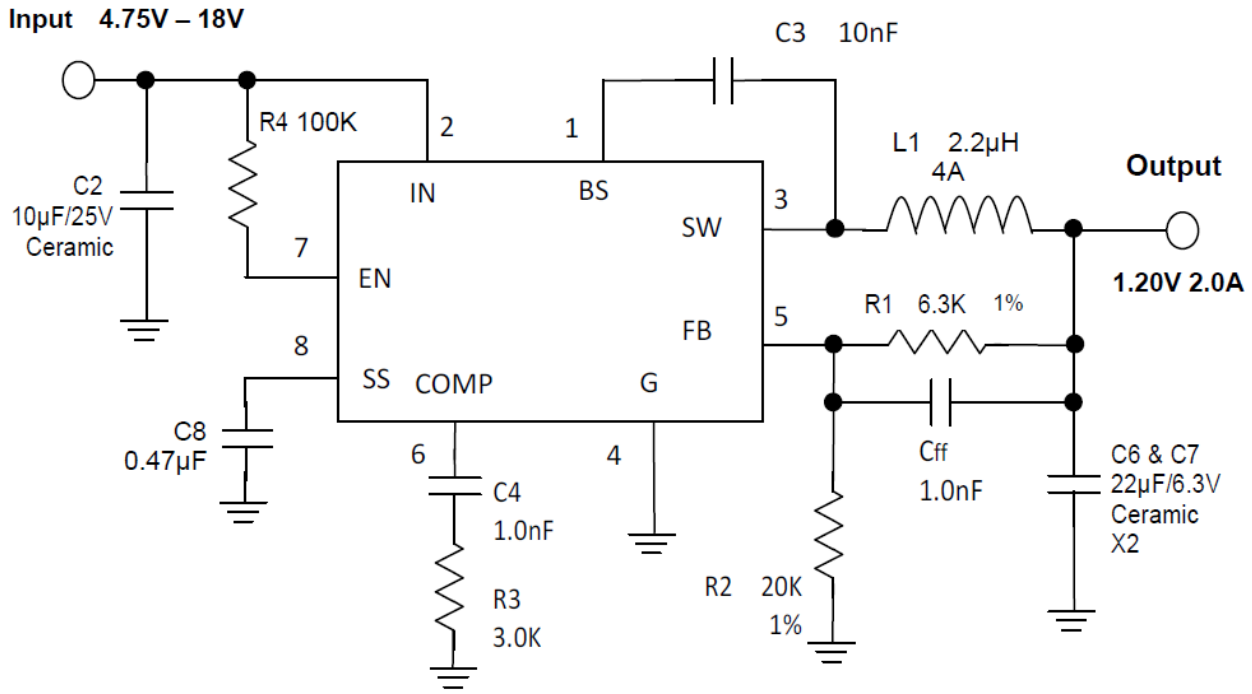


Figure 2

RECOMMENDED COMPONENT SELECTION

V_{OUT}	C_{OUT}	R1	R2	R3(comp)	C4(comp)	Cff	L(inductor)
1.0V	22μF Ceramic X2	2.0K	20K	3.0KΩ	1.0nF	2.2nF	2.2μH
1.2V	22μF Ceramic X2	6.3K	20K	3.0KΩ	1.0nF	1.0nF	2.2μH
1.8V	22μF Ceramic X2	19.4K	20K	3.0KΩ	1.0nF	680pF	3.3μH
2.5V	22μF Ceramic X2	34.5K	20K	3.0KΩ	1.0nF	680pF	4.7μH
3.3V	22μF Ceramic X2	52.2K	20K	3.0KΩ	1.0nF	680pF	6.8μH
5.0V	22μF Ceramic X2	89.5K	20K	3.0KΩ	1.0nF	390pF	22μH
1.0V	47μF SP Cap	2.0K	20K	3.0KΩ	1.0nF	2.2nF	2.2μH
1.2V	47μF SP Cap	6.3K	20K	3.0KΩ	1.0nF	1.0nF	2.2μH
1.8V	47μF SP Cap	19.4K	20K	3.0KΩ	1.0nF	680pF	3.3μH
2.5V	47μF SP Cap	34.5K	20K	3.0KΩ	1.0nF	680pF	4.7μH
3.3V	47μF SP Cap	52.2K	20K	3.0KΩ	1.0nF	680pF	6.8μH
5.0V	47μF SP Cap	89.5K	20K	3.0KΩ	1.0nF	390pF	22μH

APPLICATION NOTES

a) C2 ceramic capacitor as close as possible to the chip PIN2 and PIN4 placed;

b) When using 47 μH inductors, each switching and transmission of energy, the output of the need for greater capacitance, so that the large-signal. The feedback loop is stable. 47 μH inductor, the output is required with greater than or equal to 330 μF electrolytic capacitor for energy Bulk.

c) The current path is as short as possible and as far as possible with the chip in the same PCB level. Played the hole cross-layer connections to avoid the high current path.

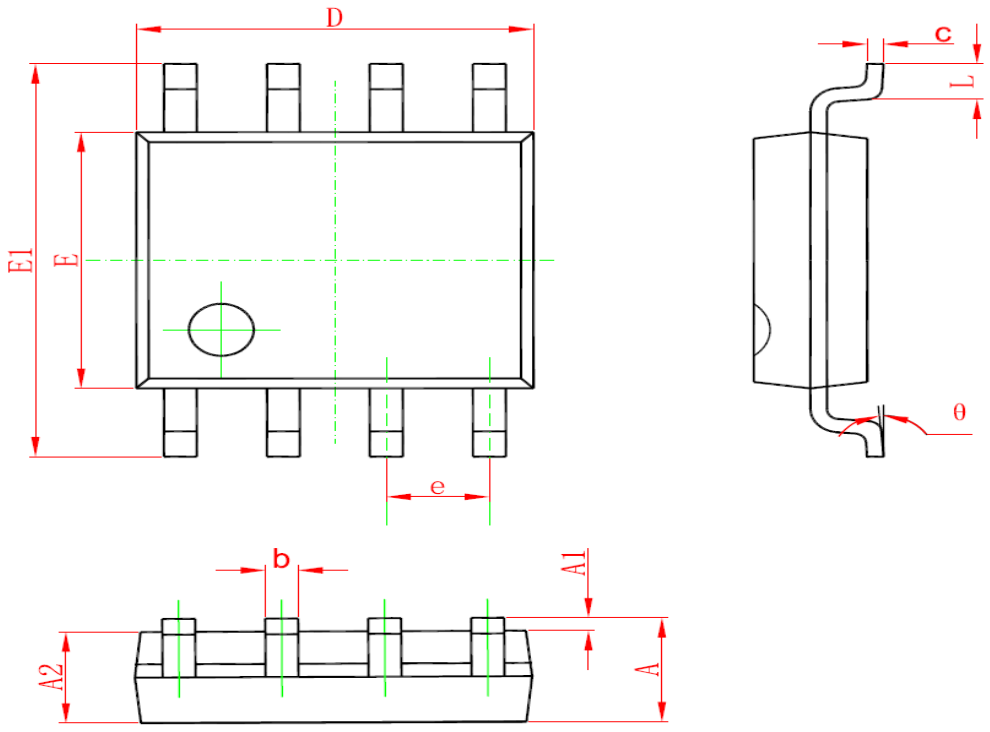
d) If feasible, cost and high efficiency design, should make full use of ceramic capacitors or smaller ESR (such as: 30mohm) electrolytic Capacity, efficiency can be effectively increased by 1%.

e) EN pin (pin 7) on the pull-up resistor is not less than 100KΩ.

f) If more than one chip share the same input capacitance of the need to adjust of 8 Jiaoruan starting capacitor capacitance value of time-delayed start of each chip to regulate avoid multiple chip start to impact on the power input capacitance. Delay Time: delay 15ms per 100nF capacitor.

PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)



Symbol	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	3.800	4.000
E1	5.800	6.200
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

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