Document Title

A7302D Data Sheet, 868MHz / 915MHz ASK Transmitter with 1~10Kbps data rate
868MHz / 915MHz FSK Transmitter with 1~20Kbps data rate

Revision History

Rev. No.	History	Issue Date	Remark
0.1	Initial issue Compared to A7302B No CKO function Seperated VDD_A and VDD_D ASK data rate 1K ~ 10Kbps FSK data rate 1K ~ 20Kbps	Oct., 2009	
1.0	Add application circuit by HW control mode	Oct., 2010	Full Production
1.1	Change English Company Name	Nov. 30, 2010	
1.2	Modify the tape reel information and the add Shenzhen office address.	Jul. 2011	
1.3	Add description of back side plate to well solder to ground in Ch7.	Oct. 2011	

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Table of Content

1. General Description

A7302D is a very **easy-to-use** CMOS RF transmitter for sub 1GHz license free ISM band (868/915MHz). It is a FSK/ASK single chip RF transmitter with 4-steps programmable power amplifier (max 6dBm @ 868MHz). This device integrates a fully VCO and integer-N PLL synthesizer. Hence, A7302D's carrier frequency F_{RF} is determined by the frequency of the reference crystal F_{XTAL}. The integer-N PLL synthesizer ensures that each RF value, ranging from 863 ~ 930 MHz, where $F_{RF} = F_{VCO} / 2$, with PLL steps of 847,5KHz (RF step = 423,75KHz when Xtal = 13,56MHz) or PLL steps of 800KHz (RF step = 400KHz when Xtal = 12MHz) , can be achieved. This is done by using a crystal as a reference frequency according to: $F_{RF} = F_{XTAL} \times N / R$, where N is the PLL feedback divider ratio and R is crystal divider to support 13,56MHz crystal.

A7302D supports FSK data rate from 1K to 20Kbps and ASK data rate from 1K to 10Kbps. In FSK modulation, this device's Fdev (frequency deviation) is controlled by crystal detuning of series an external capacitor (typical 150pF for ± 12,5KHz). In ASK modulation, this capacitor is not necessary.

For **easy-to-use**, A7302D has only two control registers, register 0 and 1. MCU can configure two registers via 3-wire SPI protocol. In addition to SPI control mode, A7302D has a special mode called **HW control mode**. In HW control mode, user just needs to apply pin setting. Then, radio control is done (register 0 and register 1 are in default values). No matter HW or SPI control mode, A7302D is very easy to use by a low cost MCU or encoder. Those features are all integrated in a small DFN 10 pins package.

For packet handling, there is no FIFO inside A7302D. Hence, MCU or Encoder just delivers the defined packet (preamble + sync word + payload) to TX_DATA pin for data transmitting.

2. Typical Applications

- Remote Control.
- Alarm and Security System.
- Smart Energy Management
- AMR (Auto Meter Reading)
- Wireless Toys.
- RKE (Remote Keyless Entry).
- Garage Door Opener.
- Home Automation.

3. Features

- Operating range: VDD=2,2~3,6V. T=-40~+85℃.
- Small DFN10 package.
- Easy to use
  - Support HW and 3-wire SPI control mode.
  - HW control mode (no need MCU for radio control, default max TX power).
  - Auto calibration.
  - Auto start-up sequence, Xtal→Auto Calibration→PLL→ TX.
- TX current 13mA (FSK, 6dBm) / 10mA (ASK, 6dBm, 50% duty cycle).
- Shut down mode current 0,1 uA.
- Two stages class-C PA, 4-steps programmable TX Power : -4 / 0 / 3 / 6 dBm.
- Fully integrated VCO, on chip loop filter and PLL synthesizer.
- RF range from 863 ~ 930MHz with RF steps where 423,75 KHz by 13,56MHz Xtal or 400KHz by 12MHz Xtal.
- Direct ASK modulation by switching PA.
- Direct FSK modulation (frequency deviation) by crystal detuning via external capacitor.
- Support low cost crystal (13,56718MHz or 12,0052MHz with ±50ppm tolerance).
- Very few external components: No need external IF/SAW filters.

4. Block Diagram

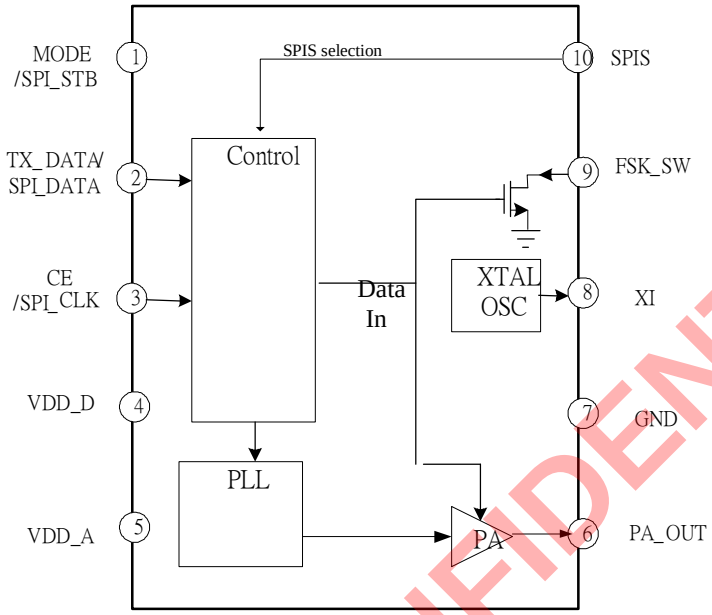


Fig 4 A7302D Block Diagram

5. Absolute Maximum Ratings

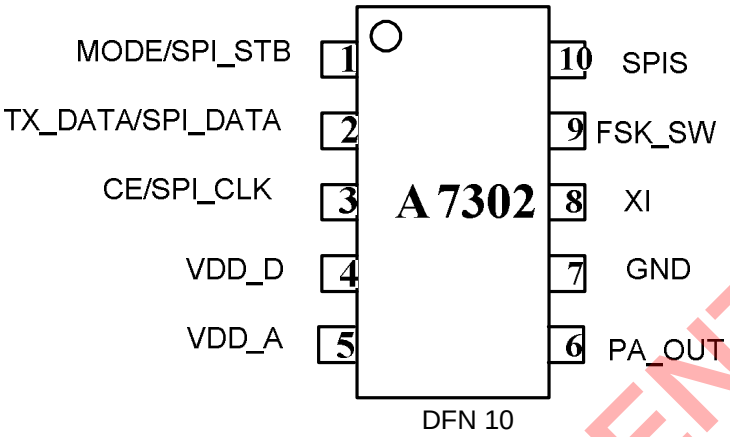
Characteristic	With respect to	Rating	Unit
Power supply voltage		-0.3~5	V
Input pin voltage		-0.3~5	V
Storage temperature range	T_{stg}	-55~150	°C
ESD Rating	HBM *	± 2K	V
	MM *	± 200	V

*Pin 6 (PA_OUT) is -2KV and -100V of HBM and MM respectively.

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device. HBM (Human Body Mode) is tested under MIL-STD-883G Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).

6. Pin Configuration



7. Pin Description

Pin No.	Pin Name	Description
1	MODE	HW control mode, mode selection. Connect to GND: 915MHz band, ASK mode. Connect 120KΩ to GND: 868MHz band, ASK mode. Connect 240KΩ to GND: 868MHz band, FSK mode. Connect to VDD: 915MHz band, FSK mode.
	SPI_STB	SPI control mode, SPI Strobe.
2	TX_DATA	HW control mode, Transmitted data input.
	SPI_DATA	SPI control mode, SPI_DATA input (SPI_STB=1) and TX_DATA input (SPI_STB = 0)
3	CE	HW control mode, Chip Enable, active high
	SPI_CLK	SPI control mode, SPI clock input
4	VDD_D	Digital power supply. (**Need low pass RC filter on this pin**.)
5	VDD_A	Analog power supply. (**Need low pass RC filter on this pin**.)
6	PA_OUT	Power Amplifier output.
7	GND	Ground.
8	XI	Crystal oscillator port (Refer to section 9.4 for Xtal spec)
9	FSK_SW	FSK deviation setting. Capacitor value determines the Freq. deviation.
10	SPIS	Control Mode selection. Low→ HW control mode (Use Pin 1 / 2 /3 to do radio control.) High→ SPI control mode.
	Back Side Plate	**Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

8. Specification

General Test Condition for A7302D: Ta = 25ºC, VDD=3.0V, Crystal=12,0052MHz, with matching network, PN9 pattern

Parameter	Description	Min.	Typ.	Max.	Unit
General					
Operating temperature		-40		85	°C
Supply voltage	ASK / FSK	2.2	3.0	3.6	V
Current consumption	Shut down mode (all circuit off)		0.1		uA
	TX mode (FSK, 6dBm), TXP = 00		13		mA
	TX mode (ASK, 6dBm, 50 % duty cycle)		10		
	TX mode (FSK, 3dBm), TXP = 01		10.5		
	TX mode (FSK, 0dBm), TXP = 10		9.5		
	TX mode (FSK, -4dBm), TXP = 11		8.5		
RF Frequency Range	13.56MHz Xtal, 423.75KHz RF step		863~930		MHz
	12MHz Xtal, 400KHz RF step		863~930		MHz
Xtal Frequency (1)	HW control mdoe, Cload = 16pF.		**13.56718 / 14.29678**		MHz
	SPI control mdoe, Cload = 14pF		**12.0052**		MHz
Xtal Series Resistance (ESR)	Cload =16pF or 14pF			60	ohm
Crystal Tolerance			+/-50		ppm
Crystal settling time (2)	with Xtal compensated capacitor, Ccomp.		5		ms
	without Ccomp.		1		ms
PLL settling time	Xtal stable to TX ready		1		ms
Data Rate	ASK	1		10	Kbps
	FSK	1		20	Kbps
TX					
Max Output Power	868MHz, VDD=3.0V		6		dBm
	915MHz, VDD=3.0V		6		
Output Power step	TXP = 00 (max)		6		dBm
	TXP = 01		3		
	TXP = 10		0		
	TXP = 11		-4		
ASK Modulation Quality	On-Off Ratio		60		dB
Phase Noise	Offset=100KHz		-88		dBc/Hz
	Offset=1MHz		-106		
Spurious Emission(3)	f < 1GHz (RBW =100kHz)			-36	dBm
	47MHz< f <74MHz 87.5MHz< f <118MHz 174MHz< f <230MHz 470MHz< f <862MHz (RBW =100kHz)			-54	dBm
	Above 1GHz (RBW = 1MHz)			-30	

(1) Refer to section 9.2 and 9.3 for details.
(2) Refer to section 9.4 for details.
(3) Pin 4 / 5 are critical paths of good spurious emission. Use suitable RC filters on those two pins for noiseless power supply is very important. Refer to section 9.5, 9.6 for details.

9. Circuit Description

A7302D supports SPI and HW control mode by setting SPIS pin. If SPIS = 0, HW control mode is active, A7302D is in defaulted configuration by pin setting for radio control. If SPIS = 1, A7302D is in SPI mode (MCU programs Register 0 and Register 1). CE pin is recommended to be controlled by MCU. When CE pin goes from low to high, A7302D is enabled from shut down mode to active mode via auto calibration.

For A7302D, signal is Digital-IN to RF-Out from pin TX_DATA to PA_OUT. In ASK modulation, data input modulates PA switching directly and therefore leads to an ASK signal. In FSK modulation, frequency deviation is determined by crystal detuning via external capacitor and therefore leads to an FSK signal.

9.1 Functional Block

A7302D is an integer-N PLL synthesizer via feedback mechanism N-counter (Na + Nb). The VCO frequency is generated as a integer multiple of Phase Detect comparison frequency which is dividing by R-counter (16) from Xtal (13.56MHz).The phase detector tunes the VCO in the locked state at wanted frequency **$F_{VCO} = F_{RF}$ x 2.** See figure 9.1 for details.

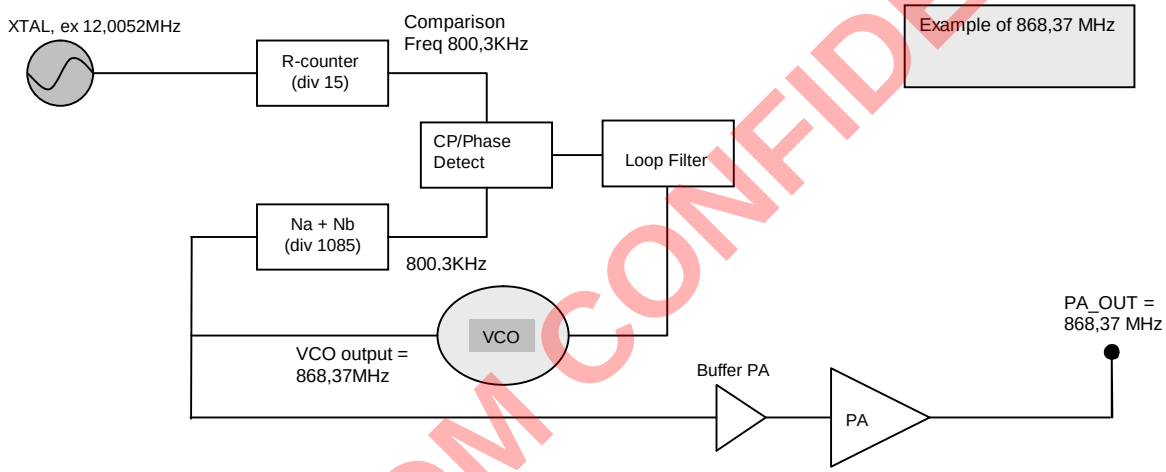


Figure 9.1.1 VCO Topology in SPI control mode.

9.2 HW Control Mode

Set SPIS pin = 0 for HW control mode, MCU has no extra efforts to do radio control but just needs to control CE and TX_DATA pin. Table 9.2.1 and Table 9.2.2 show default setting and how to do pin settings respectively. If so, A7302D is set at max TX power. Hence, MCU just needs to deliver TX data to TX_DATA pin. For different wanted frequency allocations, refer to Table 9.2.3 for crystal selection.

Default setting in HW Mode	
TX Power	typical 6 dBm
R [1:0]	R = 2
N	N=128
PLL Comparison freq.	Xtal / 2

Table 9.2.1 Default settings in HW control mode.

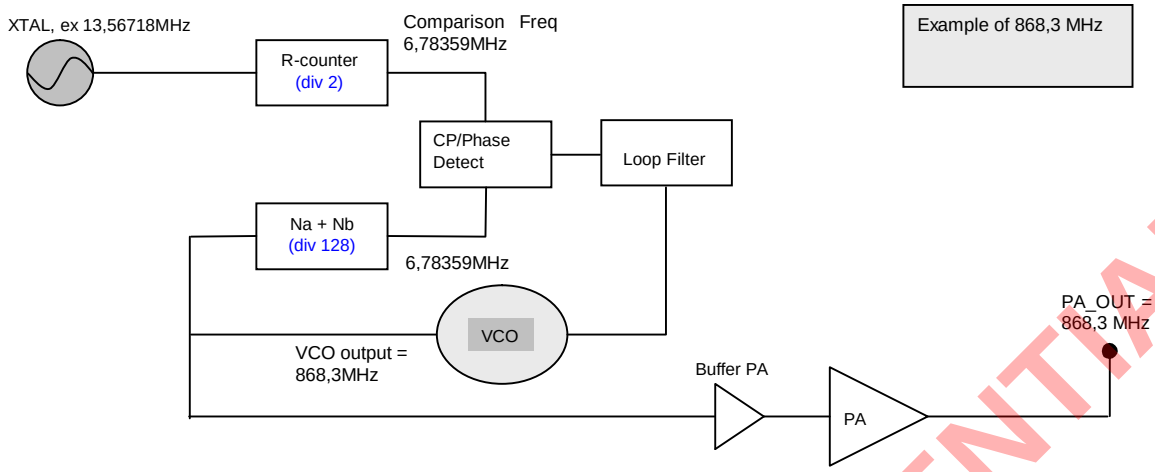


Figure 9.2.1 VCO in HW control mode.

Pin 10 (SPIS)	Pin 1 (Mode)	Pin 2 (TX_DATA)	Pin 3 (CE)
Must be 0	915M ASK = 0	Transmitting data	Shut down = 0
	868M ASK = 120 K ohm		
	868M FSK = 240 K ohm		Active = 1
	915M FSK = VDD		

Table 9.2.2 Pin setting in HW control mode.

868MHz			915MHz		
Crystal (MHz)	SPIS	F_{RF} (MHz)	Crystal (MHz)	SPIS	F_{RF} (MHz)
13,525	0	865.6	14,09375	0	902
13,53125	0	866	14,15312	0	905.8
13,55625	0	867.6	14,19531	0	908.5
13,5625	0	868	14,29375	0	914.8
13,56718	0	868.3	14,29456	0	914.852
13,56796	0	868.35	14,29687	0	915
13,56875	0	868.4	14,32031	0	916.5
13.56953	0	868.45	14,35937	0	919
13,57031	0	868.5	14,40625	0	922
13,57421	0	868.75	14,42187	0	923
13,57734	0	868.95	14,53906	0	930.5
13,58593	0	869.5			
13,58876	0	869.675			
13,59062	0	869.8			
$F_{RF} = F_{XTAL}$ x 64			$F_{RF} = F_{XTAL}$ x 64		

Table 9.2.3 Crystal selection guide in HW control mode

9.3 SPI Control Mode

Set SPIS = 1 for SPI control mode, MCU is also very easy to do radio control via 3-wire SPI because A7302D has only two 16-bit-write-only registers (Register 0 and Register 1). Then, MCU can control the device's features to meet system requirements instead of using its default settings. Please note, bit sequence is 16 bits on SPI from D0 to D15 (LSB first, D0 and D1 are address bits), but it is not a standard SPI for data bits.

For Register 0, it is used to define R counter and N counter. R counter supports 3 crystal options by 12/13.56/16MHz. N counter is separated into NA and NB to support wanted F_{RF} in every 423KHz RF step with 13,56MHz Xtal. Refer to section 9.3.2 for details.

For Register 1, it is used to set TX output power, Modulation type (FSK or ASK) as well as Band Selection. Refer to section 9.3.3 for details.

Pin 10 (SPIS)	Pin 1 (SPI_STB)	Pin 2 (SPI_DATA)	Pin 3 (SPI_CLK)
Must be 1	SPI Strobe	SPI data input and Transmitting data	SPI clock

Table 9.3.1 Pin setting in SPI control mode.

9.3.1 SPI timing

A7302D is very easy-to-use, only two steps to do radio control.

Step 1: Set wanted RF frequency by Register 0.
Step 2: Set features by Register 1.
Step 3: If A7302D is set from shut down mode to active mode, please note to do step 1 and 2 again.

Register 0 and 1 are both write-only. A7302D supports maximum 4Mbps SPI baud rate. To active SPI, SPI_STB pin must be set to high. To latch correct data, hold time and setup time between SPI_CLK and SPI_DATA must be satisfied. SPI_DATA is latched into the device at the rising edge of SPI_CLK. See below table for SPI timing characteristic.

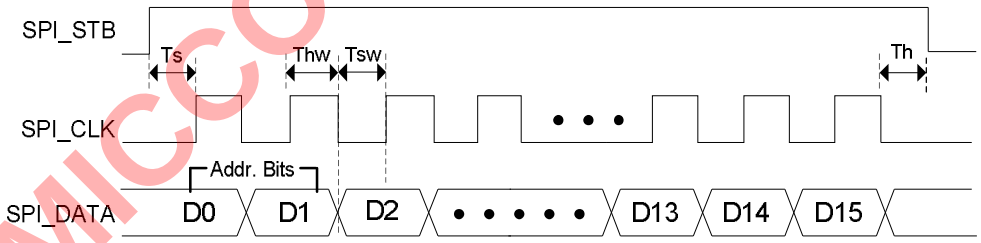


Fig 9.3.1.1 SPI timing chart

Parameter	Description	Min	Max	Unit
Fc	SPI Clock Frequency		4	MHz
Ts	SPI_STB Setup Time	50		ns
Thw	SPI_DATA Hold Time	50		ns
Tsw	SPI_DATA Setup Time	50		ns
Th	SPI_STB Hold Time	50		ns

Table 9.3.1.1 SPI timing characteristic

In SPI Control Mode, SPI_DATA and TX_DATA share to the same pin (Pin 2). SPI_STB is used to determine Pin 2 into SPI_DATA or TX_DATA. Figure 9.3.1.2 illustrates the Timing Chart of SPI_DATA and TX_DATA by setting SPI_STB.

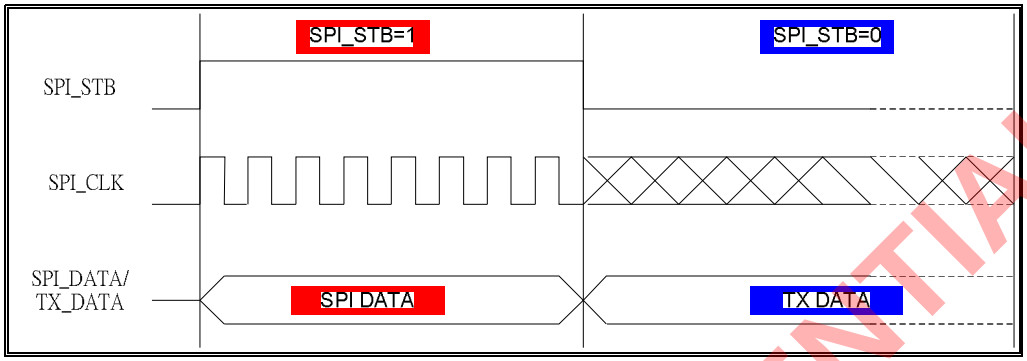


Figure 9.3.1.2 Important Timing chart of SPI_DATA and TX_DATA

9.3.2 Register 0 (Address: 00)

Name	Write-only	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register 0		R1	R0	NB7	NB6	NB5	NB4	NB3	NB2	NB1	NB0	NA3	NA2	NA1	NA0	0	0
Reset value		0	0	0	1	0	0	0	0	1	1	1	1	0	1	0	0

← Write in direction (from D0 to D15, LSB first).

D1 and D0: Address bit. Register 0 = [00], Other settings are forbidden.

R[1:0]: Crystal reference frequency.

R [1:0]	Crystal (MHz)	R counter	Note
00	Reserved	Reserved	
01	12	15	PLL step = 800KHz, RF step = 400 KHz
10	13.56	16	PLL step = 847.5KHz, RF step = 423.75 KHz
11	16	20	PLL step = 800KHz, RF step = 400 KHz

N= (16XNB) +NA. NB=46~144, NA=0~15

NB, NA: Used to define wanted F_{RF} of PLL (see below table).

NA[3:0]: NA is 0 ~ 15.

NB[7:0]: NB is 46~144.

Formula	Example	
N = 16 x NB + NA $F_{RF} = F_{XTAL}$ x N / R	NA = 13 = [1101]	
	NB = 67 = [0100-0011]	
	N = 16 x 67 + 13 = 1085	
	R = 15 (F_{XTAL} =12,0052MHz)	
	F_{RF} = 12,0052 x 1085 / 15	F_{RF} = 868,37 MHz

Band 868MHz			Band 915MHz		
NA	NB	Example	NA	NB	Example
0	60	F_{RF} = 12,0052 x (N) / 15 = 12,0052 x 1085 / 15 = 868,37 MHz	0	65	F_{RF} = 12,0052 x (N) / 15 = 12,0052 x 1143 / 15 = 914,8 MHz
1	61		1	66	
3	62		3	67	
4	63		4	68	
5	64		5	69	
6	65		6	70	
7	66		7	71	
8	67		8	72	
9	68		9	73	
10	69		10	74	
11	70		11	75	
12	71		12	76	
13	72		13	77	
14	73		14	78	
15	74		15	79	

9.3.3 Register 1 (Address: 10)

Name	Write-only	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register 1		--	--	--	--	--	--	TXP1	TXP0	CKS	ECK	STBY	BAND	FSK_ASK	CE	1	0
Reset value		0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0

← Write in direction (from D0 to D15, LSB first).

D1 and D0: Address bit. Register 1 = [10], other settings are forbidden.

TXP: TX output power control.
[00]: max. **[01]:** high. **[10]:** mid. **[11]:** min.

TXP [1:0]	TX power level	Band 868MHz	Band 915MHz
00	Max.	6 dBm	6 dBm
01	High	3 dBm	3 dBm
10	Mid.	0 dBm	0 dBm
11	Min.	-4 dBm	-4 dBm

CKS: Reserved.

ECK: Reserved.

STBY: Shall be set to [0].

BAND: RF band selection.
[0]: 868 MHz band.
[1]: 915 MHz band (default).

FSK_ASK: FSK ASK Select.
[0]: ASK (default).
[1]: FSK.

CE: Chip Enable
[0]: Shut down mode (default).
[1]:.Active mode.

9.4 Start-up Sequence

In HW control mode, CE pin is used to let A7302D from shut down mode to active mode, when CE > 1V , A7302D executes crystal start-up and auto calibration. That means, VDD shall be stable (> 90% max VDD) before CE go higher than 1V for successful calibration. Otherwise, VCO may not operate at properly frequency. For certain applications, if CE is connected to VDD directly, an extra RC delay at CE pin is necessary for proper delay of start up sequence as shown below.

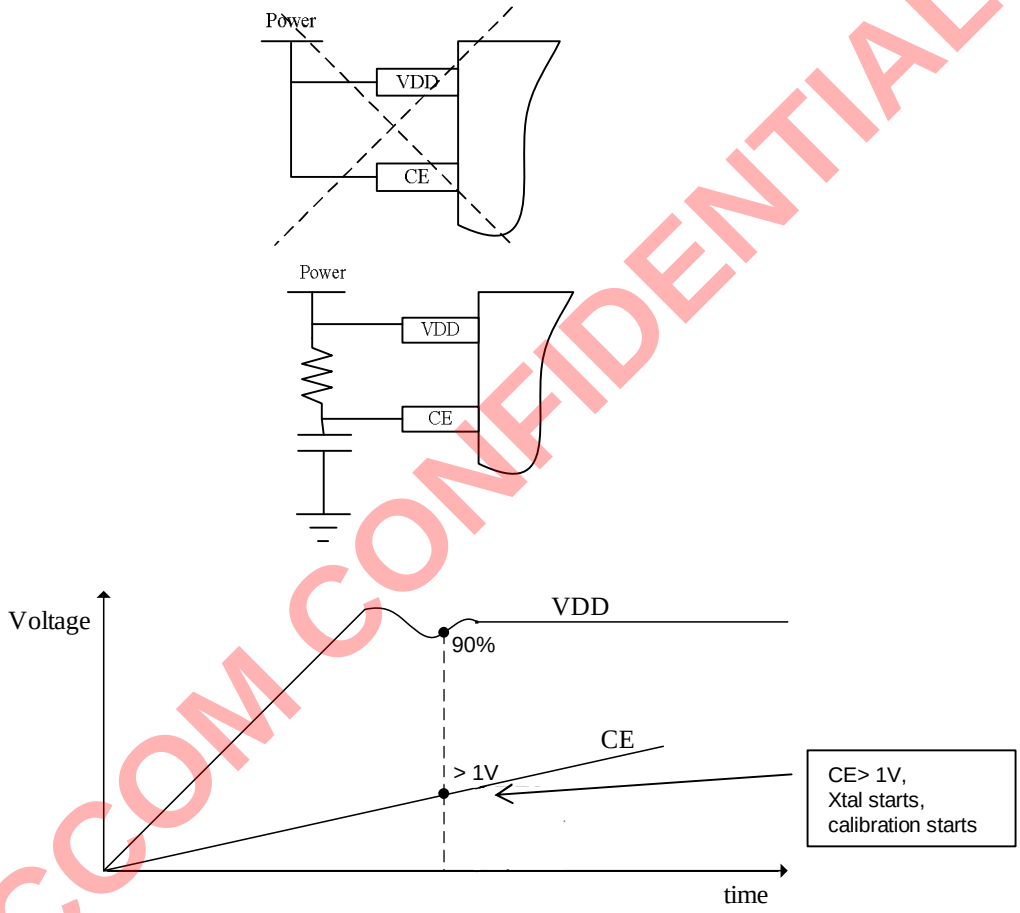
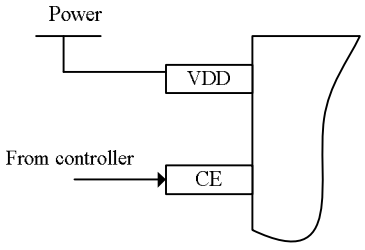


Figure 9.4.1. An extra RC delay on CE pin for correct start up sequence.

Hence, CE pin is recommended to be enabled by MCU. If so, RC delay on CE pin is not necessary, but, MCU shall let CE pin go HIGH after VDD is stable (> 90% max VDD) as shown below.



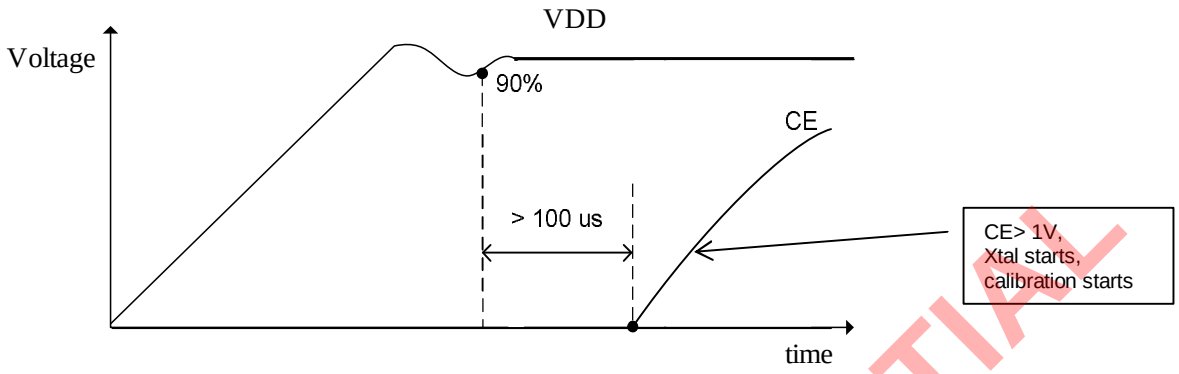


Figure 9.4.2. CE pin is controlled by MCU for a correct start up sequence.

When CE > 1V, crystal oscillator and calibration procedure are active. Figure 9.4.3 illustrates A7302D's settling time when Ccomp is NC (Note Connected). If Ccomp is added, Xtal settling time becomes longer from typical 1ms to 5 ms. See Table 9.4.1 for details.

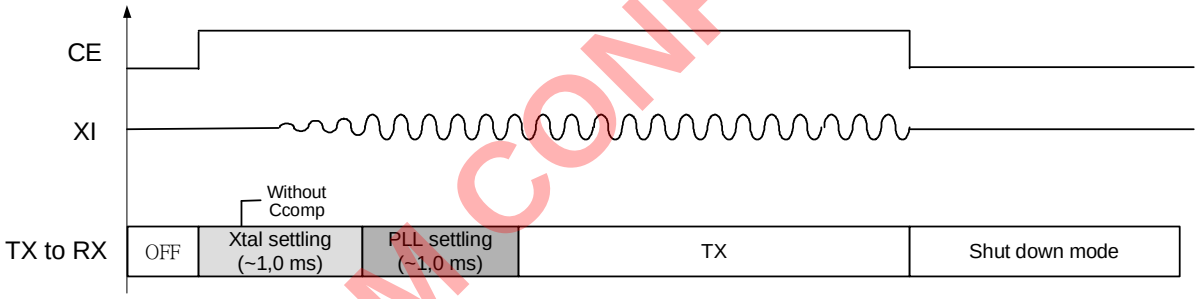


Fig 9.4.3 Settling time from shut down mode to TX mode.

A7302D's crystal oscillator is Colpitts type with integrated feedback capacitors as shown in Figure 9.4.4. The input capacitance C_{XI} from XI pin is about 14 pF ~ 16 pF. Therefore, it is recommended to use a Xtal with 16 pF or 14 pF Cload because Xtal settling time is short (~1ms). If Xtal Cload is larger than 16 pF, an external Ccomp shall be added at XI pin. Then, Xtal settling time becomes longer. Another case to add Ccomp is to fine tune $\mathbf{F_{RF}}$ for a proper frequency even though Xtal Cload =16 pF. Refer to Figure 9.4.5 and Table 9.4.1 for details.

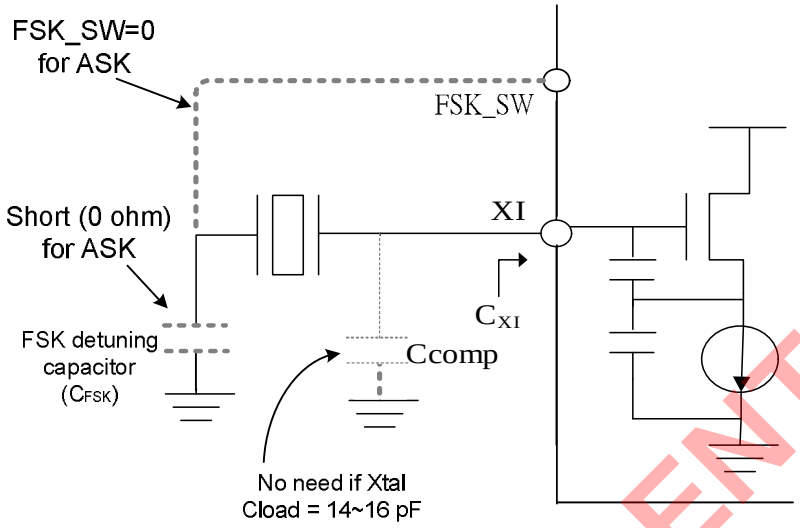


Figure 9.4.4 Schematic of crystal oscillator.

Settling Time (Typical)		
Xtal settling	Without Ccomp	1 ms
	With Ccomp	5 ms
PLL settling time		1 ms

Table 9.4.1 Typical settling time

Recommend Xtal Specification	868MHz HW control mode	915MHz HW control mode	868 / 915MHz SPI control mode
Center Frequency	13,56718 MHz	14,29687 MHz	12,0052 MHz
Load Capacitance (Cload)	16 pF	16 pF	14 pF
Equivalent Series Resistance (ESR)	=<60 ohms	=<60 ohms	=<60 ohms
Shunt Capacitance (C0)	=<5pF	=<5pF	=<5pF
Stability	± 50 ppm	± 50 ppm	± 50 ppm

Table 9.4.2 Recommend crystal spec

From Figure 9.4.4, A7302D's frequency deviation in FSK is defined by applying external capacitors (C_{FSK}) on FSK_SW pin. Fig. 9.4.5 is the equivalent circuit of detuning Xtal when TX_DATA=1 and TX_DATA = 0 respectively. Table 9.4.3 is a recommended C_{FSK} for ± 12,5KHz frequency deviation which is suitable for FSK data rate from 1K to 20Kbps when A7201 is used to be FSK RX.

Recommend C_{FSK}	Fdev	Note
150 pF	± 12,5KHz	Suitable for FSK data rate from 1K ~ 20Kbps

Table 9.4.3 Recommend Fdev in FSK

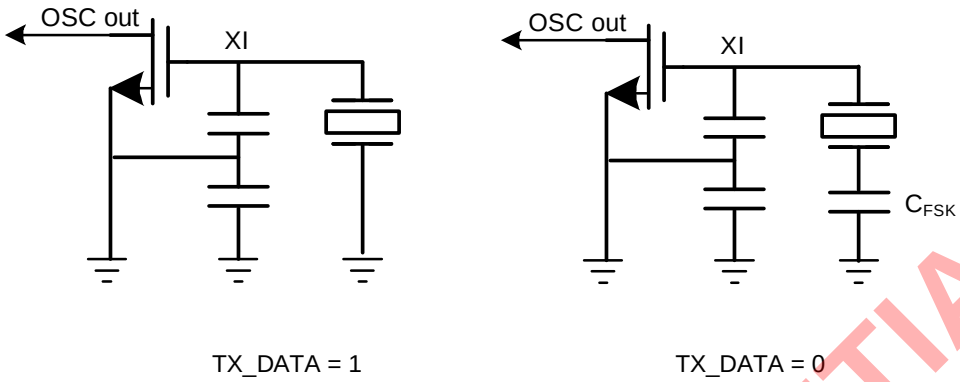


Figure 9.4.5 Equivalent circuit of crystal oscillator during FSK modulation.

9.5 TX Data Shaping

For minimizing TX transient power as well as occupied bandwidth, A7302D has built-in TX data shaping circuit as illustrated in Figure 9.5.1. Therefore, user has no need to add external RC data shaping on TX_DATA pin. TX modulated spectrum in ASK and FSK are shown in Figure 9.5.2 respectively.

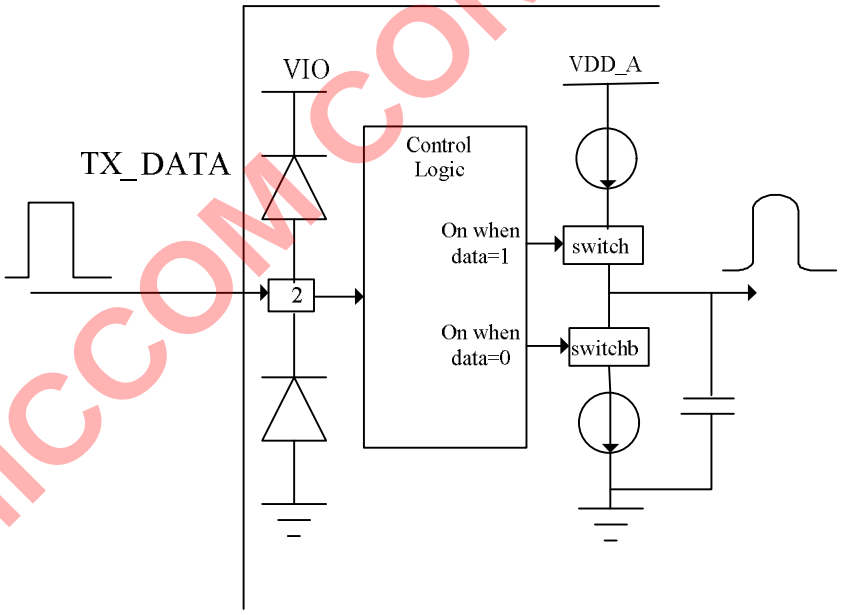


Figure 9.5.1 Data shaping circuit inside A7302D `

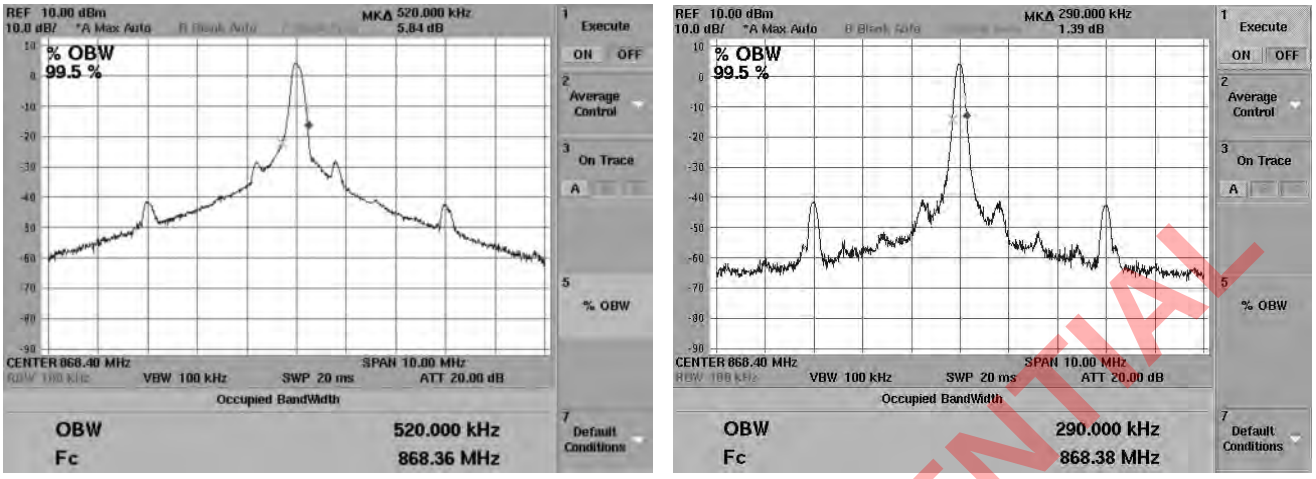


Figure 9.5.2 TX Spectrum (Spectrum Analyzer, RBW=VBW=100KHz, SPAN 10MHz)

9.6 TX Spurious Emission

Noisy VDD is a critical issue to induce A7302D a bad TX spurious emission. Inside A7302D, analog circuitry is powered by VDD_A pin and digital circuitry is powered by VDD_D pin. Please note to add low pass RC filter in front of VDD_A and VDD_D. To powered up A7302D PA, it is ok to connect (2.2 ~ 3.6V) directly. RC filters in front of VDD_D and VDD_A can isolate power noise while PA is switching. Therefore, VDD RC filters lead good results of TX spurious emission as shown below. Figure 9.6.1 illustrates R and C values used in AMICCOM's reference design. For different PCB design, R and C may be fine tuned to get optimized spurious performance.

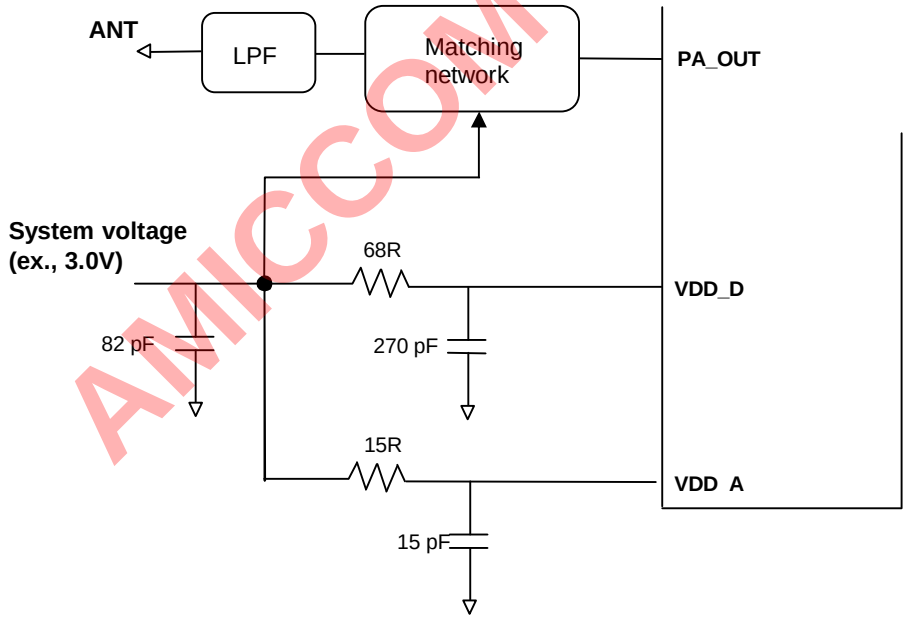


Figure 9.6.1 RC low pass filters on VDD_A and VDD_D

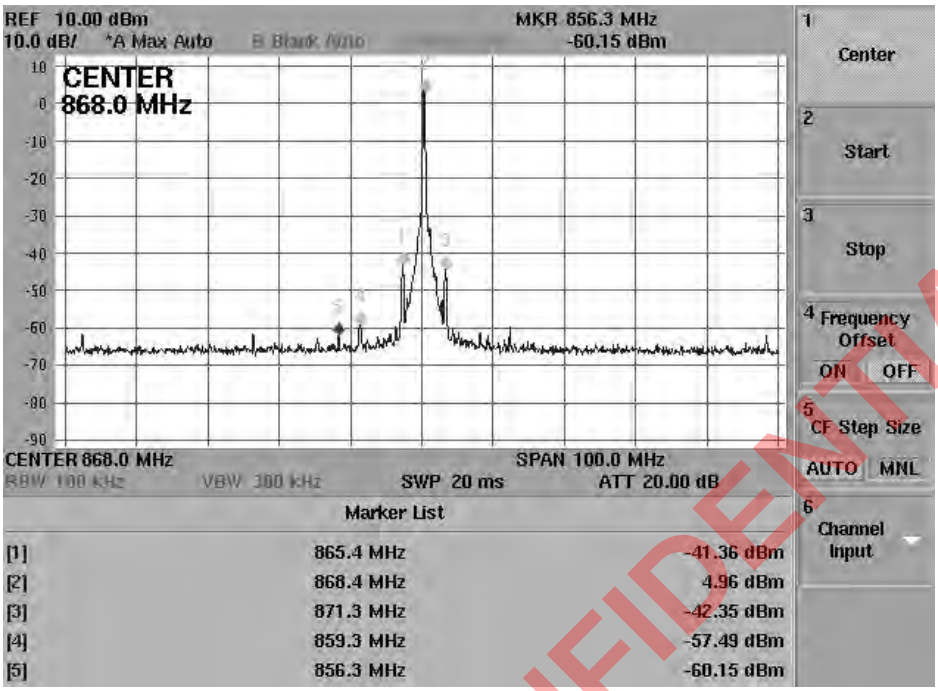


Figure 9.6.2 TX spectrum in ASK, Span 100MHz

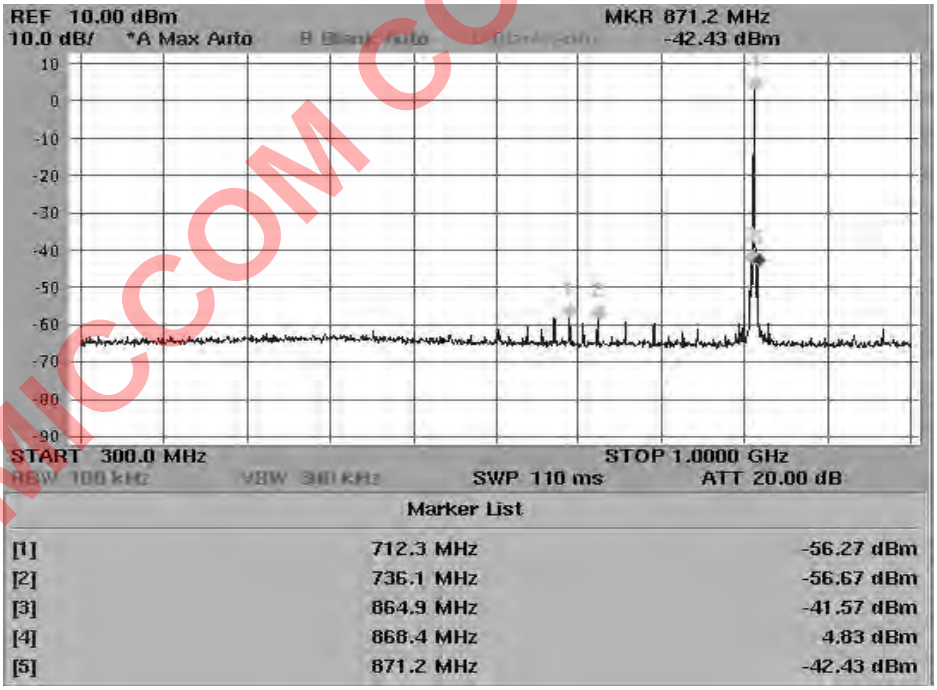


Figure 9.6.3 TX spectrum in ASK, Span 700MHz

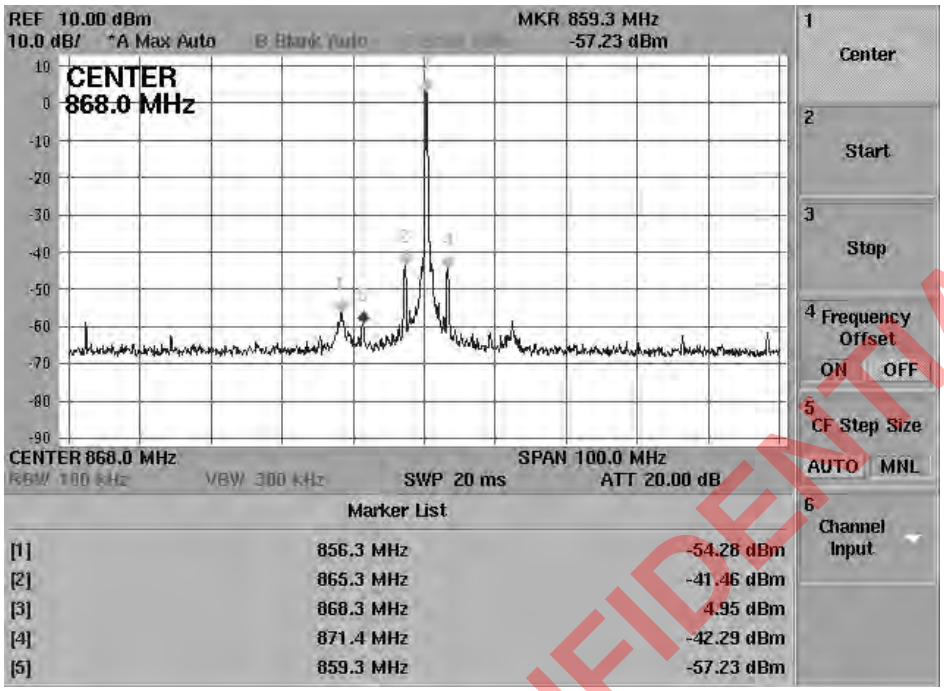


Figure 9.6.4 TX spectrum in FSK, Span 100MHz

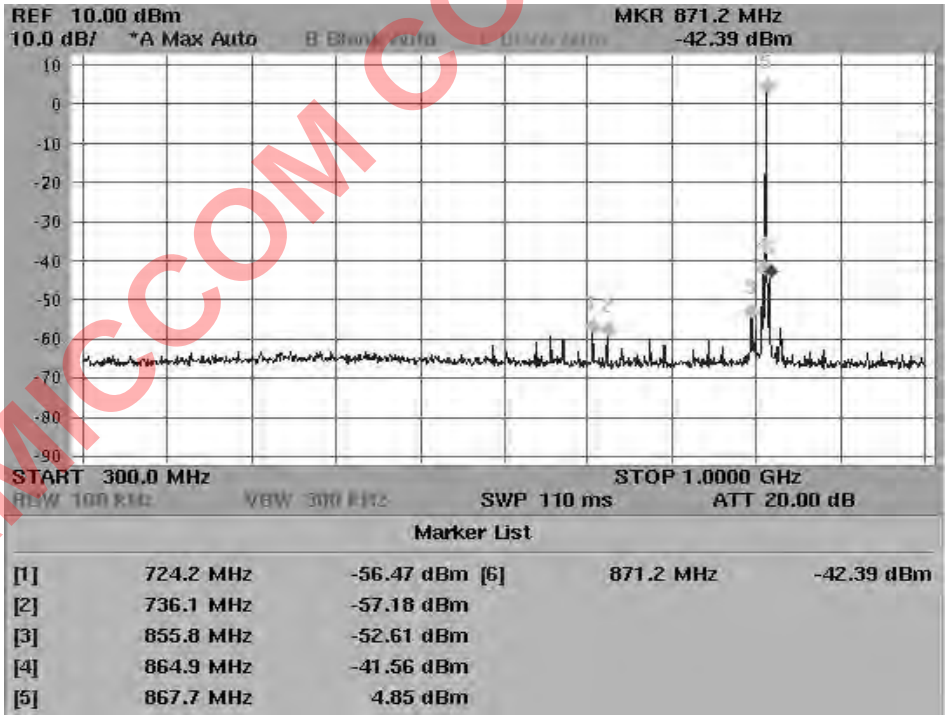
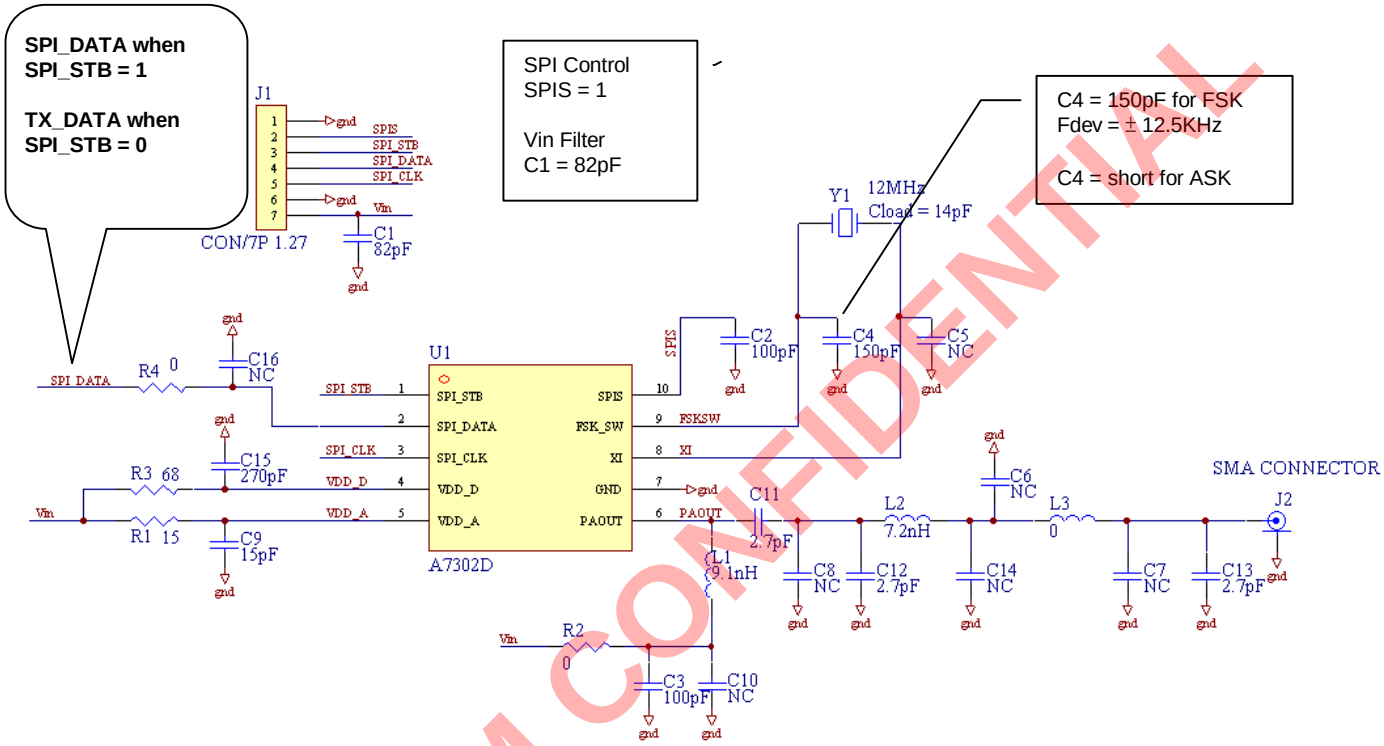


Figure 9.6.5 TX spectrum in FSK, Span 700MHz

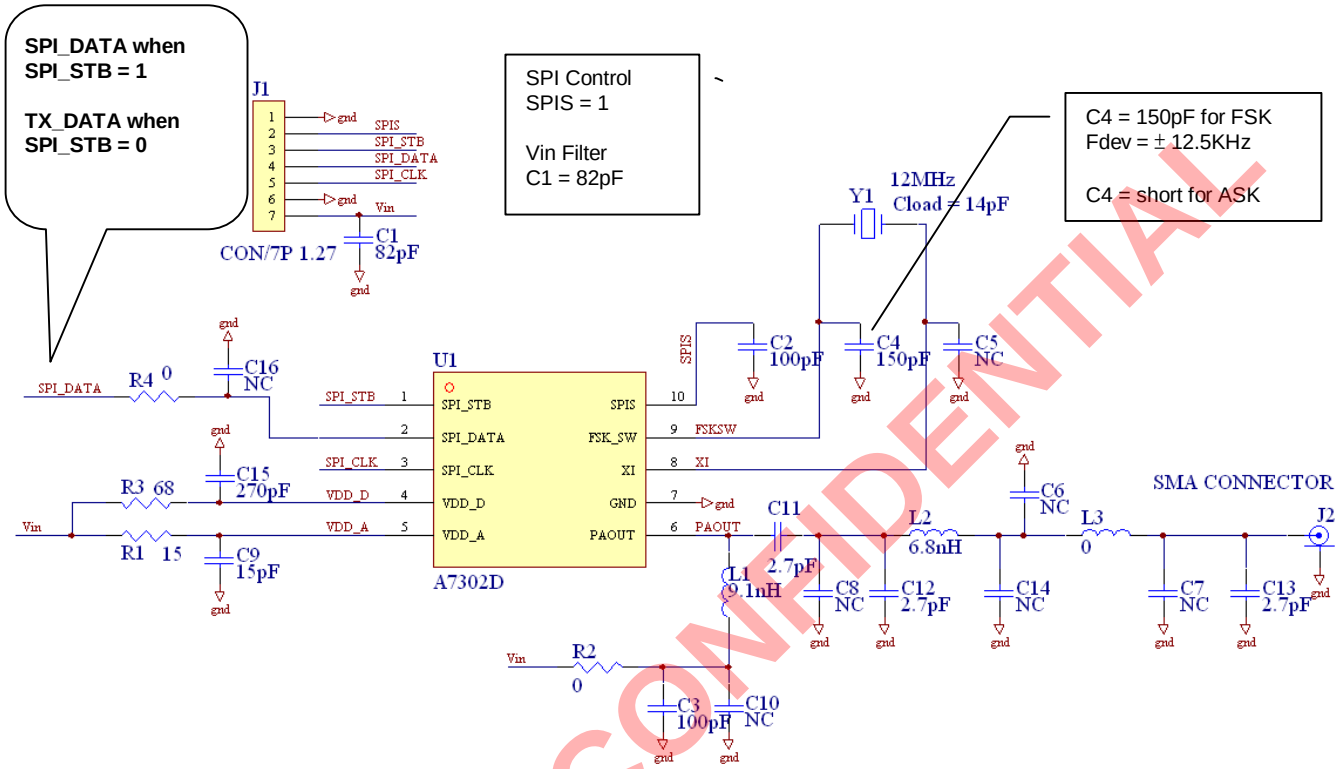
10. Application Circuit

10.1 SPI Control Mode for ASK and FSK (i.e. 868.4MHz)



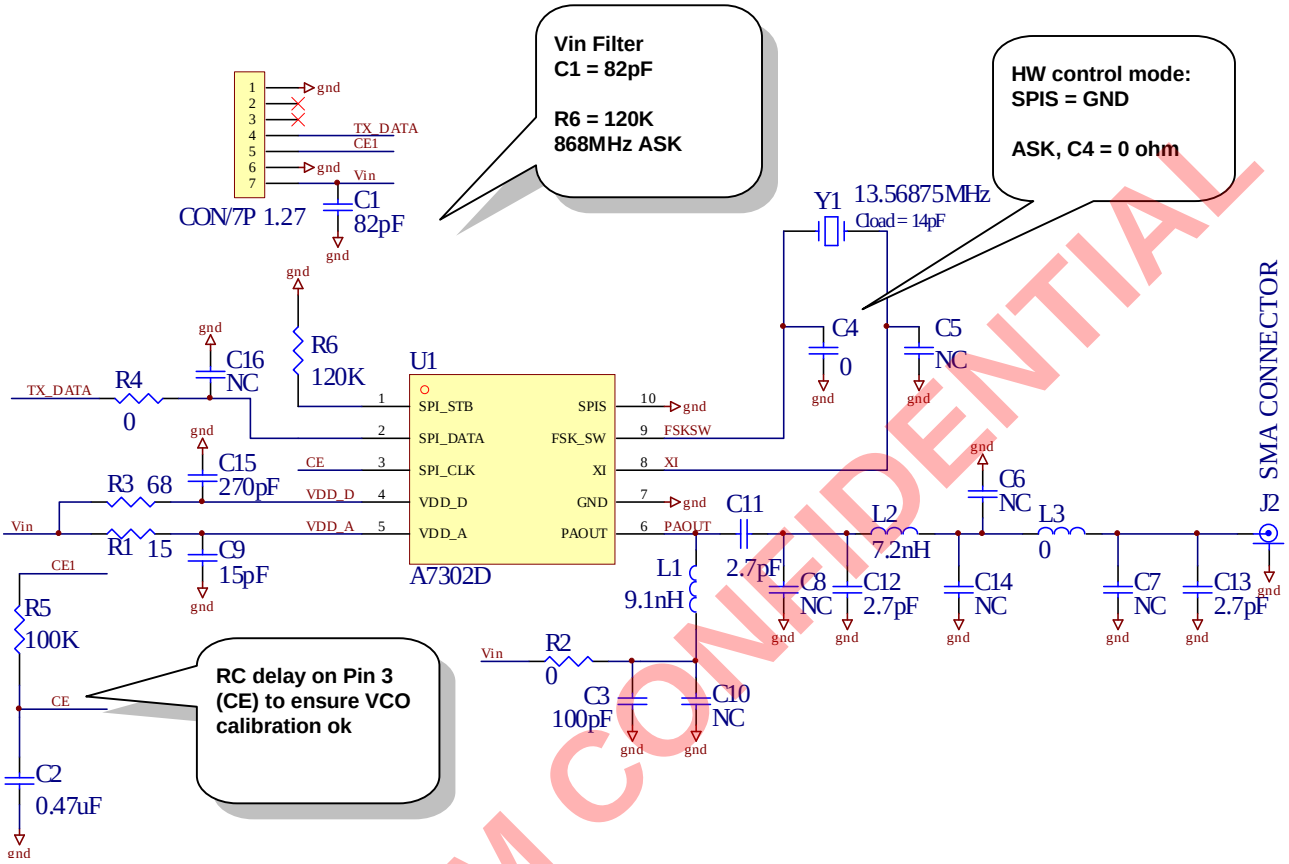
Typical Application Circuit of A7302D, Xtal = 12MHz, Cload = 14pF.

10.2 SPI Control Mode for ASK and FSK (i.e. 914.8MHz)



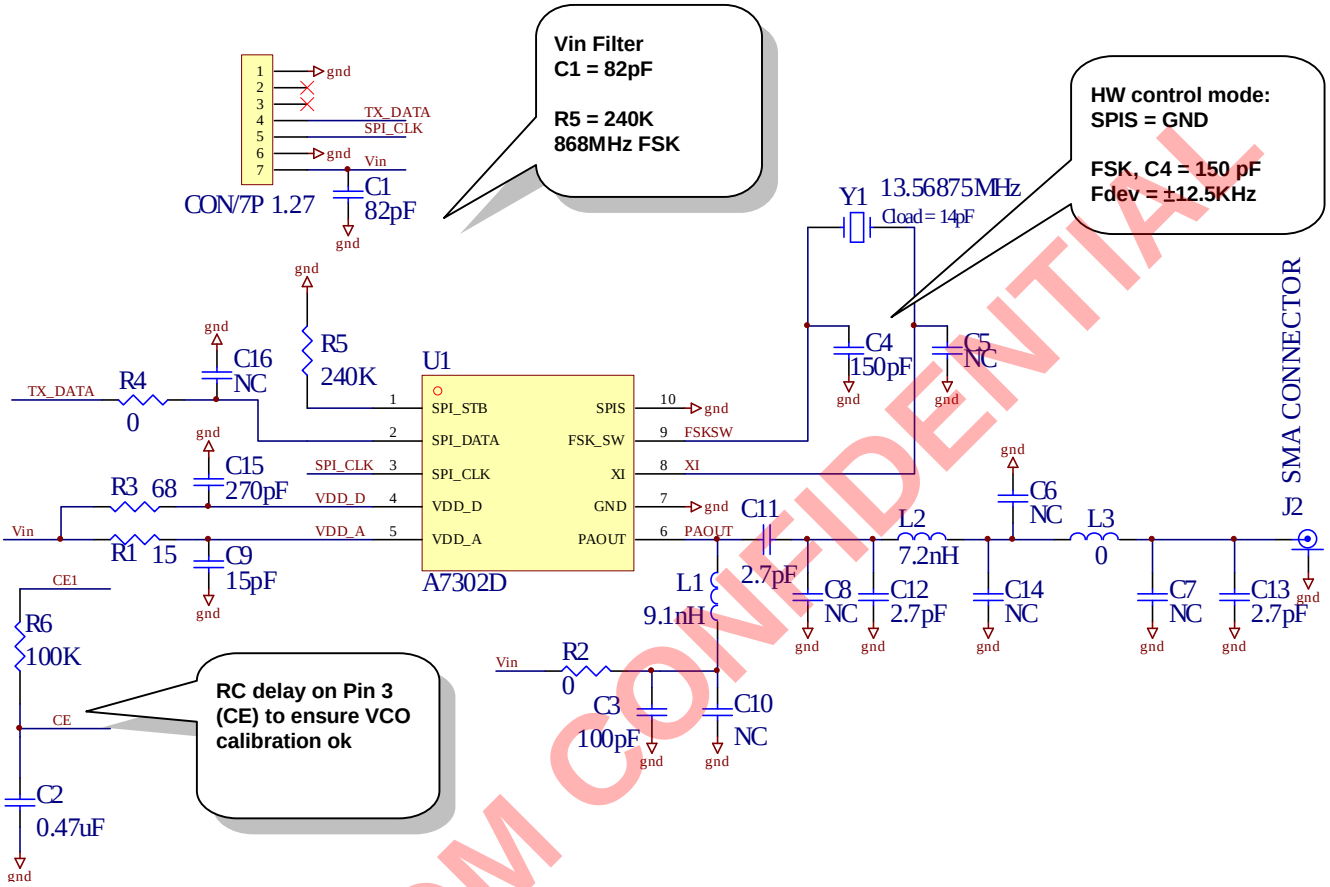
Typical Application Circuit of A7302D, Xtal = 12MHz, Cload = 14pF.

10.3 HW Control Mode for ASK (i.e. 868.4MHz)



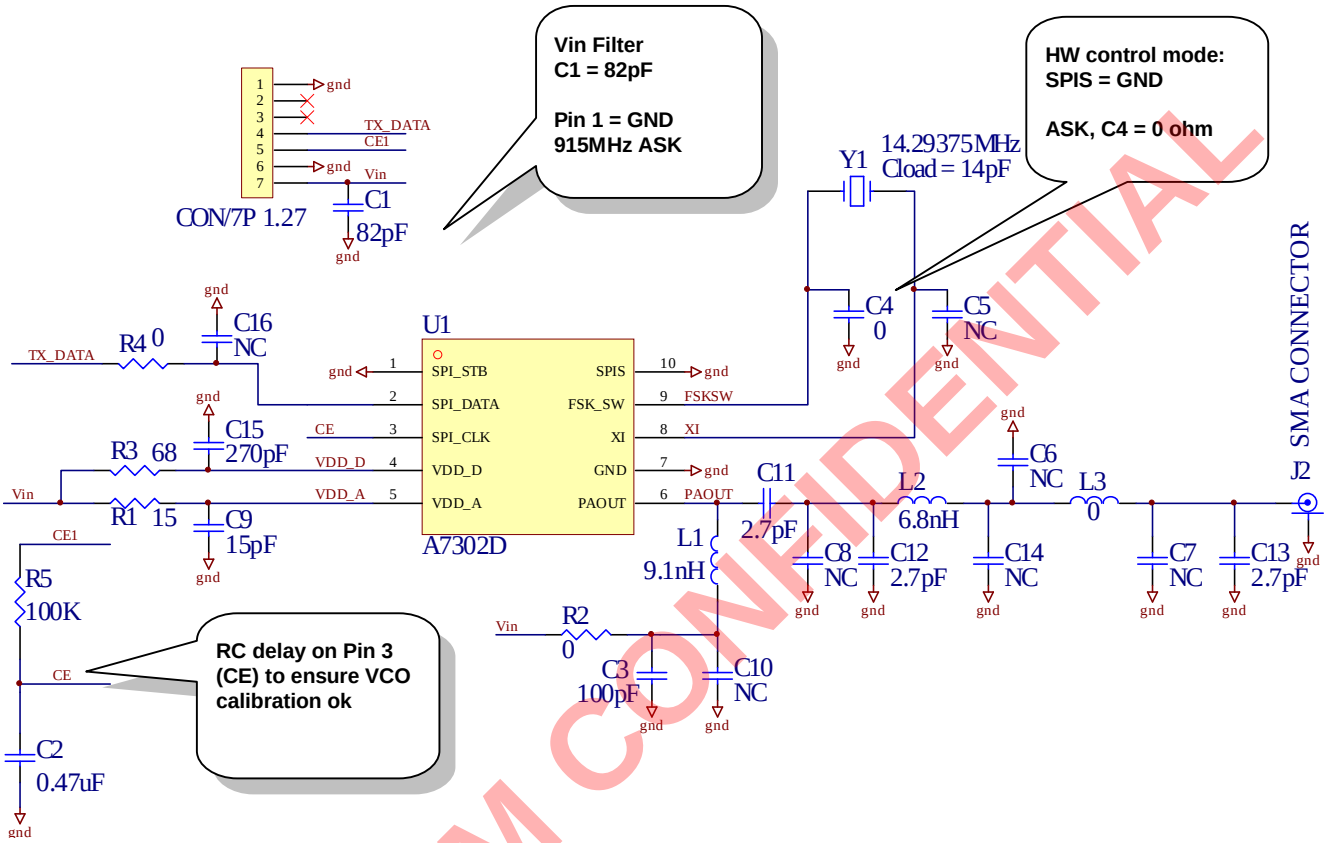
Typical Application Circuit of A7302D, Xtal = 13.56875MHz, Cload = 14pF.

10.4 HW Control Mode for FSK (i.e. 868.4MHz)



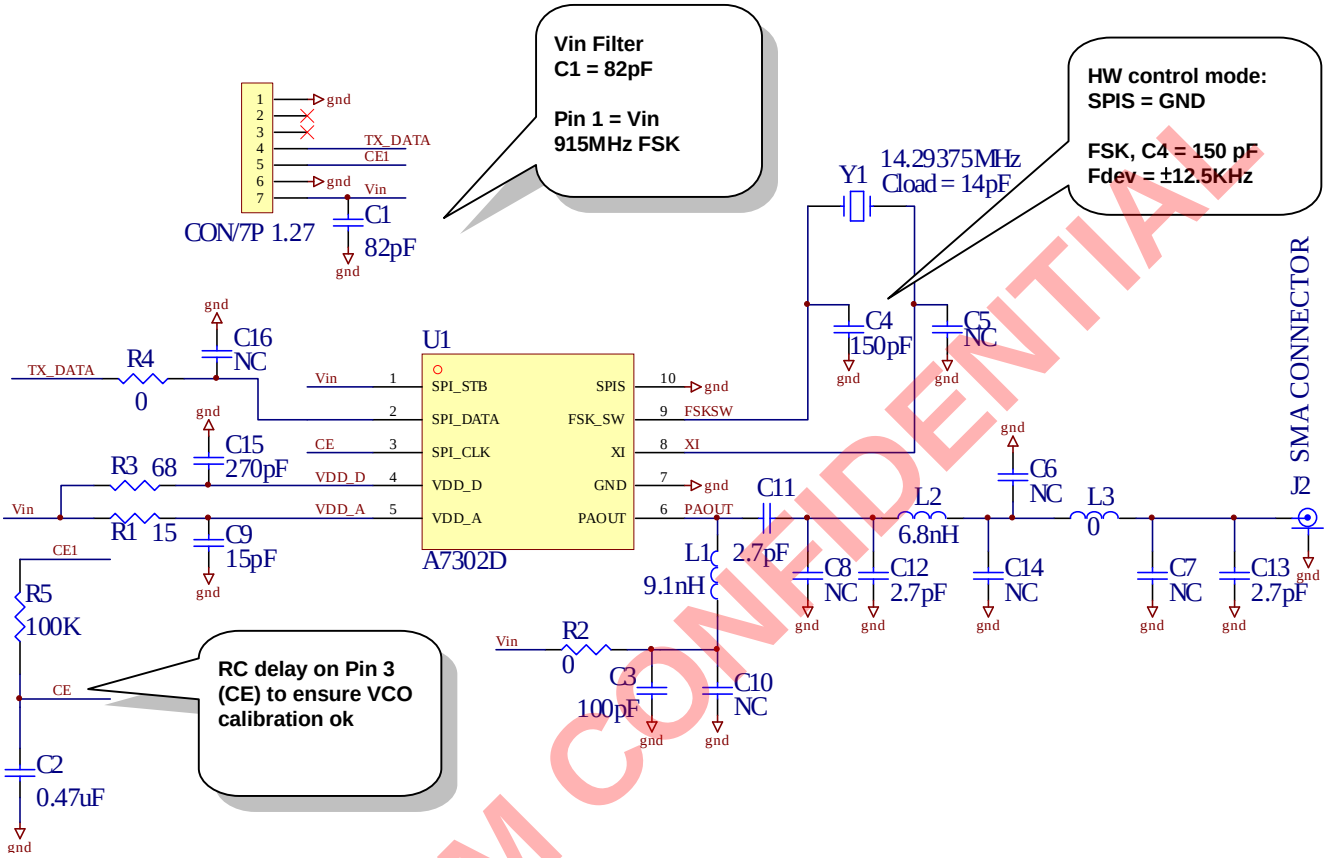
Typical Application Circuit of A7302D, Xtal = 13.56875MHz, Cload = 14pF.

10.5 HW Control Mode for ASK (i.e. 914.8MHz)



Typical Application Circuit of A7302D, Xtal = 14.29375MHz, Cload = 14pF.

10.6 HW Control Mode for FSK (i.e. 914.8MHz)



Typical Application Circuit of A7302D, Xtal = 14.29375MHz, Cload = 14pF.

11. Abbreviations

ASK	Amplitude Shift Keying
BW	Bandwidth
Fdev	Frequency Deviation
FSK	Frequency Shift Keying
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PLL	Phase Lock Loop
SPI	Serial to Parallel Interface
TX	Transmitter
VCO	Voltage Controlled Oscillator
Xtal	Crystal

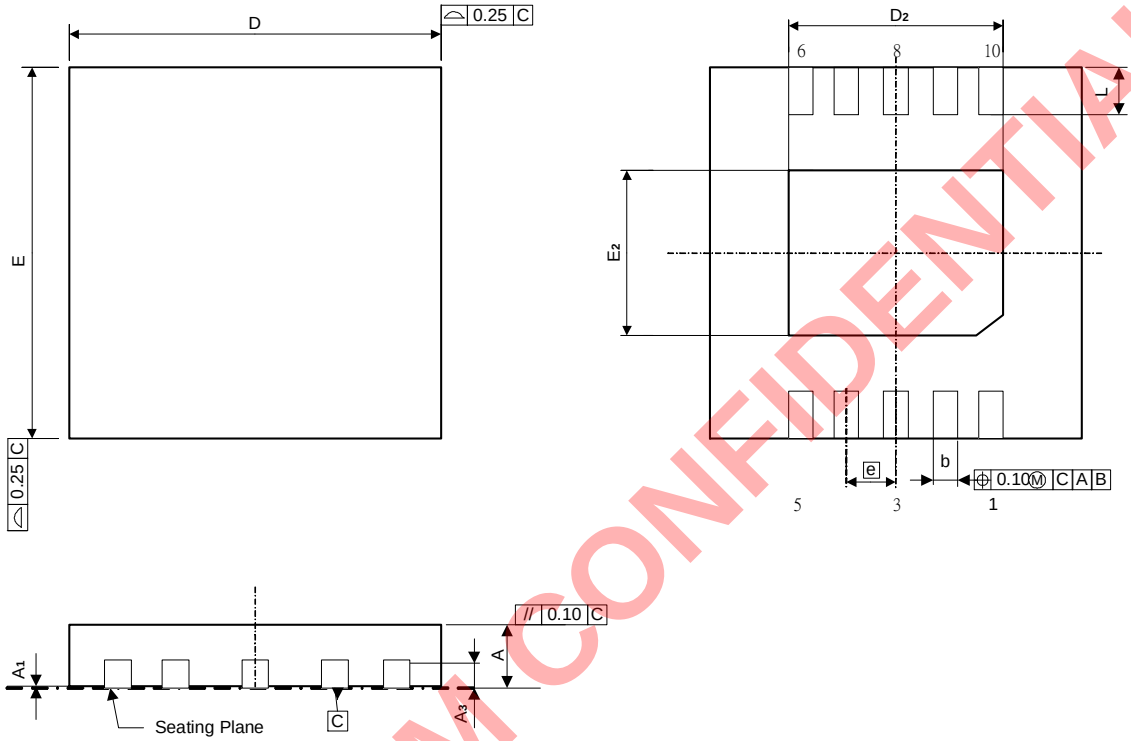
12. Ordering Information

Part No.	Package	Units Per Reel / Tube / Tray
A73C02DDF/Q	DFN10, Tape & Reel, Pb free	3Kpcs
A73C02DDF	DFN10, Tube, Pb free	121pcs
A73C02BH	Die Form, Tray, Pb free	250pcs

13. Package Information

DFN10 Outline Dimensions

TOP VIEW **BOTTOM VIEW**

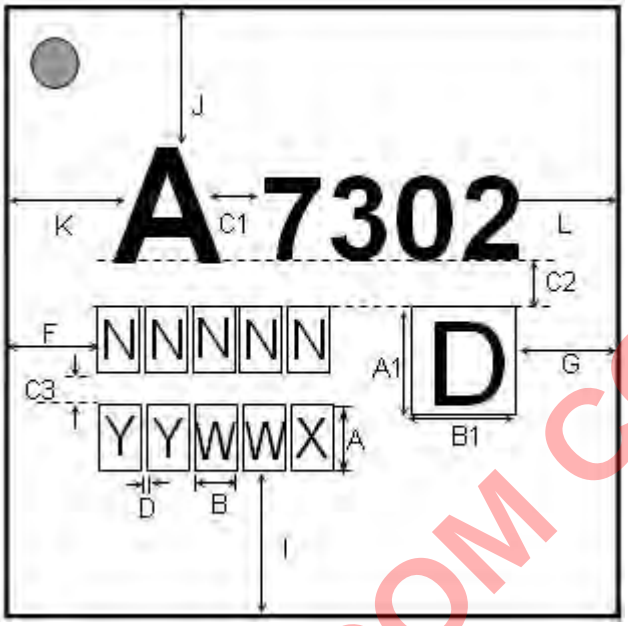


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.032	0.70	0.75	0.80
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3	0.008 REF			0.203 REF		
b	0.007	0.010	0.012	0.18	0.24	0.30
D	0.116	0.118	0.120	2.95	3.00	3.05
D_2	0.089	0.093	0.096	2.25	2.35	2.45
E	0.116	0.118	0.120	2.95	3.00	3.05
E_2	0.061	0.065	0.069	1.55	1.65	1.75
e	0.020 BSC			0.50 BSC		
L	0.014	0.016	0.018	0.35	0.40	0.45

14. Top Marking Information

A73C02DDF

- Part No. : **A73C02DDF**
- Pin Count : **10**
- Package Type : **DFN**
- Dimension : **3*3 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**



❖ CHARACTER SIZE : (Unit in mm)

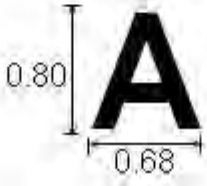
A : 0.55 A1 : 0.64
B : 0.30 B1 : 0.4
C1 : 0.25 C2 : 0.3 C3 : 0.2
D : 0.03

F=G
I=J
K=L

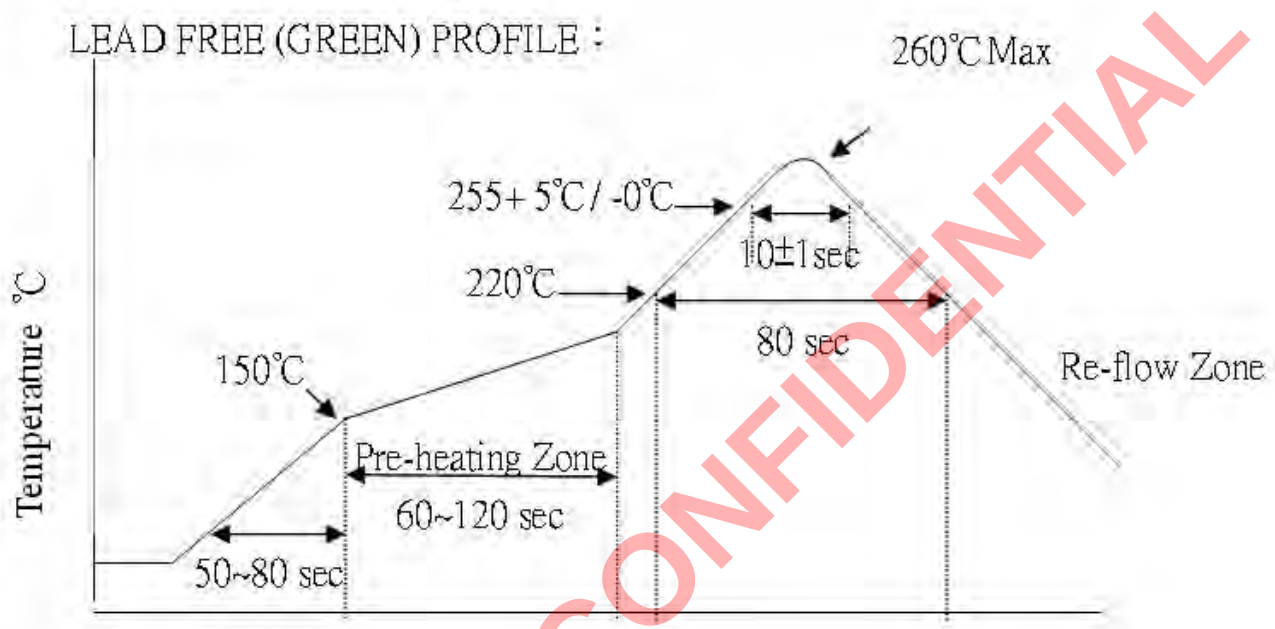
Y Y W W : DATECODE

X : PKG HOUSE ID

N N N N N : LOT NO.
(The last 5 characters, no decimals)

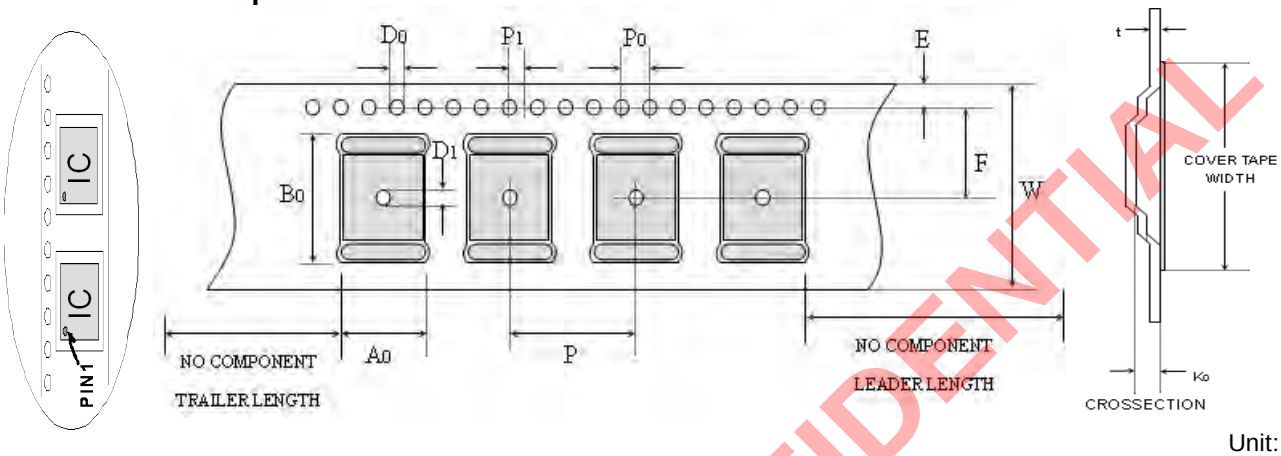


15. Reflow Profile



16. Tape Reel Information

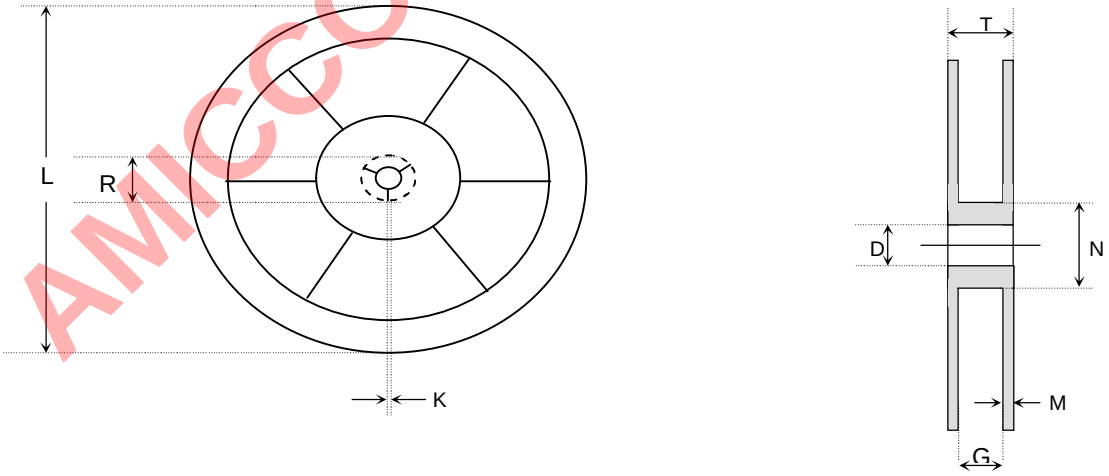
Cover / Carrier Tape Dimension



Unit: mm

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W	K0	t	Cover tape width
QFN3*3	8±0.1	3.25±0.1	3.25±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75±0.1	5.5±0.05	12±0.3	1.25±0.1	0.3±0.05	9.3±0.1
QFN 4*4	8±0.1	4.35±0.1	4.35±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75±0.1	5.5±0.05	12±0.3	1.25±0.1	0.3±0.05	9.3±0.1
QFN 5*5	8±0.1	5.25±0.1	5.25±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75±0.1	5.5±0.05	12±0.3	1.25±0.1	0.3±0.05	9.3±0.1
SSOP	12±0.1	8.2±1	8.8±1.5	4.0±0.1	2.0±0.1	1.5±0.1	1.5±0.1	1.75±0.1	7.5±0.1	16±0.1	2.1±0.4	0.3±0.05	13.3±0.1

REEL DIMENSIONS



Unit: mm

TYPE	G	N	M	D	K	L	R
QFN	12.9±0.5	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9
SSOP	16.3±1	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9

17 Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date.AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

RF ICs AMICCOM

AMICCOM

Headquarter
A3, 1F, No.1, Li-Hsin Rd. 1, Hsinchu Science Park,
Taiwan 30078
Tel: 886-3-5785818

Shenzhen Office
Rm., 2003, DongFeng Building, No. 2010,
Shennan Zhonglu Rd., Futian Dist., Shenzhen, China
Post code: 518031

Web Site
http://www.amiccom.com.tw