DESCRIPTION

The A7322 is a fully integrated, synchronous rectified step-down converter that provides wide 4.2V to 28V input voltage range and 2A continuous load current capability. The A7322 can operate at PFM mode to achieve high efficiency and reduce power loss at light load. In shutdown mode, the Max supply current is about 3μA.

The A7322 protection function includes cycle-by-cycle current limit, UVLO and thermal shutdown. Besides, internal soft-start prevents inrush current at fast power-on. This device uses slope compensated current mode control which provides fast load transient response. Internal loop compensation function reduces the external compensator components and simplifies the design process.

The A7322 is available in PSOP8 package.

ORDERING INFORMATION

Package Type	Part Number	
PSOP8 SPQ: 2,500pcs/Reel	MP8	A7322MP8R
		A7322MP8VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

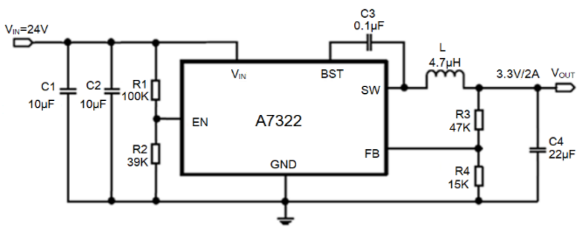
FEATURES

- Wide input voltage range: 4.2V to 28V
- 2A output current
- 0.8V reference voltage
- Low $R_{DS(ON)}$ integrated power MOSFET (180/110mΩ)
- 3μA(Max) shutdown current
- Integrated internal compensation
- High efficiency at light load
- Internal 1ms soft-start
- Cycle-by-cycle current limit
- Over-temperature protection with auto recovery
- Under voltage lockout(UVLO)
- Hiccup short circuit protection
- Available in PSOP8 package

APPLICATION

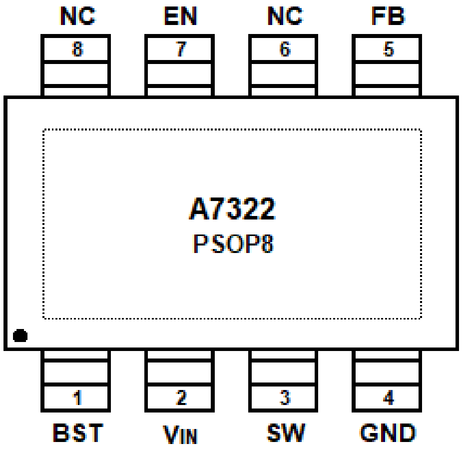
- Distributed power system
- Flat panel television and monitors
- STB (set-top-box)
- Networking, XDSL modem

TYPICAL APPLICATION



C_{IN} & C_{OUT} use ceramic capacitors application circuit

PIN DESCRIPTION



Top View

Pin #	Symbol	Description
1	BST	High side power transistor gate drive boost input.
2	V_{IN}	Power input. Bypass with a 22uF ceramic capacitor to GND.
3	SW	Power switching node to connect inductor.
4	GND	Ground
5	FB	Feedback input with reference voltage set to 0.8V.
6	NC	No connection
7	EN	Enable input. Set this pin to high level to enable the part, low level to disable.
8	NC	No connection
9	Thermal PAD	Ground. The exposed pad must be soldered to a large PCB area and connected to GND for maximum power dissipation.

ABSOLUTE MAXIMUM RATINGS

V_{IN}, Supply Voltage	-0.3V ~ 30V
V_{SW}, Switch Node Voltage	-0.3V ~ (V_{IN}+0.5V)
V_{BST}, Boost Voltage	V_{SW}-0.3V ~ V_{SW}+5V
V_{EN}, Enable Voltage	-0.3V ~ 12V
The Others Pins	-0.3V ~ 6V
Operating Temperature Range	-40°C ~ 85℃
Storage Temperature Range	-65°C ~ 150℃
Lead Temperature (soldering, 10s)	300℃

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED WORK CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{IN}		4.2	-	28	V
Ambient Temperature			-40	-	85	℃

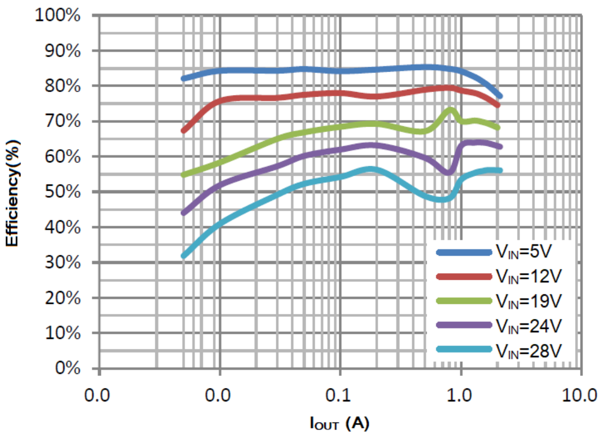
ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_A=25°C, unless otherwise stated

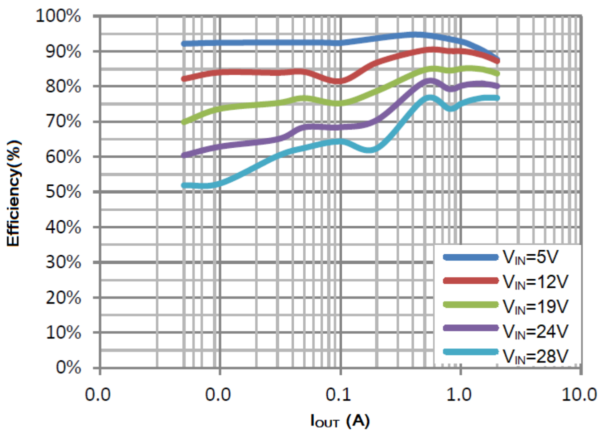
Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage Range		4.2	-	28	V
UVLO Threshold	V_{IN} rising	-	3.8	-	V
UVLO Hysteresis	V_{IN} falling	-	200	-	mV
Supply Current in Operation	V_{EN} = 5V, V_{FB} = 1V	-	150	-	uA
Supply Current in Shutdown	V_{EN} = 0V	-	1	-	uA
Regulated Feedback Voltage	3.8V ≤ V_{IN} ≤ 28V	0.784	0.8	0.816	V
High-side Switch on Resistance	V_{BST-SW} = 5V	-	180	-	mΩ
Low-side Switch on Resistance	V_{IN} = 5V	-	110	-	mΩ
High-side Switch Leakage Current	V_{EN} = 0V, V_{SW} = 0V	-	0.1	10	uA
Upper Switch Current Limit	Minimum duty cycle	3	-	-	A
Oscillation Frequency		-	500	-	kHz
Maximum Duty Cycle		-	93	-	%
Minimum on Time		-	100	-	ns
EN Input Voltage “H”		1.5	-	-	V
EN Input Voltage “L”		-	-	0.6	V
Thermal Shutdown		-	160	-	°C

TYPICAL PERFORMANCE CHARACTERISTICS

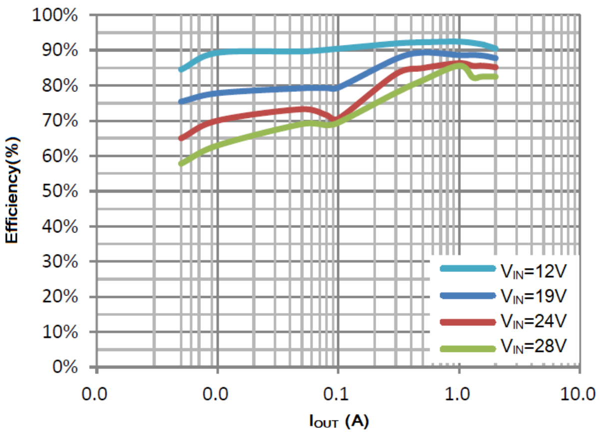
1. Efficiency vs. I_{OUT}, V_{OUT}=1.2V



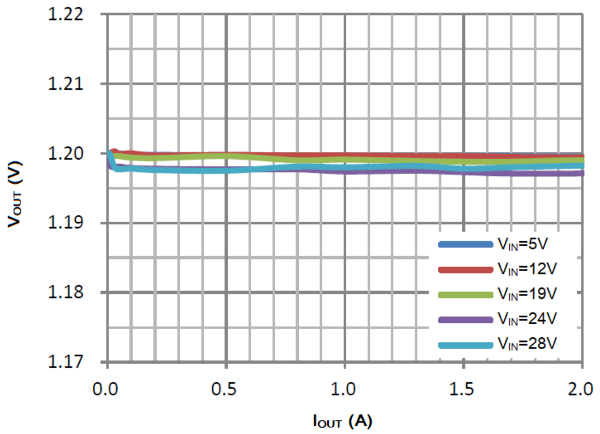
2. Efficiency vs. I_{OUT}, V_{OUT}=3.3V



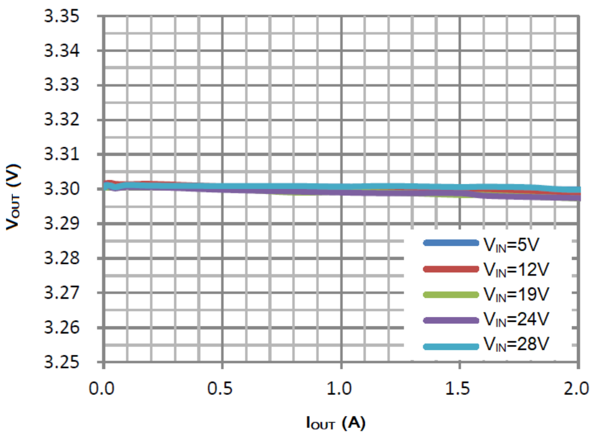
3. Efficiency vs. I_{OUT}, V_{OUT}=5.0V



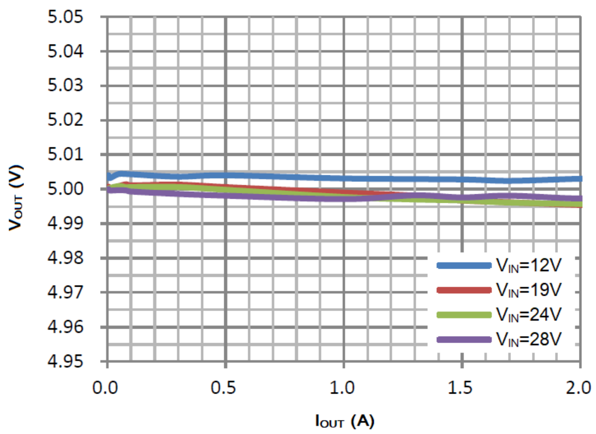
4. V_{OUT} vs. I_{OUT}, V_{OUT}=1.2V



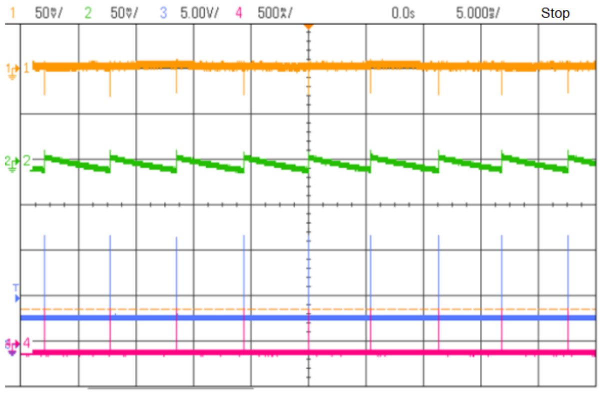
5. V_{OUT} vs. I_{OUT}, V_{OUT}=3.3V



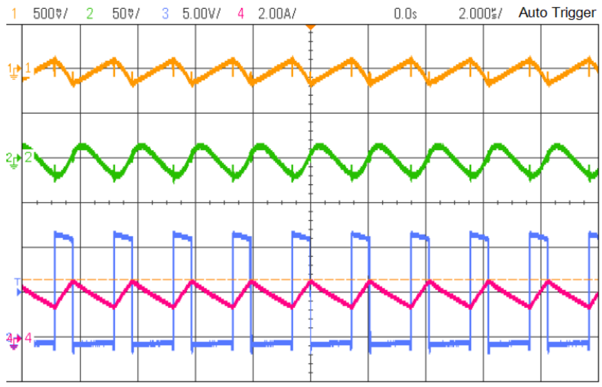
6. V_{OUT} vs. I_{OUT}, V_{OUT}=5.0V



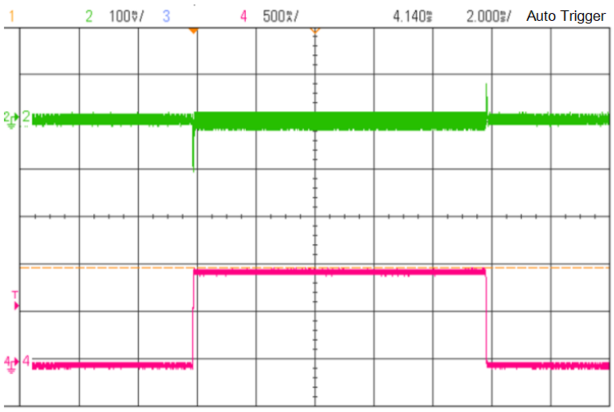
7. Steady State Waveform
V_{IN}=12V, V_{OUT}=3.3V, C_{IN}=C_{OUT}=10μF*2,
L=4.7μH, I_{OUT}=0A
Ch1—V_{IN}, Ch2—V_{OUT}, Ch3—V_{SW}, Ch4—I_{SW}



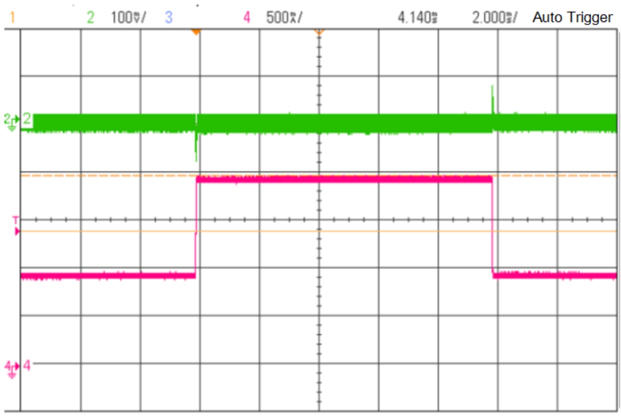
8. Steady State Waveform
V_{IN}=12V, V_{OUT}=3.3V, C_{IN}=C_{OUT}=10μF*2,
L=4.7μH, I_{OUT}=2A
Ch1—V_{IN}, Ch2—V_{OUT}, Ch3—V_{SW}, Ch4—I_{SW}



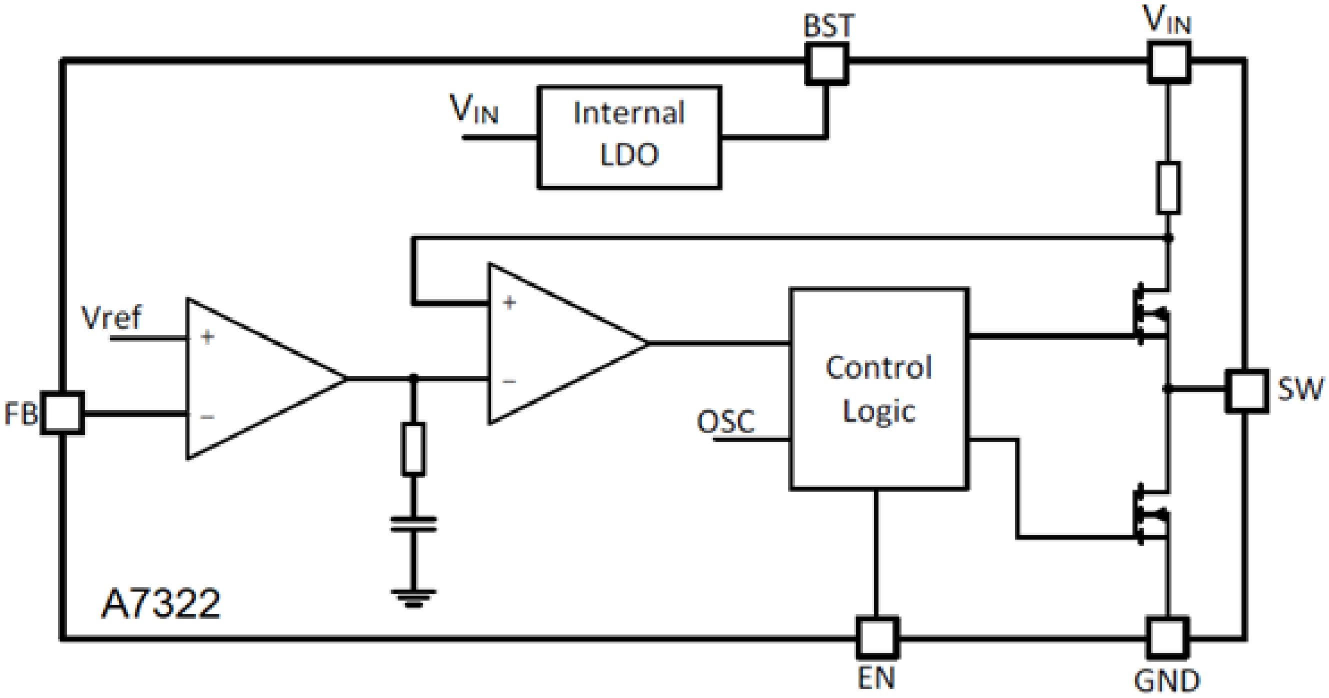
9. Load Transient
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0.01~1A
Ch2—V_{OUT}, Ch4—I_L



10. Load Transient
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=1~2A
Ch2—V_{OUT}, Ch4—I_L



BLOCK DIAGRAM



DETAILED INFORMATION

Loop Operation

The A7322 is a wide input range, high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 2A of output current, integrated with a 180/110mΩ synchronous MOSFET pair, eliminating the need for external diode. It uses a PWM current-mode control scheme. An error amplifier integrates error between the FB signal and the internal reference voltage. The output of the integrator is then compared to the sum of a current-sense signal and the slope compensation ramp. This operation generates a PWM signal that modulates the duty cycle of the power MOSFETs to achieve regulation for output voltage.

Internal soft-start

The soft-start is important for many applications because it eliminates power-up initialization problems. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

Over-current-protection and hiccup

The A7322 has a cycle-by-cycle over-current limit for when the inductor current peak value exceeds the set current-limit threshold. First, when the output voltage drops until FB falls below the Under-Voltage (UV) threshold (typically 300mV) to trigger a UV event, the A7322 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current to alleviate thermal issues and to protect the regulator. The A7322 exits hiccup mode once the overcurrent condition is removed.

Light load operation

Traditionally, a fixed constant frequency PWM DC-DC regulator always switches even when the output load is small. When energy is shuffling back and forth through the power MOSFETs, power is lost due to the finite RDSONs of the MOSFETs and parasitic capacitances. At light load, this loss is prominent and efficiency is therefore very low. A7322 employs a proprietary control scheme that improves efficiency in this situation by enabling the device into a power save mode during light load, thereby extending the range of high efficiency operation.

Startup and shutdown

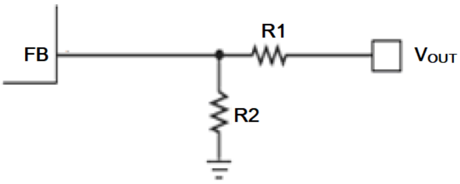
If both V_{IN} and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, V_{IN} low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATIONS INFORMATION

Setting output voltages

The external resistor divider is used to set the output voltage. The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. R2 is then given by:

$$R_2 = \frac{R_1}{V_{OUT} / V_{FB} - 1}$$



Selecting the inductor

Use a 2.2μH-to-6.8μH inductor with a DC current rating of at least 25% higher than the maximum load current for most applications. For most designs, derive the inductance value from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductor to improve efficiency.

Selecting the output capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

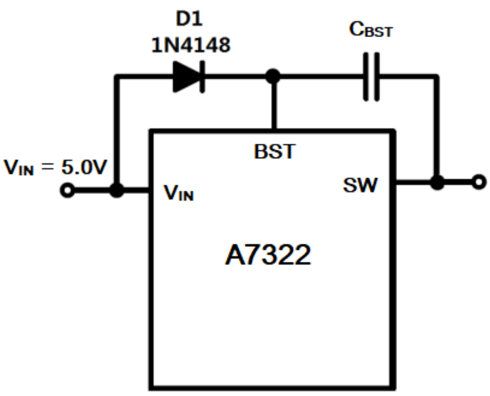
For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The A7322 can be optimized for a wide range of capacitance and ESR values.

Selecting the external boost diode

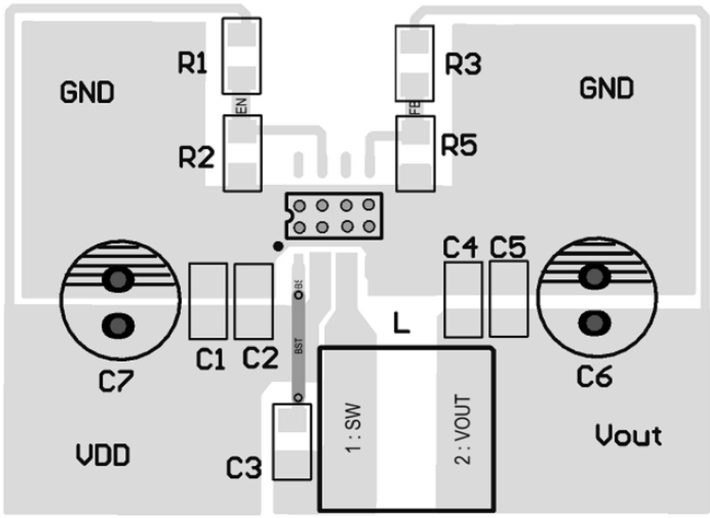
It is recommended to add an external Boost Diode to improve efficiency and stability in these situations when the input voltage is fixed at 5.0V.Any a readily and cheap diode can meet the need of these application such as 1N4148.



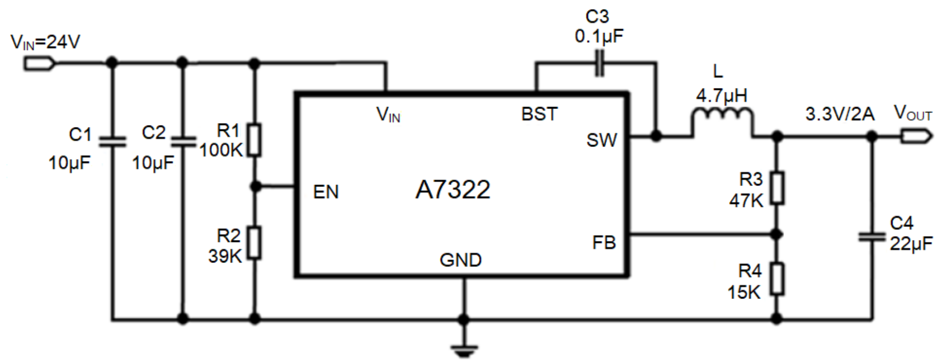
PCB LAYOUT RECOMMENDATION

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

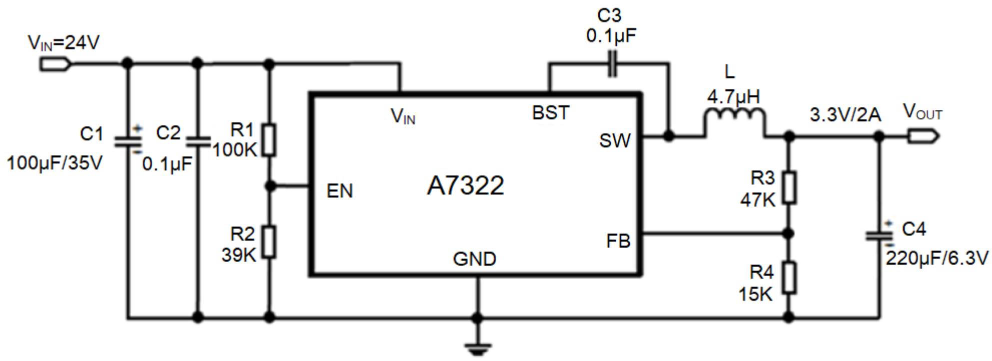
1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (SW).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.



TYPICAL APPLICATION



$_{IN}$ & C_{OUT} use ceramic capacitors application circuit



C_{IN} & C_{OUT} use electrolytic capacitors application circuit

NOTE: If the input voltage is below 12V, R1 can be set to 0K and R2 can be removed.

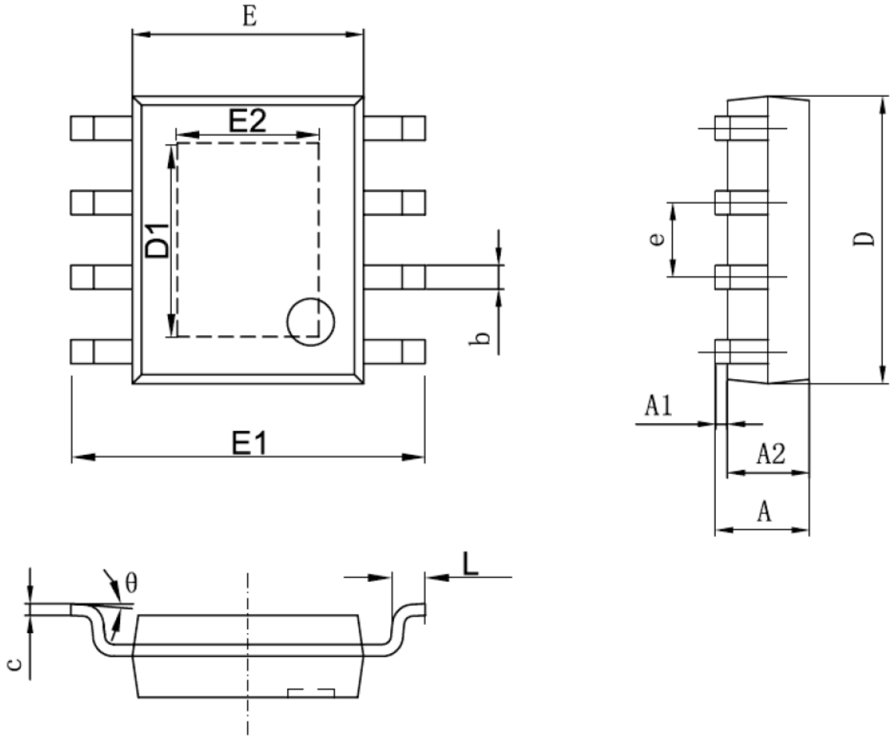
Table1. Recommended component values

V_{IN}=24V, the recommended BOM list is shows as below.

V_{OUT}	C1	C2	L	R3	R4	C4
5V			3.3uH-6.8uH	68K	13K	
3.3V			2.2uH-4.7uH	47K	15K	
2.8V	10uF/MLCC	10uF/MLCC	2.2uH-4.7uH	30K	12K	22uF/MLCC
2.5V			2.2uH-4.7uH	39K	18K	
1.8V			2.2uH-4.7uH	15K	12K	
1.2V			2.2uH-3.3uH	7.5K	15K	
5V			3.3uH-6.8uH	68K	13K	
3.3V			2.2uH-4.7uH	47K	15K	
2.8V	100uF/35V/ECL	0.1uF/MLCC	2.2uH-4.7uH	30K	12K	220uF/6.3V/ECL
2.5V			2.2uH-4.7uH	39K	18K	
1.8V			2.2uH-3.3uH	15K	12K	
1.2V			2.2uH-3.3uH	7.5K	15K	

PACKAGE INFORMATION

Dimension in PSOP8 Package (Unit: mm)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.350	1.70	0.053	0.067
A1	0.0	0.120	0.00	0.005
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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