Document Title

A7328 Data Sheet, Sub 1GHz FSK/GFSK Transmitter with 2K~2Mbps data rate

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue.	Dec. , 2009	Objective
0.1	Update register, pin order, etc.	Feb., 2010	Objective
0.2	Update RF parameters	Nov., 2010	Preliminary
0.3	Update recommended setting of Freq. deviation	Jan., 2011	Preliminary
0.4	Modify the tape reel information and the add Shenzhen office address.	Jul. 2011	Preliminary
1.0	Full production.	Jan., 2012	

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1. Typical Application

- ISM band Communication System
- Remote Control
- Wireless Home Automation
- Wireless audio/vedio streaming
- Wireless Toy and Gaming
- Wireless Alarm and Security

2. General Description

A7328 is a high performance and low cost sub 1GHz (433M / 868M / 915MHz) transmitter. With on chip fractional-N synthesizer, this device supports frequency hopping system in data rate (on-air) from 2Kbps up to 2Mbps. Additional device features such as built-in 64 bytes TX FIFO, CRC (CCITT CRC-16 or CRC-DNP), FEC (7, 4) Hamming code, Machester encoding and SPI interface are used to simplify system development and cost. In addition to FIFO mode, A7328 also supports direct mode with TX data clock. All features make this device easy to be used together with a low cost MCU (micro-controller).

For packet handling, A7328 has built-in 64-bytes TX FIFO (could be extended to 256 bytes) for data buffering and burst transmission, thermal sensor for monitoring relative temperature, one channel 8-bits ADC. Those functions are very easy to use while developing a wireless system. All features are integrated in a small QFN 4X4 16 pins package.

A7328's data rate is up to 2Mbps programmed by 3-wire or 4-wire SPI.For power saving, A7328 supports deep sleep mode, sleep mode, idle mode, and standby mode. For easy-to-use, A7328 has a unique SPI command set called **Strobe command** that are used to control A7328's state machine and registers. Based on Strobe commands, from power saving, TX delivery, frequency hopping to auto calibrations, MCU only needs to control A7328's registers and to send Strobe commands via SPI. In addition, A7328 has two general purpose I/O pins (GIO1 and CKO) to inform MCU its status so that MCU could either use polling or interrupt scheme to do radio control. Interface between MCU and A7328 is digital, it leads a simple way to develop a wireless system as well as transmission status.

3. Feature

- Small size (QFN4 X4, 16 pins).
- Support 433/868/915 MHz band.
- Support FSK/GFSK modulation.
- Programmable data rate from 2kbps to 2Mbps.
- Deelp sleep current (TBD).
- Sleep current (1.5 uA).
- TX current (35mA @ 10 dBm, 915MHz)
- TX current (32mA @ 10 dBm, 433.92MHz)
- On-Chip VCO and Fractional-N PLL.
- Programmable RF output power -20dBm ~ 10dBm.
- On chip regulator, supports input voltage 2.2 ~ 3.6V.
- Easy to use
  - Support 3-wire or 4-wire SPI.
  - Unique Strobe command via SPI.
  - Change frequency channel by ONE register setting.
  - Auto Calibrations.
  - Auto FEC by (7, 4) Hamming code.
  - Auto Manchester encoding.
  - Data Whitening for packet encryption.
  - 64 bytes TX FIFO.
  - Dynamic FIFO Length
  - Easy FIFO / Segment FIFO / FIFO Extension (up to 256 bytes).
- Support low cost crystal (12 / 16 MHz).
- Support low accuracy crystal within ± 50 ppm.
- Support crystal sharing (1 / 2 / 4 / 8MHz) to MCU.
- Built-in thermal sensor to monitor relative temperature.
- Built-in 1 channel 8-bits ADC (range 0.3 V ~ 1.5 V).
- Built-in Battery Detector.

4. PIN Configuration

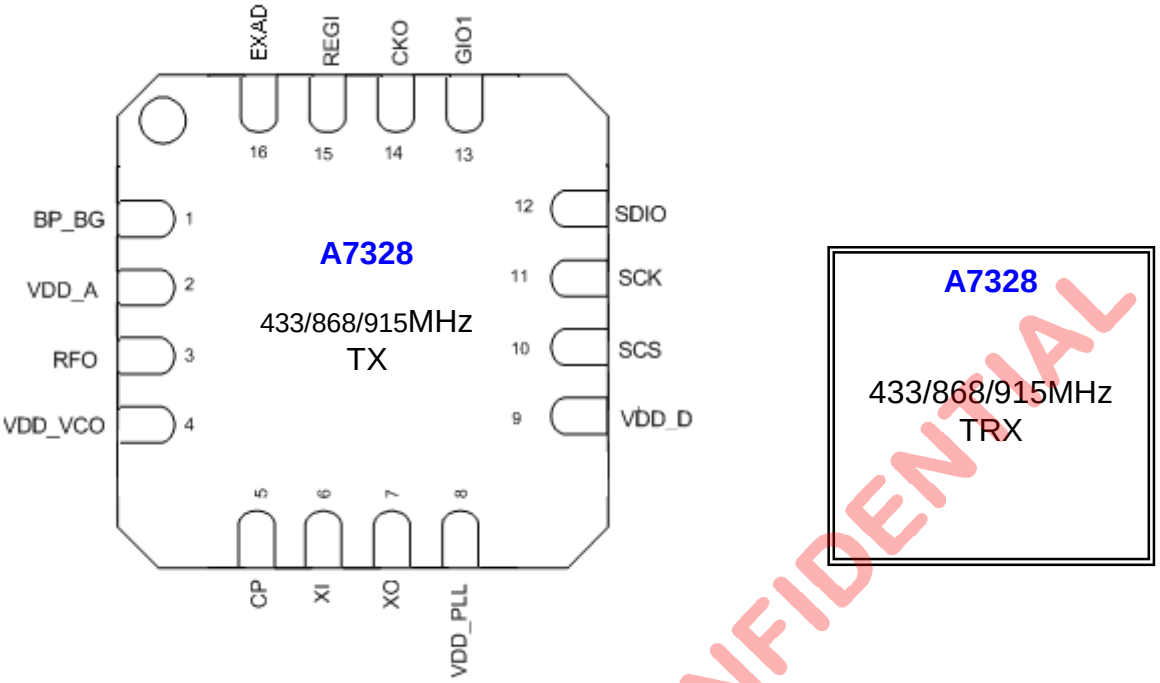


Figure 4.1 QFN 4x4 Package Top View

5. PIN Description (I: Input, O: Output, I/O: Input or Output, G: Ground, D: Digital)

Pin No.	Symbol	I/O	Function Description
1	BP_BG	O	Band-gap bypass. Connect to bypass capacitor.
2	VDD_A	O	Analog supply voltage output. Connect to bypass capacitor.
3	RFO	O	RF output. Connect to PA matching circuit.
4	VDD_VCO	I	VCO power supply input. Connect to VDD_A.
5	CP	O	Charge-pump output. Connect to loop filter.
6	XI	I	Crystal oscillator input.
7	XO	O	Crystal oscillator output.
8	VDD_PLL	O	PLL power supply input. Connect to VDD_A.
9	VDD_D	O	Digital supply voltage output. Connect to bypass capacitor.
10	SCS	DI	SPI chip select input.
11	SCK	DI	SPI clock input.
12	SDIO	DI/O	SPI data In/Out.
13	GIO1	DI/O	Multi-function IO / SPI data output.
14	CKO	DO	Multi-function clock output / WTR output.
15	REGI	I	Regulator input. Connect to VDD supply.
16	EXAD	I	External ADC input.
	Back side plate	**G**	**Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

6. Block Diagram

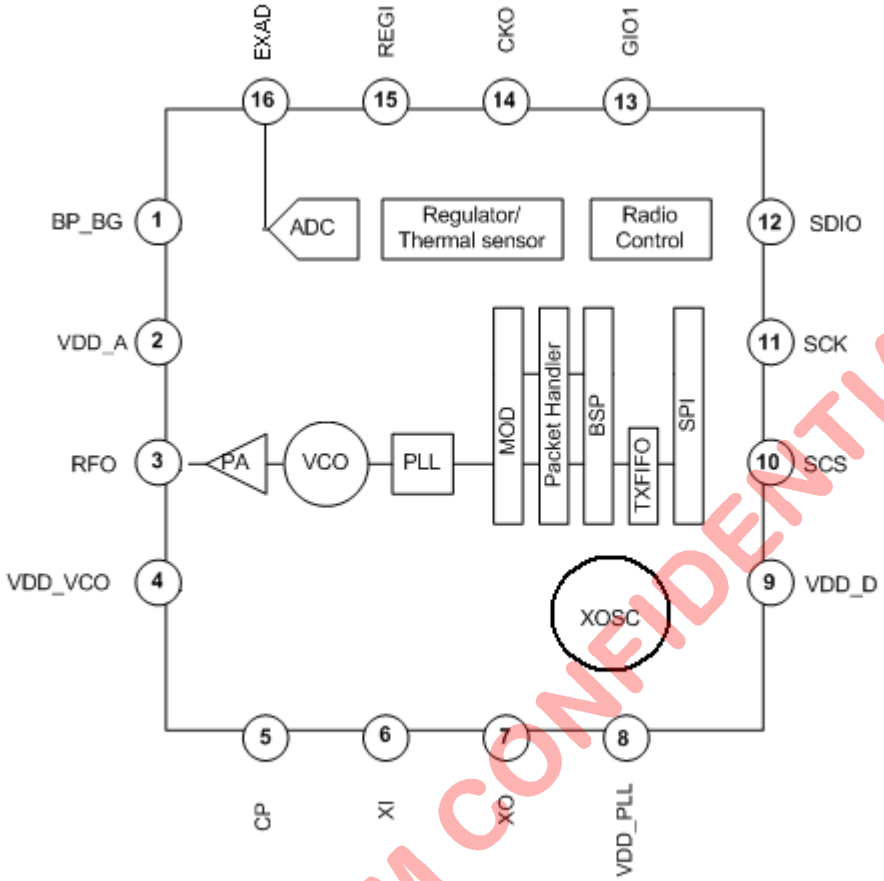


Figure 6.1 Block Diagram

7. Absolution Maximum Rating

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.9	V
Other I/O pins range	GND	-0.3 ~ VDD+0.3	V
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM *	± 2K	V
	MM *	± 100	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.

*Device is Moisture Sensitivity Level III (MSL 3).

8. Electrical Specifications

(Ta=25℃, VDD=3.3V, F_{XTAL} =16MHz, RF = 915MHz, with Matching Network and low pass filter, On Chip Regulator = 1.8V, unless otherwise noted.)

Parameter	Description	Minimum	Typical	Maximum	Unit
General					
Operating Temperature		-40		85	℃
Supply Voltage (VDD)	Regulator supply input	2.2	3.3	3.6	V
Current Consumption	Deep sleep Mode (1*) (no register retention)		TBD		uA
	Sleep Mode (regulator on) (1*)		1.5		uA
	Idle Mode (1*)		0.15		uA
	Standby Mode (XOSC on, Clock generator on)		2		mA
	PLL Mode		10		mA
	TX Mode @915MHz, 10dBm		32		mA
	TX Mode @868MHz, 10dBm		31		mA
	TX Mode @433MHz, 10dBm		32		mA
	TX Mode @915MHz, 1dBm		22		mA
	TX Mode @868MHz, 1dBm		20		mA
	TX Mode @433MHz, 1dBm		19		mA
Phase Locked Loop					
X'TAL Start-up Time (2*)			400		μs
PLL settling time			60		μs
X'TAL Frequency (F_{XTAL})			12, **16**		MHz
Xtal Series Resistance (ESR)	Cload =18pF			80	ohm
VCO Operation Frequency		1600		2000	MHz
PLL phase noise	Offset 100k (RBW = 1KHz, VBW=30Hz)		-85		dBc
	Offset 500k (RBW = 1KHz, VBW=100Hz)		-105		dBc
	Offset 2M (RBW = 1KHz, VBW=300Hz)		-110		dBc
Transmitter					
TX Power Range		-20	10		dBm
Data rate		2K	500K	2M	bps
Frequency Deviation	2Mbps		500		KHz
	1Mbps		500		KHz
	500Kbps		187.5		KHz
	≦100Kbps		46.875 or 93.75		KHz
Out Band Spurious Emission (4*) With HPF	25MHz~470MHz			-36	dBm
	470MHz~862MHz			-53	
	862MHz~ 1GHz			-36	
	above 1GHz			-30	
2nd harmonic	With LPF			-30	dBm
3rd harmonic	With LPF			-30	dBm
TX Settling Time (5*)	@C1=560pF,C2=10nF,R2=1K		80		μs
Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V

Note 1: In deep sleep mode, registers (data) have no retention. When digital I/O pins are configed as input, those pins shall NOT be floating but pull either high or low (SCS shall be pulled high only); otherwise, more leakage current will be occured.
Note 2: Refer to Delay Register II (17h) to set up crystal settling delay.
Note 3: Refer to Delay Register I (16h) to set up PDL (PLL settling delay).
Note 4: Measured with on board filter.
Note 5: Refer to Delay Register I (16h) to set up TDL delay

9. Control Register

A7328 has totally built-in 52 control registers that cover all radio control. MCU can access those control registers via 3-wire or 4-wire SPI (max. SPI data rate up to 10 Mbps). User can refer to chapter 10 for details about SPI interface. A7328 is simply controlled by registers and outputs its status to MCU by GIO1 pin or CKO pin (WTR).

9.1 Control Register Table

Address / Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h Mode	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
	R	-			CER	XER	PLLER		TRER
01h Mode control	W	DDPC			SPSS	WOTE		FMS	ADCM
	R	DDPC				WOTE		FMS	ADCM
02h Calc	R/W	-	-	-	VCC	VBC	VDC		
03h FIFO I	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
04h FIFO II	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
05h FIFO Data	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
06h ID Data	R/W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
07h RC OSC I	W	WWS_SL7	WWS_SL6	WWS_SL5	WWS_SL4	WWS_SL3	WWS_SL2	WWS_SL1	WWS_SL0
	R	CALWR	RCOC6	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
08h RC OSC II	W	WWS_SL9	WWS_SL8	WWS_AC5	WWS_AC4	WWS_AC3	WWS_AC2	WWS_AC1	WWS_AC0
09h RC OSC III	W	BBCKS1	BBCKS0	RCOT1	RCOT0	CALWR	RCOSC_E	TSEL	TWWS_E
0Ah CKO Pin	W	ECKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
0Bh GIO1 Pin I	W	-	-	GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
0Ch Data Rate Clock	W	IFS	--	GRC3	GRC1	GRC1	GRC0	CGS	XS
	R	IFS	--	GRC3	GRC2	GRC1	GRC0	-	-
0Dh PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
0Eh PLL II	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
0Fh PLL III	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
10h PLL IV	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
	R	0	AC14-FP14	AC13-FP13	AC12-FP12	AC11-FP11	AC10-FP10	AC9-FP9	AC8-FP8
11h PLL V	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
	R	AC7-FP7	AC6-FP6	AC5-FP5	AC4-FP4	AC3-FP3	AC2-FP2	AC1-FP1	AC0-FP0
12h Channel Group I	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
13h Channel Group II	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
14h TX I	W	GDR	GF	TMDE	TXDI	TME	FDP2	FDP1	FDP0
15h TX II	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
16h Delay I	W	DPR2	DPR1	DPR0	TDL1	TDL0	PDL2	PDL1	PDL0
17h Delay II	W	WSEL2	WSEL1	WSEL0				WOTS1	WOTS0
18h Xtal Load	W			CSXTL4	CSXTL3	CSXTL2	CSXTL1	CSXTL0	INTXC
19h PLL component	W	EDRL	HECS	STS	RGC1	RGC0	VRPL1	VRPL0	INTPRC

1Ah ADC control I	W	AVSEL1	AVSEL0	MVSEL1	MVSEL0			RMP1	RMP0
1Bh ADC Control II	W	---	CELS	XADPS	---	RADC	FSARS	XADS	CDM
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
1Ch Code I	W	MCS	WHTS	FECS	CRCS	IDL1	IDL0	PML1	PML0
1Dh Code II	W	HWCKS	WS6	WS5	WS4	WS3	WS2	WS1	WS0
1Eh PA Timing	W	-	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
1Fh VCO current Calibration	W	---	VCRLS	VBS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
	R	-	-	-	VCCF	VCB3	VCB2	VCB1	VCB0
20h VCO band Calibration I	W	DDC1	DDC0	MDAGS	CWS	MVBS	MVB2	MVB1	MVB0
	R	-	-	-	-	VBCF	VB2	VB1	VB0
21h VCO band Calibration II	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
22h VCO deviation Calibration I	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
23h VCO deviation Calibration II	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
24h VCO deviation Calibration III	W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
25h VCO modulation Delay	W	DMV1	DMV0	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
26h Battery detect	W	ECKS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BD_E
	R	-	RGV1	RGV0	BDF	BVT2	BVT1	BVT0	BD_E
27h TX test	W	ASKS	PAC1	PAC0	TDC1	TDC0	TBG2	TBG1	TBG0
28h Charge Pump Current I	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
29h Charge Pump Current II	W	CPTX3	CPTX2	CPTX1	CPTX0				
2Ah Crystal test	W	LVR	RGS	MD1	MD0	DBD	XCC	XCP1	XCP0
2Bh PLL test	W	SDMS	CPS	PRIC1	PRIC0	PRRC1	PRRC0	SDPW	NSDO
2Ch VCO test	W	DEVGD2	DEVGD1	DEVGD0	LOB1	LOB0	DIVRF1	DIVRF0	VCBS
2Dh RF Analog test	W		MDEN	OLM	CPH	CPCS	RFT2	RFT1	RFT0
2Eh Channel Select	W	DMGS		RSIS	ROSCS	CHD3	CHD2	CHD1	CHD0
2Fh VRB	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
30h SDR	W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
31h FCR	W	FCL1	FCL0	CRCINV	CRCDNP			---	---
3Eh FCB	W	FCB7	FCB6	FCB5	FCB4	FCB3	FCB2	FCB1	FCB0

Legend: - = unimplemented

9.2 Control Register Description

9.2.1 Mode Register (Address: 00h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R				CER	XER	PLLER		TRER
	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN		RESETN
Reset		--	--	--	--	--	--	--	--

RESETN: Write to this register by 0x00 to issue reset command, then it is auto clear

CER: Chip Status. (Read only)
[0]: Chip is disabled. [1]: Chip is enabled.

XER: Xtal Status. (Read only)
[0]: Crystal oscillator is disabled. [1]: Crystal oscillator is enabled.

PLLER: PLL Status. (Read only)
[0]: PLL is disabled. [1]: PLL is enabled after PLL strobe command.

TRER: TRX Status I. (Read only)
[0]: TRX is disabled. [1]: TRX is enabled.

9.2.2 Mode Control Register (Address: 01h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DDPC				WOTE		FMS	ADCM
	W	DDPC			SPSS	WOTE		FMS	ADCM
Reset		0				0		0	0

DDPC (Direct mode data pin control): Direct mode modem data can be accessed via SDIO pin.
[0]: Disable. **[1]:** Enable.

WOTE: Reserved for internal usage, shall be set to [0].

FMS: Direct/FIFO mode select.
[0]: Direct mode. **[1]:** FIFO mode.

ADCM: ADC measurement (Auto clear when done).
[0]: Disable. **[1]:** Enable.

ADCM	A7328 @ Standby mode
[0]	Disable ADC
[1]	Measure thermal sensor.

Refer to chapter 17 for details.

9.2.3 Calibration Control Register (Address: 02h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	--	--	--	VCC	VBC	VDC		
Reset		--	--	--	0	0	0		

VCC: VCO Current calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable .

VBC: VCO Bank calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VDC: VCO Deviation calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

9.2.4 FIFO Register I (Address: 03h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
	R								

Reset		0	0	1	1	1	1	1	1

FEP [7:0]: FIFO End Pointer for TX FIFO.

9.2.5 FIFO Register II (Address: 04h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
Reset		0	1	0	0	0	0	0	0

FPM [1:0]: FIFO Pointer Margin.
Used in FIFO extension mode.

PSA [5:0]: Used for Segment FIFO.
Used in FIFO segment mode.

Refer to chapter 16 for details.

9.2.6 FIFO DATA Register II (Address: 05h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
Reset		0	0	0	0	0	0	0	0

FIFO [7:0]: TX FIFO
TX FIFO is ok to do read and write.

Refer to chapter 16 for details.

9.2.7 ID DATA Register (Address: 06h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset		0	0	0	0	0	0	0	0

ID [7:0]: ID Data.
Programmble to 2 / 4 / 6 / 8 bytes according to IDL[1:0] (1Ch).
ID data is ok to do read and write.

Refer to section 10.6 and chapter 16 for details.

9.2.8 RC OSC Register I (Address: 07h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	RCOC6	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
	W	WWS_SL7	WWS_SL6	WWS_SL5	WWS_SL4	WWS_SL3	WWS_SL2	WWS_SL1	WWS_SL0
Reset		0	0	0	0	0	0	0	0

RCOC [6:0]: RC Oscillator Calibration result (read only).

WWS_SL [7:0]: Reserved.

9.2.9 RC OSC Register II (Address: 08h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	WWS_SL9	WWS_SL8	WWS_AC5	WWS_AC4	WWS_AC3	WWS_AC2	WWS_AC1	WWS_AC0
	R								
Reset		0	0	0	0	0	0	0	1

WWS_AC [5:0]: Reserved.

WWS_SL [9:8]: Reserved.

9.2.10 RC OSC Register III (Address: 09h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	BBCKS1	BBCKS0	RCOT1	RCOT0	CALWR	RCOSC_E	TSEL	TWWS_E
Reset		0	0	0	0	1	1	0	1

BBCKS [1:0]: Clock select for digital block. Recommend BBCKS = [00].
[00]: F_{SYCK} . **[01]:** F_{SYCK} / 2. **[10]:** F_{SYCK} / 4. **[11]:** F_{SYCK} / 8.

RCOT [1:0]: RC OSC current select.
[00]: 240nA
[01]: 280nA
[10]: 320nA
[11]: 360nA

CALWR: RC Oscillator Calibration Enable.
[0]: Disable. **[1]:** Enable.

RCOSC_E: RC Oscillator Enable.
[0]: Disable. **[1]:** Enable.

TSEL: Reserved.

WWS_E: Reserved.

9.2.11 CKO Pin Control Register (Address: 0Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	ECKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
Reset		1	0	1	1	1	0	1	0

ECKOE: CKO pin output enable.
[0]: Disable. **[1]:** Enable.

CKOS [3:0]: CKO pin output select.
[0000]: DCK (TX data clock).
[0001]: RCK (RX recovery clock).
[0010]: FPF (FIFO pointer flag).
[0011]: Logic OR gate by EOP, EOVBC, EOFBC, EOVCC, EOVDC and RSSC_OK. (Internal usage only).
[0100]: F_{SYCK} / 2.
[0101]: F_{SYCK} / 4.
[0110]: F_{SYCK} / 8.
[0111]: F_{SYCK} / 16.
[1000]: WCK.
[1001]: PF8M.
[1010]: ROSC.
[1011]: OKADCN.
[1100]: BDF.
[1101]: F_{SYCK} .
[1110]: **WTR.**
[1111]: Reserved.

CKOI: CKO pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

CKOE: CKO pin Output Enable.
[0]: High Z. **[1]:** Enable.

SCKI: SPI clock input invert.
[0]: Non-inverted input. **[1]:** Inverted input.

9.2.12 GIO1 Pin Control Register (Address: 0Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W			GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
Reset				0	0	0	0	0	1

GIO1S [3:0]: GIO1 pin function select.

GIO1S [3:0]	TX state
[0000]	**WTR** (Wait until TX finish)
[0001]	EOAC (end of access code)
[0010]	TMEO or TMEOD output
[0011]	Reserved.
[0100]	Reserved.
[0101]	Reserved.
[0110]	**SDO** (4 wires SPI data out)
[0111]	Direct mode data input.
[1000]	FMTDO (FIFO mode Data out)
[1001]	TXD (Direct mode data out)
[1010]	PDN_TX
[1011]	Reserved.
[1100]	EOADC
[1101]	Reserved.
[1110]	**BDF**
[11xx]	Reserved.

GIO1I: GIO1 pin output invert.
[0]: Non-inverted output. **[1]:** Inverted output.

GIO1OE: GIO1 pin output enable.
[0]: High Z. **[1]:** Enable.

9.2.13 Data Rate Clock Register (Address: 0Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	IFS		GRC3	GRC2	GRC1	GRC0	--	--
	W	IFS		GRC3	GRC2	GRC1	GRC0	CGS	XS
Reset		0		0	1	1	1	1	1

IFS: IF Frequency Select.
[0]: 500KHz. **[1]:** 2MHz.

GRC [3:0]: Generator Reference Counter.
Clock generation reference = $F_{CRYSTAL}$ / (GRC+1) = 2MHz.
Refer to chapter 13 for details.

CGS: Clock generator enable. Recommend CGS = [1].
[0]: Disable. **[1]:** Enable.

XS: Crystal oscillator select. Recommend XS = [1]
[0]: Use external clock. **[1]:** Use external crystal.

9.2.14 PLL Register I (Address: 0Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset		0	0	0	0	0	0	0	0

CHN [7:0]: RF LO channel number.

Refer to chapter 14 for details.

9.2.15 PLL Register II (Address: 0Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
Reset		0	0	1	0	1	1	1	0

DBL: Crystal frequency doubler enable.
[0]: Disable. $F_{XREF} = F_{XTAL}$. **[1]:** Enable. $F_{XREF} = 2 * F_{XTAL}$.

RRC [1:0]: RF PLL reference counter setting.

The PLL comparison frequency, $F_{PFD} = F_{CRYSTAL}*(DBL+1) / (RRC+1)$.

CHR [3:0]: PLL channel step setting.
Refer to chapter 14 for details.

9.2.16 PLL Register III (Address: 0Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
Reset		0	1	1	1	0	0	0	0

BIP [8:0]: LO base frequency integer part setting (write only).
BIP [8:0] are from address (0Eh) and (0Fh).

IP [8:0]: LO frequency integer part value (read only).
IP [8:0] are from address (0Eh) and (0Fh).

The wanted RF formula

$$F_{LO\_BASE} = \frac{1}{n} F_{PFD} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}})$$
$$= \frac{1}{n}(DBL+1) \cdot \frac{F_{XTAL}}{RRC[1:0]+1} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}})$$

where f_{dev} is the wanted TX frequency deviation.
Where n = 2 for MD = [10] or [11], 868M / 915MHz band
Where n = 4 for MD = [01], 433M band
Where n = 6 for MD = [00], 315MHz band

MD[1:0] is located at address 2Ah [Bit5, Bit4].

DBL and RRC[1:0] are located at address 0Eh.

Refer to chapter 14 for details.

9.2.17 PLL Register IV (Address: 10h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R		AC14/FP14	AC13/FP13	AC12/P12	AC11/ FP11	AC10/FP10	AC9/FP9	AC8/FP8
	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
Reset		1	1	0	0	0	0	0	0

9.2.18 PLL Register V (Address: 11h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	AC7/FP7	AC6/FP6	AC5/FP5	AC4/FP4	AC3/FP3	AC2/FP2	AC1/FP1	AC0/FP0
	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
Reset		0	0	0	0	0	1	0	0

BFP [15:0]: LO base frequency fractional part setting. ([0x0000] is forbidden.)
BFP [15:0] are from address (10h) and (11h),

AC [14:0]: Frequency compensation value (read only).

9.2.19 Channel Group Register I (Address: 12h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
Reset		0	0	1	1	1	1	0	0

CHGL [7:0]: PLL channel group low boundary setting.

9.2.20 Channel Group Register II (Address: 13h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
Reset		0	1	1	1	1	0	0	0

CHGH [7:0]: PLL channel group high boundary setting.

PLL frequency is divided into 3 groups:

	Channel
Group1	0 ~ CHGL-1
Group2	CHGL ~ CHGH-1
Group3	CHGH ~ 255

Note: Recommend to let each group have its own VCO current, bank and deviation calibration value to get the best RF performance.

9.2.21 TX Register I (Address: 14h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	GDR	GF	TMDE	TXDI	TME	FDP2	FDP1	FDP0
Reset		0	0	1	0	1	1	1	0

GDR: Gaussian Filter Oversampling Rate Select.
[0]: BT= 0.7 **[1]:** BT= 0.5

GF: Gaussian Filter Select.
[0]: Disable. **[1]:** Enable.

TMDE: TX Modulation Enable for VCO Modulation.
[0]: Disable. **[1]:** Enable.

TXDI: TX data invert. Recommend TXDI = [0].
[0]: Non-invert. **[1]:** Invert.

TME: TX modulation enable.
[0]: Disable. **[1]:** Enable.

FDP [2:0]: Frequency deviation power setting.

9.2.22 TX Register II (Address: 15h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset		1	1	0	0	0	0	0	0

FD [7:0]: Frequency deviation setting.

For both Gaussian filter is on (GS =1) or off（GS = 0）:

$$f_{dev} = \frac{1}{n} \cdot f_{PFD} \cdot FD[7:0] \cdot \frac{2^{(FDP[2:0]-1)}}{2^{16}} \quad \text{(unit: Hz)}$$

where f_{dev} is the wanted TX frequency deviation.

Where n = 2 for MD = [10] or [11], 868M / 915MHz band
Where n = 4 for MD = [01], 433M band
Where n = 6 for MD = [00], 315MHz band

MD[1:0] is VCO divider located at address 2Ah [Bit5, Bit4].

FDP[2:0] is located at address 14h [Bit2, Bit1, Bit0].

Freq. Band	Data Rate	FD[7:0]	Fdev (KHz)
915MHz	2Mbps	0x40	500

	1Mbps	0x40	500
	500Kbps	0x18	187.5
	≦100Kbps	0x0C	93.75 (larger Fdev setting)
	≦100Kbps	0x06	46.875 (smaller Fdev setting)

Freq. Band	Data Rate	FD[7:0]	Fdev (KHz)
868MHz	500Kbps	0x18	187.5
	≦100Kbps	0x0C	93.75 (larger Fdev setting)
	≦100Kbps	0x06	46.875 (smaller Fdev setting)

Freq. Band	Data Rate	FD[7:0]	Fdev (KHz)
433MHz	2Mbps	0x80	500
	1Mbps	0x80	500
	500Kbps	0x30	187.5
	≦100Kbps	0x18	93.75 (larger Fdev setting)
	≦100Kbps	0x0C	46.875 (smaller Fdev setting)

9.2.23 Delay Register I (Address: 16h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	DPR2	DPR1	DPR0	TDL1	TDL0	PDL2	PDL1	PDL0
Reset		0	0	0	1	0	0	1	0

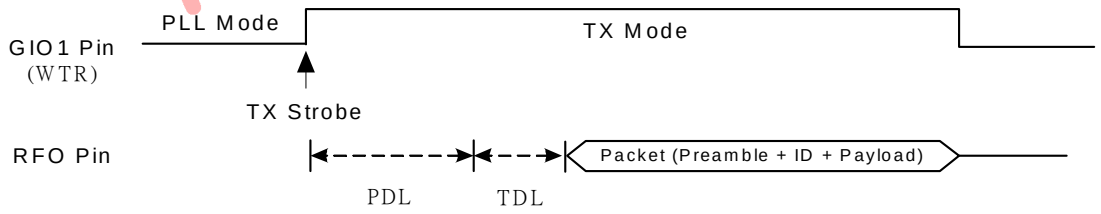
DPR [2:0]: Delay scale. Recommend DPR = [000].

TDL [1:0]: Delay for TRX settling from WPLL to TX/RX.
Delay= 20 * (TDL [1:0]+1)*(DPR [2:0]+1) us.

DPR [1:0]	TDL [1:0]	WPLL to TX	Note
00	00	20 us	
00	01	40 us	
00	10	60 us	
00	**11**	**80 us**	**Recommend**

PDL [2:0]: Delay for TX settling from PLL to WPLL.
Delay= 20 * (PDL [2:0]+1)*(DPR [1:0]+1) us.

DPR [1:0]	PDL [2:0]	PLL to WPLL (LO freq changed)	Note
00	001	40 us	
00	**010**	**60 us**	**Recommend**
00	011	80 us	
00	100	100 us	

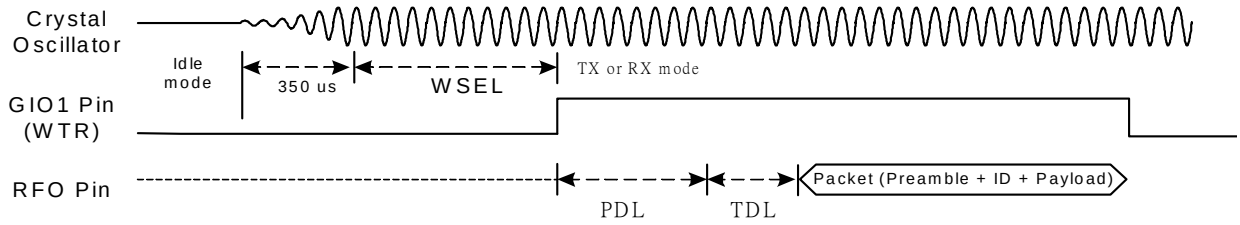


9.2.24 Delay Register II (Address: 17h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	WSEL2	WSEL1	WSEL0				WOTS1	WOTS0
Reset		0	1	0					

WSEL [2:0]: XTAL settling delay setting (200us ~ 2.5ms). Recommend WSEL = [010].

[000]: 200us. **[001]:** 400us. **[010]:** 600us, **[011]:** 800us.
[100]: 1ms. **[101]:** 1.5ms. **[110]:** 2ms. **[111]:** 2.5ms.



WOTS [1:0]: Resered. Shall be set to [00]

9.2.25 XTAL load (Address: 18h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R								
	W			CSXTL4	CSXTL3	CSXTL2	CSXTL1	CSXTL0	INTXC
Reset			0	0	0	0	0	0	0

CSXTAL[4:0]: Reserved. Shall be set to [00000]

INTXC: Reseved. Shall be set to [0]

9.2.26 PLL component (Address: 19h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	EDRL	HECS	STS	RGC1	RGC0	VRPL1	VRPL0	INTPRC
Reset		0	0	0	0	0	0	0	0

EDRL: Enable Dynamic FIFO Length
[0]: Disable. **[1]:** Enable.

HECS: Header CRC-8 Enable.
[0]: Disbale. **[1]:** enable
If HECS = 1, HEC (one byte) is added into TX-Packet.
Refer to chapter 16 for details.

STS: Reserved for internal usage. Recommend STS = [0].

RGC[1:0]: Reserved. Recommend RGC = [00].

VRPL[1:0]: Reserved. Recommend VRPL = [00].

INTPRC: Reserved. Recommend INTPRC = [0].

9.2.27 ADC control Register I (Address: 1Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R								
	W	AVSEL1	AVSEL0	MVSEL1	MVSEL0			RMP1	RMP0
Reset		0	0	0	0			0	0

AVSEL [1:0]: ADC average mode. Recommend AVSEL = [10].
[00]: No average. **[01]:** 2. **[10]:** 4. **[11]:** 8.

MVSEL [1:0]: ADC average mode for VCO calibration. Recommend MVSEL = [10].
[00]: 8. **[01]:** 16. **[10]:** 32. **[11]:** 64.

RMP[1:0]: TX ramp up scaler. Recommend RMP= [00].
[00]: 1. **[01]:** 2. **[10]:** 4. **[11]:** 8.

9.2.28 ADC control Register II (Address: 1Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	W		CELS	XADPS		RADC	FSARS	XADS	CDM
Reset		0	0	0	0	0	0	0	0

ADC [7:0]: ADC digital output value (read only).
ADC input voltage= 0.3 + 1.2 * ADC [7:0] / 256 V.

CELS: Bandgap Selection for Digital Regulator. Recommend CELS = [1].
[0]: Analog. **[1]:** Digital.

XADPS: External ADC Input Pin Selection.
[0]: Disable. **[1]:** Enable.

RADC: ADC Read Out Average Mode.
[0]: 1, 2, 4, 8 average mode. If RADC = 0, ADC average is set by AVSEL[1:0] (1Ah).
[1]: 8, 16, 32, 64 average mode. If RADC = 1, ADC average is set by MVSEL[1:0] (1Ah).

FSARS: ADC Clock Select.
[0]: 4MHz. **[1]:** 8MHz.

XADS: External ADC Input Signal Select.
[0]: Disable. **[1]:** Enable.

CDM: Temperature measurement mode. Recommend CDM = [0].
[0]: Single mode. **[1]:** Continuous mode.

9.2.29 Code Register I (Address: 1Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	MCS	WHTS	FECS	CRCS	IDL1	IDL0	PML1	PML0
Reset		0	0	0	0	0	1	1	1

MSC: Manchester Enable.
[0]: Disable. **[1]:** Enable.

WHTS: Data Whitening (Data Encryption) Select.
[0]: Disable. **[1]:** Enable (The data is whitening by multiplying PN7).

FECS: FEC Select.
[0]: Disable. **[1]:** Enable (The FEC is (7, 4) Hamming code).

CRCS: CRC Select.
[0]: Disable. **[1]:** Enable. The CRC is set by CRCDNP (31h) for either CCITT-16 CRC or CRC-DNP

IDL[1:0]: ID Code Length Select. Recommend IDL= [01].
[00]: 2 bytes. **[01]:** 4 bytes. **[10]:** 6 bytes. **[11]:** 8 bytes.

PML [1:0]: Preamble Length Select. Recommend PML= [11].
[00]: 1 byte. **[01]:** 2 bytes. **[10]:** 3 bytes. **[11]:** 4 bytes.

9.2.30 Code Register II (Address: 1Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	HWCKS	WS6	WS5	WS4	WS3	WS2	WS1	WS0
Reset		0	0	1	0	1	0	1	0

HWCKS: RTC clock select.
[0]:4.096KHZ. **[1]:**2.048KHZ.

WS [6:0]: Data Whitening Seed (data encryption key).

9.2.31 PA Timing Control Register (Address: 1Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--					

	W		TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
Reset			0	0	1	0	0	1	0

TRT [2:0]: TX Ramp down discharge current select. Recommand TRT = [111].

ASMV [2:0]: TX Ramp up timing select. Recommand ASMV=[111].
[000]: 2us. **[001]:** 4us. **[010]:** 6us. **[011]:** 8us. **[100]:** 10us, **[101]:** 12us. **[110]:** 14us. **[111]:** 16us.

Actual TX ramp up time = ASMV [2:0] x RMP[1:0]

AMVS : TX Ramp Up Enable. Recommand AMVS=[1].
[0]: Disable. **[1]:** Enable.

9.2.32 VCO Current Calibration Register (Address: 1Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
	W	--	VCRLS	VBS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
Reset		--	0	0	0	0	1	0	0

VCCF : VCO Current Auto Calibration Flag.
[0]: Pass. **[1]:** Fail.

VCB [3:0]: VCO Current Bank Calibration result.
If MVCS= 0, VCB[3:0] is auto calibration result.
If MVCS= 1, VCB[3:0] is manual calibration setting.

VCRLS : VCO Current Resistor Select. Recommand VCRLS=[0].
[0]: low current. **[1]:** high current.

VBS : VCO Band Select.
[0]: 915MHz. **[1]:** 868MHz / 433MHz.

MVCS: VCO current calibration select. Recommend MVCS = [0].
[0]: Auto. **[1]:** Manual.

VCOC [3:0]: VCO Current Bank Manual Calibration setting.
Refer to chapter 15 for details.

9.2.33 VCO Bank Calibration Register I (Address: 20h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	--	VBCF	VB2	VB1	VB0
	W	DCD1	DCD0	MDAGS	CWS	MVBS	MVB2	MVB1	MVB0
Reset		1	1	0	1	0	1	0	0

VBCF: VCO Band Auto Calibration Flag.
[0]: Pass. **[1]:** Fail.

VB [2:0]: VCO Bank Calibration Value (read only).
If MVBS= 0, VB[2:0] is auto calibration result.
If MVBS= 1, VB[2:0] is manual calibration setting.

DCD [1:0]: VCO Deviation Calibration Delay.
Delay time = PDL (Delay Register I, 17h) × (DCD + 1).
Please refer to AMICCOM reference code for optimization in different RF band.

CWS: Clock Disable for VCO Modulation. Recommend CWS = [0].
[0]: Enable. **[1]:** Disable.

DAGS: DAG Calibration Value Select. Recommend DAGS = [0].
[0]: Auto. **[1]:** Manual.

MVBS: VCO Bank Calibration Select. Recommend MVBS = [0].
[0]: Auto. **[1]:** Manual.

MVB [2:0]: Manual VCO Band Setting.
VCO frequency increases when MVB increases.

Refer to chapter 15 for details.

9.2.34 VCO Bank Calibration Register II (Address: 21h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
Reset		1	0	0	0	0	0	0	0

ADAG [7:0]: Auto DAG Calibration result.

MDAG [7:0]: DAG Manual Setting Value. Recommend DAGM = [0x80].

9.2.35 VCO Deviation Calibration Register I (Address: 22h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
Reset		0	1	1	1	0	0	0	0

DEVA [7:0]: Deviation Calibration result (read only).
If MVDS (23h) = 0, DEVA [7:0] is auto calibration result ((DEVC / 8) × (DEVS + 1)).
If MVDS (23h) = 1, DEVA [7:0] is manual calibration result (DEVM [6:0]).

DEVS [3:0]: Deviation Output Scaling.

Freq. Band	Data Rate	DEVS[3:0]
915MHz	2Mbps	0111
	1Mbps	0101
	500Kbps	0111
	100Kbps	0111

Freq. Band	Data Rate	DEVS[3:0]
868MHz	500Kbps	0011
	100Kbps	0111

Freq. Band	Data Rate	DEVS[3:0]
433MHz	2Mbps	0111
	1Mbps	0111
	500Kbps	0111
	100Kbps	0101

DAMR_M: DAMR Manual Enable. Recommend DAMR_M = [0].
[0]: Disable. **[1]:** Enable.

VMTE_M: VMT Manual Enable. Recommend VMTE_M = [0].
[0]: Disable. **[1]:** Enable.

VMS_M: VM Manual Enable. Recommend VMS_M = [0].
[0]: Disable. **[1]:** Enable.

MSEL: VMS, VMTE and DAMR control select. Recommend MSEL = [0].
[0]: Auto control. **[1]:** Manual control.

9.2.36 VCO Deviation Calibration Register II (Address: 23h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
Reset		0	0	1	0	1	0	0	0

ADEV [7:0]: VCO Deviation Auto Calibration result (read only).

MVDS: VCO Deviation Calibration Select. Recommend MVDS = [0].

[0]: Auto. **[1]:** Manual.

MDEV [6:0]: VCO Deviation Manual Calibration setting.
Refer to chapter 15 for details.

9.2.37 VCO Deviation Calibration Register III (Address: 24h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W/R	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
Reset		1	0	0	0	0	0	0	0

VMG [7:0]: VM Center Value for Deviation Calibration. Recommend VMG[7:0] = [0x80].

9.2.38 VCO Modulation Delay Register (Address: 25h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	DMV1	DMV0	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
Reset		1	0	0	0	0	0	0	0

DMV [1:0]: Demodulator D/A Voltage Range Select.
[00]: 1/32*1.2. **[01]:** 1/16*1.2. **[10]:** 1/8*1.2. **[11]:** 1/4*1.2.

DEV2:0]: VCO Modulation Data Delay by 8x over-sampling Clock.

DEVD [2:0]: VCO Modulation Data Delay by XCPCK Clock. Recommend DEVD = [001].

RF Band	Data Rate	DMV[1:0]	DEVFD[2:0]	DEVD[2:0]
915MHz	2Mbps	11	100	001
	1Mbps	11	100	001
	500Kbps	10	011	000
	100Kbps	10	011	000

RF Band	Data Rate	DMV[1:0]	DEVFD[2:0]	DEVD[2:0]
868MHz	500Kbps	10	011	000
	100Kbps	10	011	000

RF Band	Data Rate	DMV[1:0]	DEVFD[2:0]	DEVD[2:0]
433MHz	2Mbps	11	011	010
	1Mbps	11	011	010
	500Kbps	10	011	000
	100Kbps	10	011	000

9.2.39 Battery Detect Register (Address: 26h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	RGV1	RGV0	BDF	BVT2	BVT1	BVT0	BD_E
	W	ECKS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BD_E
Reset		0	1	0	0	0	1	1	0

ECKS : Clock phae delay selection. Recommend ECKS = [0].
[0]: no delay. **[1]:** delay 1/2 cycle.

RGV [1:0]: Regulator Voltage Select. Recommend RGV = [11].
[00]: 2.1V. **[01]:** 2.0V. **[10]:** 1.9V. **[11]:** 1.8V.

To gain a little bit more TX power, user can set RGV larger than 1.8V

BDF : Low Battery Detection Flag (read only).
[0]: battery low. **[1]:** battery high.

QDS: VDD_A Quick Discharge Select. Recommend QDS = [1].
[0]: Disable. **[1]:** Enable.

BVT [2:0]: Battery Voltage Threshold Select.

[000]: 2.1V, **[001]:** 2.2V. **[010]:** 2.3V. **[011]:** 2.4V. **[100]:** 2.5V. **[101]:** 2.6V. **[110]:** 2.7V. **[111]:** 2.8V.
(Typical +-0.1V detection inaccuracy.)

BD_E: Battery Detect Enable.
[0]: Disable. **[1]:** Enable. It will be clear after battery detection is triggered.

9.2.40 TX Test Register (Address: 27h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	ASKS	PAC1	PAC0	TDC1	TDC0	TBG2	TBG1	TBG0
Reset		0	0	1	1	0	1	1	1

PAC [1:0]: PA Current Setting.

TDC [1:0]: TX Current Setting.

TBG [2:0]: TX Buffer Gain Setting.

RF Band	Typical power (dBm)	TBG	TDC	PAC	Typical current
915MHz	13	111	11	11	43 mA
	11	111	11	00	34 mA
	6	110	01	01	27 mA
	1	101	01	00	22 mA
	-9	011	00	00	18 mA
	-15	001	00	00	17.3 mA
	-18	000	00	00	17.2 mA

RF Band	Typical power (dBm)	TBG	TDC	PAC	Typical current
868MHz	12	111	11	11	38 mA
	11	111	11	10	34 mA
	10	111	11	00	31 mA
	8	110	11	00	28 mA
	6	110	01	01	25 mA
	4	101	11	00	24 mA
	1	101	01	00	20 mA
	-5	101	00	00	17 mA
	-15	001	00	00	15.5 mA
	-18.5	000	00	00	15.4 mA

RF Band	Typical power (dBm)	TBG	TDC	PAC	Typical current
433MHz	12	111	11	11	38 mA
	11	111	11	10	33 mA
	10	111	10	01	32 mA
	9	110	11	00	30 mA
	7	110	00	01	26 mA
	4	101	00	01	22 mA
	1	100	00	01	19 mA
	-4	011	00	00	16 mA

	-8	**010**	**00**	**00**	**15 mA**
	-11	**001**	**00**	**00**	**14.5 mA**
	-15	**000**	**00**	**00**	**14 mA**

Also, refer to App. Note for more details.

9.2.41 Charge Pump Current Register I (Address: 28h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
Reset		1	1	1	1	1	1	1	1

CPM [3:0]: Charge Pump Current Setting for VM loop. Recommend CPM = [1111].
Charge pump current = (CPM + 1) / 16 mA.

CPT [3:0]: Charge Pump Current Setting for VT loop. Recommend CPT = [0100].
Charge pump current = (CPT + 1) / 16 mA.

9.2.42 Charge Pump Current Register II (Address: 29h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CPTX3	CPTX2	CPTX1	CPTX0				
Reset		0	0	1	0				

CPTX [3:0]: Charge Pump Current Setting for TX mode.
Charge pump current = (CPTX + 1) / 16 mA.

RF Band	Data Rate	CPTX[3:0]
915MHz	2Mbps	0111
	1Mbps	0111
	500Kbps	0111
	100Kbps	1111

RF Band	Data Rate	CPTX[3:0]
868MHz	500Kbps	0111
	100Kbps	1111

RF Band	Data Rate	CPTX[3:0]
433MHz	2Mbps	0010
	1Mbps	0010
	500Kbps	0111
	100Kbps	1111

9.2.43 Crystal Test Register (Address: 2Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	LVR	RGS	MD1	MD0	DBD	XCC	XCP1	XCP0
Reset		0	0	1	0	0	1	0	1

LVR : Low Power Bandgap Select.

RGS : Low Power Regulator Voltage Select.

LVR	RGS	Low Power Regulator Voltage	Note
0	0	3/5 *REGI	
0	1	3/4 * REGI	
1	0	1.8 V	Recommended
1	1	1.6 V	

MD [1:0]: VCO Divider Select.
[00]: 1/6. **[01]:** 1/4. **[10]:** 1/2. **[11]:** 1/2.

RF Band	VBS (25h)	MD [1:0]	Note

315MHz	0	00	
433MHz	1	01	
868MHz	1	11or 10	
915MHz	0	11 or 10	

DBD : Crystal Frequency Doubler High Level Pulse Width Select. Recommend DBD = [0].
[0]: about 8 ns. **[1]:** about 16 ns.

XCC : Crystal Startup Current Selection. Recommend XCC = [1].
[0]: 0.7 mA. **[1]:** 1.5 mA.

XCP [1:0]: Crystal Oscillator Regulated Couple Setting. Recommend XCP = [00].
[00]: 1.5mA. **[01]:** 0.5mA. **[10]:** 0.35mA. **[11]:** 0.3mA.

9.2.44 PLL Test Register (Address: 2Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	SDMS	CPS	PRIC1	PRIC0	PRRC1	PRRC0	SDPW	NSDO
Reset		1	1	0	1	0	0	0	1

SMDS: Reserved. Shall be set to [0].

CPS : Charge Pump Select. Shall be set to [1].
[0]: charge-pump tri-state. **[1]:** Normal.

PRIC [1:0]: Prescaler IF Part Current Setting. Shall be set to [01].
[00]: 0.95mA. **[01]:** 1.05mA. **[10]:** 1.15mA. **[11]:** 1.25mA.

PRRC [1:0]: Prescaler RF Part Current Setting. Shall be set to [00].
[00]: 1.0mA. **[01]:** 1.2mA. **[10]:** 1.4mA. **[11]:** 1.6mA.

SDPW : Clock Delay For Sigma Delta Modulator. Shall be set to [0].
[0]: 13 ns. **[1]:** 26 ns.

NSDO : Sigma Delta Order Setting. Shall be set to [1].
[0]: order 2. **[1]:** order 3.

9.2.45 VCO Test Register (Address: 2Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	DEVGD2	DEVGD1	DEVGD0	LOB1	LOB0	DIVRF1	DIVRF0	VCBS
Reset		0	0	0	0	0	0	0	0

DEVGD [2:0]: Sigma Delta Modulator Data Delay Setting. Recommend DEVGD = [000].

LOB [1:0]: LO Buffer Current Select. Shall be set to [10].
[00]: 0.6mA. **[01]:** 0.75mA. **[10]:** 0.9mA. **[11]:** 1.05mA.

DIVRF [1:0]: RF divider Current Select. Shall be set to [00].
[00]: 1.2mA. **[01]:** 1.5mA. **[10]:** 1.8mA. **[11]:** 2.1mA.

VCBS : VCO Buffer Current Setting. Shall be set to [0].
[0]: 1mA. **[1]:** 1.5mA.

9.2.46 RF Analog Test Register (Address: 2Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W		MDEN	OLM	CPH	CPCS	RFT2	RFT1	RFT0
Reset			0	0	0	0	0	0	0

MDEN : Use for Manual VCO Calibration. Shall be set to [0].

OLM : Open Loop Modulation Enable. Shall be set to [0].
[0]: Disable. **[1]:** Enable.

CPH : Charge Pump High Current. Shall be set to [0].
[0]: Normal. **[1]:** High.

CPCS : Charge Pump Current Select. Shall be set to [1].

RFT [2:0]: RF Analog Pin Configuration. Recommend RFT= [000].

{XADS, RFT[2:0]}	BP_BG (Pin 1)	XADI
[000]	Band-gap voltage	For external AD input.
[001]	Analog temperature voltage	Analog temperature voltage
[010]	External ADC input source	For external AD input.
[011]	Internal DA output	Internal DA output
[100]	Reserved	Reserved
[101]	Reserved	Reserved
[110]	Reserved	Reserved
[111]	Reserved	Reserved

9.2.47 Channel Selct Register (Address: 2Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
Reset		0	1	0	0	0	1	0	0

CHI [3:0]: Auto IF Offset Channel Number Setting.
CHI = [0001] for 500K mode.
CHI = [0111] for 2M mode.

$F_{CHSP} \times (CHI + 1) = F_{IF}$

CHD [3:0]: Channel Frequency Offset for Deviation Calibration.
CHD = [0101] for 500K mode.
CHD = [0111] for 2M mode.

Offset channel number = +/- (CHD + 1).

9.2.48 VRB Register (Address: 2Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
Reset		0	0	0	0	0	0	0	0

VTRB [3:0]: Resistor Bank for VT RC Filtering. Shall be set to [0000].

VMRB [3:0]: Resistor Bank for VM RC Filtering. Shall be set to [0000].

9.2.49 Data Rate Divider Register (Address: 30h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
Reset		0	0	0	0	0	0	0	0

SDR [1:0]: Data Rate Setting.
Data rate = F_{IF} / (SDR+1).

IFS (0Dh)	F_{IF} (Hz)	SDR [7:0]	Data Rate
1	2M	0x00	2M
1	2M	0x01	1M
0	500K	0x00	500K
0	500K	0x01	250K
0	500K	0x03	125K
0	500K	0x04	100K

9.2.50 FCR Register (Address: 31h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FC1	FC0	CRCINV	CRCDNP			TXCS	VTBS
Reset		0	0	0	0			0	0

FCL [1:0] : Frame Control Length.
[00]: No Frame Control
[01]: 1 byte Frame Control. (FCB0), refer to 3Dh.
[10]: 2 byte Frame control. (FCB0+FCB1), refer to 3Dh.
[11]: 4 byte Frame control. (FCB0+FCB1+FCB2+FCB3), refer to 3Dh.

CRCINV: CRC Inverted Select.
[0]: normal. **[1]:** inverted.

CRCDNP: CRC Mode Select.
[0]: CRC-CCITT ($X^{16}+ X^{12}+ X^5+ 1$). **[1]:** CRC-DNP ($X^{16}+ X^{13}+ X^{12}+ X^{11}+ X^{10}+ X^8+ X^6+ X^5+ X^2+ 1$).

10. SPI

A7328 only supports one SPI bus with maximum data rate 10Mbps. MCU should assert SCS pin low (SPI chip select) to active accessing of A7328. Via SPI bus, user can access **control registers** and issue **Strobe command**. Figure 10.1 gives an overview of SPI access manners.

3-wire SPI (SCS, SCK and SDIO) or 4-wire SPI (SCS, SCK, SDIO and GIO1) configuration is provided. For 3-wire SPI, SDIO pin is configured as bi-direction to be data input and output. For 4-wire SPI, SDIO pin is data input and GIO1 pin is data output. In such case, GIO1S (0bh) should be set to [0110].

For SPI write operation, SDIO pin is latched into A7328 at the rising edge of SCK. For SPI read operation, if input address is latched by A7328, data output is aligned at falling edge of SCK. Therefore, MCU can latch data output at the rising edge of SCK.

To control A7328's internal state machine, it is very easy to send Strobe command via SPI bus. The Strobe command is a unique command set with total 8 commands. See section 10.3, 10.4 and 10.5 for details.

	SPI chip select	Data In	Data Out
3-Wire SPI	SCS pin = 0	SDIO pin	SDIO pin
4-Wire SPI	SCS pin = 0	SDIO pin	GIO1 (GIO1S=0110)

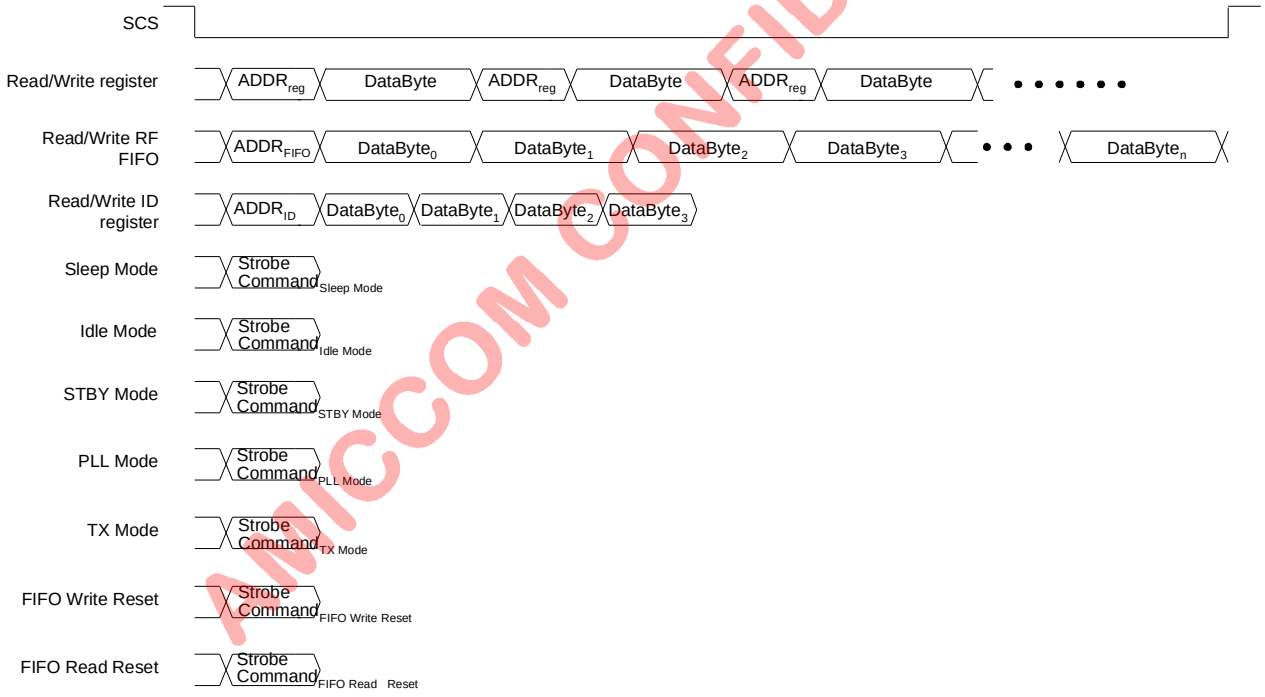


Figure 10.1 SPI Access Manners

10.1 SPI Format

The first bit (A7) is critical to indicate A7328 the following instruction is “Strobe command” or “control register”. See Table 10.1 for SPI format. Based on Table 10.1, if A7=0, A7328 is informed for control register accessing. So, A6 bit is used to indicate read (A6=1) or write operation (A6=0). See Figure 10.2 and Figure 10.3 for details.

Address Byte (8 bits)								Data Byte (8 bits)							
CMD	R/W	Address						Data							
A7	A6	A5	A4	A3	A2	A1	A0	7	6	5	4	3	2	1	0

Table 10.1 SPI Format

Address byte:

Bit 7: Command bit
[0]: Control register command.
[1]: Strobe command.

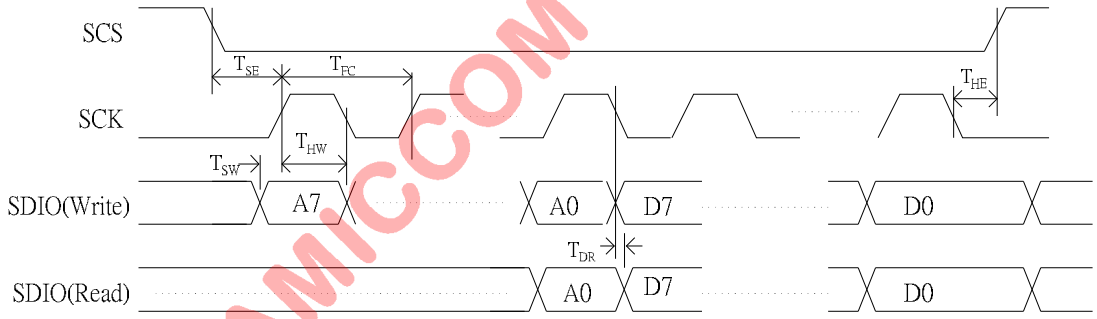
Bit 6: R/W bit
[0]: Write data to control register.
[1]: Read data from control register.

Bit [5:0]: Address of control register

Data Byte:
Bit [7:0]: SPI input or output data, see Figure 10.2 and Figure 10.3 for details.

10.2 SPI Timing Characteristic

No matter 3-wire or 4-wire SPI bus is configured, the maximum SPI data rate is 10 Mbps. To active SPI bus, SCS pin must be set to low. For correct data latching, user has to take care hold time and setup time between SCK and SDIO. See Table 10.2 for details.



Parameter	Description	Min.	Max.	Unit
F_C	FIFO clock frequency.		10	MHz
T_{SE}	Enable setup time.	50		ns
T_{HE}	Enable hold time.	50		ns
T_{SW}	TX Data setup time.	50		ns
T_{HW}	TX Data hold time.	50		ns
T_{DR}	RX Data delay time.	0	50	ns

Table 10.2 SPI Timing Characteristic

10.3 SPI Timing Chart

In this section, 3-wire and 4-wire SPI bus read / write timing are described.

10.3.1 Timing Chart of 3-wire SPI

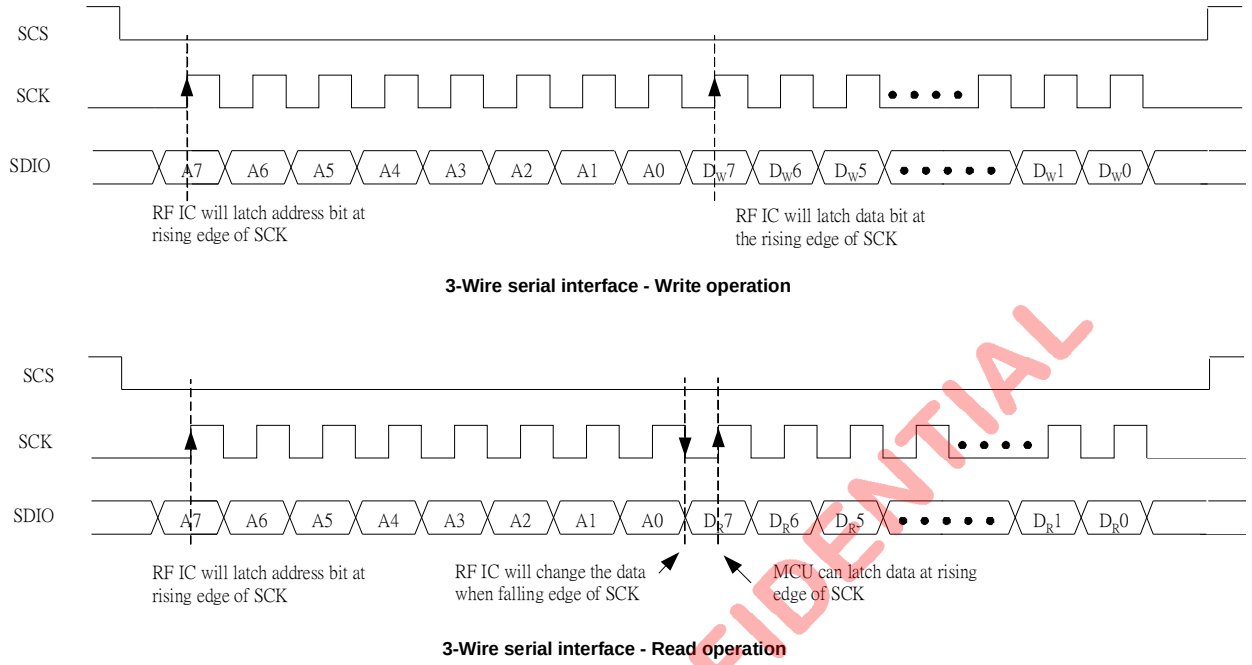


Figure 10.2 Read/Write Timing Chart of 3-Wire SPI

10.3.2 Timing Chart of 4-wire SPI

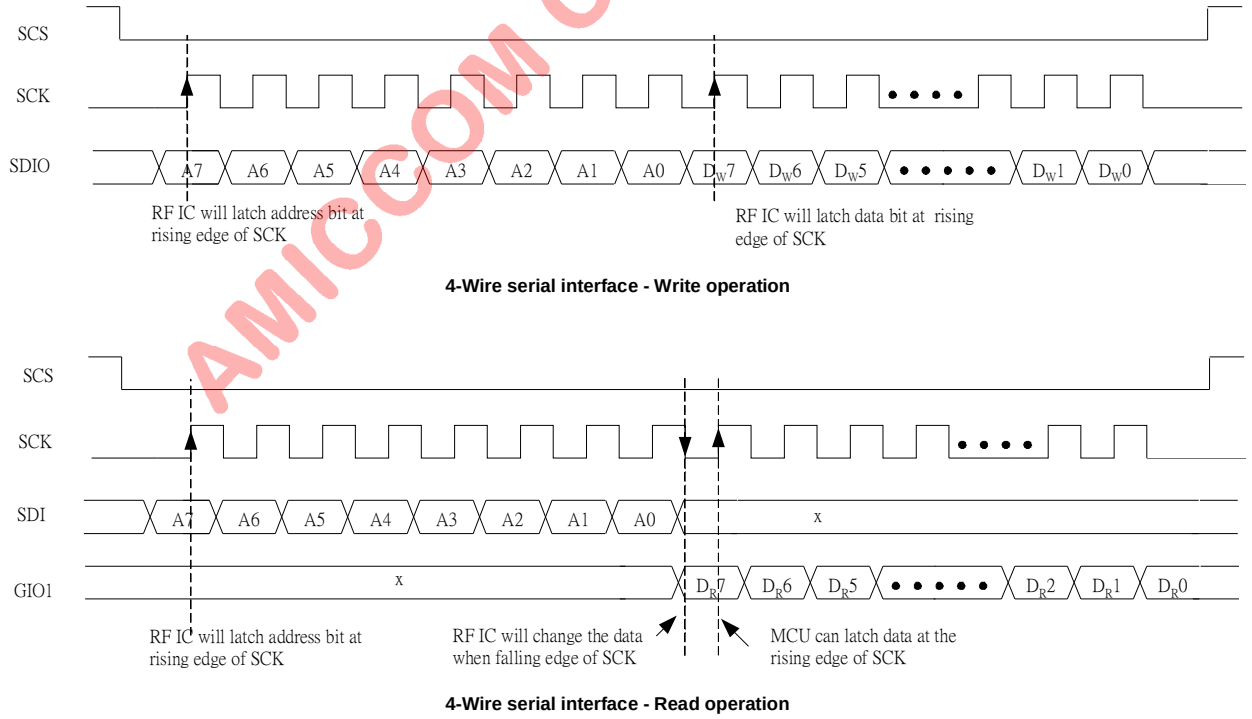


Figure 10.3 Read/Write Timing Chart of 4-Wire SPI

10.4 Strobe Commands

A7328 supports 8 Strobe commands to control internal state machine for chip's operations. Table 10.3 is the summary of Strobe commands.

Be notice, Strobe command could be defined by 4-bits (A7~A4) or 8-bits (A7~A0). If 8-bits Strobe command is selected, A3 ~ A0 are don't care conditions. In such case, SCS pin can be remaining low for asserting next commands.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	x	x	x	Sleep mode
1	0	0	1	x	x	x	x	Idle mode
1	0	1	0	x	x	x	x	Standby mode
1	0	1	1	x	x	x	x	PLL mode
1	1	0	1	x	x	x	x	TX mode
1	1	1	0	x	x	x	x	FIFO write pointer reset
1	0	0	0	1	0	0	0	Deep sleep mode (Tri-state of GIO1)
1	0	0	0	1	0	1	1	Deep sleep mode (Internal Pull-High of GIO1)

Table 10.3 Strobe Commands by SPI bus

10.4.1 Strobe Command - Sleep Mode

Refer to Table 10.3, user can issue 4 bits (1000) Strobe command directly to set A7328 into Sleep mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	0	0	0	0	Sleep mode

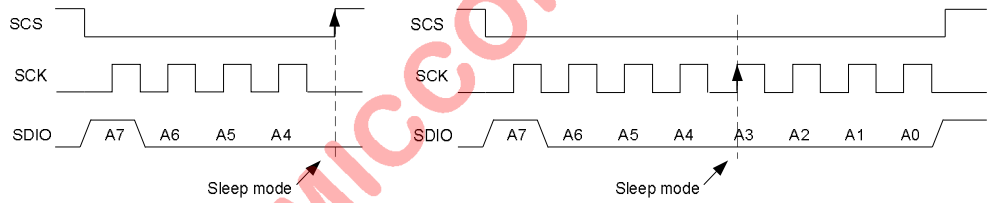


Figure 10.4 Sleep mode Command Timing Chart

10.4.2 Strobe Command - Idle Mode

Refer to Table 10.3, user can issue 4 bits (1001) Strobe command directly to set A7328 into Idle mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	1	x	x	x	x	Idle mode

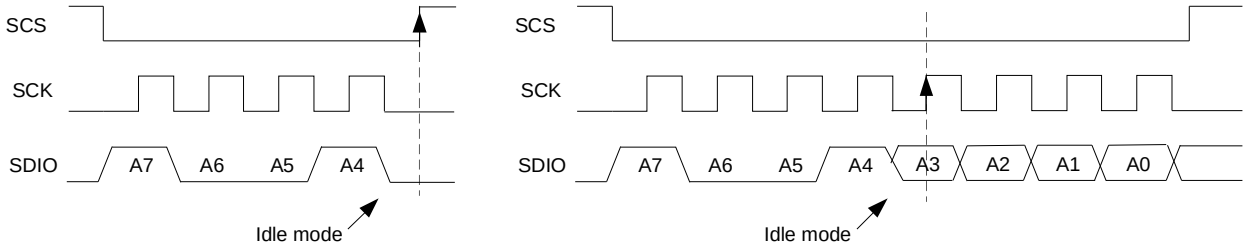


Figure 10.5 Idle mode Command Timing Chart

10.4.3 Strobe Command - Standby Mode

Refer to Table 10.3, user can issue 4 bits (1010) Strobe command directly to set A7328 into Standby mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	0	x	x	x	x	Standby mode

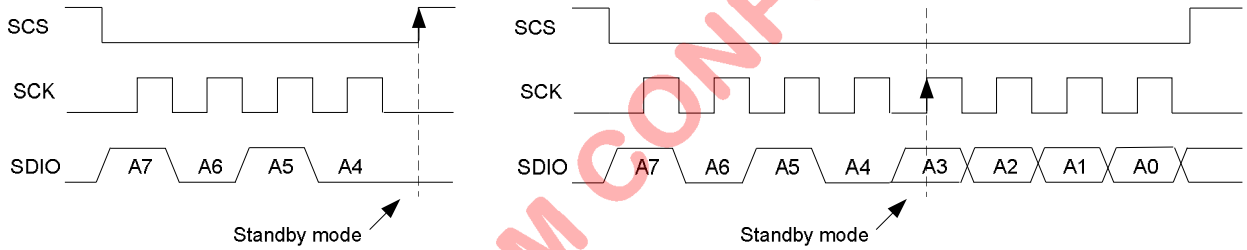


Figure 10.6 Standby mode Command Timing Chart

10.4.4 Strobe Command - PLL Mode

Refer to Table 10.3, user can issue 4 bits (1011) Strobe command directly to set A7328 into PLL mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	1	x	x	x	x	PLL mode

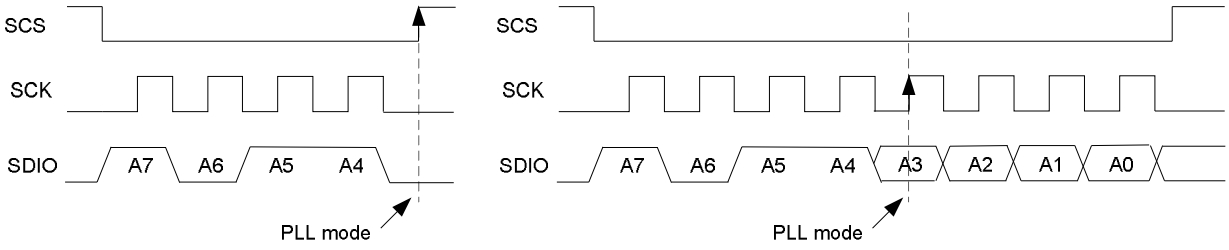


Figure 10.7 PLL mode Command Timing Chart

10.4.5 Strobe Command - TX Mode

Refer to Table 10.3, user can issue 4 bits (1101) Strobe command directly to set A7328 into TX mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	1	x	x	x	x	TX mode

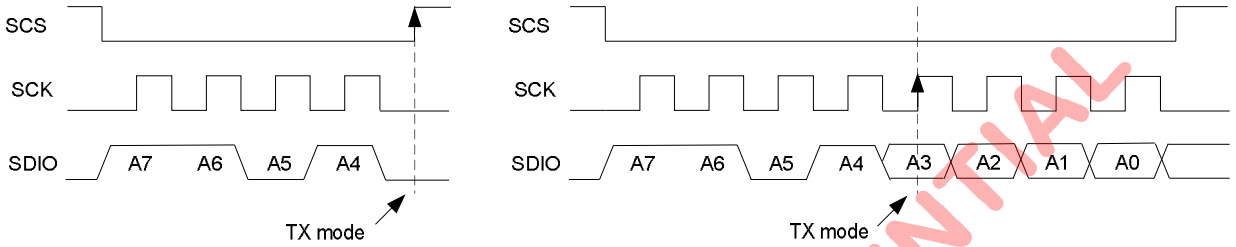


Figure 10.8 TX mode Command Timing Chart

10.4.6 Strobe Command – FIFO Write Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1110) Strobe command directly to reset A7328 FIFO write pointer. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	x	x	FIFO write pointer reset

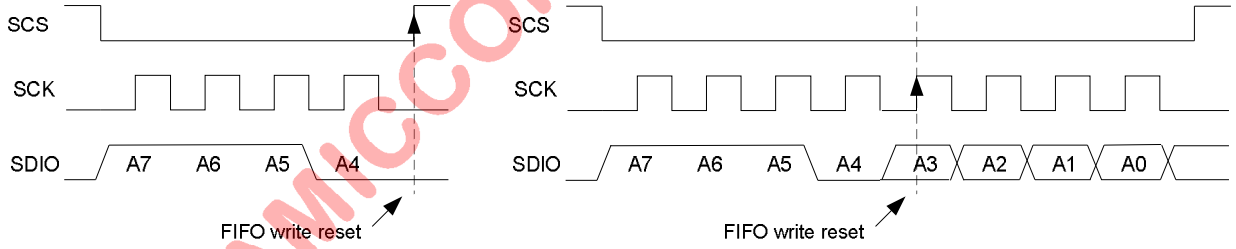


Figure 10.9 FIFO write pointer reset Command Timing Chart

10.4.7 Strobe Command – Deep Sleep Mode

Refer to Table 10.3, user can issue 8 bits (1000-0000) Strobe command directly to switch off power supply to A7328.In this mode, A7328 is staying minimum current comsuption and all registers are no data retention. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	1	0	0	0	Tri-state of GIO1 (no register retention)
1	0	0	0	1	0	1	1	Internal Pull-High of GIO1 / GIO2 (no register retention)

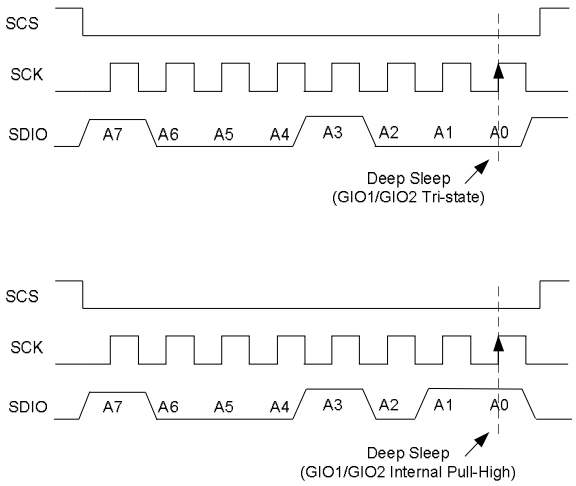


Figure 10.10 Deep Sleep Mode Timing Chart

10.5 Reset Command

In addition to power on reset (POR), MCU could issue software reset to A7328 by setting Mode Register (00h) through SPI bus as shown below. As long as 8-bits address (A7~A0) are delivered zero and data (D7~D0) are delivered zero, A7328 is informed to generate internal signal “RESETN” to initial itself. After reset command, A7328 is in standby mode.

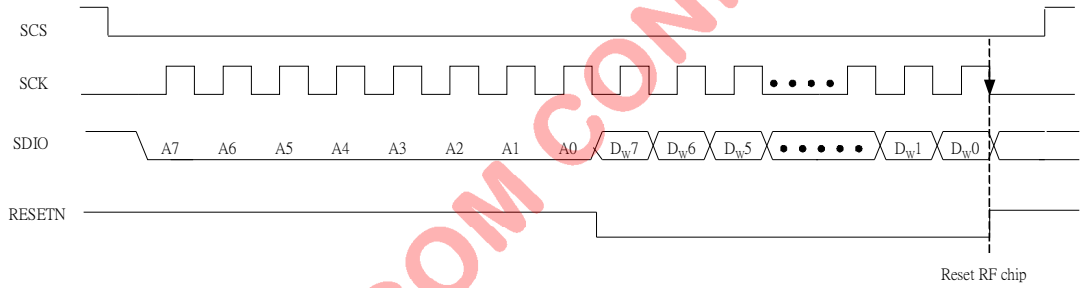


Figure 10.11 Reset Command Timing Chart

10.6 ID Accessing Command

A7328 has built-in 32-bits ID Registers for customized identification code. It is accessed via SPI bus. ID length is recommended to be 32 bits by setting IDL (20h).

Figure 10.13 and 10.14 are timing charts of 32-bits ID accessing via 3-wire SPI.

10.6.1 ID Write Command

User can refer to Figure 10.2 for SPI write timing chart. Below is the procedure of ID write command.

Step1: Deliver A7~A0 = 00000110 (A7=0 for control register, A6=0 for write operation, ID addr = 06h).
Step2: Via SDIO pin, 32-bits ID are written in sequence by Data Byte 0, 1, 2 and 3.
Step3: Toggle SCS pin to high when step2 is completed.

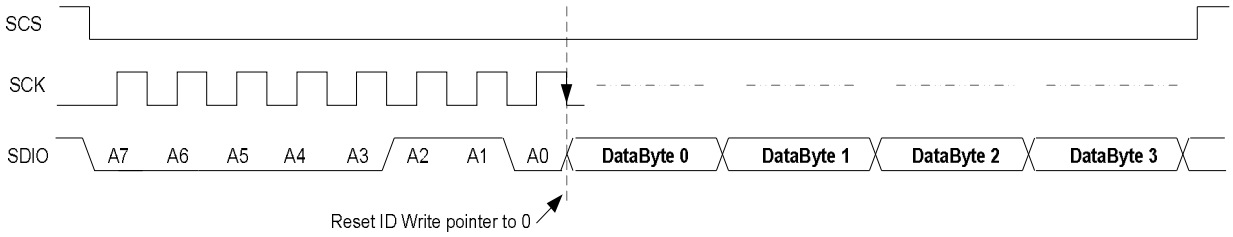


Figure 10.12 ID Write Command Timing Chart

10.6.2 ID Read Command

User can refer to Figure 10.2 for SPI read timing chart in details. Below is the procedure of ID read command.

Step1: Deliver A7~A0 = 01000110 (A7=0 for control register, A6=1 for read operation, ID addr = 06h).
Step2: Via SDIO pin, 32-bits ID are read in sequence by Data Byte 0, 1, 2 and 3.
Step3: Toggle SCS pin to high when step2 is completed.

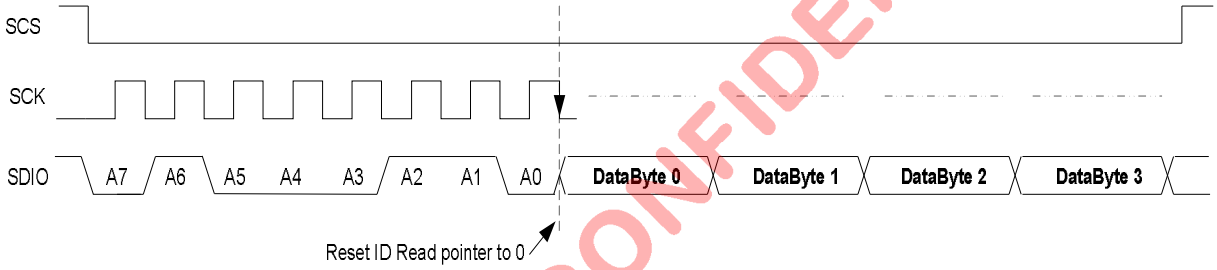


Figure 10.13 ID Read Command Timing Chart

10.7 FIFO Accessing Command

A7328 has 64 bytes TX FIFO, user just needs to set FMS (01h) =1 to enable FIFO mode. In FIFO mode, before packet is delivered, write wanted data into TX FIFO and issue TX strobe command.

User can choose polling or interrupt scheme for FIFO accessing. FIFO status is output via GIO1 pin by setting GIO1 (0Bh).

10.7.1 TX FIFO Write Command

User can refer to Figure 10.2 for SPI write timing chart. Below is the procedure of TX FIFO write command.

Step1: Deliver A7~A0 = 00000101 (A7=0 for control register, A6=0 for write operation, FIFO addr = 05h).
Step2: Via SDIO pin, write (n+1) bytes TX data into TX FIFO in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when step2 is completed.
Step4: Send TX Strobe command for packet transmitting. Refer to Figure 10.9.

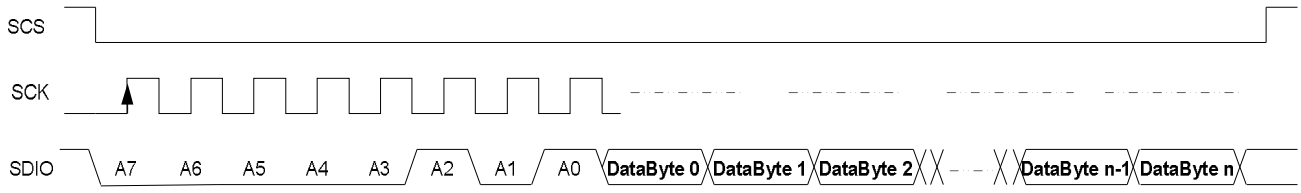


Figure 10.14 TX FIFO Write Command Timing Chart

11. State machine

In chapter 9 and chapter 10, user can learn both accessing A7328's control registers as well as issuing Strobe commands. From section 10.2 ~ 10.6, it is clear to know configurations of 3-wire SPI and 4-wire SPI, Strobe command, software reset, and how to access ID Registers and TX FIFO.

In section 11.1, built-in state machine is introduced. Then, combined with Strobe command, software reset and A7328's control registers, section 11.2 , 11.3 and 11.4 demonstrate 3 state diagrams to explain how transitions of A7328's operation.

From accessing data point of view, if FMS=1 (01h), FIFO mode is enabled, otherwise, A7328 is in direct mode. If FMS=1 and FIFO Read/Write at standby mode, we call it is Normal FIFO mode. Otherwise, If FMS=1 and FIFO Read/Write at PLL mode, we called it is Quick FIFO mode due to the reduction of PLL settling time. If FMS=1 and FIFO Read/Write at IDLE mode, we called it is Power Saving FIFO mode due to the reduction of average current.

	SPI chip select	Data In	Data Out	Operation Mode	Clock Recovery for Direct Mode
3-Wire SPI	SCS pin = 0	SDIO pin	SDIO pin	FIFO (FMS=1) Direct(FMS=0)	CKO pin (CKOS = 0001)
4-Wire SPI	SCS pin = 0	SDIO pin	GIO1 (GIO1S=0110)	FIFO (FMS=1) Direct(FMS=0)	CKO pin (CKOS = 0001)

(1) Normal FIFO Mode (FMS=1 and FIFO R/W @ Standby mode)
(2) Quick FIFO Mode (FMS=1 and FIFO R/W @ PLL mode)
(3) Power Saving FIFO Mode (FMS=1 and FIFO R/W @ IDLE mode)
(4) Quick Direct Mode (FMS=0 and FIFO ignored, write packet @ TX mode, read packet @ RX mode)

11.1 Key states

A7328 supports 6 key operation states. Those are,
(1) Standby mode
(2) Sleep mode
(3) Idle mode
(4) PLL mode
(5) TX mode
(6) CAL mode

After power on reset or software reset, A7328 is automatically into standby mode. Then, user has to do calibration process because all control registers are in initial values. The calibration process of A7328 is very easy, user only needs to issue Strobe commands and enable calibration registers. If so, the calibrations are automatically completed by A7328's internal state machine. See 11.2, 11.3, 11.4 and chapter 15 for details. After calibration, A7328 is ready to do TX operation. User can start wireless transmission.

11.1.1 Standby mode

When Standby Strobe is issued, A7328 enters standby mode automatically. Internal power management is listed below. Be noted that A7328 is in standby mode after power on reset or software reset.

Standby mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	OFF	OFF	OFF	OFF	(1010xxxx)b See Figure 10.6

11.1.2 Sleep mode

When Sleep Strobe is issued, A7328 enters sleep mode automatically. In sleep mode, A7328 still can accept other strobe commands via SPI bus. But, A7328 can not support Read/Write FIFO in sleep mode. Internal power management is listed below.

Sleep mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
OFF	OFF	OFF	OFF	OFF	OFF	(1000xxxx)b See Figure 10.4

11.1.3 Idle mode

When Idle Strobe is issued, A7328 enters idle mode automatically. In idle mode, A7328 can accept other strobe commands as well as supporting Read/Write FIFO. Internal power management is listed below.

Idle mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	OFF	OFF	OFF	OFF	OFF	(1001xxxx)b See Figure 10.5

11.1.4 PLL mode

When PLL Strobe is issued, A7328 enters PLL mode automatically. In PLL mode, internal PLL and VCO are both turned on to generate LO (local oscillator) frequency before TX and RX operation. Internal power management is listed below. According to PLL Register I, II, III, IV and V, PLL circuitry is easy to control by user's definition.

PLL mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	ON	ON	OFF	OFF	(1011xxxx)b See Figure 10.7

11.1.5 TX mode

When TX Strobe is issued, A7328 enters TX mode automatically for data delivery. Internal power management is listed.

(1) If A7328 is in FIFO mode, TX data packet (Preamble + ID + Payload) is delivered through TX circuitry. Then, A7328 supports auto-back function to previous state for the next packet.

(2) If A7328 is in direct mode, TX data packet is also delivered through TX circuitry. Then, A7328 stays in TX mode. User has to issue Strobe command to back to previous state.

TX mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	ON	ON	OFF	ON	(1101xxxx)b See Figure 10.9

11.1.6 CAL mode

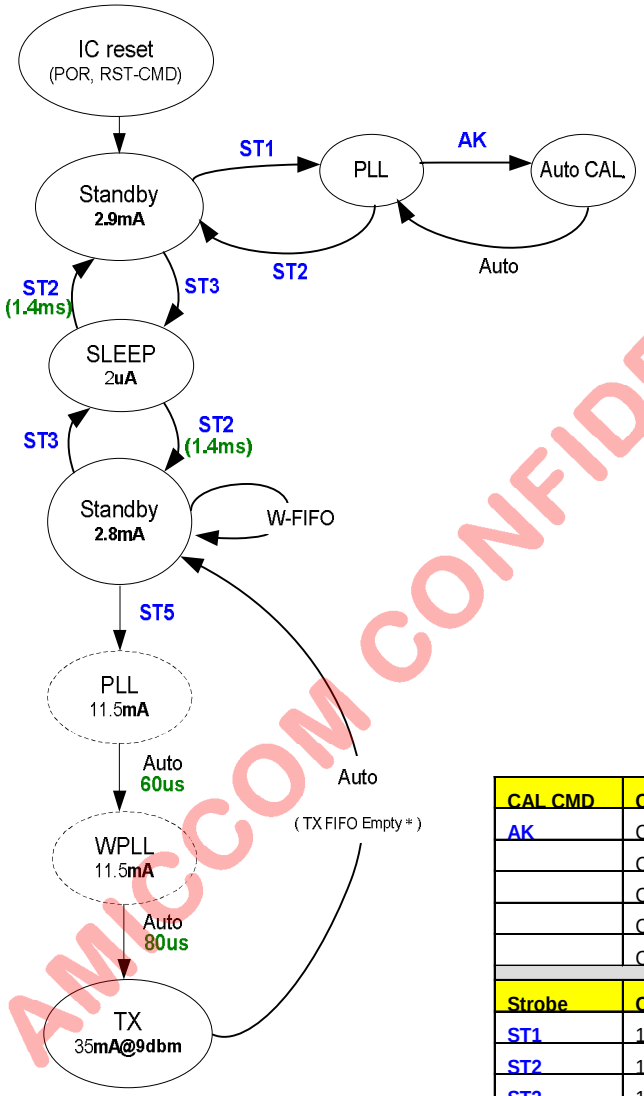
Calibration process shall be done after power on reset or software reset. Calibration items include VCO band and VCO current. It is easy to implement calibration process by Strobe command and enable CALC (02h) control register. See chapter 15 for details.

Be noted that VCO Calibration is executed in PLL mode only.

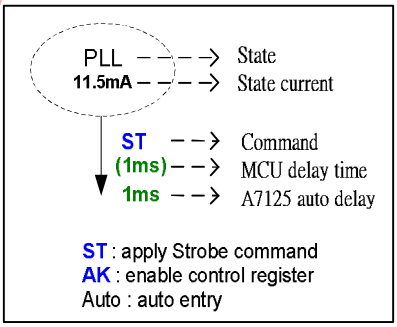
11.2 Normal FIFO Mode

This mode is suitable for requirement of general purpose applications. After calibration, user can issue Strobe command to enter standby mode where write TX FIFO. From standby mode to packet data transmitting, only one Strobe command is needed. Once transmission is done, A7328 is auto back to standby mode.

If all packets are finished and deeper power saving is necessary, user can issue Strobe command to ask A7328 staying in sleep mode. Figure 11.1 is the state diagram of Normal FIFO mode.



SYMBOL EXPLAIN



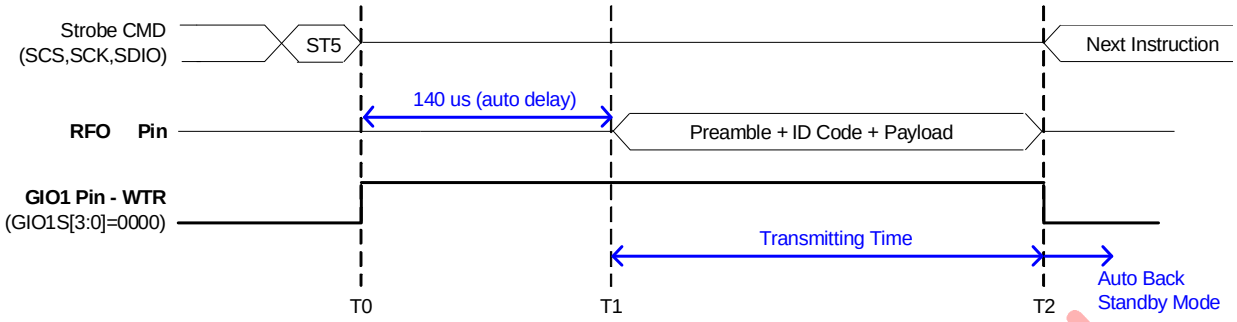
CAL_CMD	CMD Value	Calibration	Section
AK	CALC.0=1.	RSSI	15.3
	CALC.1=1.	IF Filter	15.2
	CALC.2=1.	VCO Deviation	15.6
	CALC.3=1.	VCO Bank	15.5
	CALC.4=1.	VCO Current	15.4

Strobe	CMD Value	Note	Section
ST1	1011b	Enter to PLL	10.4.4
ST2	1010b	Enter to Standby	10.4.3
ST3	1000b	Enter to SLEEP	10.4.1
ST4	1001b	Enter to IDLE	10.4.2
ST5-TX	1101b	Enter to TX	10.4.6
RST-CMD	00000000b	Software Reset	10.5

- Be notice, refer to chapter 16 for definition of RX FIFO Full and TX FIFO Empty.

Figure 11.1 State diagram of Normal FIFO Mode

From Figure 11.1, when ST5 command is issued for TX operation, see Figure 11.2 for detailed timing. A7328 status can be represented to GIO1 to MCU for timing control.



T0-T1: Auto Delay by Register setting (PDL + TDL)

LO Freq.	Standby to WPLL (PDL)	WPLL to TX (TDL)	TX Ready Time
Changed	60 us	80 us	140 us
No Changed	60 us	80 us	140 us

Figure 11.2 Transmitting Timing Chart of Normal FIFO Mode

12 Crystal Oscillator Circuit

A7328 needs external crystal or external clock that is either 8/12/16 MHz, to generate internal wanted clock.

Relative Control Register

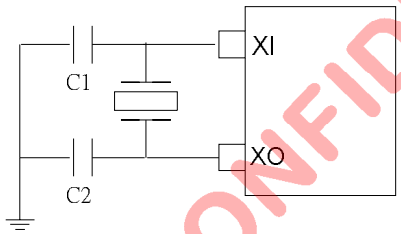
Data Rate Clock Register (Address: 0Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	SDR1	SDR0	GRC3	GRC2	GRC1	GRC0	--	--
	W	SDR1	SDR0	GRC3	GRC2	GRC1	GRC0	CGS	XS
Reset		0	0	0	1	1	1	1	1

12.1 Use External Crystal

Figure 12.1 shows the connection of crystal network between XI and XO pins. C1 and C2 capacitance are used to adjust different crystal loading. A7328 support low cost crystal within ± 50 ppm accuracy. Be aware that crystal accuracy requirement includes initial tolerance, temperature drift, aging and crystal loading.

Note: set XS= 1 (0Ch) to select external crystal oscillator.



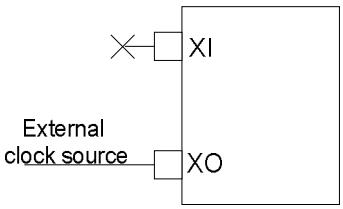
i.e., Crystal = 16MHz (Cload =18pF), C1=C2=27pF.

Figure12.1 Crystal network connection for using external crystal

12.2 Use External Clock

A7328 has built-in AC couple capacitor to support external clock input. Figure 11.2 shows how to connect. In such case, XI pin is left opened.

To use external clock from MCU instead of external crystal, user just sets XS= 0 (0Ch) to active AC couple capacitor. Be notice, the frequency accuracy of external clock shall be controlled within ± 50ppm and the clock swing (peak-to-peak) shall be larger than 1.5V.



(External clock is controlled within ± 50ppm.)

Figure 12.2 Connect to external clock source

13. System Clock

A7328 supports different external crystal frequency by programmable “Data Rate Clock Register” (0Ch). Based on this, two important internal clocks F_{CGR} and F_{SYCK} are generated.

(1) F_{CGR}: Clock Generation Reference = $F_{CRYSTAL}$ / (GRC+1) = 2MHz. where GRC is max 15.
(2) F_{SYCK}: System Clock = 64 MHz

Relative Control Register

Data Rate Clock Register (Address: 0Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	IFS		GRC3	GRC2	GRC1	GRC0	--	--
	W	IFS		GRC3	GRC2	GRC1	GRC0	CGS	XS
Reset		0		0	1	1	1	1	1

Data Rate Divider Register (Address: 30h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
Reset		0	0	0	0	0	0	0	0

PLL Register II (Address: 0Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
Reset		0	0	1	0	1	1	1	0

13.1 Derive System Clock

Because A7328 supports different external crystals, GRC [3:0] (0Ch) are used to get 2 MHz Clock Generation Reference (F_{CGR}) for internal usage.

$$F_{CGR} = \frac{F_{XREF}}{(GRC[3:0]+1)}.$$

Below is block diagram of system clock. F_{XTAL} is the crystal frequency. User can set registers to get F_{SYCK} = 64MHz. F_{XREF} is the reference clock of Clock Generator to generate F_{CGR} = 2MHz and F_{SPLL} = 64MHz. After delay circuitry, System clock is derived, F_{SYCK} = 64MHz. ADC clock (F_{ADC} = 4MHz or 8MHz) is from F_{SYCK} = 64MHz after frequency divider.

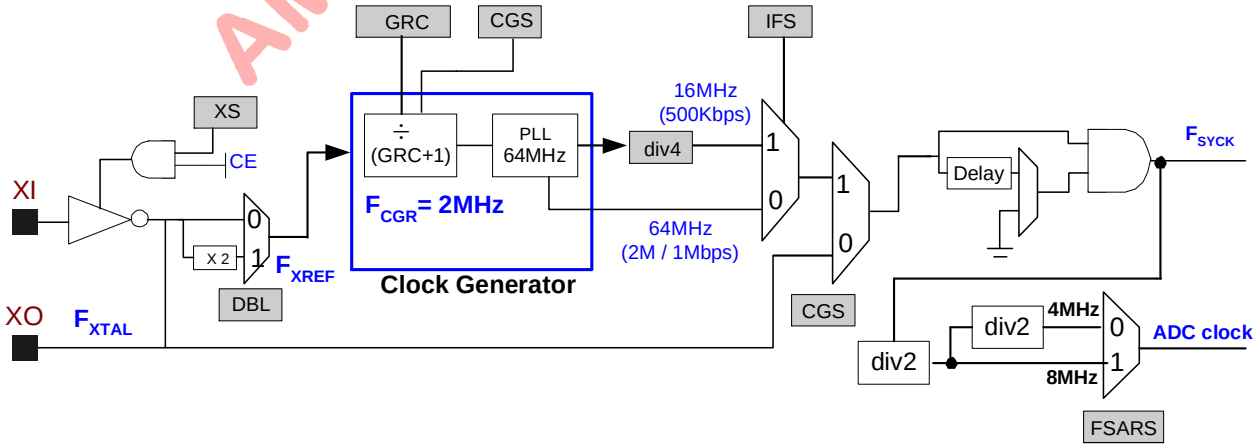


Figure 13.1 System Clock Block Diagram

Recommend to set DBL (0Eh) = [0], then, $F_{XREF} = F_{XTAL}$

Crystal Frequency (F_{XTAL})	Internal Crystal Reference (F_{XREF})	Clock Generation Reference (F_{CGR})	GRC [3:0]	CGS
16 MHz	16 MHz	Must be 2 MHz	[0111]	1
12 MHz	12 MHz	Must be 2 MHz	[0101]	1
8 MHz	8 MHz	Must be 2 MHz	[0011]	1

13.2 Data Rate

A7328 supports programmable data rate by setting SDR [7:0] (39h). Data rate = (F_{IFCK} / (SDR [1:0] +1)). The data rate clock is from IF clock (F_{IFCK}). F_{IFCK} is 2MHz for 2M/1M mode and 500KHz for data rate below 500Kbps.

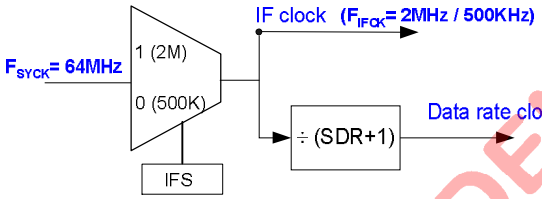


Figure 13.2 Data Rate Block Diagram

A7328 Data Rate = (F_{IFCK} / (SDR [1:0] +1)).

F_{SYCK} (system clock)	F_{IFCK} (IF clock)	SDR [7:0] (30h)	Data Rate
64 MHz	2 MHz	[0000-0000]	2 Mbps
64 MHz	2 MHz	[0000-0001]	1 Mbps
64 MHz	500 KHz	[0000-0000]	500Kbps
64 MHz	500 KHz	[0000-0100]	100Kbps

14. Transceiver Frequency

A7328 is a sub 1GHz transmitter with embedded PA up to 10 dBm.. For TX frequency setting, user just needs to set up LO (Local Oscillator) frequency for one-way radio transmission.

To target full range of 915MHz ISM band (902 MHz to 928 MHz), A7328 applies offset concept by LO frequency **F_{LO} = F_{LO_BASE} + F_{OFFSET}.** Therefore, for different applications, A7328 is easy to implement frequency hopping and multi-channels by **ONE** register setting, **PLL Register (CHN [7:0], 0Dh).**

The wanted RF formula

$$F_{LO\_BASE} = \frac{1}{n} F_{PFD} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}}) = \frac{1}{n}(DBL+1) \cdot \frac{F_{XTAL}}{RRC[1:0]+1} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}})$$

where f_{PFD} is the comparison frequency of PLL.
Where n = 2 for MD = [10] or [11], 868M / 915MHz band
Where n = 4 for MD = [01], 433M band
Where n = 6 for MD = [00], 315MHz band

MD[1:0] is located at address 2Ah [Bit5, Bit4].

DBL and RRC[1:0] are located at address 0Eh.

Below is the LO frequency block diagram.

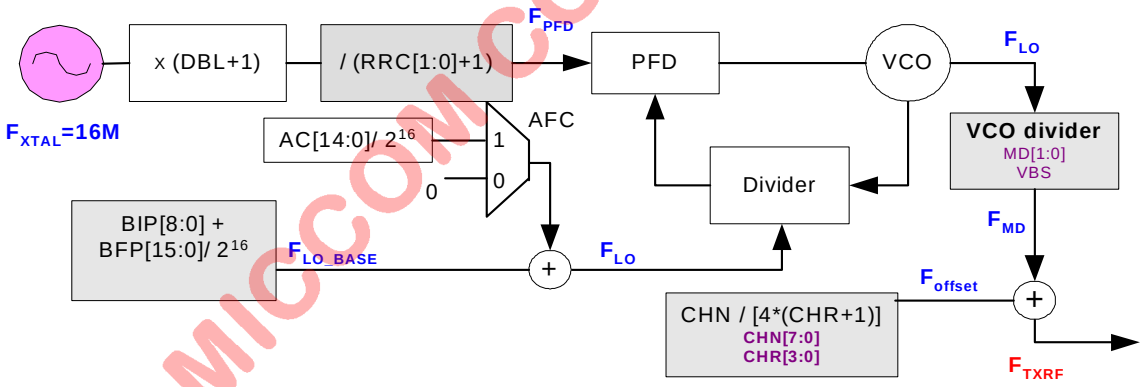


Figure 14.1 Block Diagram of Local Oscillator

14.1 LO Frequency Setting

From Figure 14.1, F_{LO} is the VCO frequency to result the wanted F_{TXRF} through VCO divider. To set up F_{LO}, it is easy to implement by below 6 steps.

1. Set the base frequency (**F_{LO_BASE}**) by PLL Register II, III, IV and V (0Eh, 0Dh, 10h and 11h).
   For example, set **F_{LO_BASE} ~ 1800.002MHz**.

2. Set the channel step (F_{CHSP}) by PLL Register II (0Fh).
   A7328 supports channel steps by **250K.**

3. Set CHN [7:0] to get offset frequency by PLL Register I (0Eh).
   F_{OFFSET} = CHN [7:0] x F_{CHSP}

4. LO frequency is equal to base frequency.
   F_{LO} = F_{LO_BASE}

5. MD frequency is equal to VCO frequency divides by VCO divider (MD[1:0]).
   F_{MD} = F_{LO} / (VCO Divider)

6. For TX radio frequency (**F_{TXRF}**) is equal to MD frequency plus offset frequency.
   F_{TXRF} = F_{MD} + F_{OFFSET}

$$F_{LO\_BASE} = \frac{1}{n} F_{PFD} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}})$$
$$= \frac{1}{n} (DBL + 1) \cdot \frac{F_{XTAL}}{RRC[1:0] + 1} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}})$$

Base on the above formula, for example, if select 16MHz crystal (F_{XTAL} = 16 MHz.) and select channel step F_{CHSP} = 250 KHz, To get **F_{LO_BASE} and F_{LO}** ,see Table 14.1, 14.2 and Figure 14.2 for details.

How to set F_{LO_BASE} ~ 900.001 MHz

STEP	ITEMS	VALUE	NOTE
1	F_{XTAL}	16 MHz	Crystal Frequency
2	DBL	0	Disable double function
3	RRC	0	If so, F_{PFD}= 16MHz
4	BIP	0x70	To get F_{LO} =1792 MHz
5	BFP[15:8], PLL IV	0x80	To get F_{LO} ~ 1800.002 MHz
5	BFP[7:0], PLL V	0x08	
6	F_{LO_BASE}	**~1800.002 MHz**	LO Base frequency

Table 14.1 How to set F_{LO_BASE}

How to set F_{TXRF} ~ 915.001 MHz

STEP	ITEMS	VALUE	NOTE
1	F_{LO_BASE}	~1800.002 MHz	After set up BIP and BFP
2	VBS ; MD	VBS=[0] ; MD=[10b]	To get F_{RF_BASE} ~ 900.001 MHz
3	F_{MD}	~900.001 MHz	VCO divider frequency
4	CHR	7	To get F_{CHSP}= 250 KHz
5	F_{CHSP}	250 KHz	Channel step = 250KHz
6	CHN	0x3C	Set channel number = 60
7	F_{OFFSET}	15 MHz	F_{OFFSET}= 250 KHz * (60) = 15MHz
8	F_{TXRF}	**~915.001 MHz**	F_{TXRF} = F_{TXRF} = F_{MD} + F_{OFFSET}

Table 14.2 How to set F_{TXRF}

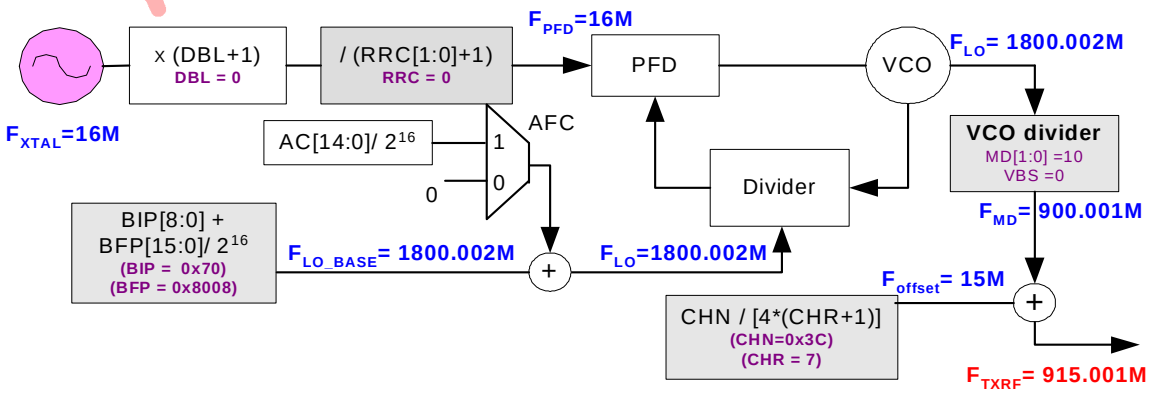


Figure 14.2 Block Diagram of F_{LO} ~ 915.001 MHz

15. Calibration

A7328 needs calibration process during initialization by below 5 items, they are, VCO Current, VCO Bank, VCO Deviation.

1. VCO Current Calibration is to find adequate VCO current.
2. VCO Bank Calibration is to select best VCO frequency bank for the calibrated frequency.
3. VCO Deviation Calibration is to calibrate 500 KHz deviation of VCO.

VCO Current, Bank and Deviation shall be calibrated in PLL mode. User can set A7328 in PLL mode and enable 5 control registers together, then, all calibration procedures are automatically executed and its results are stored in calibration flags.

Relative Control Register

Calibration Control Register (Address: 02h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	--	--	--	VCC	VBC	VDC		
Reset		--	--	--	0	0	0	0	0

15.1 Calibration Procedure

1. Initialize all control registers (refer to A7328 reference code).
2. Select auto value mode (set MVCS, MVBS, MVDS= 0).
3. Set A7328 in PLL mode.
4. Enable VCO Current, Bank and Deviation Calibration (VCC, VBC, VDC= 1).
5. After calibration done, VCC, VBC and VDC are auto clear.
6. Check pass or fail by calibration flag (VCCF, VBCF).

15.2 VCO Current Calibration

VCO Current Calibration Register (Address: 1Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
	W	--	--	VCCS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
Reset		--	--	1	0	1	1	0	0

1. Initialize all control registers (refer A7328 reference code).
2. Set MVCS= 0 for auto calibration.
3. Set A7328 in PLL mode.
4. Set VCC= 1 (02h).
5. VCC is auto clear after calibration done.
6. User can read calibration flag (VCCF, 1Fh) to check pass or fail.
7. User can read VCB [3:0] (1Fh) to get the auto calibration value.

15.5 VCO Bank Calibration

VCO Bank Calibration Register I (Address: 1Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	--	VBCF	VB2	VB1	VB0
	W	DDC1	DDC0	DAGS	--	MVBS	MVB2	MVB1	MVB0
Reset		1	1	0	--	0	1	0	0

1. Initialize all control registers (refer A7328 reference code).
2. Set MVBS= 0 for auto calibration.
3. Set A7328 in PLL mode.
4. Set VBC= 1 (02h).

5. The maximum calibration time for VCO Bank Calibration is about 240 us (4 * PLL settling time).
6. VBC is auto clear after calibration done.
7. User can read calibration flag (VBCF, 20h) to check pass or fail.
8. User can read VB [2:0] (1Fh) to get the auto calibration value.

15.6 VCO Deviation Calibration

VCO Deviation Calibration Register II (Address: 21h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
Reset		0	0	1	0	1	0	0	0

1. Initialize all control registers (refer A7328 reference code).
2. Set MVDS= 0 for auto calibration.
3. Set A7328 in PLL mode.
4. Set VDC= 1 (02h).
5. VDC is auto clear after calibration done.
6. User can read ADEV [7:0] (22h) to get the auto calibration value.
7. No need to check calibration flag.

16. FIFO (First In First Out)

A7328 supports separated 64-bytes TX FIFO by enabling FMS =1 (01h). For FIFO accessing, TX FIFO represents transmitted payload.

In chapter 10 and 11, user can also find below FIFO information.
(1) Figure 10.15 and 10.16 for FIFO accessing via 3-wire SPI.
(2) Section 10.4.7 and 10.4.8 for FIFO pointer reset command.
(3) Figure 11.2 and Figure 11.3 for Normal/Quick FIFO mode.

16.1 Packet Format of FIFO mode

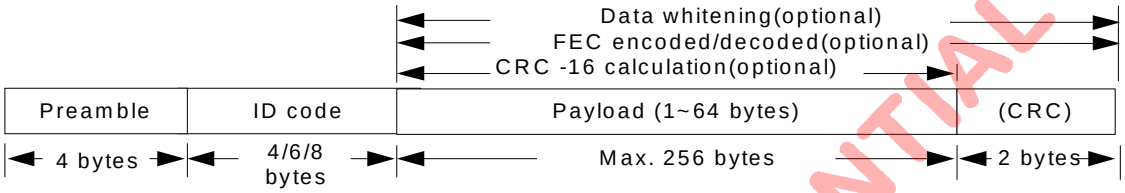


Figure 16.1 Packet Format of FIFO mode

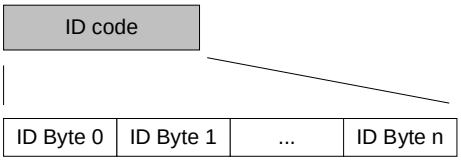


Figure 16.2 ID Code Format

Preamble:
The packet is led by preamble which is composed of alternate 0 and 1. If the first bit of ID code is 0, preamble shall be 0101…0101. In the contrast, if the first bit of ID code is 1, preamble shall be 1010…1010.
Preamble length is recommended to set 4 bytes by PML [1:0] (1Ch).

ID code:
ID code is recommended to set 4 bytes by IDL=1 (1Ch) and ID Code is sequenced by ID Byte 0, 1, 2 and 3.

Payload:
Payload length is programmable by FEP [7:0] (03h). The physical FIFO depth is 64 bytes. A7328 also supports logical FIFO extension up to 256 bytes. See section 16.5 for details.

CRC (option):
In FIFO mode, if CRC is enabled (CRCS=1, 1Ch), 2-bytes of CRC value is transmitted automatically after payload.

Relative Control Register

Mode Register (Address: 00h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	FECF	CRCF	CER	XER	PLLER	TRSR	TRER
	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
Reset		--	--	--	--	--	--	--	--

FIFO Register I (Address: 03h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	0	1	1	1	1	1	1

Code Register I (Address: 1Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	MCS	WHTS	FECS	CRCS	IDL1	IDL0	PML1	PML0
Reset		0	0	0	0	0	1	1	1

16.2 Bit Stream Process

A7328 supports 3 optional bit stream process for payload, they are,
(1) CCITT-16 CRC
(2) (7, 4) Hamming FEC
(3) Data Whitening by XOR PN7 (7-bits Pseudo Random Sequence).

CRC (Cyclic Redundancy Check):

1. CRC is enabled by CRCS= 1 (1Ch). TX circuitry calculates the CRC value of payload (preamble, ID code excluded) and transmits 2-bytes CRC value after payload.

FEC (Forward Error Correction):

1. FEC is enabled by FECS= 1 (1Ch). Payload and CRC value (if CRCS=1) are encoded by (7, 4) Hamming code.
2. Each 4-bits (nibble) of payload is encoded into 7-bits code word and delivered out automatically.
   (ex. 64 bytes payload will be encoded to 128 code words, each code word is 7 bits.)

Data Whitening:

1. Data whitening is enabled by WHTS= 1 (1Ch). Payload and CRC value (if CRCS=1) or their encoded code words (if FECS=1) are encrypted by bit XOR operation with PN7. The initial seed of PN7 is set by WS [6:0] (1Dh).

16.3 Transmission Time

Based on CRC and FEC options, the transmission time are different. See table 16.1 for details.

Data Rate = 2 Mbps

Data Rate (Mbps)	Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
2	32	32	512	Disable	Disable	576 bit * 0.5 us = 288 us
2	32	32	512	16 bits	Disable	592 bit * 0.5 us = 296 us
2	32	32	512	Disable	512 * 7 / 4	960 bit * 0.5 us = 480 us
2	32	32	512	16 * 7 / 4	512 * 7 / 4	988 bit * 0.5 us = 494 us

Table 16.1 Transmission time of 2 Mbps data rate

Data Rate = 1 Mbps

Data Rate (Mbps)	Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
1	32	32	512	Disable	Disable	576 bit * 1.0 us = 576 us
1	32	32	512	16 bits	Disable	592 bit * 1.0 us = 592 us
1	32	32	512	Disable	512 * 7 / 4	960 bit * 1.0 us = 960 us
1	32	32	512	16 * 7 / 4	512 * 7 / 4	988 bit * 1.0 us = 988 us

Table 16.2 Transmission time of 1 Mbps data rate

Data Rate = 500 Kbps

Data Rate (Kbps)	Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
500	32	32	512	Disable	Disable	576 bit X 2 us = 1.152 ms
500	32	32	512	16 bits	Disable	592 bit X 2 us = 1.184 ms
500	32	32	512	Disable	512 x 7 / 4	960 bit X 2 us = 1.920 ms
500	32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 2 us = 1.976 ms

Table 16.3 Transmission time of 500Kbps data rate

Data Rate = 100 Kbps

Data Rate (Kbps)	Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
100	32	32	512	Disable	Disable	576 bit X 10 us = 5.76 ms
100	32	32	512	16 bits	Disable	592 bit X 10 us = 5.92 ms
100	32	32	512	Disable	512 x 7 / 4	960 bit X 10 us = 9.6 ms
100	32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 10 us = 9.88 ms

16.4 Usage of TX FIFO

In application points of view, A7328 supports 3 options of FIFO arrangement.
(1) Easy FIFO
(2) Segment FIFO
(3) FIFO Extension

For FIFO operation, A7328 supports Strobe command to reset TX FIFO pointer as shown below. User can refer to section 10.5 for FIFO write pointer reset and FIFO read pointer reset.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	X	x	FIFO write pointer reset (for TX FIFO)

FIFO Register I (Address: 03h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	0	1	1	1	1	1	1

FIFO Register II (Address: 04h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
Reset		0	1	0	0	0	0	0	0

FIFO DATA Register (Address: 05h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
Reset		0	0	0	0	0	0	0	0

16.4.1 Easy FIFO

In Easy FIFO, max FIFO length is 64 bytes. FIFO length is equal to **(FEP [7:0] +1)**. User just needs to control FEP [7:0] (03h) and disable PSA and FPM as shown below.

Register setting

TX	Control Registers		
FIFO Length (byte)	**FEP[7:0] (03h)**	**PSA[5:0] (04h)**	**FPM[1:0] (04h)**
1	0x00	0	0
8	0x07	0	0
16	0x0F	0	0
32	0x1F	0	0
64	0x3F	0	0

Table 16.3 Control registers of Easy FIFO

Procedures of TX FIFO Transmitting

1. Initialize all control registers (refer A7328 reference code).
2. Set FEP [7:0] = 0x3F for 64-bytes FIFO.
3. Refer to Figure 11.2 and Figure 11.3
4. Send Strobe command – TX FIFO write pointer reset.
5. MCU writes 64-bytes data to TX FIFO.
6. Send TX Strobe Command.
7. Done.

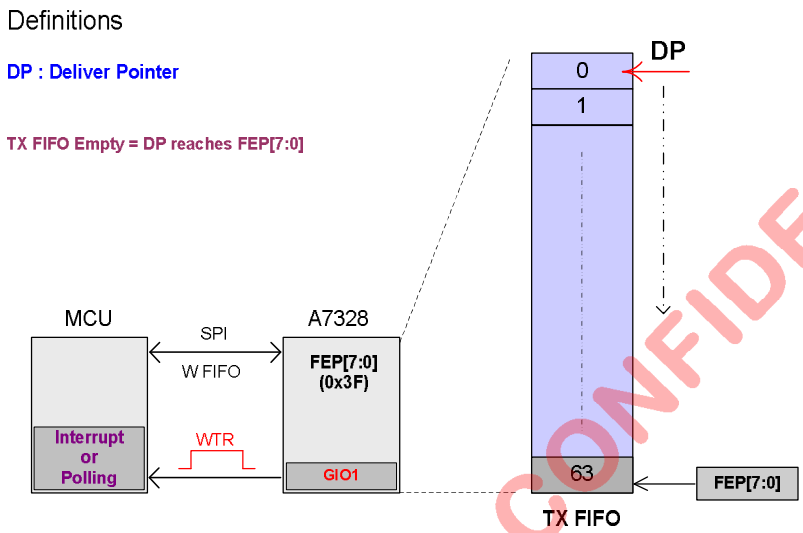


Figure 16.3 Easy FIFO

16.4.2 Segment FIFO

In Segment FIFO, TX FIFO length is equal to (FEP [7:0] − PSA [5:0]+1). FPM [1:0] should be zero. This function is very useful for button applications. In such case, each button is used to transmit fixed code (data) every time. During initialization, each fixed code is written into corresponding segment FIFO once and for all. Then, if button is triggered, MCU just assigns corresponding segment FIFO (PSA [5:0] and FEP [7:0]) and issues TX strobe command.

If TX FIFO is arranged into 8 segments, each TX segment is 8 bytes

TX				Control Registers		
Segment	**PSA**	**FEP**	**FIFO Length (byte)**	**PSA[5:0] (04h)**	**FEP[7:0] (03h)**	**FPM[1:0] (04h)**
1	PSA1	FEP1	8	0x00	0x07	0
2	PSA2	FEP2	8	0x08	0x0F	0
3	PSA3	FEP3	8	0x10	0x17	0
4	PSA4	FEP4	8	0x18	0x1F	0
5	PSA5	FEP5	8	0x20	0x27	0
6	PSA6	FEP6	8	0x28	0x2F	0
7	PSA7	FEP7	8	0x30	0x37	0
8	PSA8	FEP8	8	0x38	0x3F	0

Table 16.4 Segment FIFO is arranged into 8 segments

Procedures of TX FIFO Transmitting

1. Initialize all control registers (refer A7328 reference code).
2. Refer to Figure 11.2 and Figure 11.3 (in chapter 11).
3. Send Strobe command – TX FIFO write pointer reset.
4. MCU writes fixed code into corresponding segment FIFO once and for all.
5. To consign Segment 1, set PSA = 0x00 and FEP= 0x07
   To consign Segment 2, set PSA = 0x08 and FEP= 0x0F
   To consign Segment 3, set PSA = 0x10 and FEP= 0x17
   To consign Segment 4, set PSA = 0x18 and FEP= 0x1F
   To consign Segment 5, set PSA = 0x20 and FEP= 0x27
   To consign Segment 6, set PSA = 0x28 and FEP= 0x2F
   To consign Segment 7, set PSA = 0x30 and FEP= 0x37
   To consign Segment 8, set PSA = 0x38 and FEP= 0x3F
6. Send TX Strobe Command.
7. Done.

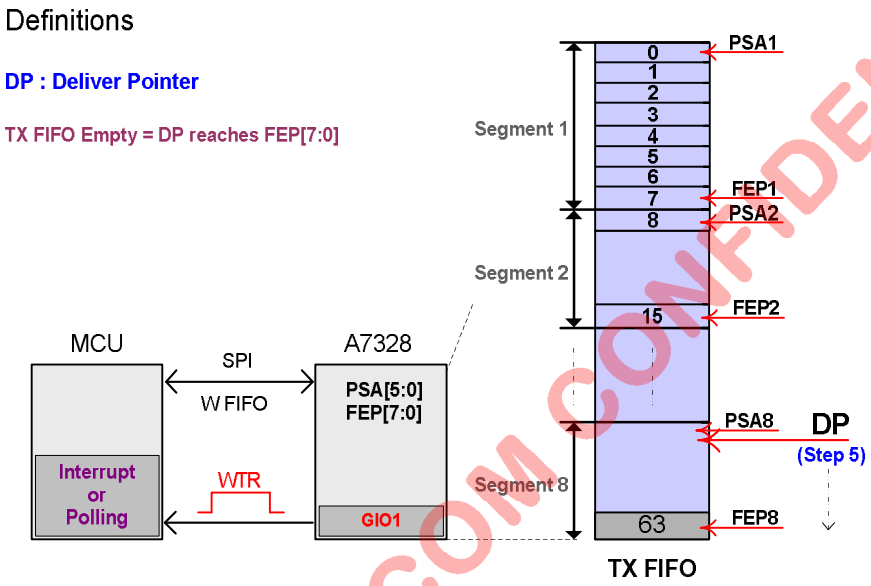


Figure 16.4 Segment FIFO Mode

16.4.3 FIFO Extension

In FIFO Extension, FIFO length is equal to **(FEP [7:0] +1)**. PSA [5:0] shall be zero, and FPM [1:0] is used to set FIFO Pointer Flag (FPF) to MCU. FIFO extension could be set up to 256 bytes by FEP [7:0] with different FPF trigger conditions.

Be notice, setting of SPI data rate is important to prevent error operation of FIFO extension. The min. SPI data rate shall be equal or greater than **(A7328 data rate + 500Kbps)** and refer Table 16.4 and 16.5 for max. SPI Data Rate.

If A7328 data rate = 2Mbps and FIFO extension = 256 bytes.

TX			Control Registers		
FIFO Length (byte)	**FPF Trigger Condition**	**Max. SPI Data Rate**	**FEP[7:0]**	**FPM[1:0]**	**PSA[5:0]**
256	Delta = 04	10 Mbps	0xFF	00	0
	Delta = 08	10 Mbps		01	0
	Delta = 12	10 Mbps		10	0
	Delta = 16	**8 Mbps**		**11**	0

Table 16.5 How to set FIFO extension when A7328 is at 2Mbps data rate

If A7328 data rate = 1Mbps and FIFO extension = 256 bytes.

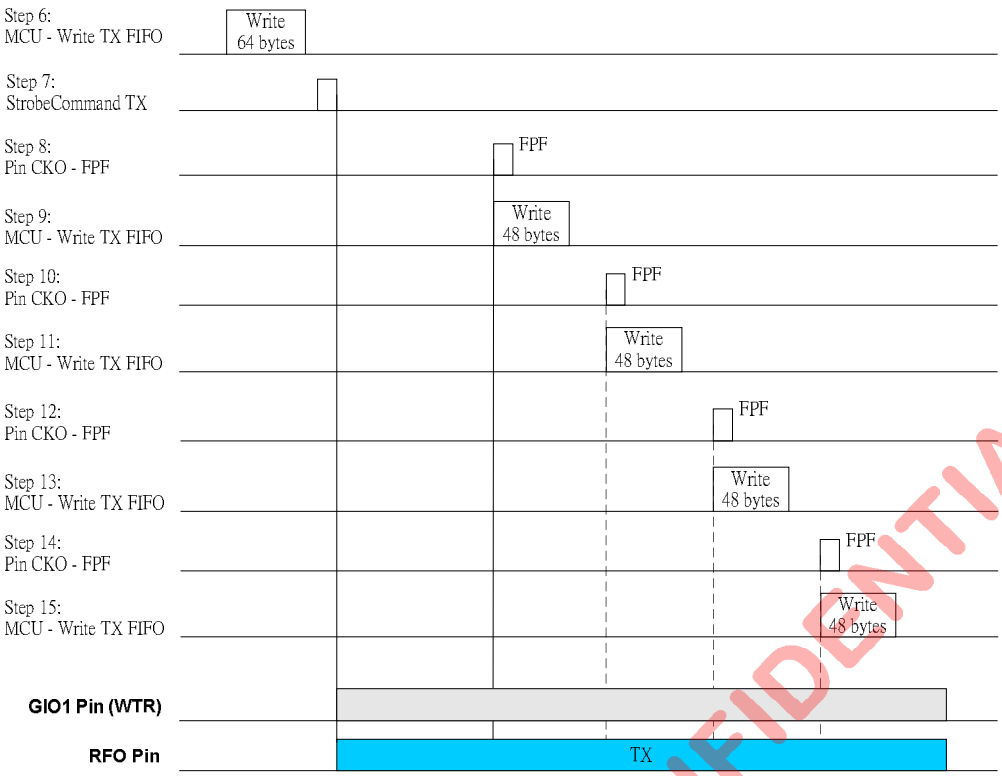
TX			Control Registers		
FIFO Length (byte)	**FPF Trigger Condition**	**Max SPI Data Rate**	**FEP[7:0]**	**FPM[1:0]**	**PSA[5:0]**
256	Delta = 04	10 Mbps	0xFF	00	0
	Delta = 08	**8 Mbps**		**01**	0
	Delta = 12	5 Mbps		10	0
	Delta = 16	4 Mbps		11	0

Table 16.6 How to set FIFO extension when A7328 is at 1Mbps data rate

Please refer to AMICCOM's reference code (FIFO extension) for details.

Procedures of TX FIFO Extension

1. Initialize all control registers (refer A7328 reference code).
2. Set FEP [7:0] = 0xFF for 256-bytes FIFO extension.
3. Set FPM [1:0] = 11 for FPF trigger condition.
4. Set CKO Register = 0x12
5. Send Strobe command – TX FIFO write pointer reset.
6. MCU writes 1st 64-bytes TX FIFO.
7. Send TX Strobe command.
8. MCU monitors FPF from A7328's CKO pin.
9. FPF triggers MCU to write 2nd 48-bytes TX FIFO.
10. Monitor FPF.
11. FPF triggers MCU to write 3rd 48-bytes TX FIFO.
12. Monitor FPF.
13. FPF triggers MCU to write 4th 48-bytes TX FIFO.
14. Monitor FPF.
15. FPF triggers MCU to write 5th 48-bytes TX FIFO.
16. Done.



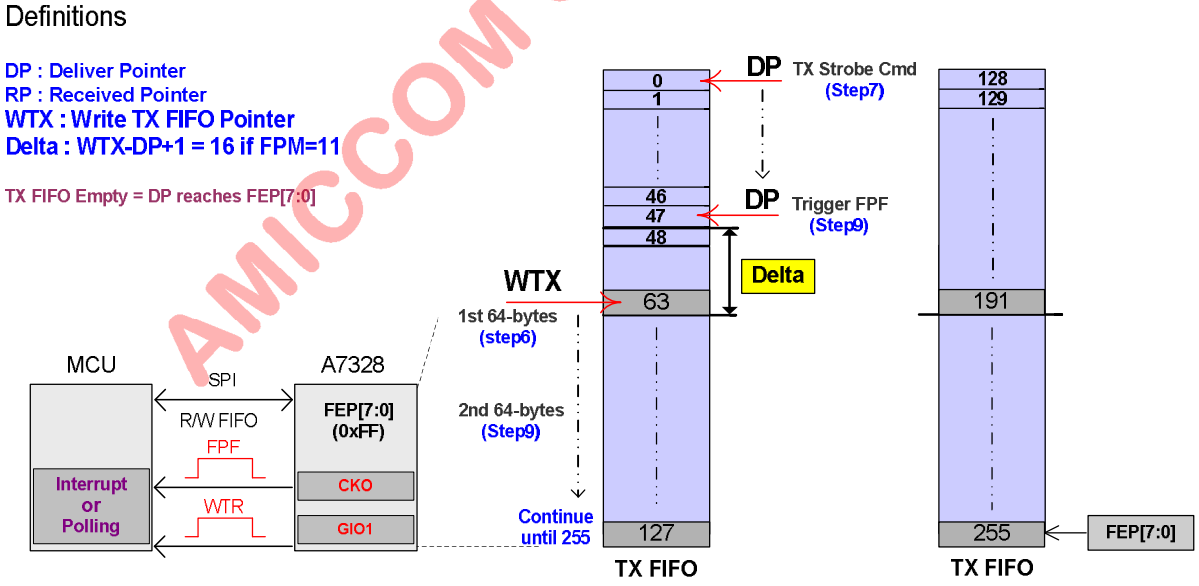


Figure 16.5 TX FIFO Extension

17. ADC (Analog to Digital Converter)

A7328 has built-in 8-bits ADC that supports multi-functions to do temperature measurement and convert external analog voltage (BP_RSSI pin) into 8-bits digital value. User can set FSARS (1Bh) to select 4MHz or 8MHz ADC clock (F_{ADC}). The converting time is 20 x ADC clock periods. FSARS = 0 is recommended to result less power comsumption.

Bit		Description	
XADS (1Bh)	RSS (1Fh)	Standby mode	RX mode
0	0	Temperature	None
0	1	None	RSSI / Carrier detect
1	x	External voltage via BP_RSSI pin	None

XADS (1Bh)	RFT[2:0] (2Dh)	BP_BG (Pin 1)	XADI
0	[00]	Band-gap voltage	For external AD input.
0	[01]	Analog temperature voltage	Analog temperature voltage
0	[10]	External ADC input source	For external AD input.

17.1 Temperature Measurement

A7328 has built-in thermal sensor. Combined with 8-bits ADC, it can be used to monitor the relative environment temperature. Below is the measurement procedure:

1. Set RSS= 0 (1Fh), FSARS= 0 (1Bh).
2. Enter Standby mode.
3. Set ADCM= 1 (01h). A7328 will enable relative temperature measurement automatically.
4. After measurement done, ADCM is auto clear.
5. User can read digital temperature value from ADC [7:0] (1Bh).

17.2 External Voltage Measurement

BP_RSSI pin can be programmed to be input pin for external voltage measurement which range is 0.3V ~ 1.5V. Below is the measurement procedure:

1. Connect external voltage input to BP_RSSI pin.
2. Set XADS= 1 (1Bh).
3. Enter standby mode.
4. Set ADCM= 1 (01h) to enable external voltage measurement.
5. After measurement done, ADCM is auto clear.
6. User can read digital external voltage value from ADC [7:0] (1Bh).

18. Battery Detect

A7328 has built-in battery detector to check supply voltage (REGI pin). The detect range is 2.1V ~ 2.8V into 8 levels.

Relative Control Register

Battery Detect Register (Address: 26h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	RGV1	RGV0	BDF	BVT2	BVT1	BVT0	BD_E
	W	ECKS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BD_E
Reset		0	1	0	0	0	1	1	0

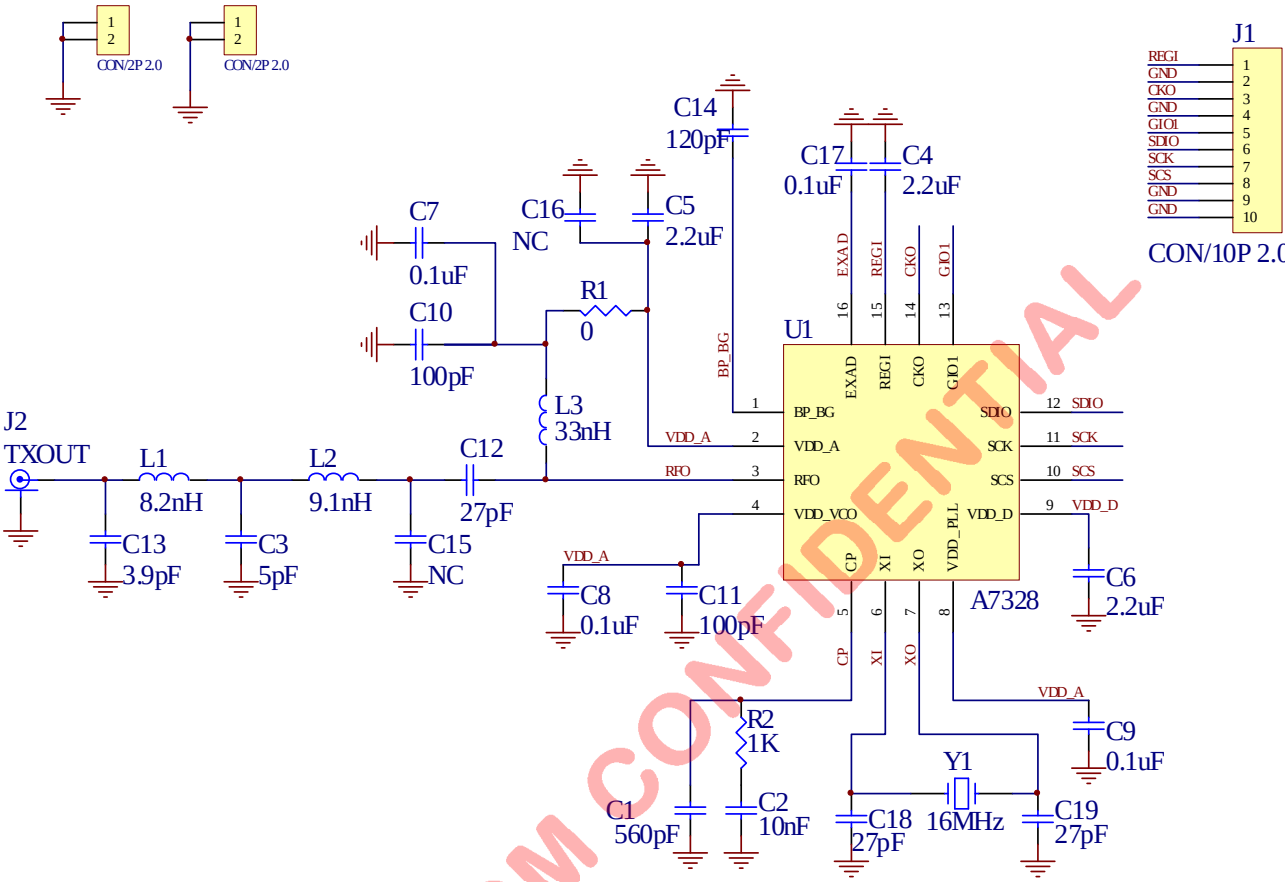
BVT [2:0]: Battery Voltage Threshold Select.
[000]: 2.1V, **[001]:** 2.2V. **[010]:** 2.3V. **[011]:** 2.4V. **[100]:** 2.5V. **[101]:** 2.6V. **[110]:** 2.7V. **[111]:** 2.8V.
(Typical +-0.1V detection inaccuracy.)

Below is the procedure of battery detector for low voltage detection (ex., below 2.3V):

1. Set A7328 in idle, standby or PLL mode.
2. Set BVT = [010] and enable BD_E = 1.
3. After 5 us, BD_E is auto clear.
4. Check BDF.
   If REGI pin > 2.3V,
   BDF = 1. Else, BDF = 0.

19. Application Circuit

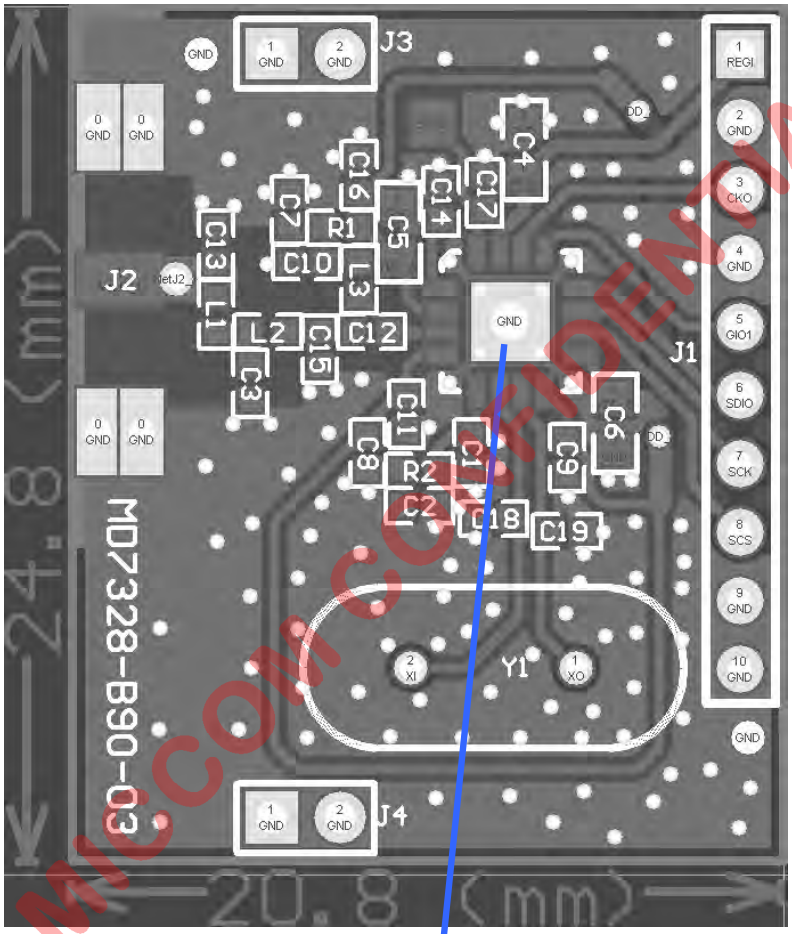
19.1 MD7328-B90 (915MHz Band)



1. A7328 schematic for RF layouts with single ended 50Ω RF output.
2. C20 and C21 must be matched to the crystal's load capacitance (Cload). Y1 is a 16MHz crystal with 18 pF Cload.

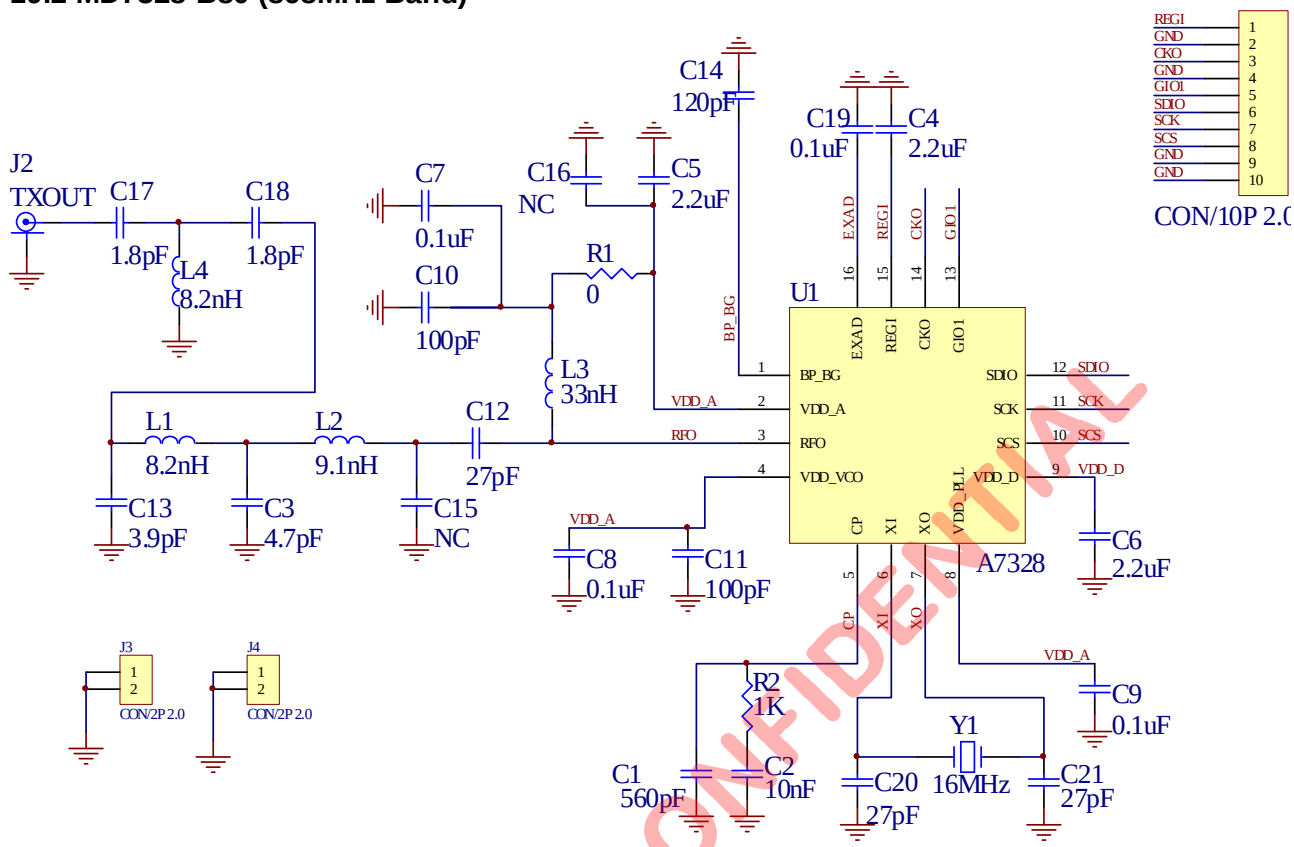
MD7328-B90 is based on a design by a double-sided **FR-4** board of **0.8mm** thickness. All passive components are 0402 size. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. Keep sufficient via holes to connect the top layer ground areas to the bottom layer ground plane. **Be notice, IC back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

To get a good RF performance, a well designed PCB is necessary. A poor layout can lead to loss of RF performance especially on matching networks as well as VDD bypass capacitors. PCB layout of critical traces shall follow AMICCOM's recommended values and layout placement. Long power supply lines on the PCB should be avoided. Keep GND via holes as close as possible to A7328's **GND** pad and IC back side plate (**GND**).



Be Notice,
1. IC Back side plate shall be well-solder to ground (U1 area) for good RF performance.

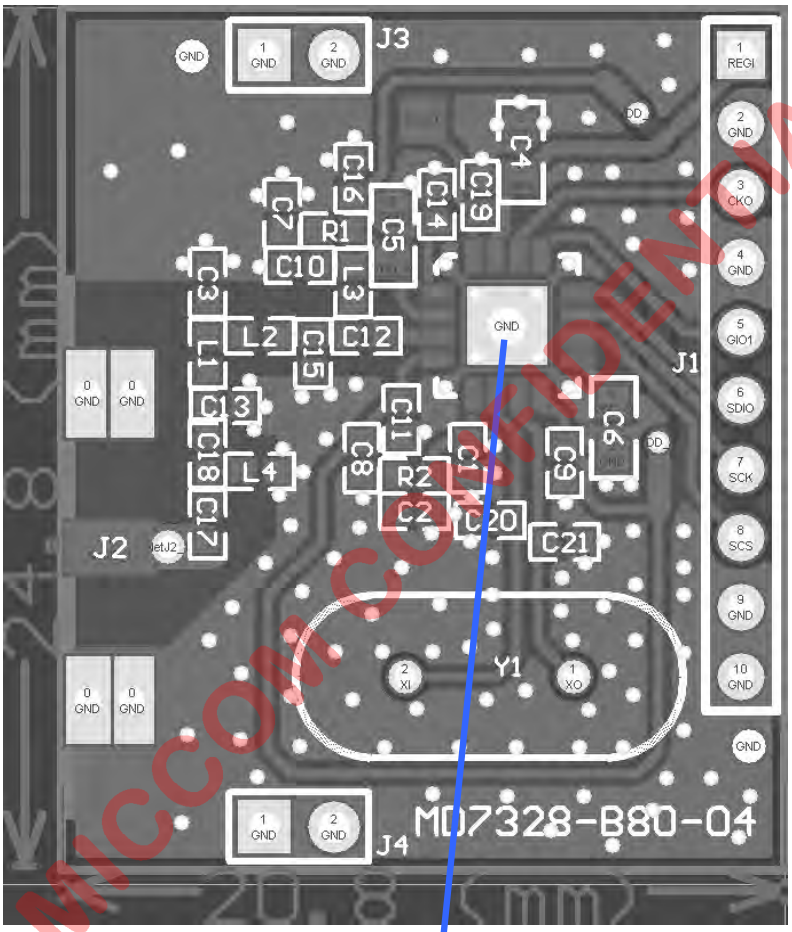
19.2 MD7328-B80 (868MHz Band)



1. A7328 schematic for RF layouts with single ended 50Ω RF output.
2. C20 and C21 must be matched to the crystal's load capacitance (Cload). Y1 is a 16MHz crystal with 18 pF Cload.

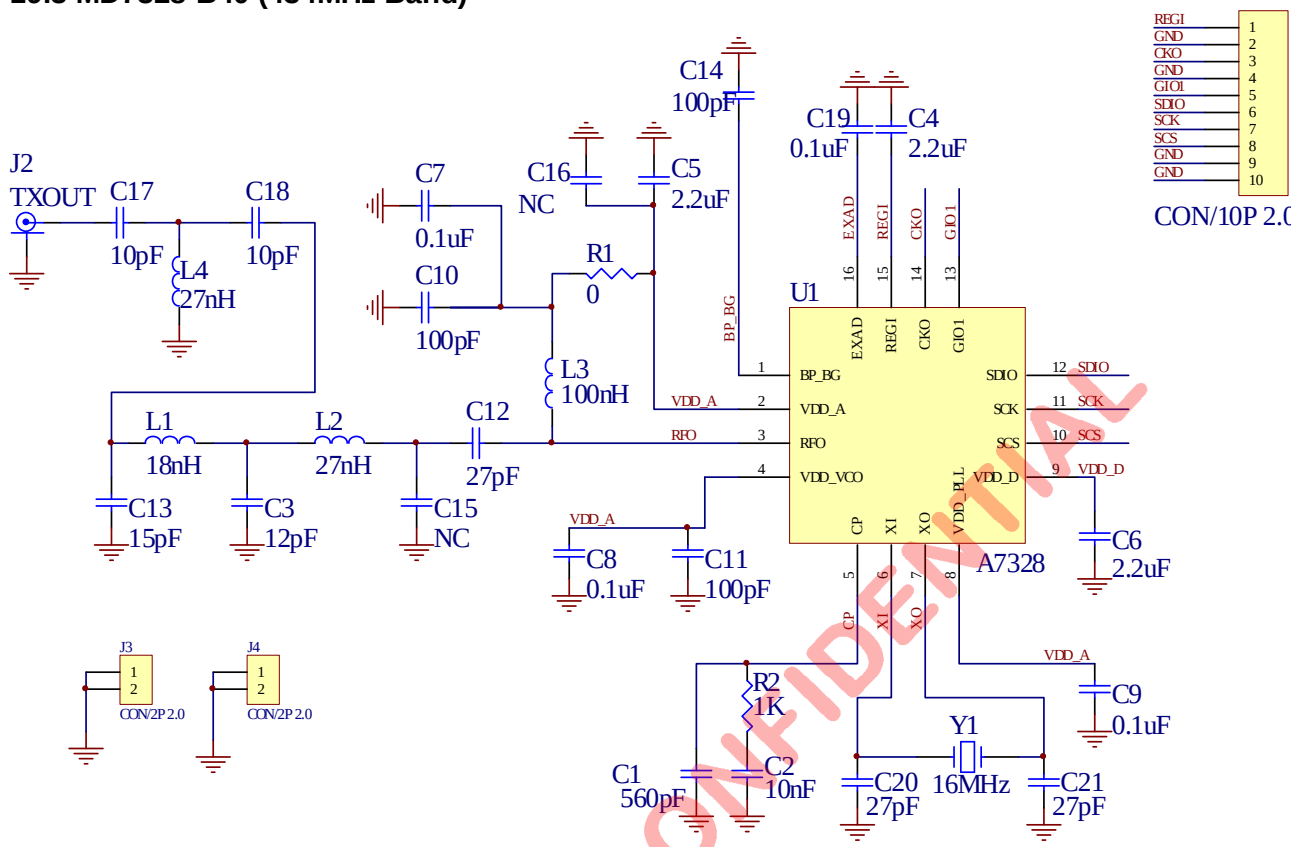
MD7328-B80 is based on a design by a double-sided **FR-4** board of **0.8mm** thickness. All passive components are 0402 size. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. Keep sufficient via holes to connect the top layer ground areas to the bottom layer ground plane. **Be notice, IC back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

To get a good RF performance, a well designed PCB is necessary. A poor layout can lead to loss of RF performance especially on matching networks as well as VDD bypass capacitors. PCB layout of critical traces shall follow AMICCOM's recommended values and layout placement. Long power supply lines on the PCB should be avoided. Keep GND via holes as close as possible to A7328's **GND** pad and IC back side plate (**GND**).



Be Notice,
2. IC Back side plate shall be well-solder to ground (U1 area) for good RF performance.

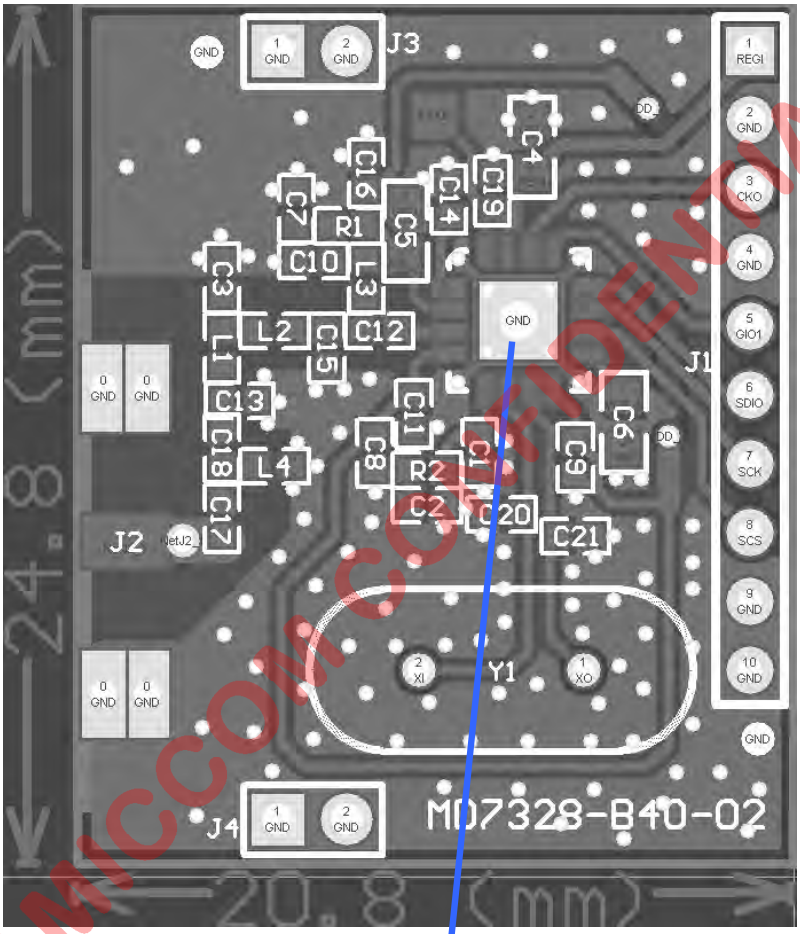
19.3 MD7328-B40 (434MHz Band)



3. A7328 schematic for RF layouts with single ended 50Ω RF output.
4. C20 and C21 must be matched to the crystal's load capacitance (Cload). Y1 is a 16MHz crystal with 18 pF Cload.

MD7328-B40 is based on a design by a double-sided **FR-4** board of **0.8mm** thickness. All passive components are 0402 size. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. Keep sufficient via holes to connect the top layer ground areas to the bottom layer ground plane. **Be notice, IC back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

To get a good RF performance, a well designed PCB is necessary. A poor layout can lead to loss of RF performance especially on matching networks as well as VDD bypass capacitors. PCB layout of critical traces shall follow AMICCOM's recommended values and layout placement. Long power supply lines on the PCB should be avoided. Keep GND via holes as close as possible to A7328's **GND** pad and IC back side plate (**GND**).



Be Notice,
3. IC Back side plate shall be well-solder to ground (U1 area) for good RF performance.

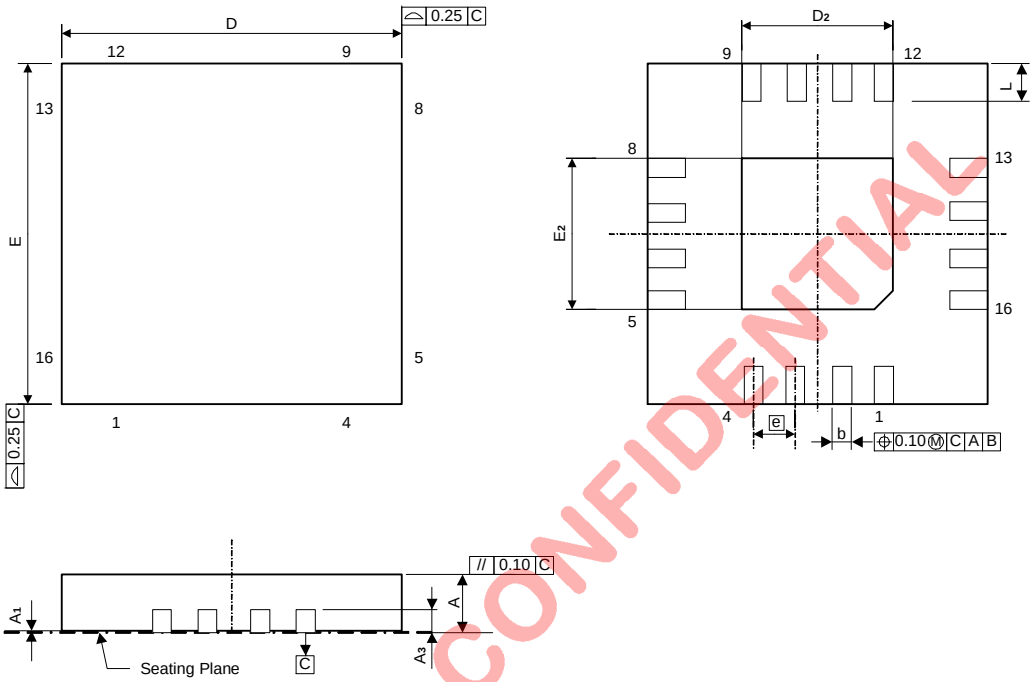
20. Ordering Information

Part No.	Package	Units Per Reel / Tray
A73C28AQFI/Q	QFN16L, Pb Free, Tape & Reel, -40℃～85℃	3K
A73C28AQFI	QFN16L, Pb Free, Tray, -40℃～85℃	490EA

21. Package Information

QFN 16L (4 X 4 X 0.8mm) Outline Dimensions unit: inches/mm

TOP VIEW **BOTTOM VIEW**

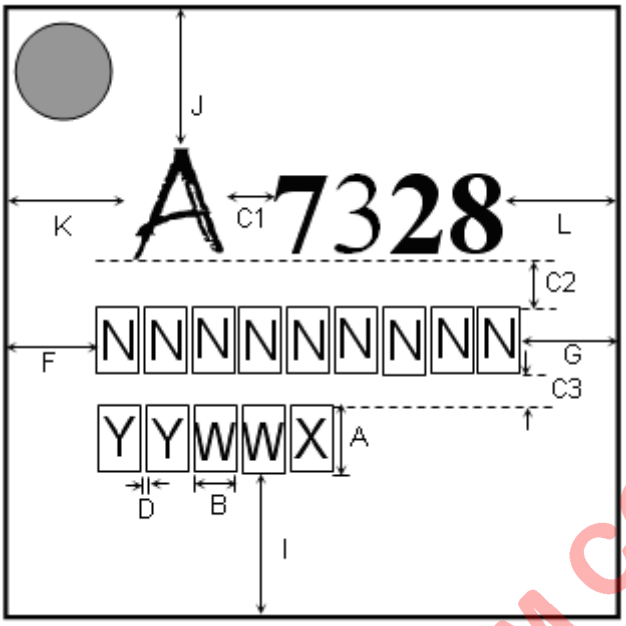


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.032	0.7	0.75	0.8
A_1	0	0.001	0.002	0	0.02	0.05
A_3	0.008REF					
b	0.001	0.012	0.015	0.25	0.3	0.35
D	0.152	0.157	0.163	3.85	4.00	4.15
D_2	0.079	0.091	0.102	2.00	2.30	2.60
E	0.152	0.157	0.163	3.85	4.00	4.15
E_2	0.079	0.091	0.102	2.00	2.30	2.60
e	0.026BSC					
L	0.016	0.021	0.026	0.40	0.53	0.65

22. Top Marking Information

A73C28AQFI

- Part No. : **A73C28AQFI**
- Pin Count : **16**
- Package Type : **QFN**
- Dimension : **4*4 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**



❖ **CHARACTER SIZE : (Unit in mm)**

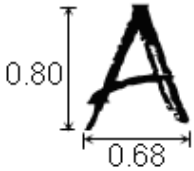
A : 0.55
B : 0.36
C1 : 0.25 C2 : 0.3 C3 : 0.2
D : 0.03
A1 : 0.75
B2 : 0.7

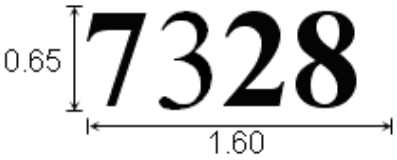
F=G
I=J
K=L

YYWW : DATECODE

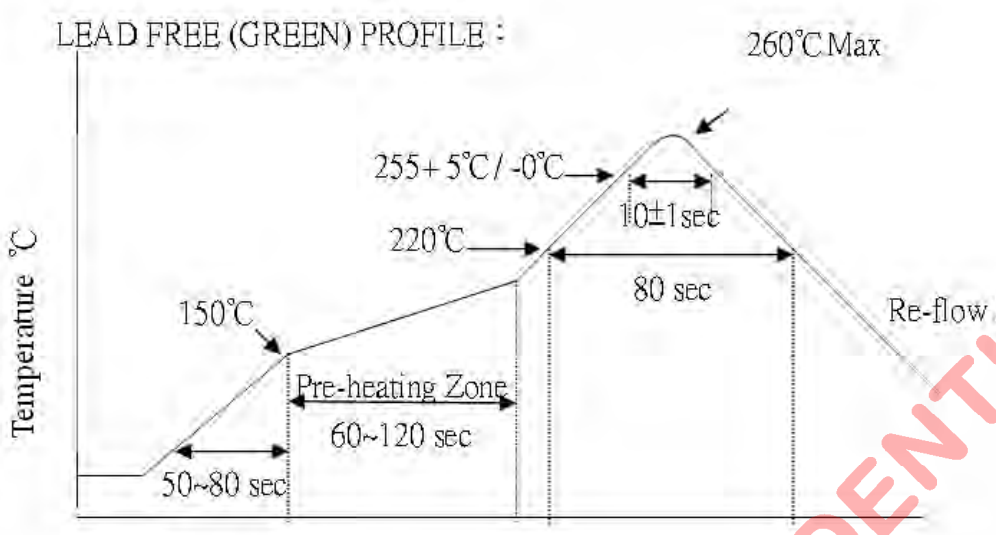
X : PKG HOUSE ID

NNNNNNNNN : LOT NO.
(max. 9 characters)



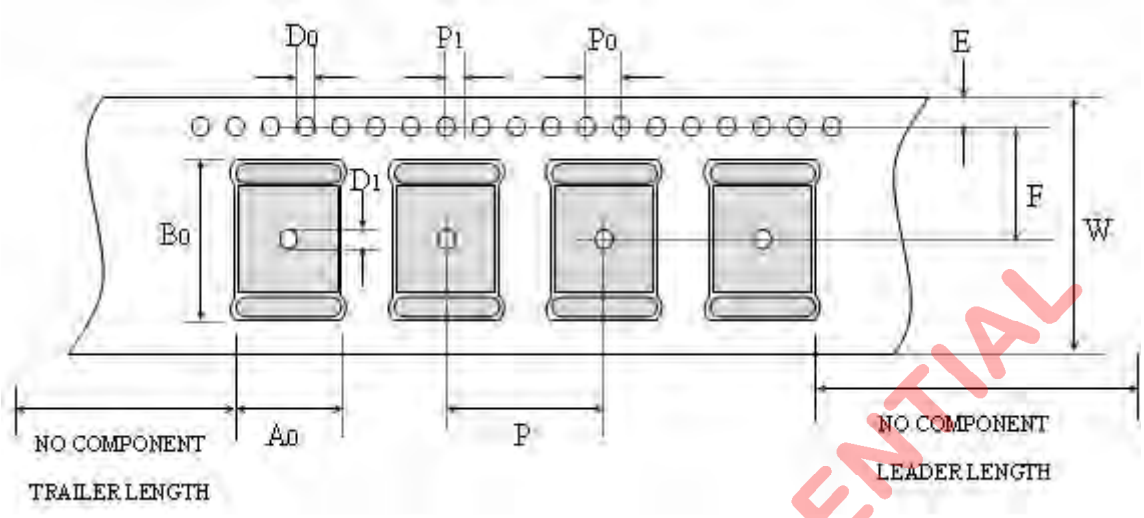


23. Reflow Profile



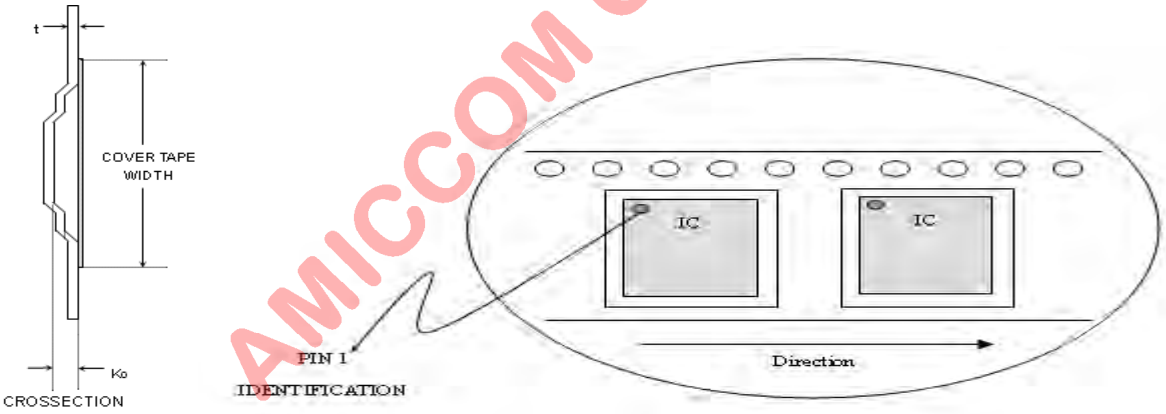
24. Tape Reel Information

Cover / Carrier Tape Dimension



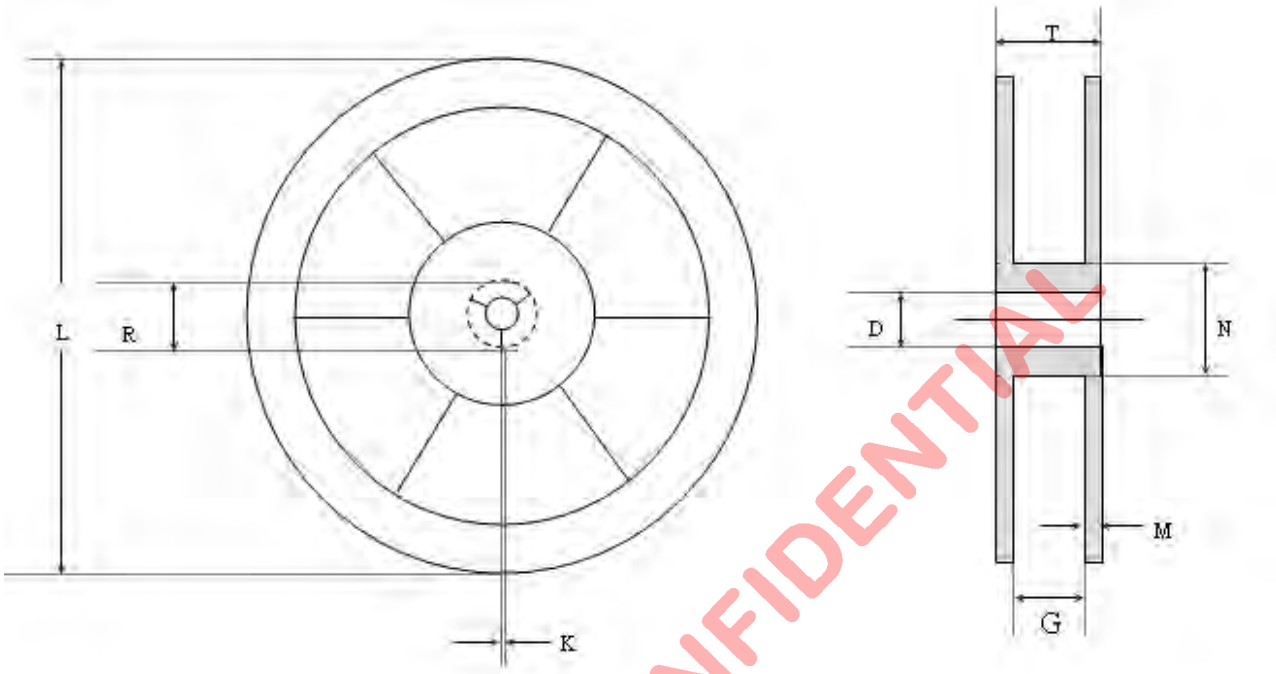
Unit: mm

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W
20 QFN 4*4	8	4.35	4.35	4.0	2.0	1.5	1.5	1.75	5.5	12
24 QFN 4*4	8	4.4	4.4	4.0	2.0	1.5	1.5	1.75	5.5	12
32 QFN 5*5	8	5.25	5.25	4.0	2.0	1.5	1.5	1.75	5.5	12
QFN3*3 / DFN-10	4	3.2	3.2	4.0	2.0	1.5	-	1.75	1.9	8
20 SSOP	12	8.2	7.5	4.0	2.0	1.5	1.5	1.75	7.5	16
24 SSOP	12	8.2	8.8	4.0	2.0	1.5	1.5	1.75	7.5	16



TYPE	K0	t	COVER TAPE WIDTH
20 QFN (4X4)	1.1	0.3	9.2
24 QFN (4X4)	1.4	0.3	9.2
32 QFN (5X5)	1.1	0.3	9.2
QFN3*3 / DFN-10	0.75	0.25	8
20 SSOP	2.5	0.3	13.3
24 SSOP	2.1	0.3	13.3

REEL DIMENSIONS



Unit: mm

TYPE	G	N	T	M	D	K	L	R
20 QFN(4X4) 24 QFN(4X4) 32 QFN(5X5) QFN(3X3) / DFN-10	12.8+0.6/-0.4	100 REF	18.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330＋ 0.00/-1.0	20.2
20 SSOP 24 SSOP	16.4+2.0/-0.0	100 REF	22.4(MAX)	1.75±0.25	13.0+0.2/-0.2	1.9±0.4	330＋ 0.00/-1.0	20.2

25 Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date.AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

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