DESCRIPTION

A7330 is a wide input voltage, high efficiency step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. A7330 provides up to 3.1A output current at 125kHz switching frequency.

A7330 integrates control scheme to achieve high-accuracy constant current control without the expensive, high accuracy current sense resistor. It also integrates adaptive gate drive to achieve excellent EMI performance passing EN55022 Class B EMC standard without adding additional EMI components while maintaining high conversion efficiency.

Protection features include cycle-by-cycle current limit, thermal shutdown, and frequency foldback at short circuit.

The A7330 is available in PSOP8 package.

ORDERING INFORMATION

Package Type	Part Number	
PSOP8 SPQ: 4,000pcs/Reel	MP8	A7330MP8R
		A7330MP8VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

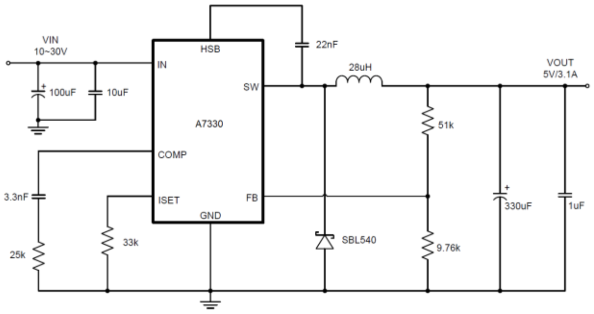
FEATURES

- Up to 3.1A output current
- 125kHz Switching Frequency Eases EMI Design
- 91% Efficiency (V_{OUT}=5V@2.4A at V_{IN}=12V)
- Resistor Programmable for Output Cable Drop Compensation
- Cycle-by-Cycle Current Limit, Input Over Voltage Protect, Thermal Shutdown, Input Under Voltage Lockout
- Integrated Soft Start
- ±7.5% CC Accuracy
- ±2% CV Accuracy
- High-Side R_{DSON} 50mΩ
- Available in PSOP8 package

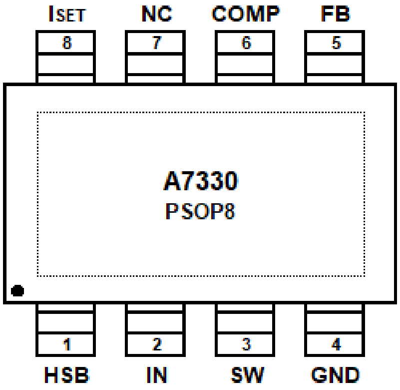
APPLICATION

- Car Charger/ Adaptor
- General-Purpose CV/CC Power Supply
- Rechargeable Portable Devices

TYPICAL APPLICATION



PIN DESCRIPTION



Top View

Pin #	Symbol	Function
1	HSB	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22nF capacitor from HSB pin to SW pin.
2	IN	Power Supply Input. Bypass this pin with a 10μF ceramic capacitor to GND, placed as close to the IC as possible.
3	SW	Power Switching Output to External Inductor.
4	GND	Ground. Connect this pin to a large PCB copper area for best heat dissipation. Return FB, COMP, and ISET to this GND, and connect this GND to power GND at a single point for best noise immunity.
5	FB	Feedback Input. The voltage at this pin is regulated to 800mV. Connect to the resistor divider between output and GND to set the output voltage.
6	COMP	Error Amplifier Output. This pin is used to compensate the converter.
7	NC	No connection.
8	I_{SET}	Output Current Setting Pin. Connect a resistor from I_{SET} to GND to program the output current.
	Exposed Pad	Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

ABSOLUTE MAXIMUM RATINGS

V_{IN}, IN to GND	-0.3V ~ 32V
V_{SW}, SW to GND	-1V ~ V_{IN}+1V
V_{GATE}, HSB to GND	V_{SW}-0.3V ~ V_{SW}+7V
V_{IO}, FB, I_{SET}, COMP to GND	-0.3V ~ 6V
T_{STG}, Storage Temperature Range	-40℃ ~ 150℃
T_J, Operating Junction Temperature	-40℃ ~ 150℃
ESD Human Model	4kV

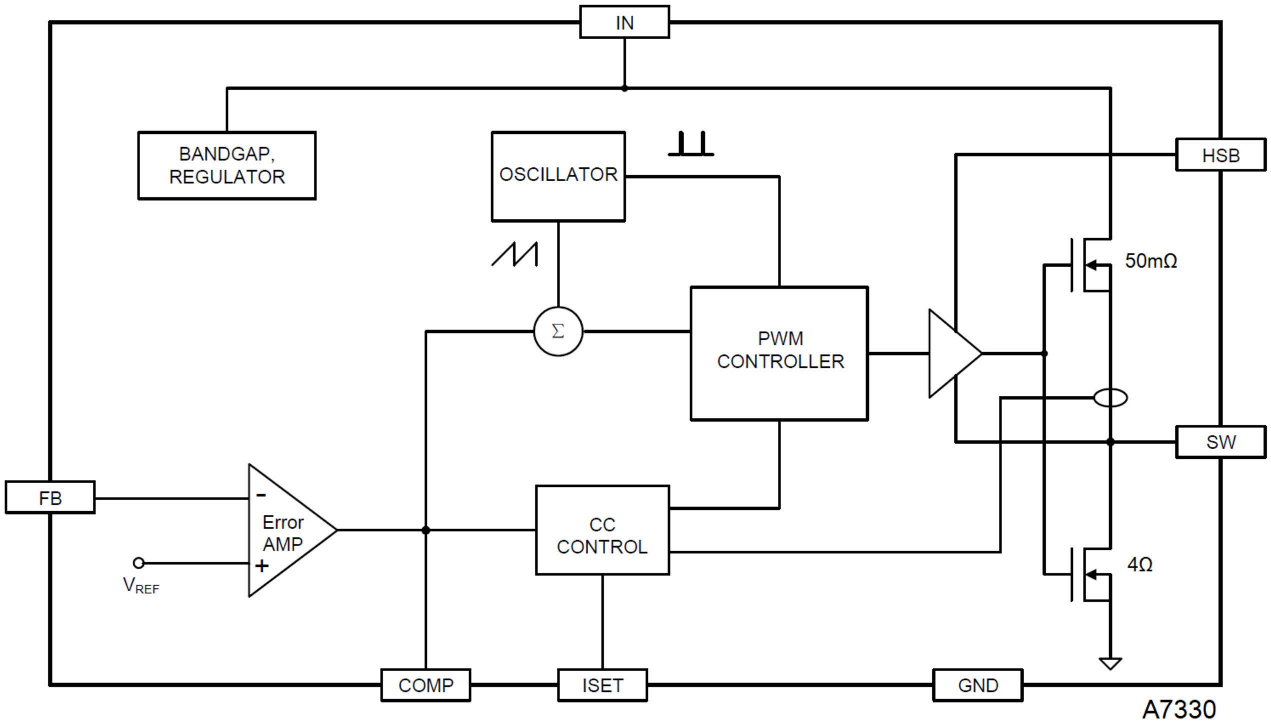
Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A =+25°C, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage		6.4	-	30	V
Input Voltage Surge		-	-	32	V
V_{IN} UVLO Turn-On Voltage	Input Voltage Rising	5.6	6	6.4	V
V_{IN} UVLO Hysteresis	Input Voltage Falling	-	0.5	-	V
Standby Supply Current	V_{FB}=1V	-	0.88	1.4	mA
Feedback Voltage		785	800	815	mV
Internal Soft-Start Time		-	500	-	μs
Error Amplifier Transconductance	$V_{FB}=V_{COMP}=0.8V$ $\Delta I_{COMP}=\pm 10\mu A$	-	650	-	μA/V
Error Amplifier DC Gain		-	4000	-	V/V
Switching Frequency	V_{FB}=0.8V	-	125	-	kHz
Foldback Switching Frequency	V_{FB}=0V	-	18	-	kHz
Maximum Duty Cycle		-	87	-	%
Minimum On-Time		-	300	-	ns
COMP to Current Limit Transconductance	V_{COMP}=1.7V	-	3.47	-	A/V
Secondary Cycle-by-Cycle Current Limit		-	6.4	-	A
Slope Compensation	Duty=DMAX	-	3	-	A
I_{SET} Voltage		-	1	-	V
I_{SET} to I_{OUT} DC Room Temp Current Gain	I_{OUT}/I_{SET} , R_{ISET}=25kΩ	-	90000	-	A/A
CC Controller DC Accuracy	R_{ISET}=24.9kΩ, V_{OUT}=4.0V	-	3500	-	mA
Thermal Shutdown Temperature	Temperature Rising	-	155	-	℃
Thermal Shutdown Temperature Hysteresis	Temperature Falling	-	25	-	℃

BLOCK DIAGRAM



DETAILED INFORMATION

Application Information

CV/CC Loop Regulation

As seen in Function Block Diagram, the A7330 is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows:

A switching cycle starts when the falling edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes high, the High-Side Power Switch turns off.

At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using HSB as the positive rail. This pin is charged to V_{SW}+5V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.8V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the CC limit set by the ISET resistor. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

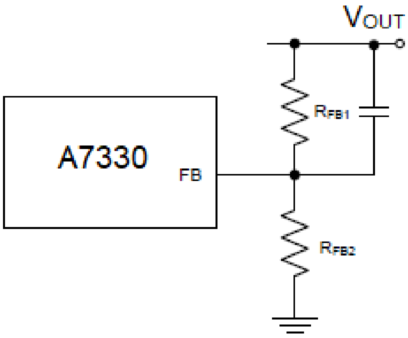
The Oscillator normally switches at 125kHz. However, if FB voltage is less than 0.6V, then the switching frequency decreases until it reaches a typical value of 18kHz at V_{FB} = 0.15V.

Thermal Shutdown

The A7330 disables switching when its junction temperature exceeds 155℃ and resumes when the temperature has dropped by 25℃.

Output Voltage Setting

The figure shows the connections for setting the output voltage.

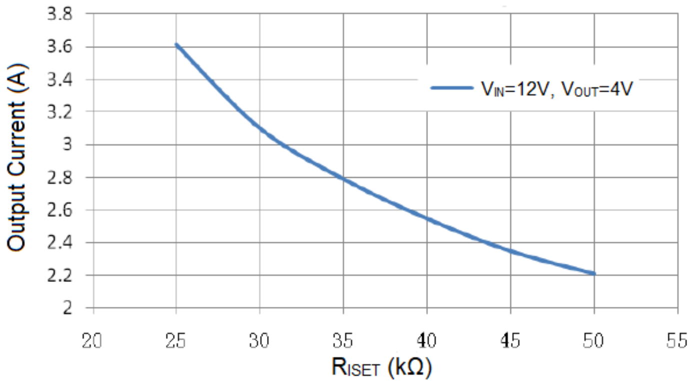


Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Adding a capacitor in parallel with R_{FB1} helps the system stability. Typically, use $R_{FB2} \approx 10k\Omega$ and determine R_{FB1} from the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.8V} - 1\right)$$

CC Current Setting

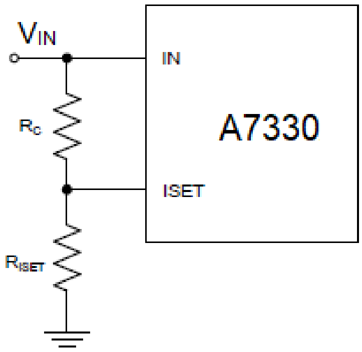
A7330 constant current value is set by a resistor connected between the I_{SET} pin and GND. The CC output current is linearly proportional to the current flowing out of the I_{SET} pin. The voltage at I_{SET} is roughly 1V and the current gain from I_{SET} to output is roughly 90000. To determine the proper resistor for a desired current, please refer to figure below.



Output Current vs. R_{ISET}

CC Current Line Compensation

When operating at constant current mode, the current limit increase slightly with input voltage. For wide input voltage applications, a resistor R_C may be added to compensate line change and keep output high CC accuracy, as shown figure below.



Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value.

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{LOADMAX} \times K_{RIPPLE}}$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE}=30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK\text{-}PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}}$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK\text{-}PK}$$

The selected inductor should not saturate at I_{LPK}.

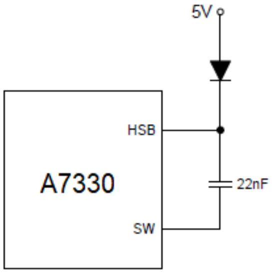
The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK\text{-}PK}$$

I_{LIM} is the internal current limit, which is typically 5.4A, as shown in Electrical Characteristics Table.

External High Voltage Bias Diode

It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148 or BAT54, as figure shown below.



This diode is also recommended for high duty cycle operation and high output voltage applications.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10µF. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1µF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} \times K_{RIPPLE} \times R_{ESR} + \frac{V_{IN}}{28 \times \int_{SW}{}^{2} LC_{OUT}}$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

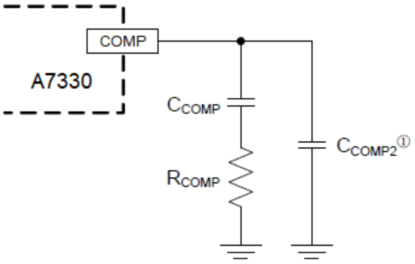
For ceramic output capacitor, typically choose a capacitance of about 22µF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

Stability Compensation

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in figure below.



NOTE ①: C_{COMP2} is needed only for high ESR output capacitor

The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.8V}{I_{OUT}} \times A_{VEA} \times G_{COMP}$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}}$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}}$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}}$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}}$$

The following steps should be used to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R_{COMP}:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} \int SW}{10 G_{EA} G_{COMP} \text{ x } 0.8V}$$

$$=5.17 \text{ x } 10^7 V_{OUT} C_{OUT} \ldots\ldots\ldots\ldots (\Omega)$$

STEP 2. Set the zero fZ1 at 1/4 of the cross over frequency. If R_{COMP} is less than 15kΩ, the equation for C_{COMP} is:

$$C_{COPM} = \frac{2.83 \text{ x} 10^5}{R_{COMP}} \ldots\ldots\ldots\ldots\ldots\ldots\text{(F)}$$

If R_{COMP} is limited to 15kΩ, then the actual cross over frequency is 6.58 / ($V_{OUT}C_{OUT}$). Therefore:

$$C_{COMP} = 6.45 \text{ x } 10^{-6} V_{OUT} C_{OUT} \ldots\ldots\ldots\text{(F)}$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESRCOUT} \geq \left(\text{Min} \frac{1.77 \text{x} 10^{-6}}{C_{OUT}}, 0.06 \text{ x } V_{OUT} \right) \ldots\ldots\ldots\ldots (\Omega)$$

And the proper value for C_{COMP2} is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}}$$

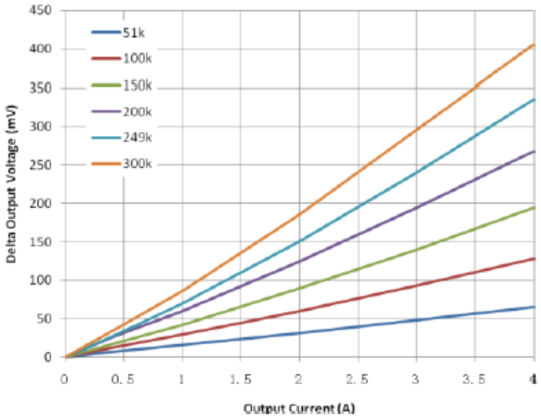
Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.

CC Loop Stability

The constant-current control loop is internally compensated over the 2000mA-3500mA output range. No additional external compensation is required to stabilize the CC current.

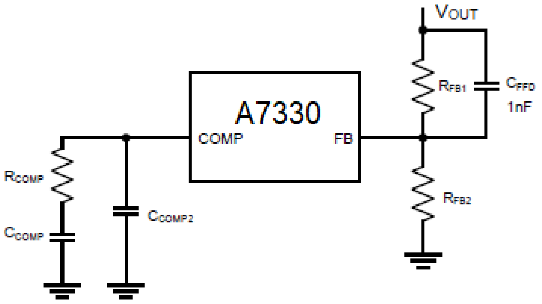
Output Cable Resistance Compensation

To compensate for resistive voltage drop across the charger's output cable, the A7330 integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin. Use the curve in figure below to choose the proper feedback resistance values for cable compensation. R_{FB1} is the high side resistor of voltage divider.



Delta Output Voltage vs. Output Current

In the case of high R_{FB1} used, the frequency compensation needs to be adjusted correspondingly. As show in figure below, adding a capacitor in paralleled with R_{FB1} or increasing the compensation capacitance at COMP pin helps the system stability.



PC Board Layout Guidance

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1) Arrange the power components to reduce the AC loop size consisting of C_{IN}, IN pin, SW pin and the schottky diode.

2) Place input decoupling ceramic capacitor C_{IN} as close to IN pin as possible. C_{IN} is connected power GND with vias or short and wide path.

3) Return FB, COMP and I_{SET} to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.

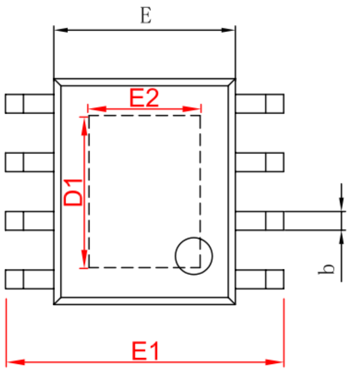
4) Use copper plane for power GND for best heat dissipation and noise immunity.

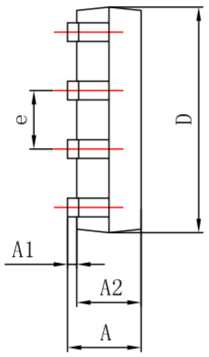
5) Place feedback resistor close to FB pin.

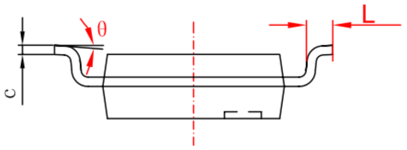
6) Use short trace connecting HSB-C_{HSB}-SW loop.

PACKAGE INFORMATION

Dimension in PSOP8 Package (Unit: mm)







Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.002	0.006
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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