DESCRIPTION

A7425 is a wide input voltage, high efficiency current mode Synchronous step-down DC/DC converter. A7425 provides up to 3A output current at 500kHz switching frequency.

A7425 integrates a 130mΩ high side and an 80mΩ low side MOSFET to achieve high conversion efficiency up to 96%. The current mode control architecture supports fast transient response and simple compensation circuit.

Protection features include cycle-by-cycle current limit, thermal shutdown, and short circuit protection.

The A7425 is available in PSOP8 package.

FEATURES

- Up to 40V Input Surge Voltage
- Continuous Operating Input Voltage up to 36V
- Up to 3A Output Current
- 500kHz Switching Frequency
- Up to 96% Efficiency
- Stable with Low-ESR Ceramic Output Capacitors
- Resistor Programmable High-Side MOSFET Peak Current Limit from 1.0A to 3.5A
- ±2% Feedback Voltage Accuracy
- Power Saving Mode reduces the quiescent current to 0.9mA
- Advanced Feature Set
  Integrated Soft-Start of Thermal Shutdown
  Cycle-by-Cycle Current Limit protection

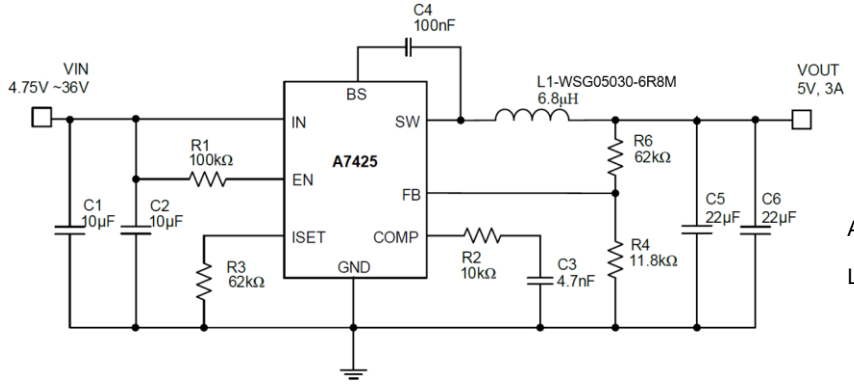
ORDERING INFORMATION

Package Type	Part Number	
PSOP8 SPQ: 4,000pcs/Reel	MP8	A7425MP8R
		A7425MP8VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

APPLICATION

- Distributed Power Systems
- Notebook Computers
- Broadband Communications
- Flat Panel TVs and Monitors
- Vehicle Electronics

TYPICAL APPLICATION

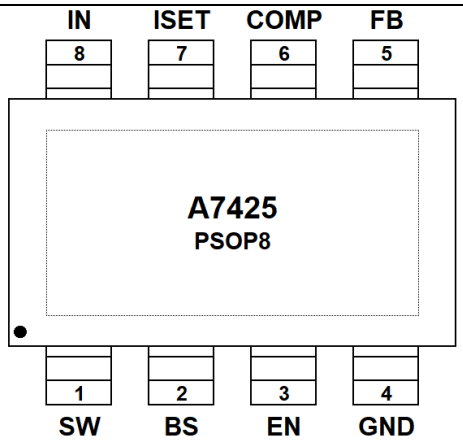


A7425 external Inductor suggest

L1=AiT Semi's # WSG05030-6R8M

V_{OUT} (V)	R6(kΩ)	R4(kΩ)	R2(kΩ)	L1(µH)	C3(nF)	C5(µF)	C6(µF)
12	270	19.6	10	6.8	4.7	22	22
9	200	19.6	10	6.8	4.7	22	22
5	62	11.8	10	6.8	4.7	22	22
3.3	62	20	4.3	4.7	4.7	22	22

PIN DESCRIPTION



PSOP8, MP8

Top View

Pin #	Symbol	Function
1	SW	Power Switching Output to External Inductor.
2	BS	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 100nF capacitor from BS pin to SW pin.
3	EN	Enable Input. EN is pulled up to 4.5V and contains a precise 2 V logic threshold. Drive this pin to a logic-high or leave unconnected to enable the IC. Drive to a logic-low to disable the IC and enter shutdown mode.
4	GND	Ground. Connect this pin to a large PCB copper area for best heat dissipation. Return FB, COMP, and ISET to this GND, and connect this GND to power GND at a single point for best noise immunity.
5	FB	Feedback Input. The voltage at this pin is regulated to 0.8V. Connect to the resistor divider between output and GND to set the output voltage.
6	COMP	Error Amplifier Output. This pin is used to compensate the converter.
7	ISET	Output Current Setting Pin. Connect a resistor from ISET to GND to program the output current limit.
8	IN	Power Supply Input. Bypass this pin with a suitable large ceramic capacitor to GND, placed as close to the IC as possible.
9	Exposed Pad	Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage	-0.3V ~ 42V
SW Voltage	-0.3V ~ 42V
Boost Voltage	-0.3V ~ (V_{SW} + 5.5V)
EN Pin	-0.3V ~ 6V
FB COMP ISET Pin	-0.3V ~ 5.5V
Junction Temperature	Internal Limited
Storage Temperature	-55°C ~ 150°C
Lead Temperature (Soldering 10 sec.)	260°C
Class 2 Ratings per ESDA/JEDEC JS-001-2014 Human Body Model	±4kV
Operating Temperature	-40°C ~ 85°C
Junction Temperature	125°C
$R_{\theta JA}$, PSOP8	50°C/W
$R_{\theta JC}$, PSOP8	15°C/W

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25℃, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}		4.75	-	36	V
UVLO Threshold	V_{UVLO}	V_{IN} Rising	3.9	4.1	4.3	V
Hysteresis	$V_{UVLOHYS}$	V_{IN} Falling	-	250	-	mV
Operation Current	I_{VIN}	I_{OUT}=0mA	-	0.9	-	mA
Quiescent Current	I_Q	V_{FB}=1V	-	0.8	1	mA
Shutdown Supply Current	$I_{SHUTDOWN}$	EN=0V	-	6	10	μA
Enable Threshold (High)	V_{EN_HIGH}		2	-	-	V
Enable Hysteresis	V_{EN_HYS}		-	-	0.4	V
Enable Internal Pull Up	I_{EN}		-	6	-	μA
ISET Voltage	V_{ISET}		0.98	1.005	1.04	V
ISET to I_{OUT} DC Current Gain	G_{ISET}	R_{ISET}=62kΩ	-	20,000	-	A/A
High-Side MOSFET Current Limit	I_{LIM_HS}	R_{ISET}=62kΩ	-	4	-	A
Output Sink Current	I_{SINK}	V_{FB}=0.7V	-	70	-	μA
Output Source Current	I_{SOURCE}	V_{FB}=0.9V	-	30	-	μA
Open Loop Gain	G_{VO}		-	4,000	-	V/V
Feedback Voltage	V_{FB}		788	800	812	mV
Feedback Current	I_{FB}		-	50	-	nA
Switching Frequency	$f_{SW\_0.8V}$	V_{FB}=0.8V	450	500	550	kHz
Hiccup Waiting Time	t_{FSW_0V}	V_{FB}=0V	-	200	-	ms
Maximum Duty Cycle	D_{MAX}	f_{SW}=500kHz	-	93	-	%
High-Side MOSFET On Resistance*	$R_{DS(ON\_H)}$		-	130	-	mΩ
Low-Side MOSFET On Resistance*	$R_{DS(ON\_L)}$		-	80	-	mΩ
High-Side MOSFET Leakage Current	I_{HIGH_LEAK}	V_{SW} = 0V	-	-	1	μA
Low-Side MOSFET Leakage Current	I_{LOW_LEAK}	V_{SW} = V_{IN}	-	-	1	μA
Soft-Start Time*	t_{SS}		-	1.5	-	ms
Thermal Shutdown Threshold NOTE1	T_{SDN}		-	160	-	°C
Thermal Shutdown Hysteresis	T_{SDN_HYS}		-	25	-	°C

*Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

All curves taken at V_{IN} = 12 V, V_{OUT} = 5 V, with configuration in Typical Application Circuit in this datasheet.

T_A = 25 °C, unless otherwise specified.

Fig.1 Efficiency vs. Output Current

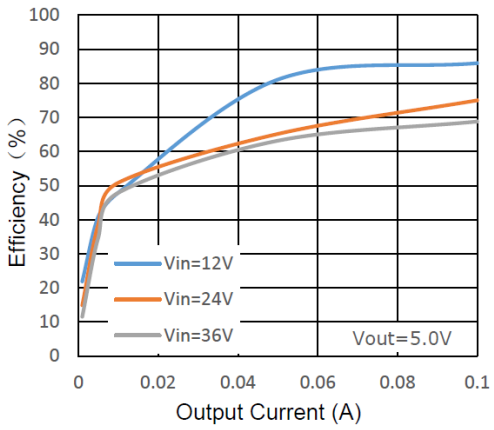


Fig.2 Efficiency vs. Output Current

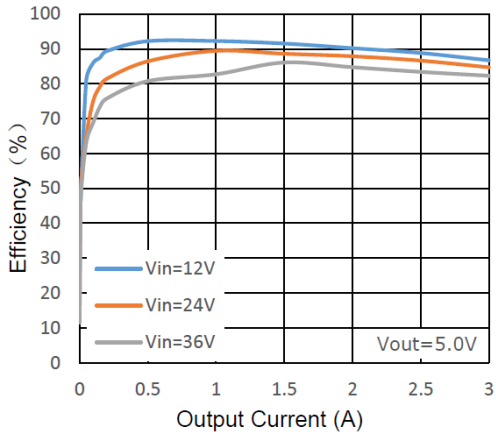


Fig.3 Reference Voltage vs. Input Voltage

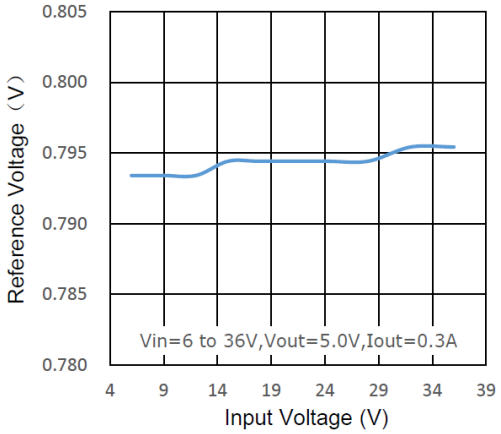


Fig.4 Reference vs. Temperature

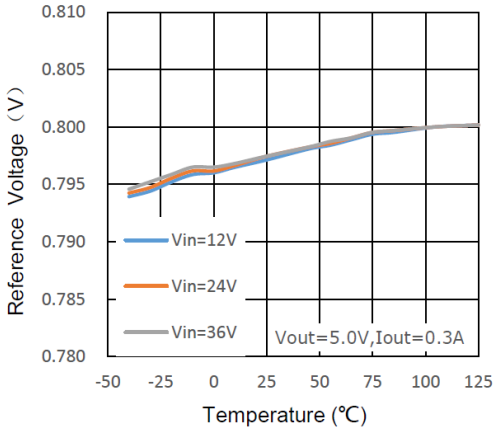


Fig.5 Output Voltage vs. Output Current

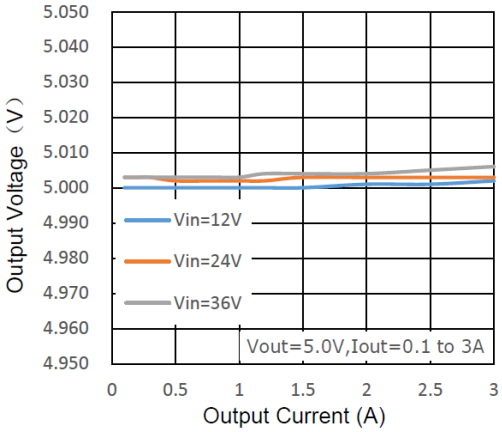


Fig.6 Switching Frequency vs. Input Voltage

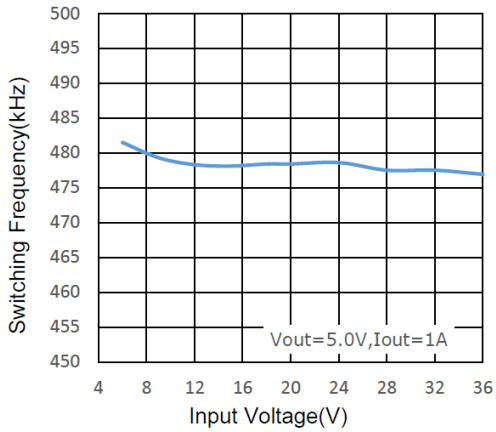


Fig.7 Reference Voltage vs. Input Voltage

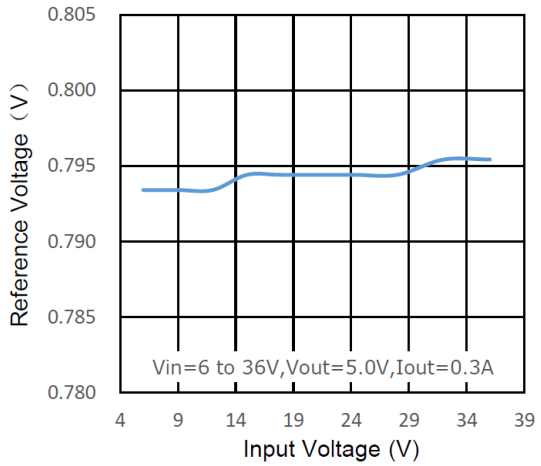


Fig.8 Reference Voltage vs. Temperature

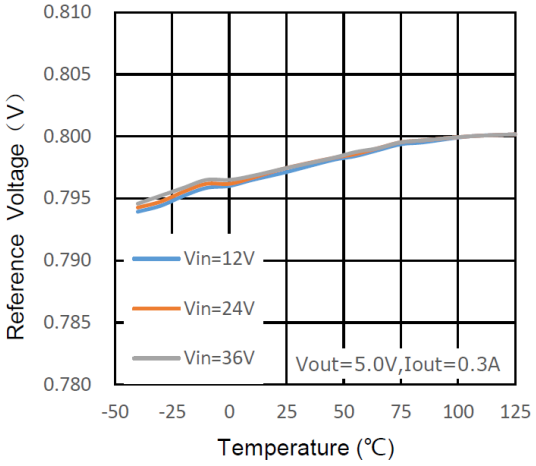


Fig.9 Load Transient Response

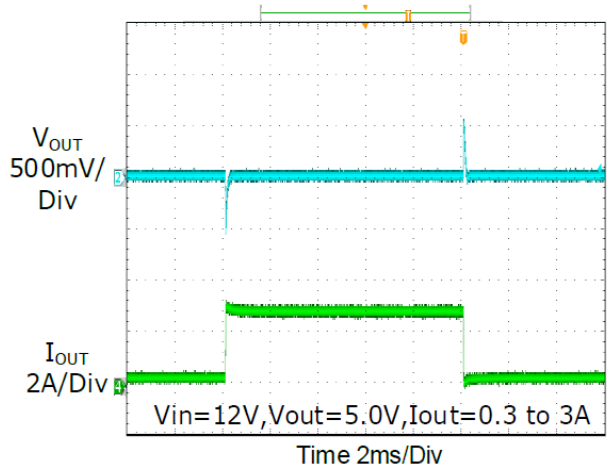


Fig.10 Load Transient Response

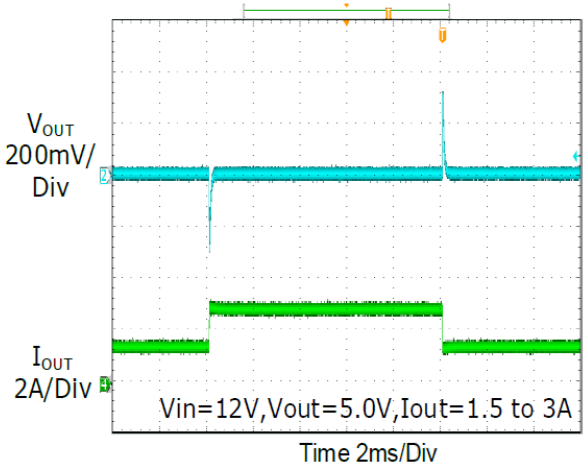


Fig.11 Switching

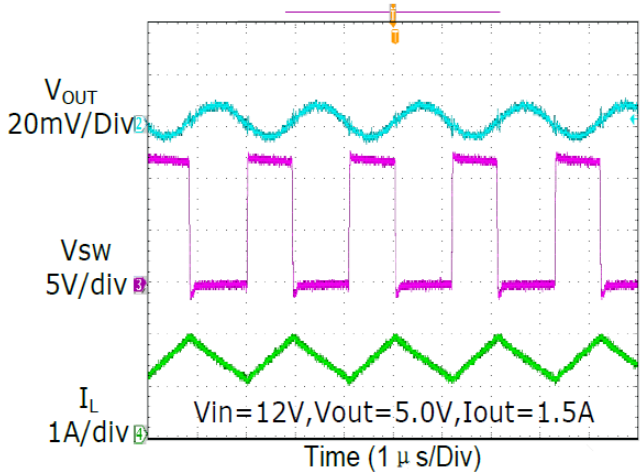


Fig.12 Switching

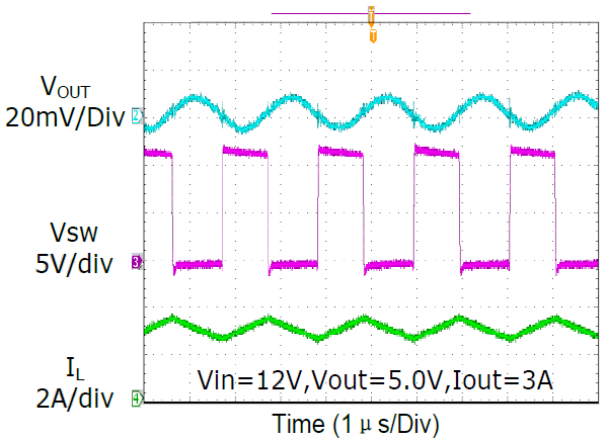


Fig.13 Power On from EN

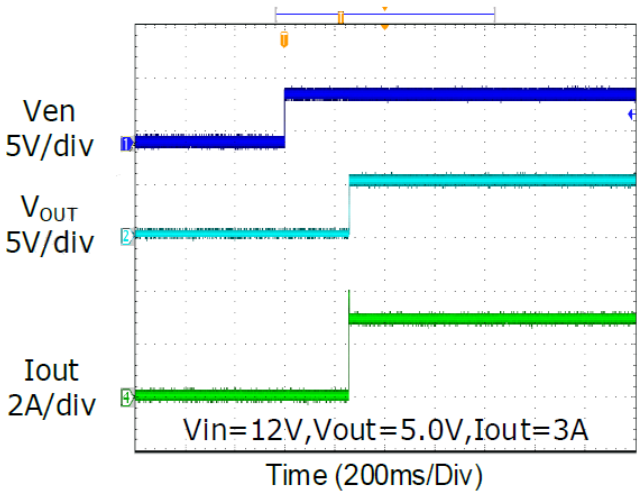


Fig.14 Power Off from EN

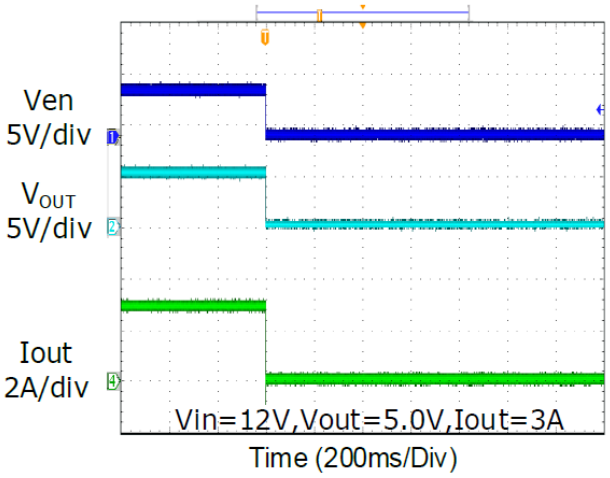
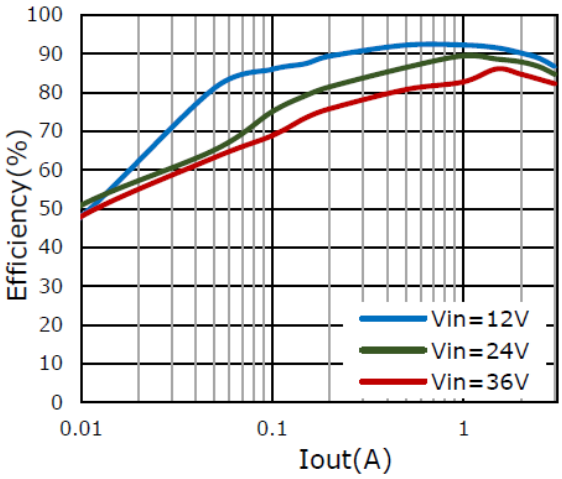
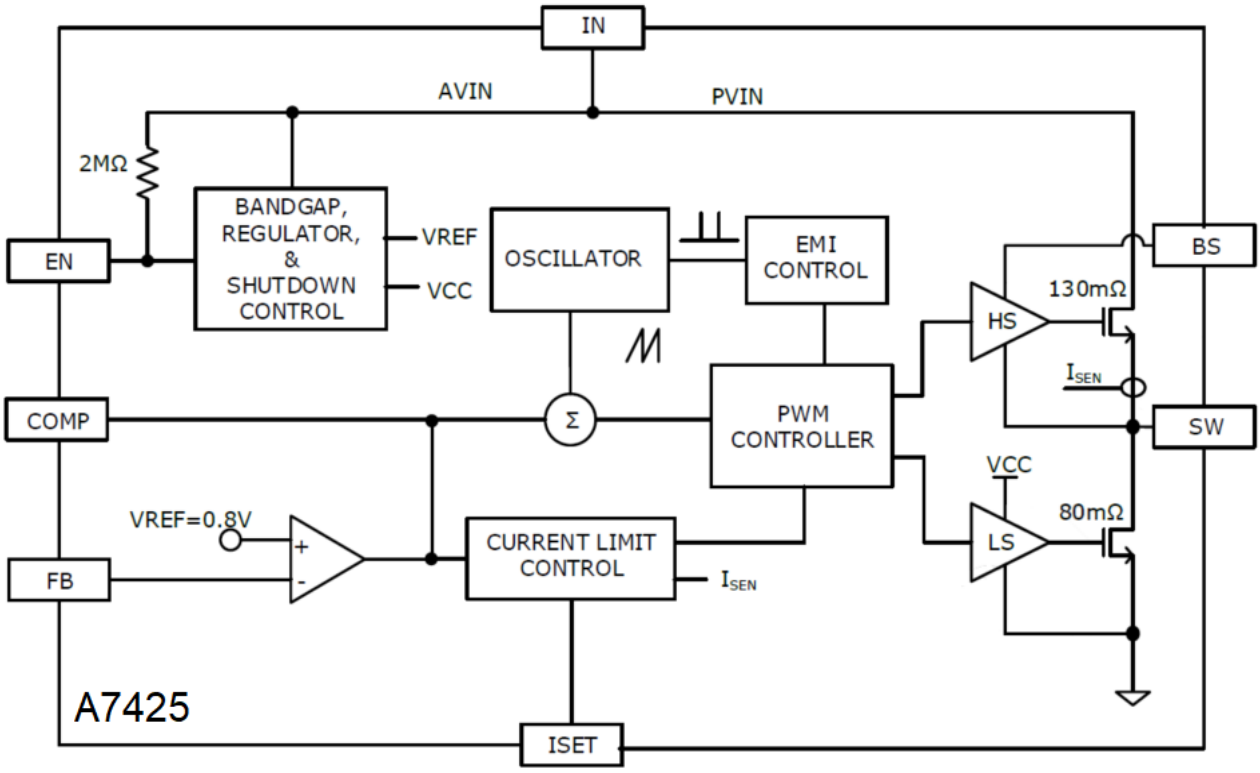


Fig.15 Efficiency vs. I_{OUT} @ V_{OUT}=5V



BLOCK DIAGRAM



DETAILED INFORMATION

Operation

As seen in Functional Block Diagram, the A7425 is a peak current mode pulse width modulation (PWM) converter. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off. At this point, the SW side of the inductor swings to ground through the internal Low Side Power Switch, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using BS as the positive rail. This pin is charged to V_{SW} + 5V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.8 V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the current limit set by the ISET resistor. At this point, the output voltage will drop with increasing load.

The Oscillator normally switches at 500kHz. However, if FB voltage is lower than 0.4V, A7425 will go into short circuit of auto-restart mode with very low power.

Power Saving Mode Operation

At very light loads, the A7425 will enter Power Saving Mode. In this mode, the regulator automatically skips switching cycles with internal control loop, and its quiescent current is reduced to 0.9mA.

Enable Pin

The A7425 has an enable input EN for turning the IC on or off. The EN pin contains a precision 2V comparator with 200mV hysteresis and a 2MΩ pull-up resistance. The comparator can be used with a resistor divider from V_{IN} to program a startup voltage higher than the normal UVLO value. It can be used with a resistor divider from V_{OUT} to disable charging of a deeply discharged battery, or it can be used with a resistor divider containing a thermistor to provide a temperature-dependent shutoff protection for over temperature battery. The thermistor should be thermally coupled to the battery pack for this usage.

If left floating, the EN pin will be pulled up to roughly 5V by the internal 2MΩ pull-up resistance. It can be driven from standard logic signals greater than 2V, or driven with open-drain logic to provide digital on/off control.

Thermal Shutdown

The A7425 disables switching when its junction temperature exceeds 160℃ and resumes when the temperature has dropped by 25℃.

DETAILED INFORMATION

Output Voltage Setting

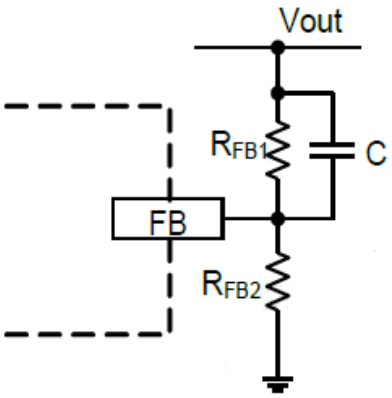


Figure 16. Output Voltage Setting

Figure 16 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Adding a capacitor in parallel with R_{FB1} helps the system stability. Typically, use $R_{FB2} \approx 10k\Omega$ and determine R_{FB1} from the following equation:

$$R_{FB1} = R_{FB2} \left(\frac{V_{OUT}}{0.8V} - 1 \right)$$

Current Setting

The current limit of high side MOSFET is adjustable by an external resistor connected to the ISET pin. The current limit range is from 1.0A to 3.5A. When the inductor current reaches the current limit threshold, the COMP voltage will be clamped to limit the inductor current.

Notice that the value of R_{ISET} is inversely proportional to High-Side MOSFET Peak Current Limit. To determine the proper resistor for a desired current, please refer to Figure 17 below.

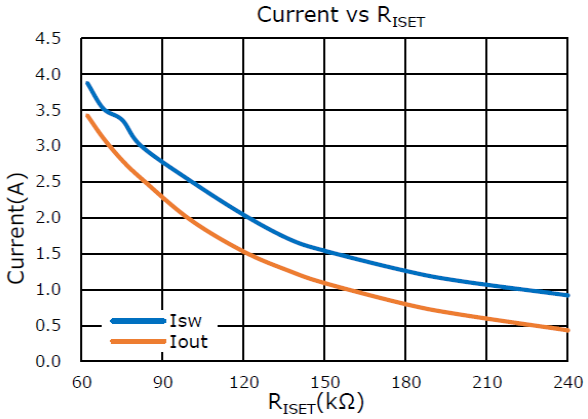


Figure 17. Curve for Programming Output CC Current with Typical Application Circuit

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value:

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L=\frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\,F_{SW}I_{LOADMAX}\,K_{RIPPLE}}$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK\text{-}PK} = \frac{V_{OUT}\,x\,(V_{IN} - V_{OUT})}{L\,x\,V_{IN}\,x\,f_{SW}}$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK\text{-}PK}$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK\text{-}PK}$$

I_{LIM} is the internal current limit, which is typically 4A, as shown in Electrical Characteristics Table.

External High Voltage Bias Diode

It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The high voltage bias Diode can be a low cost one such as 1N4148 or BAT54.

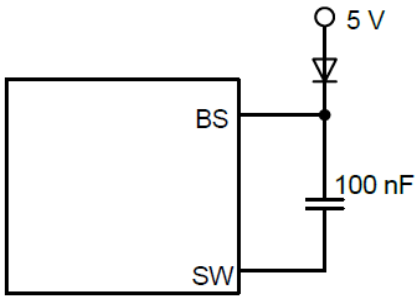


Figure 18. External High Voltage Bias Diode

This diode is also recommended for high duty cycle operation and high output voltage applications.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than two pieces of 10μF capacitors in parallel. Low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and GND pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if another parallel ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{V_{IN}}{8 \times f_{SW}^2 \, L C_{OUT}}$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output capacitor, typically choose a capacitance of about two pieces of 22μF capacitors in parallel. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

Stability Compensation

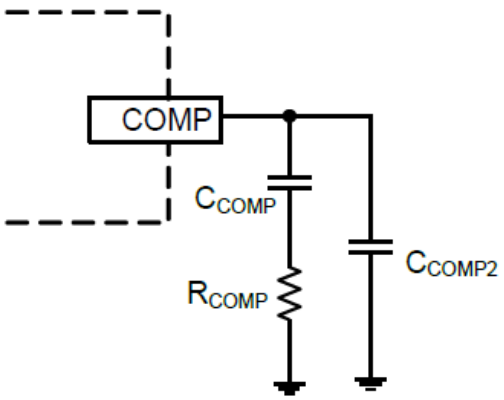


Figure 19. Stability Compensation

C_{COMP2} is needed only for high ESR output capacitor. The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 19. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.8V}{I_{OUT}} A_{VEA} G_{COMP}$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}}$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}}$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}}$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}}$$

The following steps should be used to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R_{COMP}:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \times 0.8V} (\Omega)$$

STEP 2. Set the zero f_{Z1} at 1/4 of the cross over frequency. The equation for C_{COMP} is:

$$C_{COMP} = \frac{4}{2\pi f_{SW} R_{COMP}} (F)$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESRCOUT} \geq \frac{2}{2\pi f_{SW} C_{OUT}} (\Omega)$$

And the proper value for C_{COMP2} is:

$$C_{OMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}}$$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.

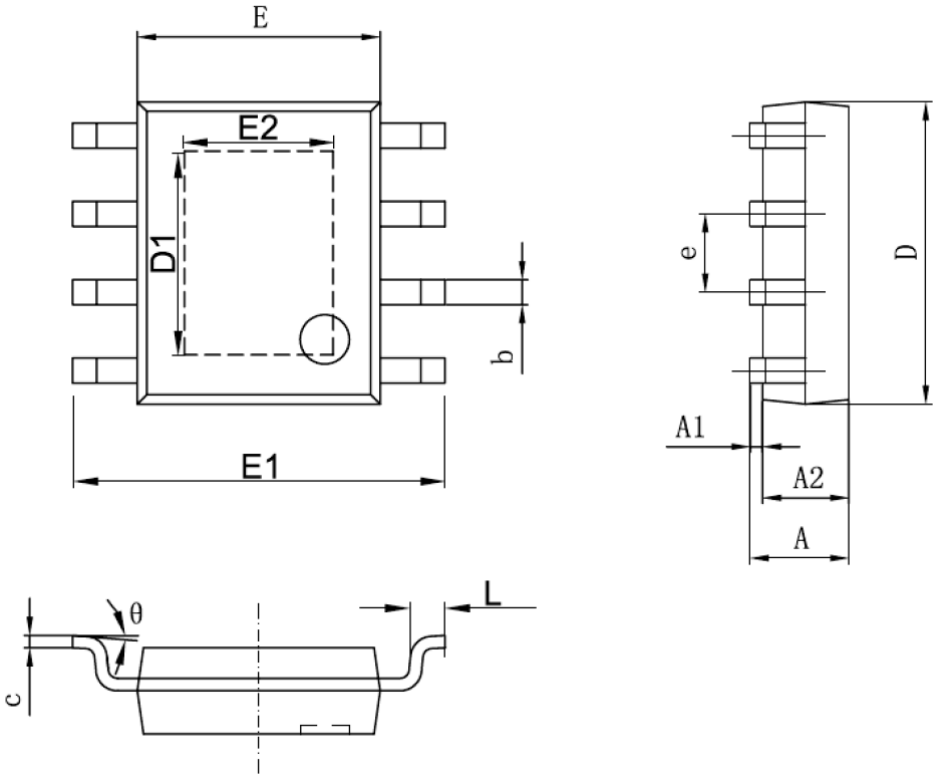
PC Board Layout Guidance

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1) Arrange the power components to reduce the AC loop size, consisting of input ceramic capacitor C1、C2, IN pin, SW pin .
2) Place input decoupling ceramic capacitor C1、C2 as close to IN pin as possible. C1、C2 is connected power GND with vias or short and wide path.
3) Return FB, COMP and ISET to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.
4) Use copper plane for power GND for best heat dissipation and noise immunity.
5) Place feedback resistor close to FB pin.
6) Use short trace connecting BS-C4-SW loop.

PACKAGE INFORMATION

Dimension in PSOP8 (Unit: mm)



Symbol	Millimeters	
	Min	Max
A	1.300	1.700
A1	0.000	0.100
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
D1	3.050	3.250
E	3.800	4.000
E1	5.800	6.200
E2	2.160	2.360
e	1.270 BSC	
L	0.400	1.270
θ	0°	8°

IMPORTANT NOTICE

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