## Document Title

A8108 Data Sheet, 2.4GHz Wireless Transceiver USB SoC

## Revision History

| Rev. No. | History | Issue Date | Remark |
|---|---|---|---|
| 0.1 | Initial issue. | Aug., 2014 | Objective |

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## 1. General Description

A8108 is a low cost 2.4GHz ISM SoC. In the RF part, this device integrates both high sensitivity receiver ( - 96dBm @500kbps) and a programmable high efficiency power amplifier (0 ~ 6dBm). It also integrates high speed pipeline 8051 MCU, 32KBytes In-system programmable flash memory, 256B internal SRAM, 512B external SRAM, USB 2.0 compatible controller and various powerful functions.

A8108 supports fast PLL settling time (75 us) for frequency hopping system. For packet handling, A8108 has built-in auto-ack and auto-resend, CRC for error packet filtering, RSSI for clear channel assessment, thermal sensor to monitor relative temperature, WOR (Wake on RX) function to support periodically wake up from sleep mode to RX mode and listen for incoming packets without MCU interaction. Those functions are very easy to use while developing a wireless system. All features are integrated in a small QFN 5x5 32 pins package.

## 2. Typical Applications

- 2400 ~ 2483.5 MHz ISM frequency hopping system
- Smart remote controller dongle
- Wireless USB dongle
- Wireless keyboard and mouse
- Wireless toy and gaming

## 3. Feature

- Package size (QFN5 X5, 32 pins).
- 32KByte flash, 256Bytes internal data RAM, 512Bytes external data RAM..
- High performance pipeline complicated 8051
- Operation clock: 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of crystal oscillator.
- USB 2.0 compatible controller for Interrupt input/output.
- UART, $I^2C$, SPI serial communication
- Three 16/8-bit counter/timers
- ~~Two Channel PWM~~
- Watchdog timer
- Sleep timer
- In-Circuit Debugger
- In-System programming/ In-Application programming
- 14 GPIO
- RX current consumption with MCU in operation mode :18mA
- TX current consumption with MCU in operation mode (22mA @ 0dBm).
- Deep sleep current (T.B.D/ PM3 without Sleep timer)
- Low sleep current (4 uA)
- Frequency band: 2400 – 2483MHz.
- FSK and GFSK modulation
- High sensitivity:
  - -95dBm at 500Kbps data rate
  - -104dBm at 25Kbps data rate
  - -107dBm at 2Kbps data rate
- Programmable data rate 2K ~ 500Kbps.
- Fast settling time synthesizer for frequency hopping system.
- Built-in thermal sensor for monitoring relative temperature.
- Built-in one channel 8-bits ADC for external analog voltage (0V ~ 1.2V).
- Built-in eight channels 12-bits ADC for general purpose analog input (0V ~ 1.8 V).
- Built-in Low Battery Detector.
- Support low cost crystal (8 /12 / 16 / 24MHz).
- Easy to use.
  - Change frequency channel by ONE register setting.
  - 8-bits Digital RSSI for clear channel indication.
  - Auto RSSI measurement.
  - Auto WOR (wake up when receive RX packet).
  - Auto WOT (wake up to transmit TX packet).
  - Auto Calibrations.
  - Auto IF function.
  - Auto Frequency Compensation.
  - Auto CRC Check.

- Auto FEC by (7, 4) Hamming code (1 bit error correction / code word).
- Data Whitening for encryption and decryption.
- Separated 64 bytes RX and TX FIFO.

## 4. Pin Configurations

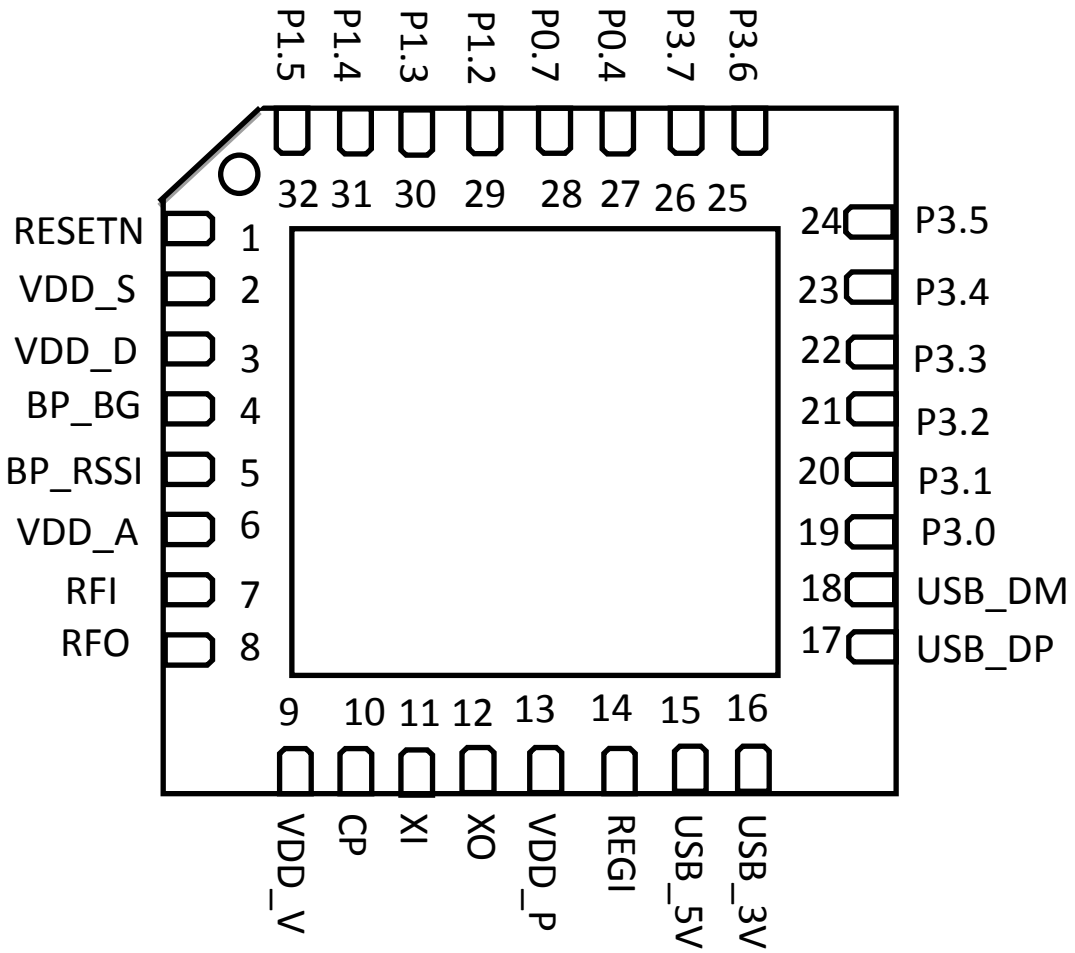



Fig 4-1. A8108 QFN 5x5 32 Package Top View

## 5. Pin Description (I: input; O: output, I/O: input or output)

32PIN

| Pin No. | Symbol | I/O | Function Description |
|---|---|---|---|
| 1 | RESETN | DI | RESETN |
| 2 | VDD_S | AO | VDD_S |
| 3 | VDD_D | AO | VDD_D |
| 4 | BP_BG | AO | BP_BG |
| 5 | BP_RSSI | AO | Connect to bypass capacitor for RSSI reading. |
| 6 | VDD_A | AO | VDD_A |
| 7 | RFI | IO | Low noise amplifier input. |
| 8 | RFO | IO | Power amplifier output. |
| 9 | VDD_V | AI | VCO supply voltage input. |
| 10 | CP | AI | |
| 11 | XI | AI | Crystal oscillator input. |
| 12 | XO | AO | Crystal oscillator output. |
| 13 | VDD_P | AO | PLL supply voltage output. Connect to bypass capacitor. |
| 14 | REGI | AIO | Internal Regulator node |
| 15 | USB_5V | AI | Internal Regulator input (External Power input) |
| 16 | USB_3V | AIO | Internal USB 3.3V node |
| 17 | USB_DP | DIO/AO | USB DP |
| 18 | USB_DM | DIO/AI | USB DM |
| 19 | P3.0 | DIO | P3.0 /UART0_RX |
| 20 | P3.1 | DIO | P3.1/UART0_TX |
| 21 | P3.2 | DIO/AI | P3.2/INT0/ADC0 |
| 22 | P3.3 | DIO/AI | P3.3/INT1/ADC1 |
| 23 | P3.4 | DIO/AI | P3.4/Timer0_TO/ADC2 |
| 24 | P3.5 | DIO/AI | P3.5/Timer1_T1/ADC3 |
| 25 | P3.6 | DIO/AI | P3.6/RTC_I |
| 26 | P3.7 | DIO/AI | P3.7/RTC_O |
| 27 | P0.4 | DIO | P0.4/GPIO/ ICE mode |
| 28 | P0.7 | DIO | P0.7/INT2/GIO1 |
| 29 | P1.2 | DIO | P1.2/INT3/GIO2(output) |
| 30 | P1.3 | DIO | P1.3/INT4/CKO |
| 31 | P1.4 | DIO | P1.4/TTAG_TTDIO |
| 32 | P1.5 | DIO | P1.5/TTAG_TTCK |
| | **Back side plate** | G | Ground.<br>Back side plate shall be well-solder to ground; otherwise, it will impact RF performance. |

## 6. Chip Block Diagram

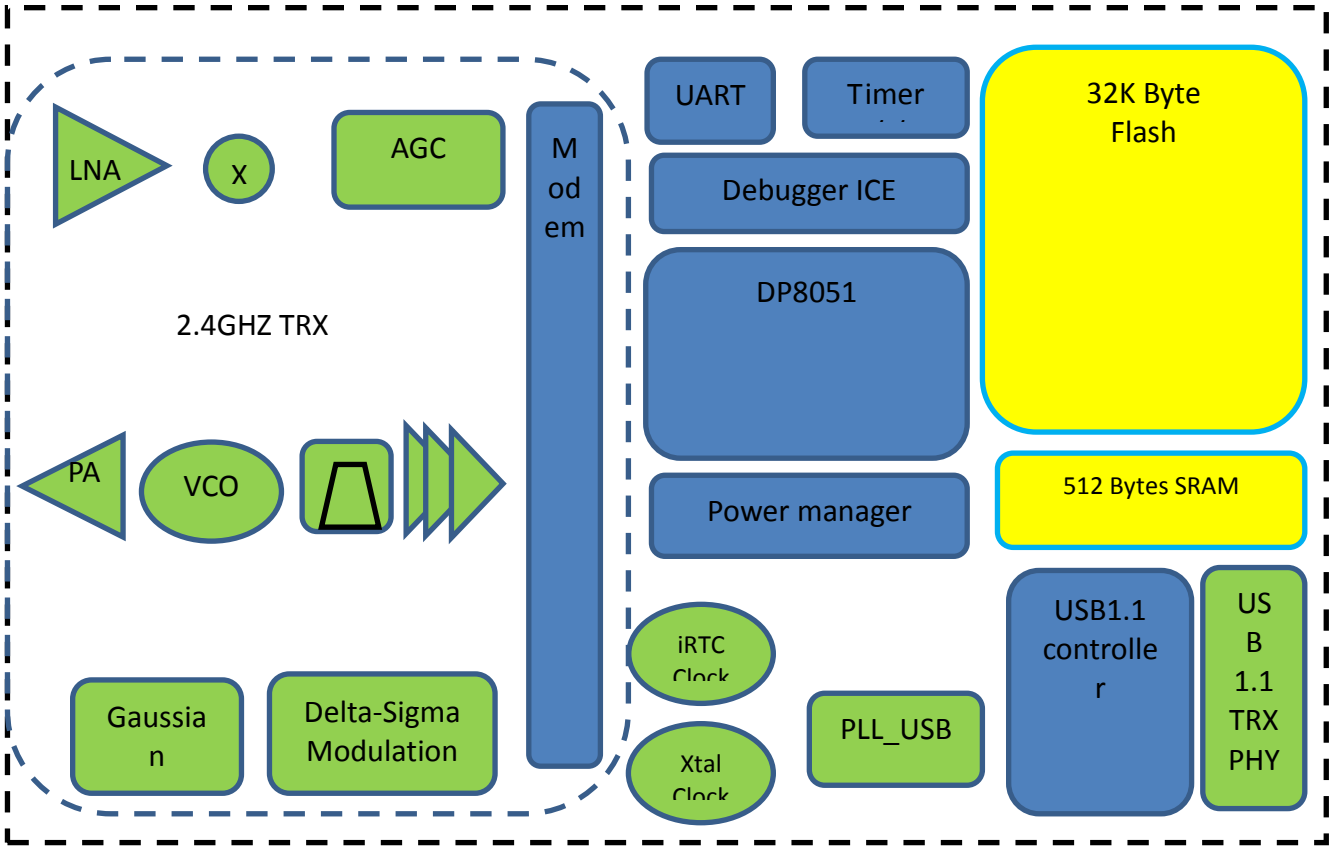



Fig 6-1. A8108 Block Diagram

## 7. Absolute Maximum Ratings

| Parameter | With respect to | Rating | Unit |
|---|---|---|---|
| Supply voltage range (VDD) | GND | -0.3 ~ 3.6 | V |
| Digital IO pins range | GND | -0.3 ~ VDD+0.3 | V |
| Voltage on the analog pins range | GND | -0.3 ~ 2.1 | V |
| Input RF level | | 18 | dBm |
| Storage Temperature range | | -55 ~ 125 | °C |
| ESD Rating | HBM | ± 2K | V |
| | MM | ± 100 | V |

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).

## 8. Electrical Specification

(Ta=25℃, **VDD=3.3V**, $F_{XTAL}$ =24.576MHz, with Matching, Balun and low pass filter, On Chip Regulator = **1.8V**, CODEC sampling rate= 8KSPS, unless otherwise noted.)

| Parameter | Description | Min. | Type | Max. | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| Operating Temperature | | -40 | | 85 | °C |
| Supply Voltage (VDD) | with internal regulator | 2.7 | 3.3 | 3.6 | V |
| Current Consumption (MCU) | Sleep mode (TWOR off) *1 | | 3 | | μA |
| | Sleep mode (TWOR on) *1 | | 5.5 | | μA |
| | Normal Mode (Regulator on, XOSC on) | | 3 | | mA |
| Current Consumption (TRX) | PLL mode | | 10 | | mA |
| | RX Mode (4Mbps / AGC on) | | 18 | | mA |
| | TX Mode / 21dBm (TBC = 3, TDC = 3, TXC = 3) | | 18.5 | | mA |
| **PLL block** | | | | | |
| Crystal start up time*2 | Idle to standby (Xtal, 49US type, is stable at 40ppm) | | 0.6 | | ms |
| Crystal frequency | | | **16** | | MHz |
| Crystal tolerance | | | ±50 | | ppm |
| Crystal ESR | | | | 80 | ohm |
| VCO Operation Frequency | | 2400 | | 2483.5 | MHz |
| PLL settling time*3 | Loop filter based on app. circuit. (Standby to PLL) | | 75 | | μS |
| **Transmitter** | | | | | |
| Output power range | | -10 | 0 | 6 | dBm |
| Out Band Spurious Emission *4 (PA = 0 dBm) | 30MHz~1GHz | | | -36 | dBm |
| | 1GHz~12.75GHz | | | -30 | dBm |
| | 1.8GHz~ 1.9GHz | | | -47 | dBm |
| | 5.15GHz~ 5.3GHz | | | -47 | dBm |
| Frequency deviation*5 | Data rate 500K | | 186k | | Hz |
| Data rate | | | 500k | | bps |
| TX ready time*6 | Standby to TX | | 70 | | μS |
| **Receiver** | | | | | |
| Receiver sensitivity @ BER = 0.1% | 500k mode | | -96 | | dBm |
| Interference *7 | IF center frequency | | 1000/2000 | | dB |
| | Co-Channel ($C/I_0$) | | 11 | | dB |
| | 1st Adjacent Channel ($C/I_1$) | | 2 | | dB |
| | 2nd Adjacent Channel ($C/I_2$) | | -18 | | dB |
| | 3rd Adjacent Channel ($C/I_3$) | | -28 | | dB |
| | Image ($C/I_{IM}$) | | - 12 | | dB |
| Maximum Operating Input Power | @RF input (BER=0.1%) | | | 0 | dBm |
| RX Spurious Emission *4 | 30MHz~1GHz | | | -52 | dBm |
| | 1GHz~12.75GHz | | | -47 | |
| RSSI Range | AGC = on | -100 | | -10 | dBm |

| | | | | | |
|---|---|---|---|---|---|
| **12Bit SAR ADC** | | | | | |
| Input voltage range | | 0 | | 1.8 | V |
| External reference voltage | | | 1.8 | | V |
| Input capacitor | | | 25 | | pF |
| Bandwidth | | | 200 | | KHz |
| EOB, effective number of bits | | | 10 | | bit |
| INL | | | +/- 2 | | LSB |
| DNL | | | +/-1 | | LSB |
| Conversion time | | 128 | | 8 | uS |
| Current consumption | | | 0.4 | | mA |
| **24Bit ADC** | | | | | |
| Resistor for oscillation | CS0, CT0 > 740pF | 1 | 10 | 100 | Kohm |
| Oscillation frequency | Resistor for oscillation=1Kohm | | 404.2 | | KHz |
| | Resistor for oscillation=10Kohm | | 62.8 | | KHz |
| | Resistor for oscillation=100Kohm | | 6.63 | | KHz |
| Current consumption | | | 0.42 | | mA |

| | | | | | |
|---|---|---|---|---|---|
| **Regulator** | | | | | |
| Regulator settling time | | | 200 | | μs |
| Band-gap reference voltage | | | 1.21 | | V |
| Regulator output voltage | | | 1.8 | | V |
| **Digital IO DC characteristics** | | | | | |
| High Level Input Voltage ($V_{IH}$) | | 0.8*VDD | | VDD | V |
| Low Level Input Voltage ($V_{IL}$) | | 0 | | 0.2*VDD | V |
| High Level Output Voltage ($V_{OH}$) | @$I_{OH}$= -0.5mA | VDD-0.4 | | VDD | V |
| Low Level Output Voltage ($V_{OL}$) | @$I_{OL}$= 0.5mA | 0 | | 0.4 | V |

Note 1: When digital I/O pins are configured as input, those pins shall NOT be floating but pull either high or low ; otherwise, leakage current will be induced.
Note 2: Xtal settling time is depend on Xtal package type, Xtal ESR and Xtal Cm.
Note 3: Refer to Delay Register I (15h) to set PDL (PLL settling delay).
Note 4: With external RF filter that provides minimum 17dB of attenuation in the band: 30MHz ~ 2GHz and 3GHz ~12.75GHz.
Note 5: Refer to TX Register II (14h) to set FD [7:0].
Note 6: Refer to Delay Register I (15h) to set PDL and TDL.
Note 7: The wanted signal is set above sensitivity level +3dB. The modulation data of wanted signal and interferer are PN9 and PN15, respectively.

## 9. SOC Architectural Overview

A8108 microcontroller is instruction set compatible with the industry standard 8051. Besides FSK/GFSK modulation RF transceiver, A8108 integrates many features, three 8/16bit counters/timers, watchdog timer, RTC, USB, UART, 4 channels ADC, battery detector. The in-system memory includes 32K bytes CPU program flash, 256 bytes CPU internal data SRAM, 512 byte CPU external data SRAM. The A8108 supports TTAG (2-wire) debug circuitry that provides full time, real-time, in-circuit debugging.

For USB controller, A8108 has basic control and 3 interrupt in/out end-points. It supports HID control for mouse application. The chip automatically handles packet handling and WOR to achieve power saving. The A8108 pass USB I/F test and could provide reliable USB communication.

# 10.SOC Architectural Overview

## 10.1 Pipeline 8051 CPU

A8108 microcontroller has pipelined RSIC architecture 10 times faster compared to standard 8051 architecture. The pipeline 8051 is fully compatible with the MCS-51™ instruction set. User can use standard 8051 assemblers and compilers to develop software. The pipelined architecture 8051 has greatly increases its instruction throughput over the standard 8051 architecture. A8108 has a total of 110 instructions. The table below shows the total number of instructions that require each execution time. For more detail information of instruction, please refer Table 10.1.

| Clock to Execute | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| Number of instructions | 24 | 38 | 29 | 11 | 8 | 1 |

## 10.2 Memory Organization

The memory organization of A8108 is similar to the standard 8051. The memory organization is shown as figure 10.1

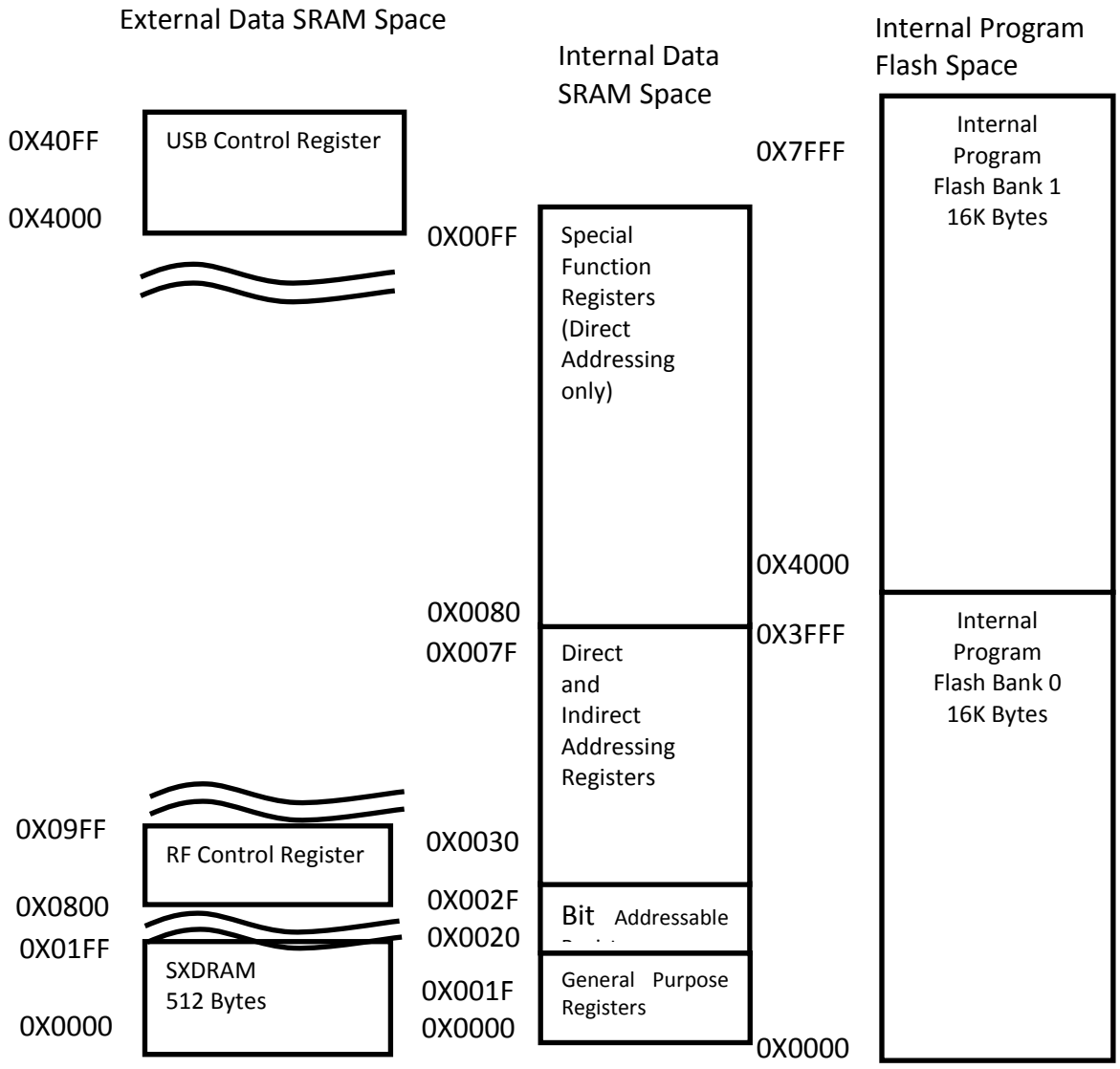



Figure 10.1 Memory Organization

### 10.2.1 Program memory

The standard 8051 core has 64KB program memory space. A8108 implement 32KB flash in two 16x 8Kb flash macro. ~~The last 2KB program memory space (0x 7800 ~ 0x7FFF) supports IAP (In-Application Programming) function. The each block size in this area is 128Bytes. User has 16 blocks in 2KB program memory space to storage data. Program memory is normally assumed to be read only. However, A8108 can write to program memory by IAP function call.~~

### 10.2.2 Data memory

The A8108 includes 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode. The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 10.1 illustrates the data memory organization of the A8108.

### 10.2.3 General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 10.2.5). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

### 10.2.4 Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination). The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction: MOV C, 22.3h moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

### 10.2.5 Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the CIP-51's resources and peripherals. The CIP-51 duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the MCU. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 10.1 lists the SFRs implemented in the CIP-51 System Controller.
The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, SCON0, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 10.1, for a detailed description of each register.

| | 0/8 | 1/9 | 2/A | 3/B | 4/C | 5/D | 6/E | 7/F |
|---|---|---|---|---|---|---|---|---|
| 0xF8 | EIP | OSCCON | | | | | | |
| 0xF0 | B | I2CSADR | I2CSCR | I2CSBUF | I2CMSA | I2CMCR | I2CMBUF | I2CMTP |
| 0xE8 | EIE | | | | SPCR | SPSR | SPDR | SSCR |
| 0xE0 | ACC | P3OE | P3PUN | P3WUN | SPCR1 | SPSR1 | SPDR1 | SSCR1 |
| 0xD8 | WDCON | P1OE | P1PUN | P1WUN | | | | |
| 0xD0 | PSW | P0OE | P0PUN | P0WUN | | | | |
| 0xC8 | T2CON | T2IF | RLDL | RLDH | TL2 | TH2 | | DEVICR |
| 0xC0 | | | | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0xB8 | IP | PCONE | RSFLAG | IOSEL | | | | |
| 0xB0 | P3 | PWM1CON | PWM1H | PWM1L | | | | |
| 0xA8 | IE | PWM0CON | PWM0H | PWM0L | | | | |
| 0xA0 | P2 | | | | | | | |
| 0x98 | SOCN0 | SBUF0 | FLASHCTRL | FLASHMR | | | | |
| 0x90 | P1 | EIF | | | | | USBADDR | USBDATA |
| 0x88 | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | CKCON | DMAIR |
| 0x80 | P0 | SP | DPL0 | DPH0 | DPL1 | DPH1 | DPS | PCON |

Table 10.1 A8108 Special Function Registers (SFRs) table

: It means bit-addressable

: It means reserved.

Following are description of SFRs related to the operation of A8108 System Controller. Detailed descriptions of the remaining SFRs are including the sections of the datasheet associated with their corresponding system function. The arithmetic section of the processor performs extensive data manipulation and is comprised of the 8-bit arithmetic logic unit (ALU), an ACC(0xE0) register, B(0xF0) register and PSW(0xD0) register.

**PSW (Address: D0h)**

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| D0h PSW | R/W | CY | AC | F0 | RS1 | RS2 | OV | F1 | P |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Program Status Word register

The ALU performs typical arithmetic operations as: addition, subtraction, multiplication, division and additional operations such as: increment, decrement, BCD-decimal-add-adjust and compare. Within logic unit are performance: AND, OR, Exclusive OR, complement and rotation. The Boolean processor performance the bit operations as: set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry.

CY - Carry flag
**AC** - Auxiliary carry
**F0** - General purpose flag 0
**RS[1:0]** - Register bank select bits

| RS[1:0] | Function description |
|---|---|
| 00 | - Bank 0, data address 0x00-0x07 |
| 01 | - Bank 1, data address 0x08-0x0F |
| 10 | - Bank 2, data address 0x10-0x17 |
| 11 | - Bank 3, data address 0x18-0x1F |

**OV** - Overflow flag
**F1** - General purpose flag 1
**P** - Parity flag
The PSW contains several bits that reflect the current state of the CPU.

**ACC (Address: E0h)**

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| E0h ACC | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Accumulator ACC Register

**B (Address: F0h)**

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| F0h<br>B | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

B Register

The B register is used during multiply and divide operations. In other cases may be used as normal SFR.

### 10.2.6 Stack

A8108 has 8-bit stack point called SP (0x81) located in the internal RAM space. It is incremented before data is stored during PUSH and CALL execution and decremented after data is popped during POP, RET and RETI execution. In the other words it always points to the last valid stack byte. The SP is accessed as any other SFRS.

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 81h<br>SP | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

Stack pointer register

### 10.2.7 Data Pointer Register

A8108 are implemented dual data pointer registers, auto increment and auto decrement to speed up data block copying. DPTR0 and DPTR1 are located at four SFR addresses. Active DPTR register is selected by SEL bit (0x86.0). If SEL = 0 the DPTR0 is selected otherwise DPTR1.

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 82h<br>DPL0 | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 83h<br>DPH0 | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Data Pointer Register DPTR0

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 84h<br>DPL1 | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 85h<br>DPH1 | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Data Pointer 1 Register DPTR1

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 86h<br>DPS | R/W | ID1 | ID0 | TSL | AU1 | AU0 | - | - | SEL |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Data Pointers Select Register

ID[1:0] - Increment/decrement function select. See table below.
TSL - Toggle select enable. When set, this bit allows the following DPTR related instruction to toggle the SEL bit following execution of the instruction:

```
MOVC A, @A+DPTR
INC DPTR
MOVX @DPTR, A
MOVX A, @DPTR
MOV DPTR, #data16
```

When TSL=0, DPTR related instructions do not affect state of SEL bit.

AU -When set to '1' performs automatic increment(0)/ decrement(1) of selected DPTR according to IDx bits, after each MOVX @DPTR, MOVC @DPTR instructions
SEL - Select active data pointer – see table below
- - Unimplemented bit. Read as 0 or 1.

| ID1 | ID0 | SEL=1 | SEL=0 |
|---|---|---|---|
| 0 | 0 | INC DPTR1 | INC DPTR |
| 0 | 1 | INC DPTR1 | DEC DPTR |
| 1 | 0 | DEC DPTR1 | INC DPTR |
| 1 | 1 | DEC DPTR1 | DEC DPTR |

Table DPTR0, DPTR1 operations

Selected data pointer register in used in the following instructions:

```
MOVX @DPTR,A
MOVX A,@DPTR
MOVC A,A+DPTR
JMP @A+DPTR
INC DPTR
MOV DPTR,#data16
```

### 10.2.8 RF Registers and RF FIFO

RF registers are RF radio control registers and located in 0x0800 ~ 0x08ff. Please refer the section 12 and the related function setting in the datasheet. A8108 has 128 Bytes FIFO located from 0x0900 to 0x09FF. A8108 has built-in separated 64-bytes TX/RX FIFO (could be extended to 256 bytes) for fata buffering and burst transmission.

## 10.3 Instruction set

A8108 use a high performance, pipeline 8051 core and it is fully compatible with the standard MCS-51™ instruction set. Standard 8051 development tools can used to develop software for A8108. All A8108 instruction sets are the binary and functional equivalent of the MCS-51™. However, instruct timing is different with the standard 8051. All instruction timings are specified in the terms of clock cycles as shown in the Table 10.2

| Mnemonic | Description | Code | Bytes | Cycles |
|---|---|---|---|---|
| ACALL addr11 | Absolute subroutine call | 0x11-0xF1 | 2 | 4 |
| ADD A,#data | Add immediate data to accumulator | 0x24 | 2 | 2 |
| ADD A,@Ri | Add indirect RAM to accumulator | 0x26-0x27 | 1 | 2 |
| ADD A,direct | Add direct byte to accumulator | 0x25 | 2 | 2 |
| ADD A,Rn | Add register to accumulator | 0x28-0x2F | 1 | 1 |
| ADDC A,#data | Add immediate data to A with carry flag | 0x34 | 2 | 2 |
| ADDC A,@Ri | Add indirect RAM to A with carry flag | 0x36-0x37 | 1 | 2 |
| ADDC A,direct | Add direct byte to A with carry flag | 0x35 | 2 | 2 |

| | | | | |
|---|---|---|---|---|
| ADDC A,Rn | Add register to accumulator with carry flag | 0x38-0x3F | 1 | 1 |
| AJMP addr11 | Absolute jump | 0x01-0xE1 | 2 | 3 |
| ANL C,/bit | AND complement of direct bit to carry | 0xB0 | 2 | 2 |
| ANL A,#data | AND immediate data to accumulator | 0x54 | 2 | 2 |
| ANL A,@Ri | AND indirect RAM to accumulator | 0x56-0x57 | 1 | 2 |
| ANL A,direct | AND direct byte to accumulator | 0x55 | 2 | 2 |
| ANL A,Rn | AND register to accumulator | 0x58-0x5F | 1 | 1 |
| ANL C,bit | AND direct bit to carry flag | 0x82 | 2 | 2 |
| ANL direct,#data | AND immediate data to direct byte | 0x53 | 3 | 3 |
| ANL direct,A | AND accumulator to direct byte | 0x52 | 2 | 3 |
| CJNE @Ri,#data | Compare immediate to ind. and jump if not equal | 0xB6-0xB7 | 3 | 5 |
| CJNE A,#data re | Compare immediate to A and jump if not equal | 0xB4 | 3 | 4 |
| CJNE A,direct re | Compare direct byte to A and jump if not equal | 0xB5 | 3 | 5 |
| CJNE Rn,#data r | Compare immediate to reg. and jump if not equal | 0xB8-0xBF | 3 | 4 |
| CLR A | Clear accumulator | 0xE4 | 1 | 1 |
| CLR bit | Clear direct bit | 0xC2 | 2 | 3 |
| CLR C | Clear carry flag | 0xC3 | 1 | 1 |
| CPL A | Complement accumulator | 0xF4 | 1 | 1 |
| CPL bit | Complement direct bit | 0xB2 | 2 | 3 |
| CPL C | Complement carry flag | 0xB3 | 1 | 1 |
| DA A | Decimal adjust accumulator | 0xD4 | 1 | 3 |
| DEC @Ri | Decrement indirect RAM | 0x16-0x17 | 2 | 3 |
| DEC A | Decrement accumulator | 0x14 | 1 | 1 |
| DEC direct | Decrement direct byte | 0x15 | 1 | 3 |
| DEC Rn | Decrement register | 0x18-0x1F | 1 | 2 |
| DIV A,B | Divide A by B | 0x84 | 1 | 6 |
| DJNZ direct,rel | Decrement direct byte and jump if not zero | 0xD5 | 3 | 5 |
| DJNZ Rn,rel | Decrement register and jump if not zero | 0xD8-0xDF | 2 | 4 |
| INC @Ri | Increment indirect RAM | 0x06-0x07 | 1 | 3 |
| INC A | Increment accumulator | 0x04 | 1 | 1 |
| INC direct | Increment direct byte | 0x05 | 2 | 3 |
| INC Rn | Increment register | 0x08-0x0F | 1 | 2 |
| INC DPTR | Increment data pointer | 0xA3 | 1 | 1 |
| JB bit,rel | Jump if direct bit is set | 0x20 | 3 | 5 |
| JBC bit,direct re | Jump if direct bit is set and clear bit | 0x10 | 3 | 5 |
| JC rel | Jump if carry flag is set | 0x40 | 2 | 3 |
| JMP @A+DPTR | Jump indirect relative to the DPTR | 0x73 | 1 | 5 |

| | | | | |
|---|---|---|---|---|
| JNB bit,rel | Jump if direct bit is not set | 0x30 | 3 | 5 |
| JNC | Jump if carry flag is not set | 0x50 | 2 | 3 |
| JNZ rel | Jump if accumulator is not zero | 0x70 | 2 | 4 |
| JZ rel | Jump if accumulator is zero | 0x60 | 2 | 4 |
| LCALL addr16 | Long subroutine call | 0x12 | 3 | 4 |
| LJMP addr16 | Long jump | 0x02 | 3 | 4 |
| MOV A,@Ri | Move indirect RAM to accumulator | 0xE6-0xE7 | 1 | 2 |
| MOV bit,C | Move carry flag to direct bit | 0x92 | 2 | 3 |
| MOV @Ri,#data | Move immediate data to indirect RAM | 0x76-0x77 | 2 | 2 |
| MOV @Ri,A | Move accumulator to indirect RAM | 0xF6-0xF7 | 1 | 2 |
| MOV @Ri,direct | Move direct byte to indirect RAM | 0xA6-0xA7 | 2 | 3 |
| MOV A,#data | Move immediate data to accumulator | 0x74 | 2 | 2 |
| MOV A,direct | Move direct byte to accumulator | 0xE5 | 2 | 2 |
| MOV A,Rn | Move register to accumulator | 0xE8-0xEF | 1 | 1 |
| MOV C,bit | Move direct bit to carry flag | 0xA2 | 2 | 2 |
| MOV direct,#data | Move immediate data to direct byte | 0x75 | 3 | 3 |
| MOV direct,@Ri | Move indirect RAM to direct byte | 0x86-0x87 | 2 | 3 |
| MOV direct,A | Move accumulator to direct byte | 0xF5 | 2 | 2 |
| MOV direct,Rn | Move register to direct byte | 0x88-0x8F | 2 | 2 |
| MOV direct1,direct2 | Move direct byte to direct byte | 0x85 | 3 | 3 |
| MOV DPTR,#data16 | Load 16-bit constant in to active DPTR | 0x90 | 3 | 3 |
| MOV Rn,#data | Move immediate data to register | 0x78-0x7F | 2 | 2 |
| MOV Rn,A | Move accumulator to register | 0xF8-0xFF | 1 | 1 |
| MOV Rn,direct | Move direct byte to register | 0xA8-0xAF | 2 | 3 |
| MOVC A,@A+DPTR | Move code byte relative to DPTR to accumulator | 0x93 | 1 | 5 |
| MOVC A,@A+PC | Move code byte relative to PC to accumulator | 0x83 | 1 | 4 |
| MOVX @DPTR,A | Move A to external SRAM (16-bit address) | 0xF0 | 1 | 1 |
| MOVX @Ri,A | Move A to external RAM (8-bit address) | 0xF2-0xF3 | 1 | 2 |
| MOVX A,@DPTR | Move external RAM (16-bit address) to A | 0xE0 | 1 | 1 |
| MOVX A,@Ri | Move external RAM (8-bit address) to A | 0xE2-0xE3 | 1 | 2 |
| MUL A,B | Multiply A and B | 0xA4 | 1 | 2 |
| NOP | No operation | 0x00 | 1 | 1 |
| ORL direct,A | OR accumulator to direct byte | 0x42 | 2 | 3 |
| ORL A,#data | OR immediate data to accumulator | 0x44 | 2 | 2 |
| ORL A,@Ri | OR indirect RAM to accumulator | 0x46-0x47 | 1 | 2 |
| ORL A,direct | OR direct byte to accumulator | 0x45 | 2 | 2 |
| ORL A,Rn | OR register to accumulator | 0x48-0x4F | 1 | 1 |

| | | | | |
|---|---|---|---|---|
| ORL C,/bit | OR complement of direct bit to carry | 0xA0 | 2 | 2 |
| ORL C,bit | OR direct bit to carry flag | 0x72 | 2 | 2 |
| ORL direct,#data | OR immediate data to direct byte | 0x43 | 3 | 3 |
| POP direct | Pop direct byte from internal ram stack | 0xD0 | 2 | 2 |
| PUSH direct | Push direct byte on to internal ram stack | 0xC0 | 2 | 3 |
| RET | Return from subroutine | 0x22 | 1 | 4 |
| RETI | Return from interrupt | 0x32 | 1 | 4 |
| RL A | Rotate accumulator left | 0x23 | 1 | 1 |
| RLC A | Rotate accumulator left through carry | 0x33 | 1 | 1 |
| RR A | Rotate accumulator right | 0x03 | 1 | 1 |
| RRC A | Rotate accumulator right through carry | 0x13 | 1 | 1 |
| SETB C | Set carry flag | 0xD3 | 1 | 1 |
| SETB bit | Set direct bit | 0xD2 | 2 | 3 |
| SJMP rel | Short jump (relative address) | 0x80 | 2 | 3 |
| SUBB A,@Ri | Subtract indirect RAM from A with borrow | 0x96-0x97 | 1 | 2 |
| SUBB A,direct | Subtract direct byte from A with borrow | 0x95 | 2 | 2 |
| SUBB A,#data | Subtract immediate data from A with borrow | 0x94 | 2 | 2 |
| SUBB A,Rn | Subtract register from A with borrow | 0x98-0x9F | 1 | 1 |
| SWAP A | Swap nibbles within the accumulator | 0xC4 | 1 | 1 |
| XCH A,@Ri | Exchange indirect RAM with accumulator | 0xC6-0xC7 | 1 | 3 |
| XCH A,direct | Exchange direct byte with accumulator | 0xC5 | 2 | 3 |
| XCH A,Rn | Exchange register with accumulator | 0xC8-0xCF | 1 | 2 |
| XCHD A,@Ri | Exchange low-order nibble indirect RAM with A | 0xD6-0xD7 | 1 | 3 |
| XRL direct,#data | Exclusive OR immediate data to direct byte | 0x63 | 3 | 3 |
| XRL A,#data | Exclusive OR immediate data to accumulator | 0x64 | 2 | 2 |
| XRL A,@Ri | Exclusive OR indirect RAM to accumulator | 0x66-0x67 | 1 | 2 |
| XRL A,direct | Exclusive OR direct byte to accumulator | 0x65 | 2 | 2 |
| XRL A,Rn | Exclusive OR register to accumulator | 0x68-0x6F | 1 | 1 |
| XRL direct,A | Exclusive OR accumulator to direct byte | 0x62 | 2 | 3 |

Table 10.2Instruction set sorted by alphabet

## 10.4 External Interrupt handler

This section describes 8051 external interrupts and their functionality. For peripheral related interrupts, please refer to an appropriate peripheral section. The external interrupts symbol is shown in figure above. And the pins functionality is described in the following table. All pins are one directional. There are no three-state output pins and internal signals.

| Name | ACTIVE | TYPE | DESCRIPTION |
|---|---|---|---|
| int0(P3.2) | low/falling | Input | External interrupt 0 line |
| int1(P3.3) | low/falling | Input | External interrupt 1 line |
| int2(P0.7) | low | Input | External interrupt 2 line |
| USB_int | failing | | |
| RF_int | failing | | |

| | | | |
|---|---|---|---|
| Key_int | failing | | |

Table 10.3 External interrupts pins description

### 10.4.1 FUNCTIONALITY

All 8051 IP cores have implemented two levels interrupt priority control. Each external interrupt can be in high or low level priority group by setting or clearing a bit in the IP(0xB8), EIP(0xF8), and DEVICR(0xCF) registers. External interrupt pins are activated at low level or by a falling edge. Interrupt requests are sampled each system clock at the rising edge of CLK

| Interrupt flag | Function | Active level/edge | Flag resets | Vector[1] | Natural priority |
|---|---|---|---|---|---|
| IE0 | Device pin INT0 | Low/falling | Hardware | 0x03 | 1 |
| TF0 | Internal, Timer 0 | - | Hardware | 0x0B | 2 |
| IE1 | Device pin INT1 | Low/falling | Hardware | 0x13 | 3 |
| TF1 | Internal, Timer 1 | - | Hardware | 0x1B | 4 |
| TI0 & RI0 | Interrupt, UART0 | - | Software | 0x23 | 5 |
| TF2 | Interrupt, Timer 2 | - | Software | 0x2B | 6 |
| INT2F | Device pin INT2 | Low | Hardware | 0x3B | 8 |
| USBINT | Interrupt flag for USB interrupt | Low | Hardware | 0x43 | 9 |
| RFINT | Interrupt, MAC/RF | - | Software | 0x53 | 11 |
| KEYINT | Interrupt, Key | - | Software | 0x5B | 12 |
| WDIF | Internal, Watchdog | - | Software | 0x63 | 13 |
| I2CMIF | Internal, I2C MASTER MODULE | - | Software | 0x6B | 14 |
| I2CSIF<br>SPIIF | Internal, DI2CS/<br>Internal, SPI | - | Software | 0x73 | 15 |

Table10.4 8051 interrupts summary

1- This is a default location when IRQ_INTERVAL = 8, in other case is equal to (IRQ_INTERVAL* n ) + 3, when n = (natural Priority - 1)

Each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the IE(0xA8), EIE(0xE8), DEVICR(0xCF). The IE contains global interrupt system disable(0) / enable(1) bit called EA.

IE register (0xA8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| A8h<br>IE | R/W | EA | - | ET2 | ES0 | ET1 | EX1 | ET0 | EX0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**EA**：Enable global interrupts
**EX0**：Enable INT0 interrupts
**ET0**：Enable Timer 0 interrupts
**EX1**：Enable INT1 interrupts
**ET1**：Enable Timer 1 interrupts
**ES**：Enable UART interrupts
**ET2**：Enable Timer 2 interrupts

All of bits that generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software. The exceptions of this rule are the request flags IE0 and IE1. If the external interrupts 0 or 1 are programmed to be level activated, IE0 and IE1 are controlled by the external source via pin INT0 and INT1, respectively. Thus, writing a one to these bits will not set the request flag IE0 and/or IE1. The same exception is related to INT2F, USBINT, RFINTF, and KEYINTF – external interrupts number 2, 3, 5, 6.

IP register (0xB8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B8h<br>IP | R/W | - | - | PT2 | PS | PT1 | PX1 | PT0 | PX0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**PX0**：INT0 priority level control (at 1-high-level)
**PT0**：Timer 0 priority level control (at 1-high-level)
**PX1**：INT1 priority level control (at 1-high-level)
**PT1**：Timer 1 priority level control (at 1-high-level)
**PS**：UART priority level control (at 1-high-level)
**PT2**：Timer 2 priority level control (at 1-high-level)

TCON register (0x88)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 88h TCON | R/W | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**IT0**：INT0 level (at 0) / edge (at 1) sensitivity
**IT1**：INT1 level (at 0) / edge (at 1) sensitivity
**IE0**：INT0 interrupt flag
Cleared by hardware when processor branches to interrupt routine
**IE1**：INT1 interrupt flag
Cleared by hardware when processor branches to interrupt routine
**TF0**：Timer 0 interrupt (overflow) flag
Cleared by hardware when processor branches to interrupt routine
**TF1**：Timer 1 interrupt (overflow) flag
Cleared by hardware when processor branches to interrupt routine

SCON register (0x98)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 98h SCON | R/W | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI0 | RI0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**RI0**：UART receiver interrupt flag
**TI0**：UART transmitter interrupt flag

EIE register (0xE8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| E8h EIE | R/W | EI2CS ESPI | EI2CM | EWDI | EKEYINT | ERFINT | - | EUSBINT | EINT2 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**EINT2**：Enable INT2 interrupts
**EUSBINT**：Enable USBINT
**ERFINT**：Enable RF INT
**EKEYINT**：Enable KEYINT
**EWDI**：Enable Watchdog interrupts
**EI2CM**：Enable I2C MASTER MODULE interrupts
**EI2CS**：Enable DI2CS interrupts
**ESPI**：Enable SPI MODULE interrupts

EIP register (0xF8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| F8h EIP | R/W | PI2CS PSPI | PI2CM | PWDI | PKEYINT | PRFINT | - | PUSBINT | PINT2 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**PINT2**：INT2 priority level control (at 1-high-level)
**PUSBINT**：USBINT priority level control (at 1-high-level)
**PRFINT**：RFINT priority level control (at 1-high-level)
**PKEYINT**：KEYINT priority level control (at 1-high-level)
**PWDI**：Watchdog priority level control (at 1-high-level)
**PI2CM**：I2C MASTER MODULE priority level control (at 1-high-level)
**PI2CS**：I2C MODULE priority level control (at 1-high-level)
**PSPI**：SPI MODULE priority level control (at 1-high-level)

EIF register (0x91)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 91h EIF | R/W | I2CSF SPIF | I2CMF | - | KEYINTF | RFINTF | - | USBINT | INT2F |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**INT2F：INT2 interrupt flag**

Should be cleared by external hardware when processor branches to interrupt routine. This bit is a copy of INT2 pin updated every CLK period. It cannot be set by software.

**USBINT：Interrupt flag for USB interrupt**

The signal for detect USB and it is inverted than connected to INT3. If this bit is '1' it means USB interrupt.

**RFINT：RFINT interrupt flag**

Must be cleared by software writing 0x08 when controlled by INT5 pin, else must be cleared by software writing 0x08 when Compare2 is enabled CCEN[5:4]=10. It cannot be set by software.

KEYINT：KEYINT interrupt flag

Must be cleared by software writing 0x10 when controlled by INT6 pin, else must be cleared by software writing 0x10 when Compare3 is enabled CCEN[7:6]=10. It cannot be set by software.

**I2CMIF**：I2C MASTER MODULE interrupt flag. Must be cleared by software writing 0x40. It cannot be set by software

**I2CSIF**：I2C MODULE interrupt flag

**SPIIF**：SPI MODULE interrupt flag

Software should determine the source of interrupt by checking both modules' interrupt related bits. Must be cleared by software writing 0x80. It cannot be set by software.

Note2: A peripheral related bit is available if this peripheral device is included in the system. Can be modified upon request. Please check your configuration.

SPIIF：SPI MODULE interrupt flag

Software should determine the source of interrupt by checking both modules' interrupt related bits. Must be cleared by software writing 0x80. It cannot be set by software.

## 10.5 Reset Circuit

Reset circuitry allows A8108 to be easily placed in a predefined default confition. LVD, Reset, POR, and Watchdog signal will reset A8108 when they happen.

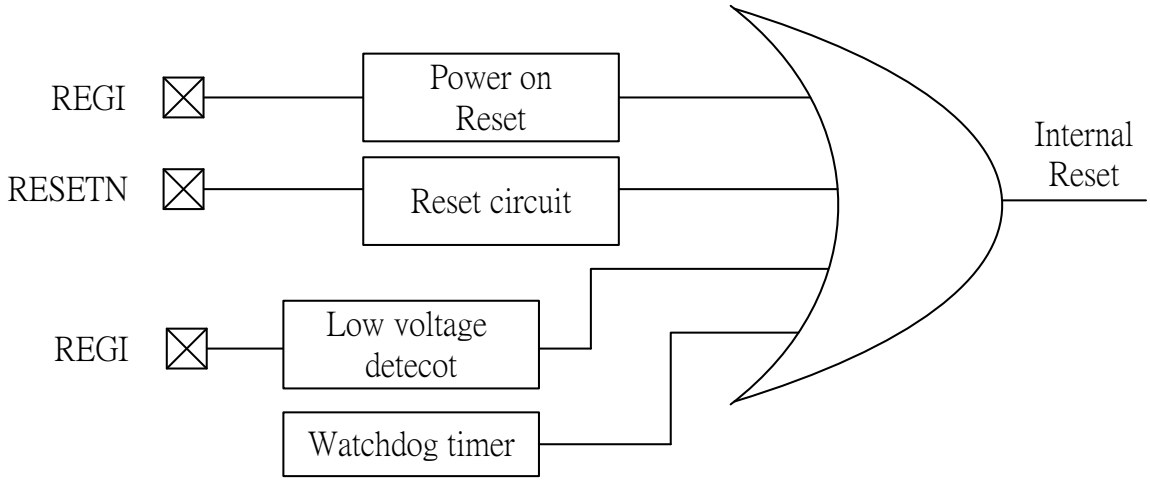


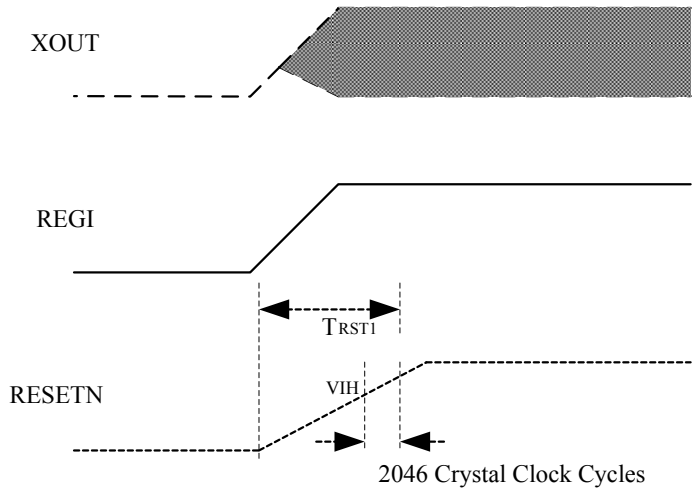

Figure 10.2 Reset source

RSFLAG: Reset Flag (0xBA):

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| BAh RSFLAG | R | - | - | - | - | - | BODF | RESETNF | PORF |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

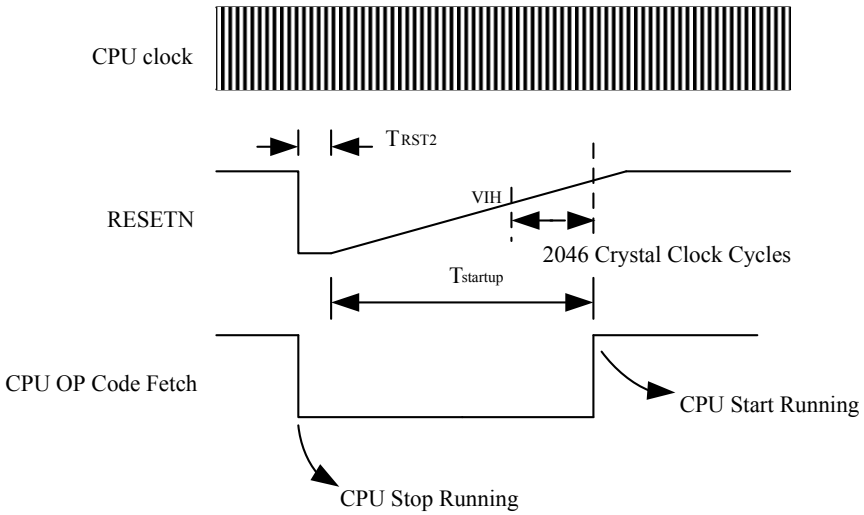
**PORF** (power-on reset flag)
= 1: Occurred Power-on Reset
= 0: No Power-on Reset
**RESETNF** (resetn flag)
= 1: Occurred ResetN reset
= 0: No ResetN resetno resetn reset
**BODF** (Low voltage detect) flag
= 1: Occurred Low Voltage Reset
= 0: No Low Voltage reset

Please refer the figure 10.3 and 10.4 for the timing diagram for stable power of reset signal and internal behavior of CPU.




$T_{RST1}$ : According to RESETN's RC delay (standard module is about 50ms)

Figure 10.3 Timing Diagram for stable power to the release of RESETN




$T_{RST2}$ : 2 Crystal Clock Cycles (min)

$T_{startup}$ : 2046 Crystal Clock Cycles + RESETN's RC delay (standard module is about 50ms)

Figure 10.4 Timing Diagram for RESETN control sequence

## 10.6 Clock source

A8108 has three clock source, crystal oscillator (pin 11,12/ Xi, XO), RTC crystal (pin 23,24/ P3.6, P3.7/ RTC_I, RTC_O) and internal RC oscillator. In the MCU part (digital peripherals ), user choices the suitable clock source by power consumptions and performance. In the RF part, the clock source only comes from XO..

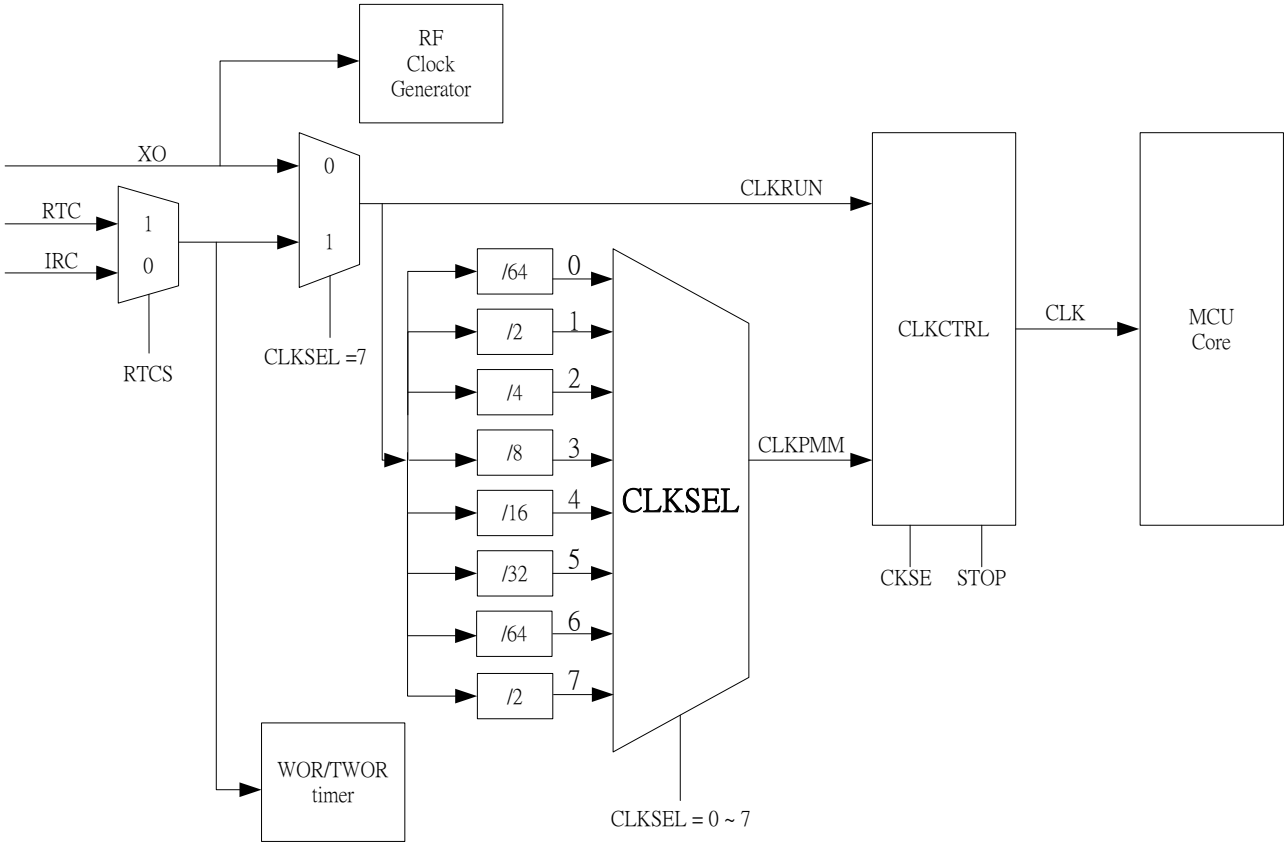



Figure 10.5 Whole chip clock

## 10.7 I/O PORTS

A8108 has 16 Digital I/O Pins. There are separated to 3 Ports (Port0, Port1 and Port3) and each of the Port pin can be defined as general-purpose I/O (GPIO) or peripheral I/O signals connected to the timers, UART, I2C and SPI functions. Thus, each pin can also be used to wake A8108 up from sleep mode. User can select each pin function by setting register. Each port has itself port register like P0 (0x80), P1 (0x90) and P3 (0xB0) that are both byte addressable and bit addressable. When reading, the logic levels of the Port's input pins are returned. Each port has three registers to setting Pull-up (PU), Output-enable (OE) and Wake-up enable (WUE). As shown the bellow block diagram, Fig. 10.4. Unused I/O pins should have a defined level and not be left floating. One way to do this is to leave the pin unconnected and configure the pin as a general-purpose I/O input with pull-up resistor.

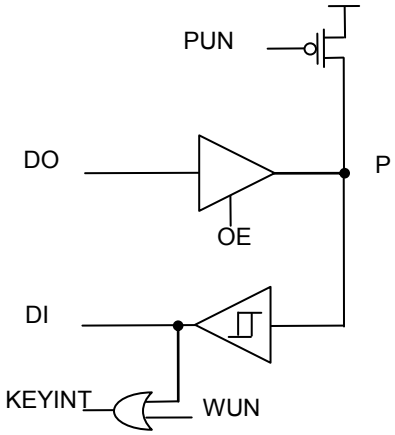



Figure10.5 Ports I/O block diagram

| OE | PUN | P | DI |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 0 | 1 | HZ | INH |
| 1 | X | DO | DO |

Table 10.5 OE and PUN setting and Output(P) and Input(DI)

| WUN | KEYINT |
|---|---|
| 0 | DI |
| 1 | 1 |

Table 10.6 WUN setting and KEYINT source

### 10.7.1 FUNCTIONALITY

It has three 8-bit full bi-directional ports, P0, P1 and P3. Each port bit can be individually accessed by bit addressable instructions.

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 80h<br>P0 | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 0 register

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 90h<br>P1 | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 1 register

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B0h<br>P3 | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 3 register

Read and write accesses to the I/O port are performed via their corresponding SFRs P0(0x80), P1(0x90), and P3(0xB0). Some port-reading instructions read the data register and others read the port's pin. The "Read-Modify-Write" instructions are directed to the data registers and are shown below. All the other instructions used to read a port exclusively read the port's pin.

| Instruction | Function description |
|---|---|
| ANL | Logic AND |
| ORL | Logic OR |
| XRL | Logic eXclusive OR |
| JBC | Jump if bit is set and clear |
| CPL | Complement bit |
| INC, DEC | Increment, decrement byte |
| DJNZ | Decrement and jump if not zero |
| MOV Px.y, C | Move carry bit to y of port x |
| CLR Px.y | Clear bit y of port x |
| SETB Px.y | Set bit y of port x |

Table10.7 Read-modify-write instructions

According the Table 10.5, all Port pins can be configured as Output, Input with pull-up resistor( around 100 Kohm) or Input. Please refer the following truth table to know every function setting. When OE=1, this pin is configured as Output. Otherwise OE =0, this pin is configured as Input. User can set PU =1 or 0 depending on application. When OE =1, PU=0 is recommended for saving power..

| OE | PU | P | DI |
|---|---|---|---|
| 1 | X | DO | DO |
| 0 | 1 | Pull-up | P |
| 0 | 0 | HZ | Input |

All Port pins can wake A8108 up when WUEN=1 and configured GPIO. All Port pins' WEU signals connect one AND gate to INT2. It means pin wake up function needs INT2 ISR to take care this interrupt.

| WUEN | WUNDI |
|---|---|
| 1 | 1 |
| 0 | DI |

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B2h P0PU | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 0 Pull Up Register

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B3h P0OE | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 0 Output Enable Register

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B4h P0WUE | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 0 Wake Up Enable Register

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B5h P1PU | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 1 Pull Up Register

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B6h P1OE | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 1 Output Enable Register

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B7h P1WUE | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 1 Wake Up Enable Register

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| AAh P3PU | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 3Pull Up Register

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ABh P3OE | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 3 Output Enable Register

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ACh P3WUE | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Port 3 Wake Up Enable Register

IOSEL Register (0xBB)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| BBh IOSEL | R/W | usb_resume_en | - | - | RTCIOS | BBIOS | - | - | URT0IOS |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**URT0IOS** (UART0 I/O select)
[1]: Port 3.0 and Port3.1 are selected for UART0 mode0 (open drain I/O)
[0]: Port 3.0 and Port3.1 are normal I/O
**BBIOS** (Base band I/O select)
[1]: Output
[0]: Input
**RTCIOS** (Real-time clock I/O select)
[1]: The pad is for RTC clock
[0]: The pad is normal I/O
usb_resume_en
[1]: Enable
[0]: Disable

**ADCCH Register (0xBC)**

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| BCh ADCCH | R/W | -- | -- | -- | -- | -- | ADCCH2 | ADCCH1 | ADCCH0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ADCIOS[2:0] (ADC I/O select)
ADCIOS0
[1]: Enable ADC analog input
[0]: Disable ADC analog input
ADCIOS[2:1]
[00]: Select P3.2 as the ADC analog input
[01]: Select P3.3 as the ADC analog input
[10]: Select P3.4 as the ADC analog input
[11]: Select P3.5 as the ADC analog input

### 10.7.2 Key interrupt

User can use P0, P1 or P3 port as key input and meanwhile these key are clicked to event a key interrupt to wake up A8108 or enter key process flow. It is a helpful use to design a remote controller and low power consumption with power saving mode setting. The KEY INT vector is located on 0x5B. User can put an interrupt service routine in 0x5B.

The KEY interrupts can wake up A8108 back to normal mode in PM1. In PM2, only Port 3.2~Port 3.5 (wakeup key) or RESETN PIN can wakeup A8108 as reset state and A8108 should to initial all needed peripherals and take care key interrupt event.

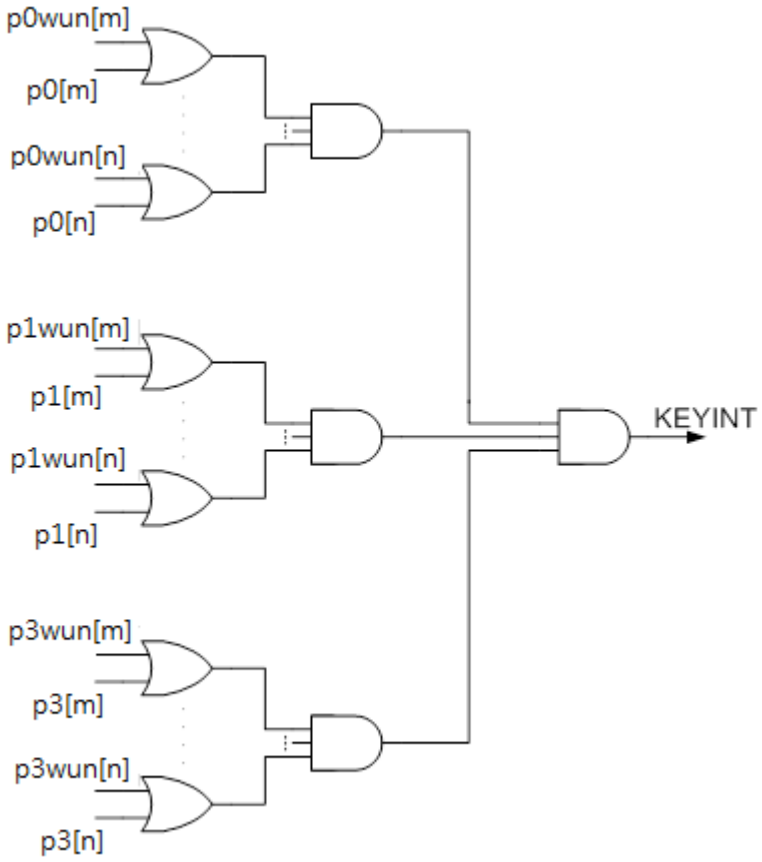



Figure10.7 Key interrupt block diagram

## 10.8 Timer 0, 1 & 2

A8108 contains three 16-bit timer/counters, Timer 0, Timer 1 and Timer 2. Timer 0 and Timer 1 in the “timer mode“, timer registers are incremented every 4/12/CLK periods depends on CKCON (0x8E) setting, when appropriate timer is enabled. In the “counter mode” the timer registers are incremented every falling transition on theirs corresponding input pins: T0 or T1. The input pins are sampled every CLK period.

The Timer 2 is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc.

### 10.8.1 Timer 0 & 1 Pins Description

The pins functionality is described in the following table. All pins are one directional.

| PIN | ACTIVE | TYPE | DESCRIPTION |
|---|---|---|---|
| T0(P3.4) | Falling | Input | Timer 0 clock line |
| GATE0(P3.2) | High | Input | Timer 0 clock line gate control |
| T1(P3.5) | Falling | Input | Tiner 1 clock line |
| GATE1(P3.3) | High | Input | Timer 1clock line gate control |

Table 10.8 Timer 0, 1 pins description

### 10.8.2 Timer 0 & 1 Functionality

Timer 0 and Timer 1 are fully compatible with the standard 8051 timers. Each timer consists of two 8-bit registers TH0 (0x8C), TL0 (0x8A), TH1 (0x8D), TL1 (0x8B). Timers 0, 1 work in the same four modes. The modes are described below.

| M1 | M0 | Mode | Function description |
|---|---|---|---|
| 0 | 0 | 0 | THx operates as 8-bit timer/counter with a divide by 32 prescaler served by lower 5-bit of TLx. |
| 0 | 1 | 1 | 16-bit timer/counter. THx and TLx are cascaded. |
| 1 | 0 | 2 | TLx operates as 8-bit timer/counter with 8-bit auto-reload by THx. |
| 1 | 1 | 3 | TL0 is configured as 8-bit timer/counter controlled by the standard Timer 0 bits. TH0 is an 8-bit timer controlled by the Timer 1 controls bits. Timer 1 holds its count. |

Table 10.9 Timer 0 and 1 modes

### 10.8.3 Timer 0 & 1 Registers

TMOD register (0x89)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 89h TMOD | R/W | GATE1 | CT | M1 | M0 | GATE0 | CT | M1 | M0 |
| | | Timer 1 control bits | | | | Timer 0 control bits | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

GATE：Gating control

=1, Timer x enabled while GATEx pin is high and TRx control bit is set.

=0, Timer x enabled while TRx control bit is set.

CT：Counter or timer select bit

=1, Counter mode, Timer x clock from Tx pin.

=0, Timer mode, internally clocked.

M[1：0]：Mode select bits

TCON register (0x88)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 88h TCON | R/W | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TR0：Timer 0 run control bit

=1, enabled.

=0, disabled.

TR1：Timer 1 run control bit

=1, enabled.

=0, disabled.

TF0：Timer 0 interrupt (overflow) flag.
Cleared by hardware when processor branches to interrupt routine.
TF1：Timer 1 interrupt (overflow) flag.
Cleared by hardware when processor branches to interrupt routine.

CKCON register (0x8E)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 8Eh CKCON | R/W | - | - | - | T1M | T0M | MD2 | MD1 | MD0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

T0M：This bit controls the division of the system clock that drives Timer 0.
=1, Timer 0 uses a divided-by-4 of the system clock frequency.
=0, Timer 0 uses a divided-by-12 of the system clock frequency.

T1M：This bit controls the division of the system clock that drives Timer 1.
=1, Timer 1 uses a divided-by-4 of the system clock frequency.
=0, Timer 1 uses a divided-by-12 of the system clock frequency.

IE register (0xA8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| A8h IE | R/W | EA | - | ET2 | ES0 | ET1 | EX1 | ET0 | EX0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

EA：Enable global interrupts.
ET0：Enable Timer 0 interrupts.
ET1：Enable Timer 1 interrupts.

IP register (0xB8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B8h IP | R/W | - | - | PT2 | PS0 | PT1 | PX1 | PT0 | PX0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PT0：Timer 0 priority level control (at 1-high level)
PT1：Timer 1 priority level control (at 1-high level)

Timer 0, 1 related bits that generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software.

| Interrupt flag | Function | Active level/edge | Flag resets | Vector | Natural priority |
|---|---|---|---|---|---|
| TF0 | Internal, Timer 0 | - | Hardware | 0x0B | 2 |
| TF1 | Internal, Timer 1 | - | Hardware | 0x1B | 4 |

Table 10.10 Timer 0, 1 interrupts

### 10.8.4 Timer 0 – Mode 0

In this mode, the Timer 0 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s. Timer 0 interrupt flag TF0 is set. The counted input is enabled to the Timer 0 when TCON.4 = 1 and either TMOD.3 = 1 or GATE0 = 1. (Setting TMOD.3 = 1 allows the Timer 0 to be controlled by external input GATE0, to facilitate pulse width measurement). The 13-bit register consists of all 8-bit of TH0 and lower 5 bits of TL0.The upper 3 bits of TL0 are indeterminate and should be ignored.

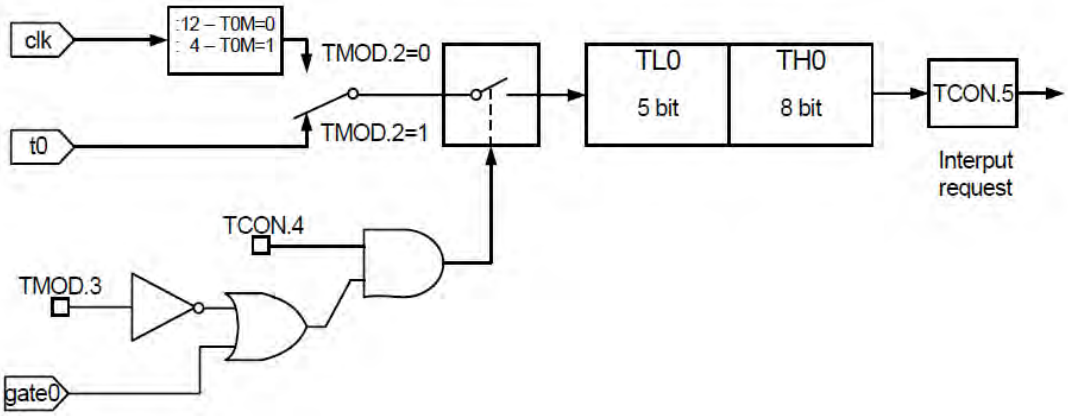



Figure10.8 Timer/Counter 0, Mode 0：13-Bit Timer/Counter

### 10.8.5 Timer 0 – Mode 1

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. Mode 1 is shown in figure below.

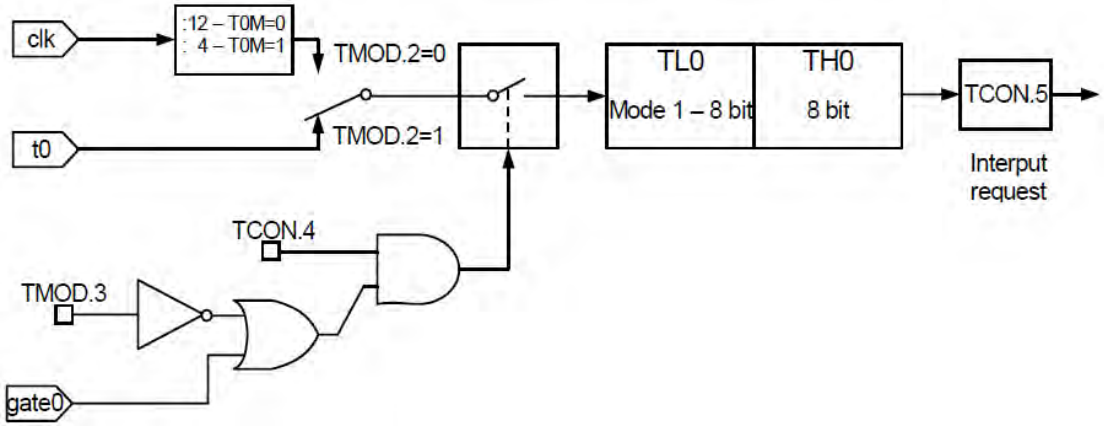



Figure10.9 Timer/Counter 0, Mode 1：16-Bit Timer/Counter

### 10.8.6 Timer 0 – Mode 2

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reloads, as shown in figure below. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is loaded by software. The reload leaves TH0 unchanged.

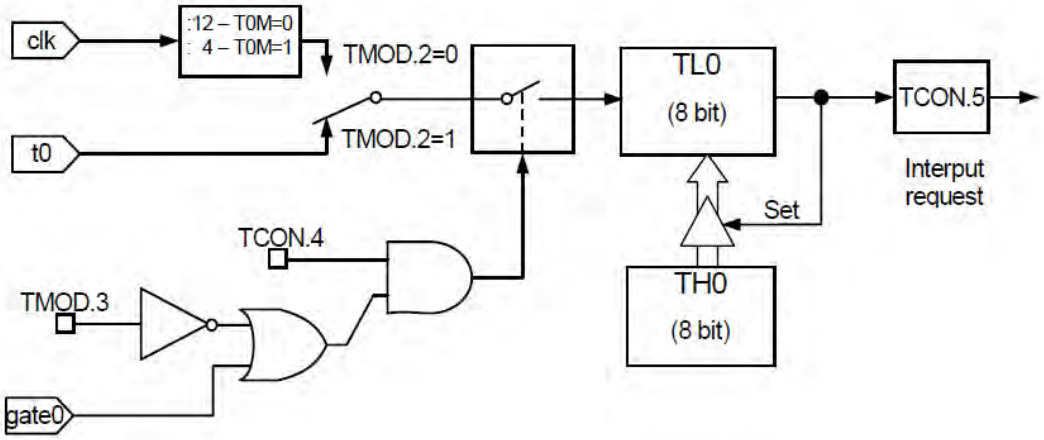



Figure10.10 Timer/Counter 0, Mode 2：8-Bit Timer/Counter with Auto-Reload

### 10.8.7 Timer 0 – Mode 3

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in figure below. TL0 uses the Timer 0 control bits：C/T, GATE, TR0, GATE0 and TF0. TH0 is locked into a timer function and use the TR1 and TF1 flag from Timer1 and controls Timer1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer/counter. When Timer 0 is in Mode 3, Timer 1 can be turned off by switching it into its own Mode 3, or can still be used by the serial channel as a baud rate generator, or in any application where interrupt from Timer 1 is not required.

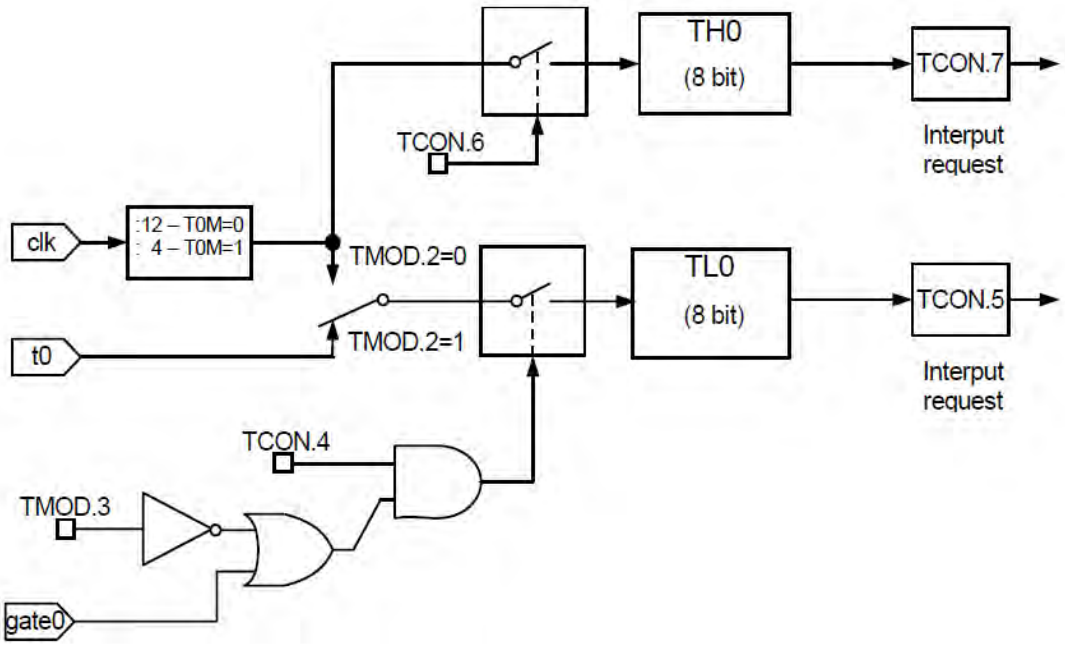



Figure10.11 Timer/Counter 0, Mode 3：Two 8-Bit Timers/Counters

### 10.8.8 Timer 1 – Mode 0

In this Mode, the Timer1 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer1 interrupt flag TF1 is set. The counted input is enabled to the Timer1 when TCON.6 = 1 and either TMOD.6 = 0 or GATE1 = 1. (Setting TMOD.7 = 1 allows the Timer1 to be controlled by external input GATE1, to facilitate pulse width measurements). The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored.

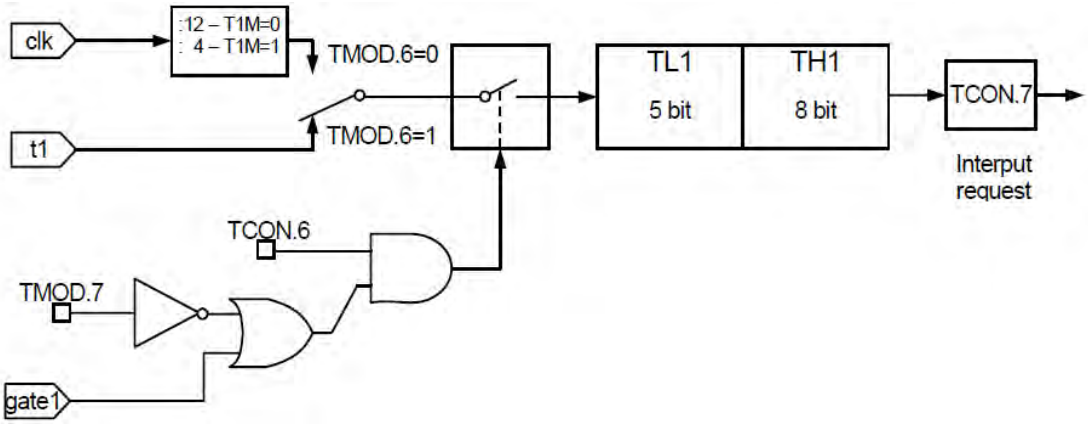



Figure10.12 Timer/Counter 1, Mode 0：13-Bit Timers/Counters

### 10.8.9 Timer 1 – Mode 1

Mode 1 is the same as Mode 0, except that timer register is running with all 16 bits. Mode 1 is shown in figure below.

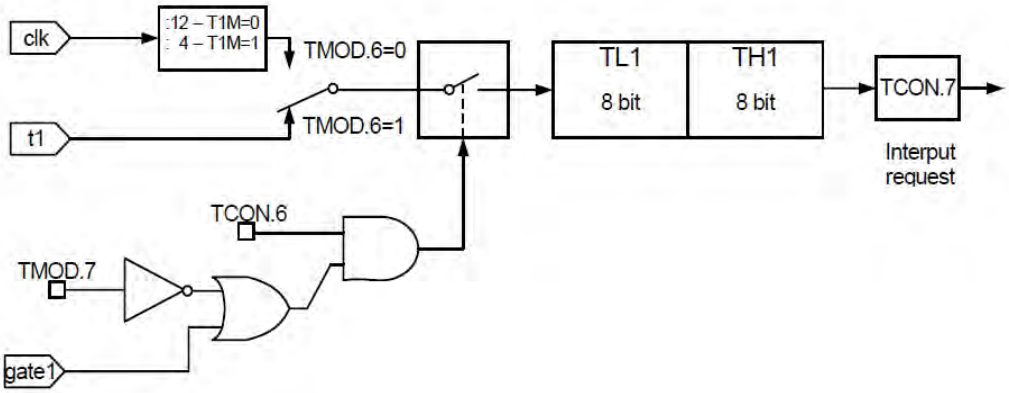



Figure10.13 Timer/Counter 1, Mode 0：16-Bit Timers/Counter

### 10.8.10 Timer 1 – Mode 2

Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reloads, as shown in figure below. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is loaded by software. The reload leaves TH1 unchanged.

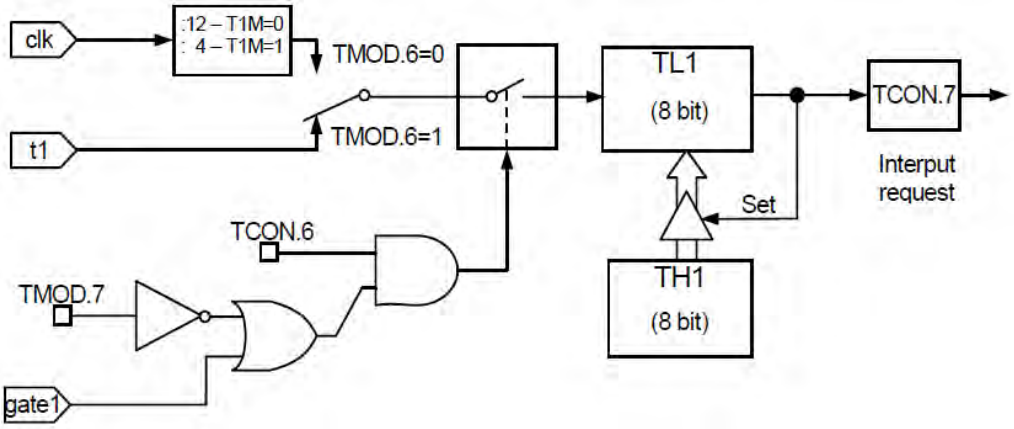



Figure10.14 Timer/Counter 1, Mode 2：8-Bit Timer/Counter with Auto-Reload

### 10.8.11 Timer 1 – Mode 3

Timer 1 in Mode 3 is held counting. The effect is the same as setting TR1=0.

### 10.8.12 Timer 2 Pins Description

### 10.8.13 Timer 2 Functionality

Timer 2 is fully compatible with the standard 8052 Timer 2. It is up counter. Totally five SFRs control the Timer 2 operation: TH2/TL2(0xCD/0xCC) counter registers, RLDH/RLDL (0xCB/0xCA) capture registers and T2CON(0xC8) control register. Timer 2 works in the three modes selected by T2CON bits as shown in table below.

| RCLK, TCLK | CPRL2 | TR2 | Function description |
|---|---|---|---|
| 0 | 0 | 1 | 16-bit auto-reload mode. The Timer 2 overflow sets TF2 bit and the TH2,TL2 registers reloaded 16-bit value from RLDH, RLDL. |
| 0 | 1 | 1 | 16-bit capture mode. The Timer 2 overflow sets TF2 bit. When the EXEN2 = 1, the TH2, TL2 register values are stored into RLDH, RLDL while falling edge is detected on T2EX pin. |
| 1 | X | 1 | Baud rate generator for the UART0 interface. It auto-reloads its counter with RLDH, RLDL values each overflows. |

| | | | |
|---|---|---|---|
| X | X | 0 | Timer 2 is off |

Table 10.12 Timer 2 modes

### 10.8.14 Timer 2 Registers

T2CON register (0xC8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| C8h<br>APOL<br>Reset | R/W | TF2<br>0 | -<br>0 | RCLK<br>0 | TCLK<br>0 | EXEN2<br>0 | TR2<br>0 | CT2<br>0 | CPRL2<br>0 |

RCLK：Receive clock enable

=1, UART0 receiver is clocked by Timer 2 overflow pulses

=0, UART0 receiver is clocked by Timer 2 overflow pulses

TCLK：Transmit clock enable

=1, UART0 transmitter is clocked by Timer 2 overflow pulses

=0, UART0 transmitter is clocked by Timer 2 overflow pulses

EXEN2：Enable T2EX pin functionality.

=0, ignore T2EX events

TR2：Start / Stop Timer 2

=1, start

=0, stop

CT2：Timer / counter select

=0, timer 2 Internally clocked

CPRL2：Capture / Reload select

=0, automatic reload occurs：on Timer 2 overflow. When RCLK or TCLK is set this bit is ignored and automatic reload on Timer 2 overflow is forced.

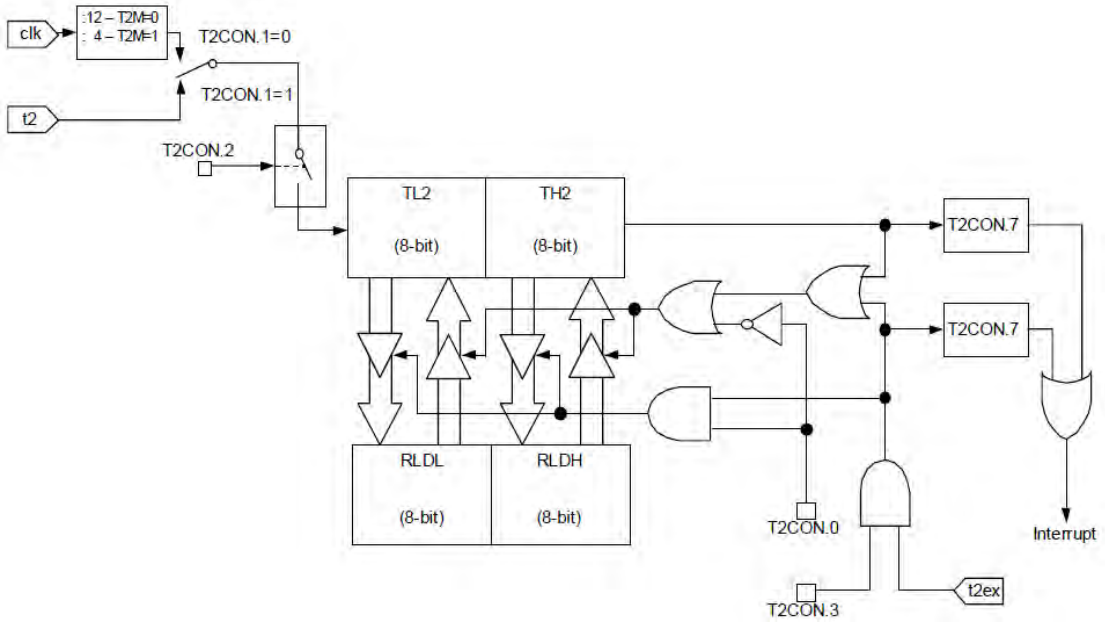



Figure10.15 Timer 2 block diagram in timer mode

CKCON register (0x8E)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 8Eh<br>CKCON<br>Reset | R/W | -<br>0 | -<br>0 | -<br>0 | T1M<br>0 | T0M<br>0 | MD2<br>0 | MD1<br>0 | MD0<br>0 |

T2M：This bit controls the division of the system clock that drives Timer 2. This bit has no effect when the timer is in baud rate generator mode.

=1, Timer 2 uses a divide-by-4 of the system clock frequency.

=0, Timer 2 uses a divide-by-12 of the system clock frequency.

Timer 2 interrupt related bits are shown below. An interrupt can be turned on/off by IE (0xA8) register, and set into high/low priority group by IP register.

IE register (0xA8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| A8h IE Reset | R/W | EA 0 | - 0 | ET2 0 | ES0 0 | ET1 0 | EX1 0 | ET0 0 | EX0 0 |

EA：Enable global interrupts.

ET2：Enable Timer 2 interrupts.

IP register (0xB8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B8h IP Reset | R/W | - 0 | - 0 | PT2 0 | PS0 0 | PT1 0 | PX1 0 | PT0 0 | PX0 0 |

PT2：Timer 2 priority level control (at 1-high level)

-：Unimplemented bit. Read as 0 or 1.

T2CON register (0xC8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| C8h T2CON Reset | R/W | TF2 0 | - 0 | RCLK 0 | TCLK 0 | EXEN2 0 | TR2 0 | CT2 0 | CPRL2 0 |

TF2：Timer 2 interrupt (overflow) flag. Must be cleared by software.

The flag will not be set when either RCLK or TCLK is set.

All Timer 2 related bits generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software.

| Interrupt flag | Function | Active level / edge | Flag resets | Vector | Natural priority |
|---|---|---|---|---|---|
| TF2 | Internal, Timer2 | - | Software | 0x2B | 6 |

Table 10.13 Timer 2 interrupt

Please see picture below. Timer2 internal logic configured as baud-rate generator is shown below.

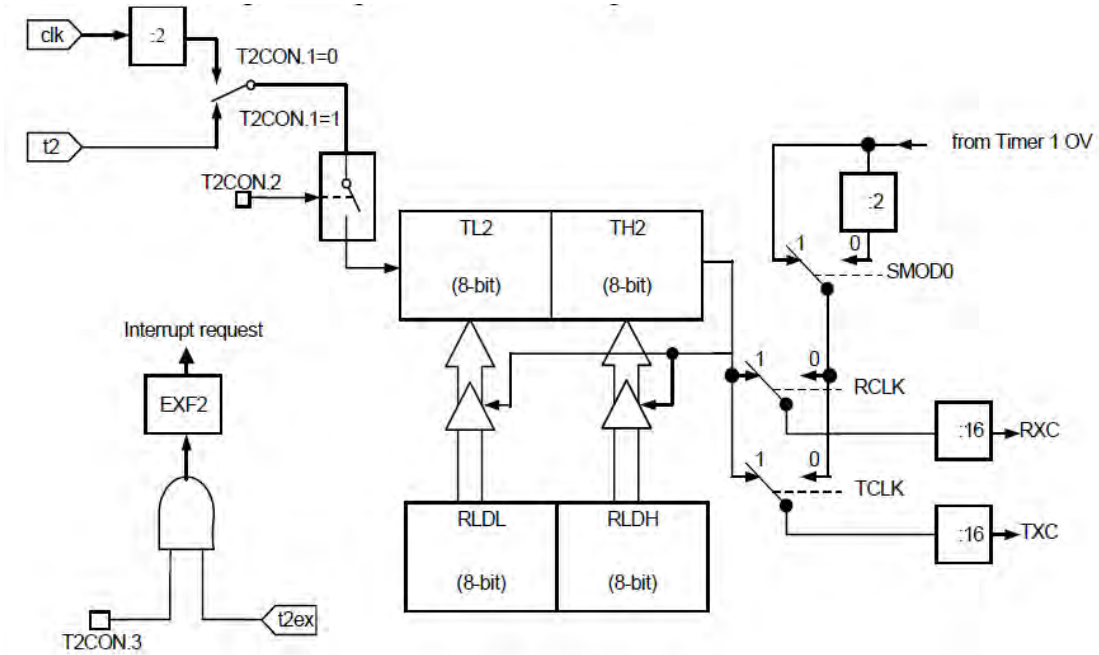



Figure10.16 Timer 2 block diagram as UART0 baud rate generator

Please note that SMOD0 bit is ignored by UART when clocked by Timer2. The RLCK/TCLK frequency is equal to：

$$xCLK = \frac{CLK}{2 \cdot (65536 - RLD)}$$

$$where\, xCLK = TCLK, RCLK$$

## 10.9 UART 0 & 1

UART0 is full duplex, meaning it can transmit and receive concurrently. It is receive double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. The serial port can operate in 4 modes: one synchronous and three asynchronous modes. Mode 2 and 3 has a special feature for multiprocessor communications. This feature is enabled by setting SM02 bit in SCON0 register. The master processor first sends out an address byte, which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM02 = 1, no slave will be interrupted by a data byte. An address byte will interrupt all slaves. The addressed slave will clear its SM02 bit and prepare to receive the data bytes that will be coming. The slaves that were not being addressed leave their SM02 set and ignoring the incoming data.

### 10.9.1 UART0 Pins Description

The UART0 pins functionality is described in the following table. All pins are one directional. There are no three-state output pins and internal signals.

| PIN | ACTIVE | TYPE | DESCRIPTION |
|---|---|---|---|
| Rxd_0(P3.0) | - | Input / Output | Serial receiver I_0 / O_0 |
| Txd_0(P3.1) | - | Output | Serial transmitter line 0 |

Table 10.14 UART0 pins description

### 10.9.2 UART0 Functionality

The UART0 has the same functionality as a standard 8051 UART. The UART0 related registers are: SBUF0(0x99), SCON0(0x98), PCON(0x87), IE(0xA8) and IP(0xB8). The UART0 data buffer (SBUF0) consists of two separate registers: transmit and receive registers. A data writes into the SBUF0 sets this data in UART0 output register and starts a transmission. A data reads from SBUF0, reads data from the UART0 receive register.

SBUF0 register (0x99)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 99h SBUF0 | R/W | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SB0[7:0]：UART0 buffer

SCON0 register (0x98)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 98h SCON0 | R/W | SM00 | SM01 | SM02 | REN0 | TB08 | RB08 | TI0 | RI0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SM02：Enable a multiprocessor communication feature

SM0[1:0]：Sets baud rate

| SM00 | SM01 | Mode | Description | Baud Rate |
|---|---|---|---|---|
| 0 | 0 | 0 | Shift register | $F_{CLK}/12$, $F_{CLK}/4$ |
| 0 | 1 | 1 | 8-bit UART | Variable(16bit) |
| 1 | 0 | 2 | 9-bit UART | $F_{CLK}/32$ or $F_{CLK}/64$ |
| 1 | 1 | 3 | 9-bit UART | Variable(16bit) |

Timer 2 cannot be used as baud rate generator when Compare Capture unit is present in the system. The UART0 baud rates are presented in the table below.

| Mode | Baud Rate | |
|---|---|---|
| Mode 0 | FCLK/12 | |
| Mode 1, 3 | Timer 1 overflow rate – $T1_{ov}$ | |
| | SMOD0 = 0 | $T1_{ov}/32$ |
| | SMOD0 = 1 | $T1_{ov}/16$ |
| | Timer 2 overflow rate – $T2_{ov}$ | |
| | SMOD0 = x | $T2_{ov}/16$ |
| Mode 2 | SMOD0 = 0 | $F_{CLK}/64$ |
| | SMOD0 = 1 | $F_{CLK}/32$ |

The SMOD0 bit is located in PCON register.

REN0：If set, enable serial reception. Cleared by software to disable reception.

TB08：The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the CPU, depending on the function it performs (parity check, multiprocessor communication etc.)

RB08：In Modes 2 and 3 it is the 9th data bit received. In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 0 this bit is not used.

PCON register (0x87)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 87h PCON | R/W | SMOD0 | SMOD1 | - | PWE | - | SWB | STOP | PMM |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SMOD0：UART0 double baud rate bit when clocked by Timer 1 only.

- INTERRUPTS

UART0 interrupt related bits are shown below. An interrupt can be turned on / off by IE register, and set into high / low priority group by IP register.

IE register (0xA8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|

| A8h IE | R/W | EA | - | ET2 | ES0 | ET1 | EX1 | ET0 | EX0 |
|---|---|---|---|---|---|---|---|---|---|
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ES0：RI0 & TI0 interrupt enable flag

IP register (0xB8)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B8h IP | R/W | - | - | PT2 | PS0 | PT1 | PX1 | PT0 | PX0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PS0：RI0 & TI0 interrupt priority flag

SCON0 register (0x98)

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 98h SCON0 | R/W | SM00 | SM01 | SM02 | REN0 | TB08 | RB08 | TI0 | RI0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TI0：Transmit interrupt flag, set by hardware after completion of a serial transfer.
Must be cleared by software.
RI0：Receive interrupt flag, set by hardware after completion of a serial reception.
Must be cleared by software.

All of bits that generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software.

| Interrupt flag | Function | Active level / edge | Flag resets | Vector | Natural priority |
|---|---|---|---|---|---|
| TI0 & RI0 | Internal, UART0 | - | Software | 0x23 | 5 |

Table 10.15 UART0 interrupt

### 10.9.3 UART0 MODE 0, SYNCHRONOUS

Pin RXD0I serves as input and RXD0O as output. TXD0 output is a shift clock. The baud rate is fixed at 1/12 of the CLK clock frequency. Eight bits are transmitted with LSB first. Reception is initialized by setting the flags in SCON0 as follows: RI0=0 and REN0=1.

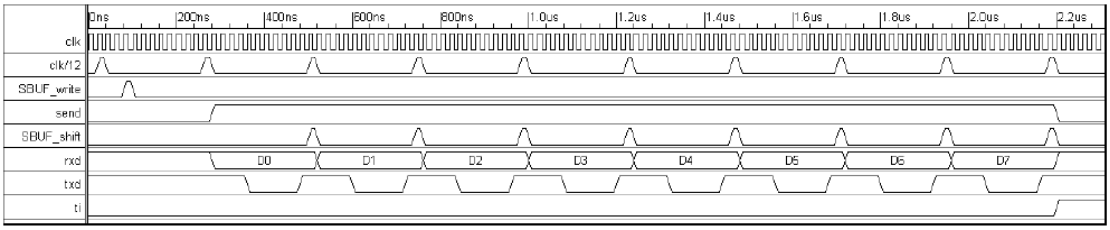



Figure10.17 UART0 transmission mode 0 timing diagram

### 10.9.4 UART0 MODE 1, 8-BIT UART, VARIABLE BAUD RATE, TIMER CLOCK SOURCE

Pin RXD0I serves as input, and TXD0 serves as serial output. 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading SBUF0, and stop bit sets the flag RB08 in the SFR SCON0. The baud rate is variable and depends from Timer 1 or Timer 2 mode. To enable Timer 2 clocking set the TCLK, RCLK bits located in T2CON (0xC8) register. SMOD0 bit is ignored when UART is clocked by Timer2.

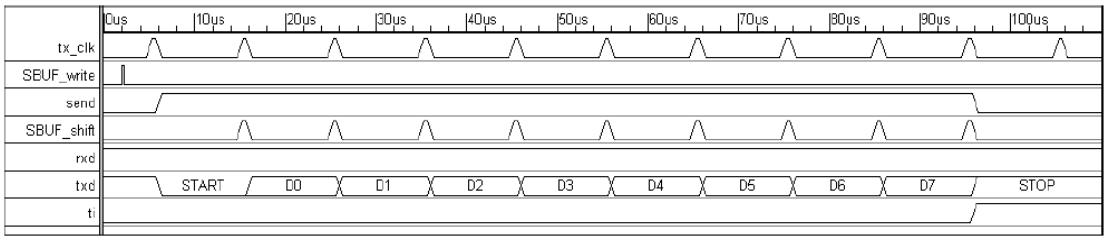



Figure10.18 UART0 transmission mode 1 timing diagram

### 10.9.5 UART0 MODE 2, 9-BIT UART, FIXED BAUD RATE

This mode is similar to Mode 1 with two differences. The baud rate is fixed at 1/32 or 1/64 of CLK clock frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9$^{th}$ bit, and a stop bit (1). The 9$^{th}$ bit can be used to control the parity of the UART0 interface: at transmission, bit TB08 in SCON0 is output as the 9$^{th}$ bit, and at receive, the 9$^{th}$ bit affects RB08 in SCON0.

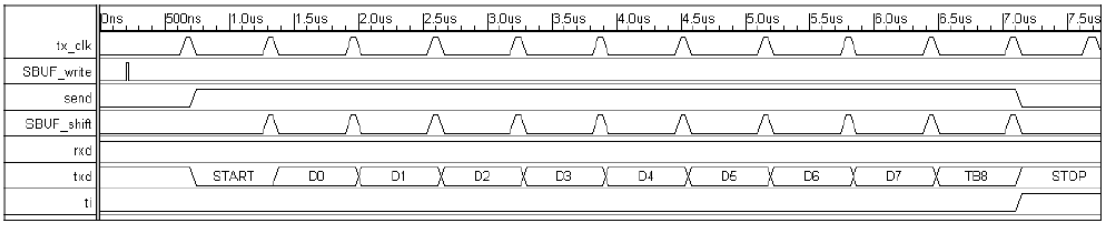



Figure10.19 UART0 transmission mode 2 timing diagram

### 10.9.6 UART0 MODE 3, 9-BIT UART, VARIABLE BAUD RATE, TIMER CLOCK SOURCE

The only difference between Mode 2 and Mode 3 is that the baud rate is a variable in Mode 3. When REN0=1 data receiving is enabled. The baud rate is variable and depends from Timer 1 or Timer 2 mode. To enable Timer 2 clocking set the TCLK, RCLK bits located in T2CON (0xC8) register. SMOD0 bit is ignored when UART is clocked by Timer2.

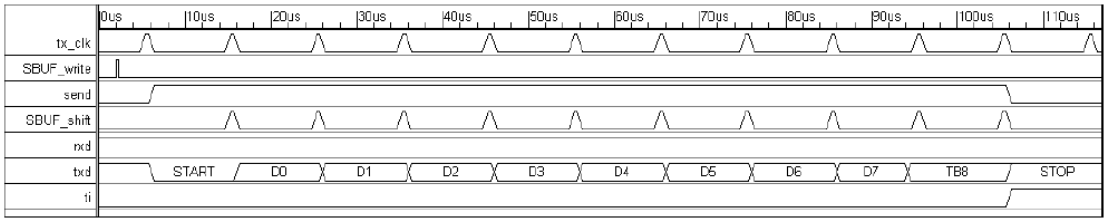


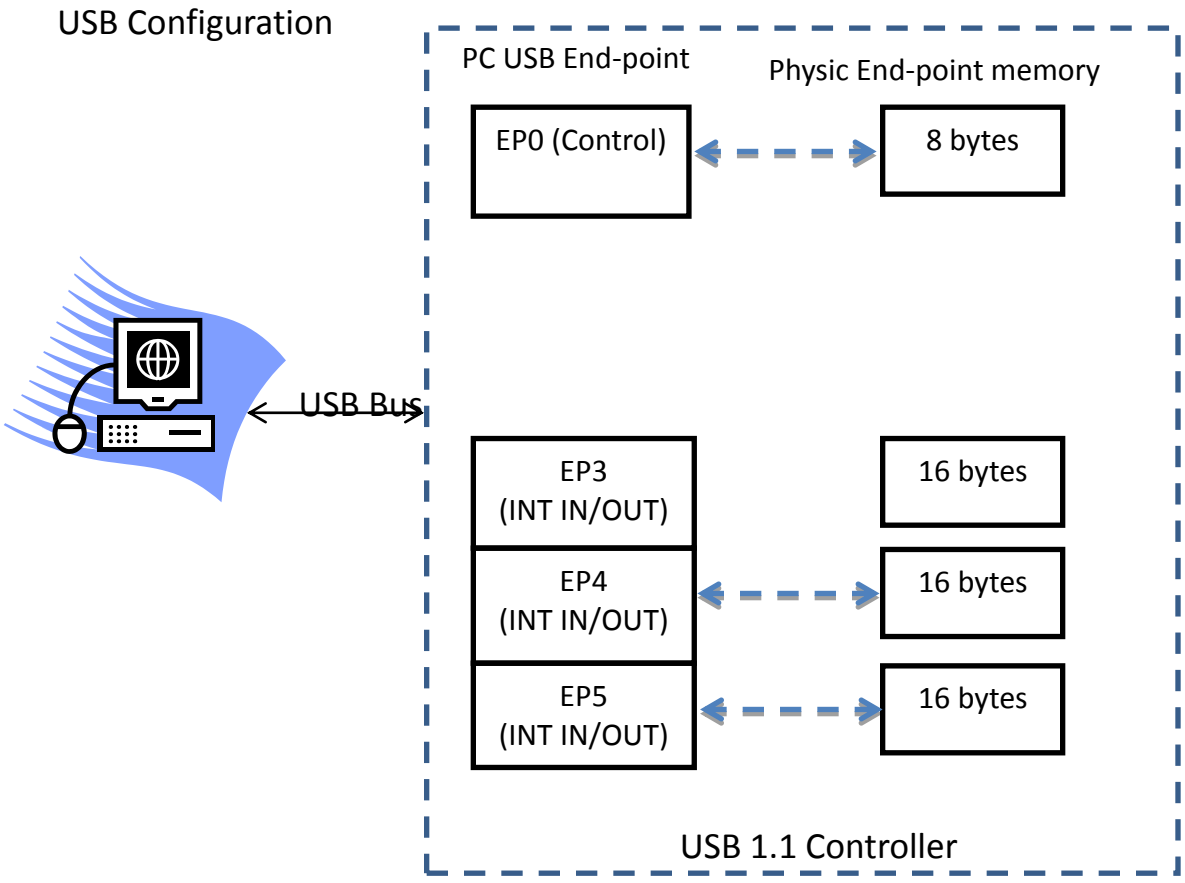

Figure10.20 UART0 transmission mode 3 timing diagram

A8108 supports different crystal frequency by programmable “Clock Register” (0Dh). Based on this, three important internal clocks $F_{CGR}$ , $F_{DR}$ and $F_{SYCK}$ are generated.

(1) $F_{XTAL}$: Crystal frequency.
(2) $F_{XREF}$: Crystal Ref. Clock = $F_{XTAL}$ * (DBL+1).
(3) $F_{CGR}$: Clock Generation Reference = 2MHz = $F_{XREF}$ / (GRC+1), where $F_{CGR}$ is used to generate 32M PLL.
(4) $F_{MCLK}$: Master Clock is either $F_{XREF}$: or 32M PLL, where $F_{MCLK}$ is used to generate $F_{SYCK}$.
(5) $F_{SYCK}$: System Clock = 16MHz=$F_{MCLK}$ / CSC= 32 * $F_{IF}$, where $F_{IF}$ is recommended to set 500KHz.
(6) $F_{DR}$: Data Rate Clock = $F_{IF}$ / (SDR+1).
(7) $F_{FPD}$: VCO Compared Clock = = $F_{XREF}$ / (RRC+1).

## 11. USB Controller Overview

A8108 USB controller has 4 end-points, one EP for basic control, and three EPs for configurable interrupt input or interrupt out The end-point memory buffers allocations are as the following diagram.




For A8108 USB controller, user could configure this USB device as: HID interface, and keyboard/mouse application. The control registers are described in the next section.

### 11.1 USB Control Registers

USB basic control Register (Address: 4000h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | - | | | | USB Interrupt clear | USB_PHY_TEST[2:0] | | |
| Reset | | | | | | 0 | 3'b001 | | |

USB Interrupt clear: To clear USB interrupt.
[0]: Disable. [1]: clear interrupt.
USB_PHY_TEST[2:0]: To set USB PHY.
[XX1]: USB PHY normal mode. [000]: SE0. [010]: TEST J. [100]: TEST K. [0]: low speed. [110]:Test eye-diagram

USB address read Register (Address: 4001h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | -- | USB Current Address [6:0] | | | | | | |
| Reset | | -- | 7'd 00 | | | | | | |

USB Current Address [6:0]:To indicate USB current address setting. Read only

USB endpoint read Register (Address: 4002h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | -- | | | | USB Current End-Point [3:0] | | | |
| Reset | | -- | | | | 4'd 0 | | | |

USB Current End-Point [3:0]:To indicate USB current end points setting. Read only.

USB UdcBuffer0_dec Register (Address: 4003h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF_BUF0_Num[3:0] | | | | EPINF BUF0 Configure | -- | EPINF BUF0 interface | |
| Reset | | 4'd 0 | | | | 0 | 0 | 2'd0 | |

USB Device EPINF_BUF0_Num [3:0]: To set USB device end_point_information_buffer0 end points value.
USB Device EPINF BUF0 Configure: To set USB device end_point_information_buffer0 configuration value..
USB Device EPINF BUF0 interface: To set USB device end_point_information_buffer0 interface value..

USB UdcBuffer1_dec Register (Address: 4004h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF BUF0 alter interface | | EPINF BUF0 type | | EPINF BUF0 direction | EPINF BUF0 maximum packet size[9:7] | | |
| Reset | | 2'd0 | | 2'd0 | | 0 | 3'd0 | | |

USB Device EPINF BUF0 alter interface To set USB device end_point_information_buffer0 alter interface value.
USB Device EPINF BUF0 type To set USB device end_point_information_buffer0 end point type.
[00]:control type; [01]:isochronous type; [10]:Buck type; [11]:interrupt type;
USB Device EPINF BUF0 direction. [0]: Out token. [1]: In token.
USB Device EPINF BUF0 maximum packet size[9:7]: To set USB device end_point_information_buffer0 maximum packet size value.

USB UdcBuffer2_dec Register (Address: 4005h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF BUF0 maximum packet size[6:0] | | | | | | | -- |
| Reset | | 7'd0 | | | | | | | 0 |

USB Device EPINF BUF0 maximum packet size[6:0]: To set USB device end_point_information_buffer0 maximum packet size value.

USB UdcBuffer3_dec Register (Address: 4006h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | EPINF BUF0 address point[15:8] | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

USB Device EPINF BUF0 address point[15:8]: To indicate USB device end_point_information_buffer0 current address pointer.
USB UdcBuffer4_dec Register (Address: 4007h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | EPINF BUF0 address point[7:0] | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

USB Device EPINF BUF0 address point[7:0]: To indicate USB device end_point_information_buffer0 current address pointer.

USB UdcBuffer5_dec Register (Address: 4008h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF_BUF3_Num[3:0] | | | | EPINF BUF3 Configure | -- | EPINF BUF3 interface | |
| Reset | | 4'd 0 | | | | 0 | 0 | 2'd0 | |

USB Device EPINF_BUF3_Num [3:0]: To set USB device end_point_information_buffer3 end points value.
USB Device EPINF BUF3 Configure: To set USB device end_point_information_buffer3 configuration value..
USB Device EPINF BUF3 interface: To set USB device end_point_information_buffer3 interface value..

USB UdcBuffer6_dec Register (Address: 4009h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF BUF3 alter interface | | EPINF BUF3 type | | EPINF BUF3 direction | EPINF BUF3 maximum packet size[9:7] | | |
| Reset | | 2'd0 | | 2'd0 | | 0 | 3'd0 | | |

EPINF BUF3 alter interface: To set USB device end_point_information_buffer3 alter interface value.
EPINF BUF3 type: To set USB device end_point_information_buffer3 end point type.
[00]: Control type; [01]: Isochronous type; [10]: Buck type; [11]: Interrupt type;
EPINF BUF3 direction: To set USB BUF3 In/Out token control bit.
[0]: Out token. [1]: In token.
EPINF BUF3 maximum packet size[9:7]: The USB device end_point_information_buffer3 maximum packet size value.

USB UdcBuffe7_dec Register (Address: 400ah)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF BUF3 maximum packet size[6:0] | | | | | | | -- |
| Reset | | 7'd0 | | | | | | | 0 |

USB Device EPINF BUF3 maximum packet size[6:0]: The USB device end_point_information_buffer3 maximum packet size value.

USB UdcBuffer8_dec Register (Address: 400bh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | EPINF BUF3 address point[15:8] | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

USB Device EPINF BUF3 address point[15:8]: To indicate USB device end_point_information_buffer3 current address pointer.

USB UdcBuffer9_dec Register (Address: 400ch)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | EPINF BUF3 address point[7:0] | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

USB Device EPINF BUF3 address point[7:0]: To indicate USB device end_point_information_buffer3 current address pointer.
USB UdcBuffer10_dec Register (Address: 400dh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF_BUF4_Num[3:0] | | | | EPINF BUF4 Configure | -- | EPINF BUF4 interface | |
| Reset | | 4'd 0 | | | | 0 | 0 | 2'd0 | |

USB Device EPINF_BUF4_Num [3:0]: To set USB device end_point_information_buffer4 end points value.
USB Device EPINF BUF4 Configure: To set USB device end_point_information_buffer4 configuration value..
USB Device EPINF BUF4 interface: To set USB device end_point_information_buffer4 interface value..

USB UdcBuffer11_dec Register (Address: 400eh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF BUF4 alter interface | | EPINF BUF4 type | | EPINF BUF4 direction | EPINF BUF4 maximum packet size[9:7] | | |
| Reset | | 2'd0 | | 2'd0 | | 0 | 3'd0 | | |

USB Device EPINF BUF4 alter interface To set USB device end_point_information_buffer4 alter interface value.
USB Device EPINF BUF4 type To set USB device end_point_information_buffer4 end point type.
[00]:control type; [01]:isochronous type; [10]:Buck type; [11]:interrupt type;
USB Device EPINF BUF4 direction.[0]: Out token. [1]: In token.
USB Device EPINF BUF4 maximum packet size[9:7]: To set USB device end_point_information_buffer4 maximum packet size value.

USB UdcBuffe12_dec Register (Address: 400fh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF BUF4 maximum packet size[6:0] | | | | | | | -- |
| Reset | | 7'd0 | | | | | | | 0 |

USB Device EPINF BUF4 maximum packet size[6:0]: To set USB device end_point_information_buffer4 maximum packet size value.

USB UdcBuffer13_dec Register (Address: 4010h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | EPINF BUF4 address point[15:8] | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

USB Device EPINF BUF4 address point[15:8]: To indicate USB device end_point_information_buffer4 current address pointer.

USB UdcBuffer14_dec Register (Address: 4011h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | EPINF BUF4 address point[7:0] | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

USB Device EPINF BUF4 address point[7:0]: To indicate USB device end_point_information_buffer4 current address pointer.

USB UdcBuffer15_dec Register (Address: 4012h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF_BUF5_Num[3:0] | | | | EPINF BUF5 Configure | -- | EPINF BUF5 interface | |
| Reset | | 4'd 0 | | | | 0 | 0 | 2'd0 | |

USB Device EPINF_BUF5_Num [3:0]: To set USB device end_point_information_buffer5 end points value.
USB Device EPINF BUF5 Configure: To set USB device end_point_information_buffer5 configuration value..
USB Device EPINF BUF5 interface: To set USB device end_point_information_buffer5 interface value..

USB UdcBuffer16_dec Register (Address: 4013h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF BUF5 alter interface | | EPINF BUF5 type | | EPINF BUF5direction | EPINF BUF5 maximum packet size[9:7] | | |
| Reset | | 2'd0 | | 2'd0 | | 0 | 3'd0 | | |

USB Device EPINF BUF5 alter interface To set USB device end_point_information_buffer5 alter interface value.
USB Device EPINF BUF5 type To set USB device end_point_information_buffer5 end point type.
[00]:control type; [01]:isochronous type; [10]:Buck type; [11]:interrupt type;
USB Device EPINF BUF5 direction.[0]: Out token. [1]: In token.
USB Device EPINF BUF5 maximum packet size[9:7]: To set USB device end_point_information_buffer5 maximum packet size value.

USB UdcBuffe17_dec Register (Address: 4014h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | EPINF BUF5 maximum packet size[6:0] | | | | | | | -- |
| Reset | | 7'd0 | | | | | | | 0 |

USB Device EPINF BUF5 maximum packet size[6:0]: To set USB device end_point_information_buffer5 maximum packet size value.

USB UdcBuffer18_dec Register (Address: 4015h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | EPINF BUF5 address point[15:8] | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

USB Device EPINF BUF5 address point[15:8]: To indicate USB device end_point_information_buffer5 current address pointer.
USB UdcBuffer19_dec Register (Address: 4016h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | EPINF BUF5 address point[7:0] | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

USB Device EPINF BUF5 address point[7:0]: To indicate USB device end_point_information_buffer5 current address pointer.

USB configure ctrl Register (Address: 4017h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | -- | | | | | | | USB_config_ctrl |
| Reset | | -- | | | | | | | 0 |

USB Device USB_config_ctrl: To set USB device end_point_information_buffer0 ~ end_point_information_buffer5 value.
[0] : disable. [1]: load USB device end_point_information_buffer0 ~ end_point_information_buffer5 value to real controller.

USB EP0 buffer control Register (Address: 4018h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP0 Stall control | EP0 status | | - | EP0 Buffer ready | EP0 Setup token ready | EP0 Out token ready | EP0 In token ready |
| Reset | | -- | | | | | | | |

USB Device EP0 Stall control: To set USB device EP0 stall state.
[0] : normal. [1]: To set EP0 stall
EP0 status[1:0]: To indicate EP0 status. Read only.
[10]: EP0 to be Out state; [01]: EP0 to be In state;
EP0 Buffer ready: To set EP0 buffer is ready or not. Write only.
[0] : EP0 buffer is not ready. [1]: EP0 buffer is ready
EP0 Setup token ready: To indicate EP0 received setup token state. Read only.
[0]: normal. [1]: EP0 setup token transaction completed.
EP0 Out token ready: To indicate EP0 received out token state. Read only.
[0]: normal. [1]: EP0 out token transaction completed.
EP0 In token ready: To indicate EP0 received In token state. Read only.
[0]: normal. [1]: EP0 In token transaction completed.

USB EP0 In-token packet size Register (Address: 4019h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | - | | | | EP0 Buffer In-token packet size | | | |
| Reset | | | | | | 4'd0 | | | |

EP0 Buffer In-token packet size[3:0]: To set valid EP0 buffer packet size before a "In_token" transaction :4'h0 ~ 4h8

USB EP0 Out-token packet size Register (Address: 401ah)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | - | | | | EP0 Buffer Out-token packet size | | | |
| Reset | | | | | | 4'd0 | | | |

EP0 Buffer In-token packet size[3:0]: To indicate valid EP0 buffer packet size after a "Out_token" transaction.

USB EP0 data buffer1 Register (Address: 401bh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP0 data buffer1 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP0 data buffer1: USB EP0 input/output data buffer1.

USB EP0 data buffer2 Register (Address: 401ch)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP0 data buffer2 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP0 data buffer2: USB EP0 input/output data buffer2.

USB EP0 data buffer3 Register (Address: 401dh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|

| Name | R/W | EP0 data buffer3 |
|---|---|---|
| Reset | | 8'd0 |

EP0 data buffer3: USB EP0 input/output data buffer3.

USB EP0 data buffer4 Register (Address: 401eh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Name | R/W | EP0 data buffer4 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP0 data buffer4: USB EP0 input/output data buffer4.

USB EP0 data buffer5 Register (Address: 401fh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Name | R/W | EP0 data buffer5 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP0 data buffer5: USB EP0 input/output data buffer5.

USB EP0 data buffer6 Register (Address: 4020h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Name | R/W | EP0 data buffer6 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP0 data buffer6: USB EP0 input/output data buffer6.

USB EP0 data buffer7 Register (Address: 4021h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Name | R/W | EP0 data buffer7 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP0 data buffer7: USB EP0 input/output data buffer7.

USB EP0 data buffer8 Register (Address: 4022h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Name | R/W | EP0 data buffer8 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP0 data buffer8: USB EP0 input/output data buffer8.

USB EP3 buffer control Register (Address: 4023h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Name | R/W | EP3 Stall control | EP3status | | - | EP3 Buffer ready | - | EP3 Out token ready | EP3 In token ready |
| Reset | | -- | | | | | | | |

USB Device EP3 Stall control: To set USB device EP3 stall state.
[0] : normal. [1]: To set EP3 stall
EP3 status[1:0]: To indicate EP3 status. Read only.
[10]: EP3 to be Out state; [01]: EP3 to be In state;
EP3 Buffer ready: To set EP4 buffer is ready or not. Write only.

[0] : EP3 buffer is not ready. [1]: EP3 buffer is ready
EP3 Out token ready: To indicate EP3 received out token state. Read only.
[0]: normal. [1]: EP3 out token transaction completed.
EP3 In token ready: To indicate EP3 received In token state. Read only.
[0]: normal. [1]: EP3 In token transaction completed.

USB EP3 In-token packet size Register (Address: 4024h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | - EP3 Buffer In-token packet size | | | | | | | |
| Reset | | 58'd0 | | | | | | | |

EP3 Buffer In-token packet size[7:0]: To set valid EP3 buffer packet size before a "In_token" transaction :8'h0 ~ 8h10

USB EP4 Out-token packet size Register (Address: 4025h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | - EP3 Buffer Out-token packet size | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 Buffer In-token packet size[3:0]: To indicate valid EP3 buffer packet size after a "Out_token" transaction:8'h0 ~ 8h10.

USB EP3 data buffer1 Register (Address: 4026h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer1 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer1: USB EP3 input/output data buffer1.

USB EP3 data buffer2 Register (Address: 4027h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer2 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer2: USB EP3 input/output data buffer2.

USB EP3 data buffer3 Register (Address: 4028h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer3 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer3: USB EP3 input/output data buffer3.

USB EP3data buffer4 Register (Address: 4029h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer4 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer4: USB EP3 input/output data buffer4.

USB EP3 data buffer5 Register (Address: 402ah)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer5 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer5: USB EP3 input/output data buffer5.

USB EP3 data buffer6 Register (Address: 402bh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer6 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer6: USB EP3 input/output data buffer6.

USB EP3 data buffer7 Register (Address: 402ch)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer7 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer7: USB EP3 input/output data buffer7.

USB EP3 data buffer8 Register (Address: 402dh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer8 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer8: USB EP3 input/output data buffer8.

USB EP3 data buffer9 Register (Address: 402eh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer9 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer9: USB EP3 input/output data buffer9.

USB EP3 data buffer10 Register (Address: 402fh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer10 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer810: USB EP3 input/output data buffer10.

USB EP3 data buffer11 Register (Address: 4030h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer11 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer11: USB EP3 input/output data buffer11.

USB EP3 data buffer12 Register (Address: 4031h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer12 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer12: USB EP3 input/output data buffer12.

USB EP3 data buffer13 Register (Address: 4032h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer13 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer13: USB EP3 input/output data buffer13.

USB EP3 data buffer14 Register (Address: 4033h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer14 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer14: USB EP3 input/output data buffer14.

USB EP3 data buffer15 Register (Address: 4034h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer15 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer15: USB EP3 input/output data buffer15.

USB EP3 data buffer16 Register (Address: 4035h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP3 data buffer16 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP3 data buffer16: USB EP3 input/output data buffer16.

USB EP4 buffer control Register (Address: 4036h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 Stall control | EP4 status | | - | EP4 Buffer ready | - | EP4 Out token ready | EP4 In token ready |
| Reset | | -- | | | | | | | |

USB Device EP4 Stall control: To set USB device EP4 stall state.

[0] : normal. [1]: To set EP5stall
EP4 status[1:0]: To indicate EP4 status. Read only.
[10]: EP4 to be Out state; [01]: EP4 to be In state;
EP4 Buffer ready: To set EP4 buffer is ready or not. Write only.
[0]: EP4 buffer is not ready. [1]: EP4 buffer is ready
EP4 Out token ready: To indicate EP4 received out token state. Read only.
[0]: normal. [1]: EP4 out token transaction completed.
EP5 In token ready: To indicate EP5 received In token state. Read only.
[0]: normal. [1]: EP4 In token transaction completed.

USB EP4 In-token packet size Register (Address: 4037h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | - EP4 Buffer In-token packet size | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 Buffer In-token packet size[3:0]: To set valid EP4 buffer packet size before a "In_token" transaction :8'h0 ~ 4h10

USB EP4 Out-token packet size Register (Address: 4038h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | - EP4 Buffer Out-token packet size | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 Buffer In-token packet size[3:0]: To indicate valid EP5 buffer packet size after a "Out_token" transaction :8'h0 ~ 4h10

USB EP4 data buffer1 Register (Address: 4039h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer1 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer1: USB EP4 input/output data buffer1.

USB EP4 data buffer2 Register (Address: 403ah)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer2 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer2: USB EP4 input/output data buffer2.

USB EP4 data buffer3 Register (Address: 403bh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer3 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer3: USB EP4 input/output data buffer3.

USB EP4 data buffer4 Register (Address: 403ch)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer4 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer4: USB EP4 input/output data buffer4.

USB EP4 data buffer5 Register (Address: 403dh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer5 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer5: USB EP4 input/output data buffer5.

USB EP4 data buffer6 Register (Address: 403eh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer6 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer6: USB EP4 input/output data buffer6.

USB EP4 data buffer7 Register (Address: 403fh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer7 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer7: USB EP4 input/output data buffer7.

USB EP4 data buffer8 Register (Address: 4040h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer8 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer8: USB EP4 input/output data buffer8.

USB EP4 data buffer9 Register (Address: 4041h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer9 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer9: USB EP4 input/output data buffer9

USB EP4 data buffer10 Register (Address: 4042h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer10 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer10: USB EP4 input/output data buffer10.
USB EP4 data buffer11 Register (Address: 4043h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer11 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer11: USB EP4 input/output data buffer11.

USB EP4 data buffer12 Register (Address: 4044h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer12 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer12: USB EP4 input/output data buffer12.

USB EP4 data buffer13 Register (Address: 4045h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer13 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer13: USB EP4 input/output data buffer13.

USB EP4 data buffer14 Register (Address: 4046h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer14 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer14: USB EP4 input/output data buffer14.

USB EP4 data buffer15 Register (Address: 4047h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer15 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer15: USB EP4 input/output data buffer15.

USB EP4 data buffer16 Register (Address: 4048h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP4 data buffer16 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP4 data buffer16: USB EP4 input/output data buffer16.

USB EP5 buffer control Register (Address: 4049h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 Stall control | EP5 status | | - | EP5 Buffer ready | - | EP5 Out token ready | EP5 In token ready |
| Reset | | -- | | | | | | | |

USB Device EP5 Stall control: To set USB device EP5 stall state.

[0] : normal. [1]: To set EP5stall
EP5 status[1:0]: To indicate EP5 status. Read only.
[10]: EP5 to be Out state; [01]: EP5 to be In state;
EP5 Buffer ready: To set EP5 buffer is ready or not. Write only.
[0] : EP5 buffer is not ready. [1]: EP5 buffer is ready
EP5 Out token ready: To indicate EP5 received out token state. Read only.
[0]: normal. [1]: EP3 out token transaction completed.
EP5 In token ready: To indicate EP5 received In token state. Read only.
[0]: normal. [1]: EP5 In token transaction completed.

USB EP5In-token packet size Register (Address: 404ah)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | - EP5 Buffer In-token packet size | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 Buffer In-token packet size[7:0]: To set valid EP5 buffer packet size before a "In_token" transaction :8'h0 ~ 4h10

USB EP5 Out-token packet size Register (Address: 404bh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | - EP5 Buffer Out-token packet size | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 Buffer In-token packet size[7:0]: To indicate valid EP5 buffer packet size after a "Out_token" transaction:8'h0 ~ 4h10

USB EP5 data buffer1 Register (Address: 404ch)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer1 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer1: USB EP5 input/output data buffer1.

USB EP5 data buffer2 Register (Address: 404dh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5data buffer2 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer2: USB EP5 input/output data buffer2.

USB EP5 data buffer3 Register (Address: 404eh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer3 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer3: USB EP5 input/output data buffer3.

USB EP5 data buffer4 Register (Address: 404fh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer4 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer4: USB EP5 input/output data buffer4.

USB EP5 data buffer5 Register (Address: 4050h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer5 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer5: USB EP5 input/output data buffer5.

USB EP5 data buffer6 Register (Address: 4051h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer6 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer6: USB EP5 input/output data buffer6.

USB EP5 data buffer7 Register (Address: 4052h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer7 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer7: USB EP5 input/output data buffer7.

USB EP5 data buffer8 Register (Address: 4053h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer8 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer8: USB EP5 input/output data buffer8.

USB EP5 data buffer9 Register (Address: 4054h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer9 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer9: USB EP5 input/output data buffer9.

USB EP5 data buffer10 Register (Address: 4055h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer10 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer10: USB EP5 input/output data buffer10.
USB EP5 data buffer11 Register (Address: 4056h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer11 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer11: USB EP5 input/output data buffer11.

USB EP5 data buffer12 Register (Address: 4057h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer12 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer12: USB EP5 input/output data buffer12.

USB EP5 data buffer13 Register (Address: 4058h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer13 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer13: USB EP5 input/output data buffer13.

USB EP5 data buffer14 Register (Address: 4059h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer14 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer14: USB EP5 input/output data buffer14.

USB EP5 data buffer15 Register (Address: 405ah)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer15 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer15: USB EP5 input/output data buffer15.

USB EP5 data buffer16 Register (Address: 405bh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | EP5 data buffer16 | | | | | | | |
| Reset | | 8'd0 | | | | | | | |

EP5 data buffer16: USB EP5 input/output data buffer16.

USB Interrupt Register (Address: 405ch)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | EP0 interrupt | EP1 interrupt | EP2 interrupt | EP4 interrupt | EP5 interrupt | EP3 interrupt | Suspend interrupt | reserved |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

EP0 interrupt: To indicate USB EP0 interrupt occurred or not.

[0]: normal [1]: EP0 interrupt occurred.
[0]: normal [1]: EP2 interrupt occurred.
EP4 interrupt: To indicate USB EP4 interrupt occurred or not.
[0]: normal [1]: EP4 interrupt occurred.
EP5 interrupt: To indicate USB EP5 interrupt occurred or not.
[0]: normal [1]: EP5 interrupt occurred.
EP3 interrupt: To indicate USB EP3 interrupt occurred or not.
[0]: normal [1]: EP3 interrupt occurred.
Suspend interrupt: To indicate USB suspend interrupt occurred or not.
[0]: normal [1]: suspend interrupt occurred.
Resume interrupt: To indicate USB resume interrupt occurred or not.
[0]: normal [1]: resume interrupt occurred.

USB Interrupt mask Register (Address: 405dh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Name | R/W | EP0 interrupt mask | Reserved | Reserved | EP4 interrupt mask | EP5 interrupt mask | EP3 interrupt mask | Suspend interrupt mask | Reserved |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

EP0 interrupt mask: To mask USB EP0 interrupt. [0]: To disable EP0 interrupt [1]: EP0 interrupt enable.
EP4 interrupt mask: To mask USB EP4 interrupt. [0]: To disable EP4 interrupt [1]: EP4 interrupt enable.
EP5 interrupt mask: To mask USB EP5 interrupt. [0]: To disable EP5 interrupt [1]: EP5 interrupt enable.
EP3 interrupt mask: To mask USB EP3 interrupt. [0]: To disable EP3 interrupt [1]: EP3 interrupt enable.
Suspend interrupt mask: To mask USB suspend interrupt. [0]: To disable suspend interrupt [1]: suspend interrupt enable.
Resume interrupt mask: To mask USB resume interrupt.[0]: To disable resume interrupt [1]: resume interrupt enable.

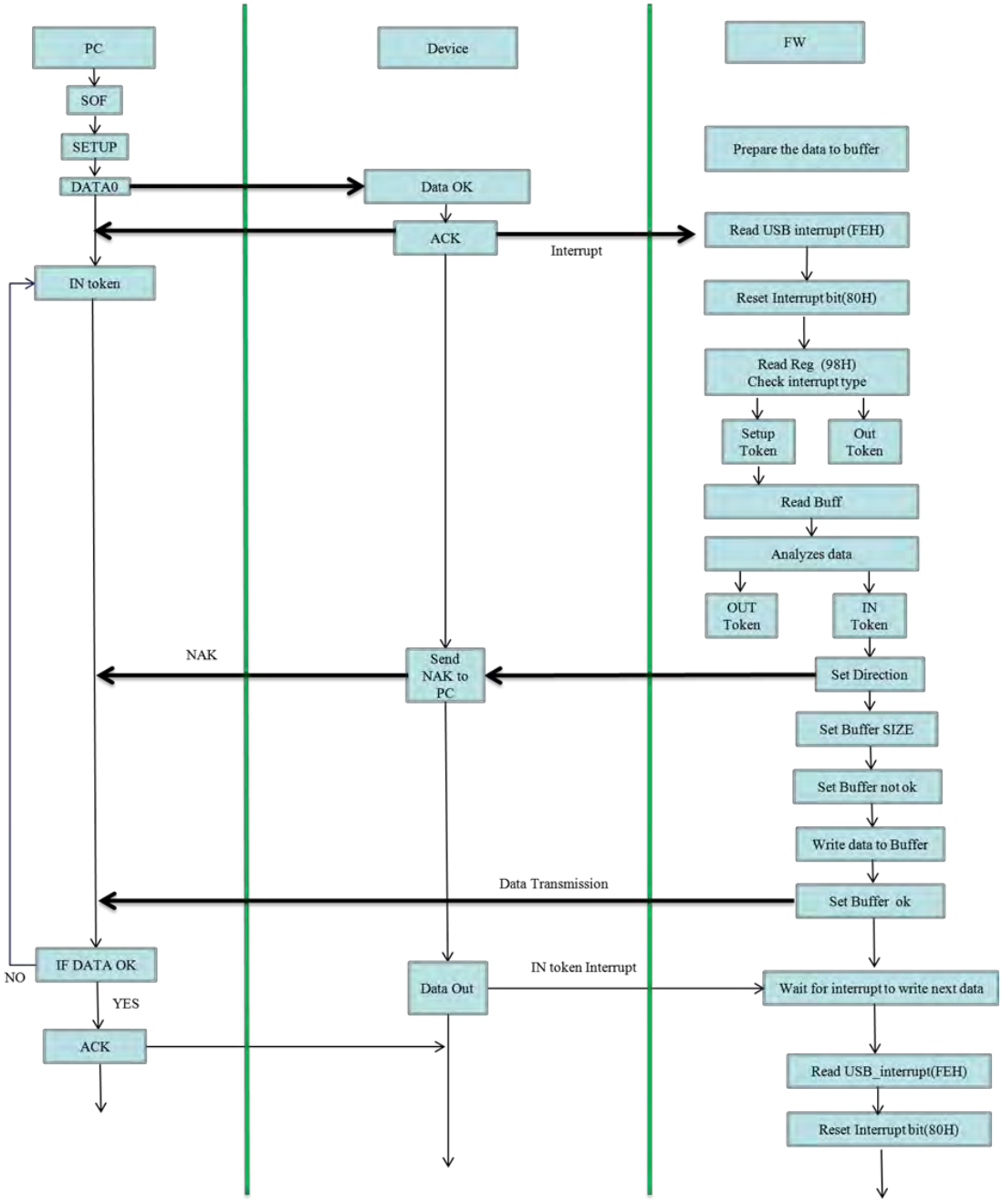
USB PHY Setting Register (Address: 405eh)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Name | R/W | Reserved | USB PHY suspend | USB PHY Speed | USB PHY mode | USB_PHY_ ENR | USB_PHY_SR[2:0] | | |
| Reset | | 0 | 0 | 1 | 1 | 0 | 3'b111 | | |

USB PHY suspend: [1]: suspend [0]:normal.
USB PHY Speed: [1]: FS driver*8 [0]0: LS driver*2
USB PHY mode: [1]: differential [0]: single.
USB_PHY_ENR: [1]:Rs = 36ohm; [0]: RS=45ohm.
USB_PHY_SR[2:0]: DP pull-high Rup control. [000]:Rup=1.279K; [001]:Rup=1.393K; [010]:Rup=1.504K; [011]:Rup=1.613K; [100]:Rup=1.718K; other: Rup=open;

## 11.2 USB Configuration

In usual, A8108 USB controller configure EP0 to be control type for basic USB control, EP3 for interrupt type for HID control. EP4 and EP5 are also configured to be interrupt type and reserved for wireless keyboard and mouse application. After USB controller configuration, A8108 could receive SIE command and automatically response ACK/NAK to USB host. At the same time, USB controller will generate interrupt int3 to A8108 MCU for firmware application. A8108 MCU could read SIE command from USB EP data buffer and response properly data to USB host. The MCU only need to handle SIE command and HID control interface. The firmware flow is as the following:



# 12. A8108 RF

A8108 integrate 2.4 Ghz GFSK transceiver and use Strobe control register (0800h) to control RF state. There are 6 Strobe commands to control internal state machine for RF operations. These modes include Sleep mode, Idle mode, Standby mode, PLL mode, RX mode and TX mode. There are 64Bytes FIFO for data transmitting, receiving. Sleep timer is used for WOR (Wake On Rx) and time-slotted mode operation.

## 12.1 Packet Format of FIFO mode

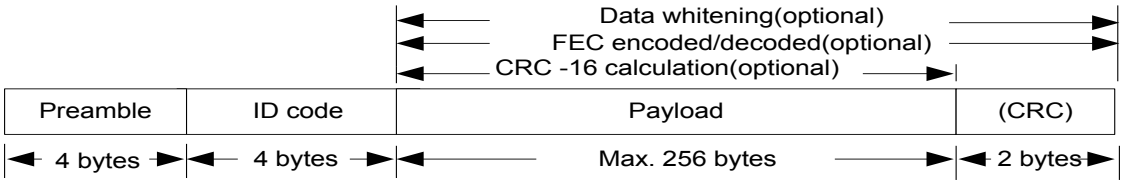
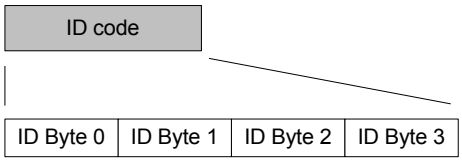



Figure 21.1 Packet Format of FIFO mode




## 12.2 Transceiver Frequency

A8108 is a half-duplex transceiver with embedded PA and LNA. The receiver is a low-IF architecture consisting of a LNA, down conversion mixers, polyphase channel filters and IF limiting amplifiers with RSSI. The transmitter is direct modulation architecture with 6 dBm maximum output power and 35 dB power control range. For TX or RX frequency setting, user just needs to set up one register, CHN (080Eh), for frequency agility.

A8108's main PLL features are:

- Frantional-N to generate RX/TX frequencies for all ISM 2.4 GHz channels
- Autonomous calibration loops for stable operation within the operating range
- Fast PLL settling to support frequency hopping

During receive operation, the frequency synthesizer works as a local oscillator. During transmit operation, the voltage-controlled oscillator (VCO) is directly modulated to generate the RF transmit signal. The frequency synthesizer is implemented as a fractional-N PLL.

$F_{LO}$ **= 2400 + (CHN x 0.5) in [MHz],** where CHN is the channel number, addr 0Eh.

A8108's LO frequency $F_{LO} = F_{LO\_BASE} + F_{OFFSET}$. Therefore, A8108 is very easy to implement frequency hopping by **ONE register setting, (CHN, 0Eh).** In general, user can plan the wanted channels by a CHN Look-Up-Table between master and slaves for two-way frequency hopping. Below is the LO frequency block diagram.

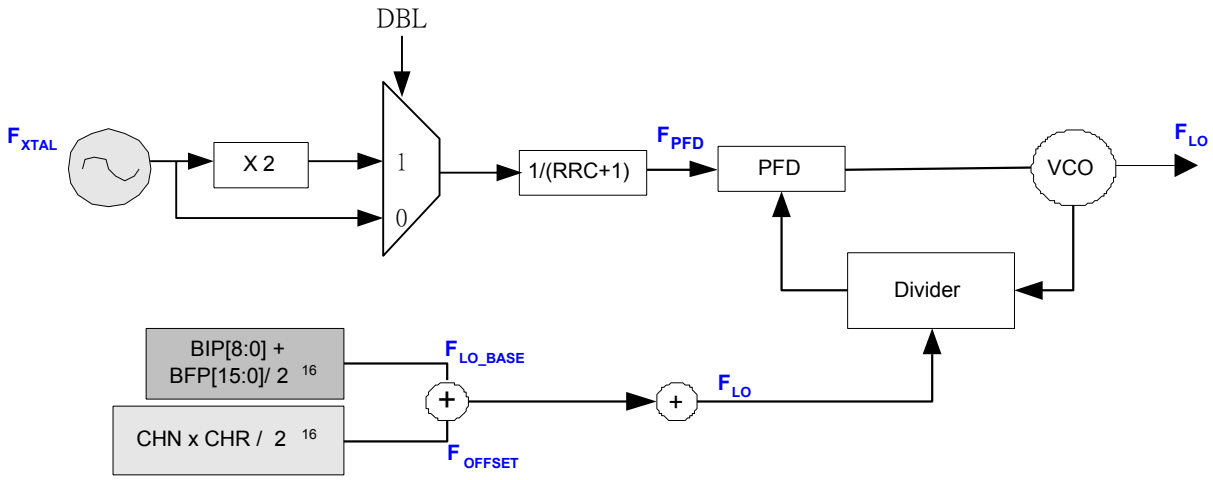



Figure 12.1 Block Diagram of Local Oscillator

### 12.3 RF Clock

The master clock of A8108 ($F_{CSCK}$= 32/64 MHz) is generated by the PLL clock generator which reference frequency ($F_{CGR}$= 2/4 MHz) is derived from frequency divider of crystal oscillator.

$F_{CGR} = \frac{F_{XREF}}{(GRC[3:0]+1)}$, where GRC [3:0] (0Ch) is the divide number to get $F_{CGR}$ from crystal oscillator.

Below is block diagram of system clock where $F_{XTAL}$ is the crystal frequency. User can set XS, GRC, CGS to get $F_{CSCK}$ = 32/64MHz. $F_{XREF}$ is a reference clock to generate $F_{CGR}$ and $F_{SPLL}$ . After delay circuitry, $F_{CSCK}$ (32/64MHz) is derived. And with BWS setting, the system clock $F_{SYCK}$ can be fixed to 8MHz.

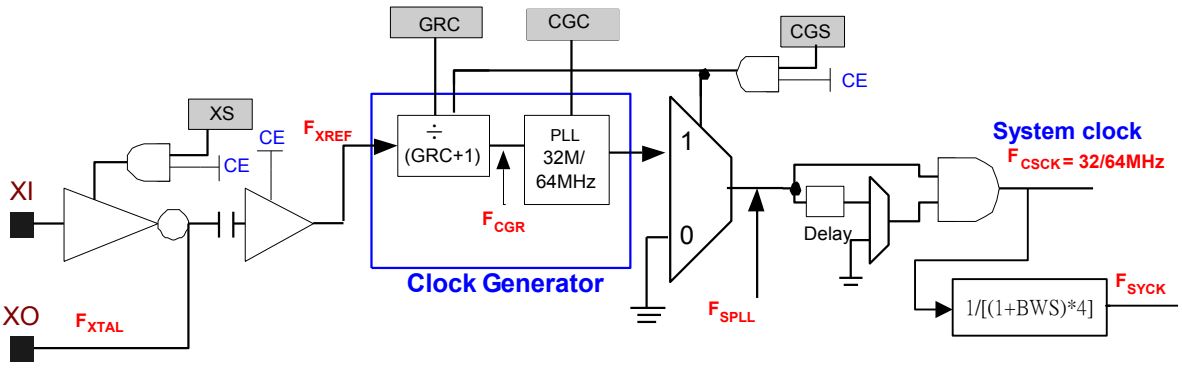



Figure 12.2 RF Clock Block Diagram

Below is the setting table of system clock for both 1MHz and 2MHz data rate

| Data rate | $F_{XTAL}$ | $F_{XREF}$ | $F_{CGR}$ | GRC [3:0] | XS | CGS | CGC | BWS | $F_{CSCK}$ | $F_{SYCK}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 1M | 16 MHz | 16 MHz | 2 MHz | [0111] | 1 | 1 | 0 | 0 | 32MHz | 8MHz |
| 2M | 16 MHz | 16 MHz | 2 MHz | [0011] | 1 | 1 | 1 | 1 | 64MHz | 8MHz |

### 12.4 LO Frequency Setting

To set up 2.4GHz LO Frequency ($F_{LO,}$), user can refer to below 4 steps.

1. Set the base frequency (**$F_{LO\_BASE}$**) by PLL Register II (080Fh) and III (0810h).
Recommend to set $F_{LO\_BASE}$ ~ 2400.001MHz.

2. Set channel step $F_{CHSP}$ = 500KHz by PLL Register II (080Fh).

3. Set CHN [7:0] to get offset frequency by PLL Register I (080Eh).
$F_{OFFSET}$ = CHN [7:0] * $F_{CHSP}$

4. LO frequency is equal to base frequency plus offset frequency.
**$F_{LO} = F_{LO\_BASE} + F_{OFFSET}$**


## 12.5 RF Register Table

### 12.5.1 Mode Register (Address: 0x800h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode | W | RESETN | FWPRN | FRPRN | ADC12RN | -- | BFCRN | -- | -- |
| | R | - | FECF | CRCF | CER | XER | PLLER | TRSR | TRER |
| Reset | | -- | -- | -- | -- | -- | -- | -- | -- |

**RESETN (CRN): Write to this register by 0x00 to issue reset command, then it is auto clear.**
**FWPRN (FWCRN): FIFO Write Point Software Reset.**
**FRPRN (FWCRN): FIFO Read Point Software Reset.**
**ADC12RN: 12-bits ADC Software Reset.**
**BFCRN: IF Filter Bank Calibration Software Reset.**

**FECF: FEC flag.**
[0]: FEC pass. [1]: FEC error.
**CRCF: CRC flag.**
[0]: CRC pass. [1]: CRC error.
**CER: RF chip enable status.**
[0]: RF chip is disabled. [1]: RF chip is enabled.
**XER: Internal crystal oscillator enabled status.**
[0]: Crystal oscillator is disabled. [1]: Crystal oscillator is enabled.
**PLLER: PLL enabled status.**
[0]: PLL is disabled. [1]: PLL is enabled.
**TRSR: TRX Status Register.**
[0]: RX state. [1]: TX state.
Serviceable if TRER=1 (TRX is enable).
**TRER: TRX state enabled status.**
[0]: TRX is disabled. [1]: TRX is enabled.

### 12.5.2 Mode Control Register 1 (Address: 0x801h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|

| MODEC1 | W | STRB7 | STRB6 | STRB5 | STRB4 | STRB3 | STRB2 | STRB1 | STRB0 |
|---|---|---|---|---|---|---|---|---|---|
| | R | ARCWTR | P_CKO | P_IRQ1O | P_IRQ2O | FPF | | | |
| Reset | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**STRB[7:0]: Strobe command register.**
[80]: Sleep mode.
[90]: Idle mode.
[A0]: Standby mode.
[B0]: PLL mode.
[C0]: TX mode.
[D0]: RX mode.
Reverse for other settings.

**ARCWTR: Read ARCWTR output signal.**
**P_CKO: Read P_CKO pin output signal.**
**P_IRQ1O: Read P_IRQ1O pin output signal.**
**P_IRQ2O: Read P_IRQ2O pin output signal.**
**FPF: Read FIFO pointer flag output signal.**

### 12.5.3 Mode Control Register 2 (Address: 0x802h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode Control I | R | DDPC | ARSSI | AIF | DFCD | WWSE | FMT | FMS | ADCM |
| | W | DDPC | ARSSI | AIF | CD | WWSE | FMT | FMS | ADCM |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**DDPC (Direct mode data pin control): Direct mode modem data can be accessed via SDIO pin when this register is enabled.**
**[0]:** Disable. **[1]:** Enable.
**ARSSI: Auto RSSI measurement while entering RX mode.**
**[0]:** Disable. **[1]:** Enable.
**AIF (Auto IF Offset): RF LO frequency will auto offset one IF frequency while entering RX mode.**
**[0]:** Disable. **[1]:** Enable.
**CD / DFCD:**
**DFCD (Data Filter by CD): The received package will be filtered out if Carrier Detector signal is inactive.**
**[0]:** Disable. **[1]:** Enable.
**CD (Read): Carrier detector signal.**
**[0]:** Input power below threshold. **[1]:** Input power above threshold.
**WWSE: Reserved for internal usage only. Shall be set to [0].**
**FMT: Reserved for internal usage only. Shall be set to [0].**
**FMS: Direct/FIFO mode select.**
**[0]:** Direct mode. **[1]:** FIFO mode.
**ADCM: ADC measurement enable (Auto clear when done).**
**[0]:** Disable measurement or measurement finished. **[1]:** Enable measurement.

| ADCM | A8108 @ Standby mode | A8108 @ RX mode |
|---|---|---|
| [0] | Disable ADC | Disable ADC |
| [1] | Measure temperature, external Analog Digital Convert | Measure RSSI, carrier detect |

### 12.5.4 Calibration Control Register (Address: 0x803h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode Control II | R/W | -- | -- | -- | -- | RSSC | VCC | VBC | FBC |
| Reset | | -- | -- | -- | -- | 0 | 0 | 0 | 0 |

**VCC: VCO Current calibration enable (Auto clear when done).**
**[0]:** Disable. **[1]:** Enable.
**VBC: VCO Bank calibration enable (Auto clear when done).**
**[0]:** Disable. **[1]:** Enable.
**FBC: IF Filter Bank calibration enable (Auto clear when done).**
**[0]:** Disable. **[1]:** Enable.

**RSSC: RSSI calibration enable (Auto clear when done).**
**[0]:** Disable. **[1]:** Enable.

### 12.5.5 FIFO Register I (Address: 0x804h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| FIFO I | W | FEP7 | FEP6 | FEP5 | FEP4 | FEP3 | FEP2 | FEP1 | FEP0 |
| Reset | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

**FEP [7:0]: FIFO End Pointer for TX FIFO and Rx FIFO.**

### 12.5.6 FIFO Register II (Address: 0x805h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| FIFO II | W | FPM1 | FPM0 | PSA5 | PSA4 | PSA3 | PSA2 | PSA1 | PSA0 |
| Reset | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**FPM [1:0]: FIFO Pointer Margin**
**PSA [5:0]: Used for Segment FIFO.**

### 12.5.7 RC OSC Register I (Address: 0x806h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RC OSC I | W | WWS_SL 7 | WWS_SL 6 | WWS_SL5 | WWS_SL4 | WWS_SL3 | WWS_SL2 | WWS_SL1 | WWS_SL0 |
| | R | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**WWS_SL [9:0]: 10-bits WWS_SL Timer for TWWS Function (7.8ms ~ 7.99s).**
**WWS_SL [9:0] are from address (0x806h) and (0x807h).**

### 12.5.8 RC OSC Register II (Address: 0x807h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RC OSC II | W | WWS_SL9 | WWS_SL8 | WWS_AC5 | WWS_AC4 | WWS_AC3 | WWS_AC2 | WWS_AC1 | WWS_AC0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**WWS_SL [9:0]: 10-bits WWS_SL Timer for TWWS Function (7.8ms ~ 7.99s).**
**WWS_SL [9:0] are from address (0x806h) and (0x807h).**
**WWS_AC [8:0]: 9-bits WWS_AC Timer for TWWS Function (244us ~ 15.6ms).**

### 12.5.9 RC OSC Register III (Address: 0x808h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RC OSC III | W | BBCKS1 | BBCKS0 | WWS_AC8 | WWS_AC7 | WWS_AC6 | RCTS | TSEL | TWOR_E |
| Reset | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**BBCKS [1:0]: Clock select for internal digital block.**
**[00]:** $F_{SYCK}$ / 8. **[01]:** $F_{SYCK}$ / 16. **[10]:** $F_{SYCK}$ / 32. **[11]:** $F_{SYCK}$ / 64.
**$F_{SYCK}$ is A8108's System clock. Refer to chapter 18 for details.**
**RCOSC_E: RC-oscillator enable.**
**[0]:** Disable. **[1]:** Enable.
**RCTS: Internal / External 32.768k Hz oscillator selection.**
**[0]:** Internal. **[1]:** External.
**TSEL: Timer select for TWWS function.**
**[0]:** Use WWS_AC. **[1]:** Use WWS_SL.
**TWWS_E: Enable TWWS function.**
**[0]:** Disable. **[1]:** Enable.

### 12.5.10 CKO Pin Control Register (Address: 0x809h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| CKO Pin Control | W | ECKOE | CKOS3 | CKOS2 | CKOS1 | CKOS0 | CKOI | WAKEBBIE | INTT1IE |
| Reset | | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |

**ECKOE: External Clock Output Enable for CKOS [3:0]= [0100] ~ [0111].**
**[0]:** Disable. **[1]:** Enable.
**CKOS [3:0]: CKO pin output select.**
**[0000]:** DCK (TX data clock).
**[0001]:** RCK (RX recovery clock).
**[0010]:** FPF (FIFO pointer flag).
**[0011]:** EOP, EOVBC, EOFBC, EOADC, EOVCC, OKADC (Internal usage only).
**[0100]:** External clock output= $F_{SYCK}$.
**[0101]:** External clock output / 2= $F_{SYCK}$ / 2.
**[0110]:** External clock output / 4= $F_{SYCK}$ / 4.
**[0111]:** External clock output / 8= $F_{SYCK}$ / 8.
**[1000]:** WCK.
**[1001]:** RCOSC.
**[1010]:** EOADC.
**[1011]:** OKADC.
**[1100]**: TMRCK_OVF(Timer clock)
**[1101]:** Reserved.
**[11xx]:** Reserved.
**CKOI: CKO pin output signal invert.**
**[0]:** Non-inverted output. **[1]:** Inverted output.
**WAKEBBIE: Wake BB interrupt enable.**
**[0]:** Disable. **[1]:** Enable.
**INTT1IE: ARCWTR interrupt enable.**
**[0]:** Disable. **[1]:** Enable.

### 12.5.11 GIO1 Pin Control Register I (Address: 0x80Ah)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| GIO1 Pin Control I | W | -- | -- | GIO1S3 | GIO1S2 | GIO1S1 | GIO1S0 | GIO1I | GIO1OE |
| Reset | | -- | -- | 0 | 0 | 0 | 0 | 0 | 1 |

**GIO1S [3:0]: GIO1 pin function select.**

| GIO1S [3:0] | TX state | RX state |
|---|---|---|
| [0000] | WTR (Wait until TX or RX finished) | |
| [0001] | EOAC (end of access code) | FSYNC (frame sync) |
| [0010] | TMEO (TX modulation enable) | CD (carrier detect) |
| [0011] | Preamble Detect Output (PMDO) | |
| [0100] | MCU wakeup signal (TWWS) | |
| [0101] | In phase demodulator input (DMII) | |
| [0110] | Reserved | |
| [0111] | TRXD In/Out (Direct mode) | |
| [1000] | RXD (Direct mode) | |
| [1001] | TXD (Direct mode) | |
| [1010] | In phase demodulator external input (EXDI0) | |
| [1011] | External FSYNC input in RX direct mode | |
| [1100] | INC | |
| [1101] | FPF | |
| [1110] | MCU_BB_INT5 | |
| [1111] | PDN_TX | |

**GIO1I: GIO1 pin output signal invert.**
**[0]:** Non-inverted output. **[1]:** Inverted output.
**GIO1OE: GIO1pin output enable.**
**[0]:** High Z. **[1]:** Enable.

### 12.5.12 GIO2 Pin Control Register II (Address: 0x80Bh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| GIO2 Pin Control II | W | -- | -- | GIO2S3 | GIO2S2 | GIO2S1 | GIO2S0 | GIO2I | GIO2OE |
| Reset | | -- | -- | 0 | 1 | 0 | 0 | 0 | 1 |

**GIO2S [3:0]: GIO2 pin function select.**

| GIO2S | TX state | RX state |
|---|---|---|
| [0000] | WTR (Wait until TX or RX finished) | |
| [0001] | EOAC (end of access code) | FSYNC (frame sync) |
| [0010] | TMEO (TX modulation enable) | CD (carrier detect) |
| [0011] | Preamble Detect Output (PMDO) | |
| [0100] | MCU wakeup signal (TWWS) | |
| [0101] | Quadrature phase demodulator input (DMIQ) | |
| [0110] | Reserved | |
| [0111] | TRXD In/Out (Direct mode) | |
| [1000] | RXD (Direct mode) | |
| [1001] | TXD (Direct mode) | |
| [1010] | Quadrature phase demodulator external input (EXDI1) | |
| [1011] | External FSYNC input in RX direct mode | |
| [1100] | DEC | |
| [1101] | FPF | |
| [1110] | PDN_RX | |
| [1111] | PDN_TX | |

**GIO2I: GIO2 pin output signal invert.**
**[0]:** Non-inverted output. **[1]:** Inverted output.
**GIO2OE: GIO2 pin Output Enable.**
**[0]:** High Z. **[1]:** Enable.

### 12.5.13 Clock Register (Address: 0x80Ch)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Clock | R/W | GRC3 | GRC2 | GRC1 | GRC0 | CSC1 | CSC0 | CGS | XS |
| Reset | | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

**GRC [3:0]: Clock generation reference counter.**

| GRC[3:0] | Note |
|---|---|
| Don't care | Recommend when CGS = 0 |
| $F_{XTAL}$ x (DBL+1) / (GRC+1) = 2M | When CGS = 1 |

**CSC [1:0]: system clock $F_{SYCK}$ divider select.**
[00]: $F_{CSCK}$ / 1. [01]: $F_{CSCK}$ / 2. [10]: $F_{CSCK}$ / 2. [11]: $F_{CSCK}$ / 4.
**CSC [1:0]: system clock $F_{SYCK}$ divider select.**

| CSC [1:0] | System Clock $F_{SYCK}$ | Note |
|---|---|---|
| 00 | $F_{MCLK}$ | $F_{SYCK}$ is used to determine<br>Data rate (0Dh)<br>ADC clock (1Dh)<br>Internal digital clock (08h)<br>CKO pin (09h) |
| 01 (Recommend) | $F_{MCLK}$ / 2 | |
| 10 | $F_{MCLK}$ / 2 | |
| 11 | $F_{MCLK}$ / 4 | |

**CGS: Clock generator enable. Recommend CGS = [0]**
[0]: Disable. [1]: Enable.

| CGS = 0 (recommend) | CGS = 1 |
|---|---|
| Disable internal 32MHz PLL clock | $F_{MCLK}$ = 32 MHz |

**XS: Crystal oscillator select.**
[0]: Use external clock. [1]: Use external crystal.

| Master clock frequency | CGS = 0 | CGS = 1 |
|---|---|---|
| DBL = 0 | Crystal frequency | 32 MHz |
| DBL = 1 | 2*crystal frequency | 32 MHz |

### 12.5.14 Data Rate Register (Address: 0x80Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Data Rate | R/W | SDR7 | SDR6 | SDR5 | SDR4 | SDR3 | SDR2 | SDR1 | SDR0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SDR [7:0]: Data rate division selection.**
**Data rate = $F_{SYCK}$ / (32*(SDR [7:0]+1)). Refer to chapter 13 for details.**

### 12.5.15 PLL Register I (Address: 0x80Eh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL I | R/W | CHN7 | CHN6 | CHN5 | CHN4 | CHN3 | CHN2 | CHN1 | CHN0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**CHN [7:0]: LO channel number select.**

### 12.5.16 PLL Register II (Address: 0x80Fh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL II | R | DBL | RRC1 | RRC0 | CHR3 | CHR2 | CHR1 | CHR0 | IP8 |
| | W | DBL | RRC1 | RRC0 | CHR3 | CHR2 | CHR1 | CHR0 | BIP8 |
| Reset | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

**DBL: Crystal frequency doubler selection.**
**[0]:** Disable. $F_{XREF} = F_{XTAL}$. **[1]:** Enable. $F_{XREF} = 2 * F_{XTAL}$.
**RRC [1:0]: RF PLL reference counter setting.**
**CHR [3:0]: PLL channel step setting.**

### 12.5.17 PLL Register III (Address: 0x810h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL III | R | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |
| | W | BIP7 | BIP6 | BIP5 | BIP4 | BIP3 | BIP2 | BIP1 | BIP0 |
| Reset | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |

**BIP [8:0]: LO base frequency integer part setting.**
**BIP [8:0] are from address (0Fh) and (10h).**
**IP [8:0]: LO frequency integer part value.**
**IP [8:0] are from address (0Fh) and (10h).**

### 12.5.18 PLL Register IV (Address: 0x811h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL IV | R | RAC15 | RAC14 | RAC13 | RAC12 | RAC11 | RAC10 | RAC9 | RAC8 |
| | W | BFP15 | BFP14 | BFP13 | BFP12 | BFP11 | BFP10 | BFP9 | BFP8 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 12.5.19 PLL Register V (Address: 0x812h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL V | R | RAC7 | RAC6 | RAC5 | RAC4 | RAC3 | RAC2 | RAC1 | RAC0 |
| | W | BFP7 | BFP6 | BFP5 | BFP4 | BFP3 | BFP2 | BFP1 | BFP0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

**BFP [15:0]: LO base frequency fractional part setting.**
**BFP [15:0] are from address (11h) and (12h).**
**RAC [15:0] (Read): Auto Frequency compensation value (if AFC (18h) =1).**

**The RAC values are showed in the following table.**

| | |
|---|---|
| {PRS(2Dh), AFC(18h)} | RAC **[15:0]** |
| 1x | PLLFF **[15:0]** |
| 01 | {0, ACO **[14:0]**} |
| 00 | {SYNCF, AC **[14:0]**} |

**PLLFF [15:0]: the fractional part in PLL.**
**ACO [14:0] is the accumulated frequency compensated value.**
**SYNCF is the SYNC word detection flag. [0]: not detected, [1]: detected.**
**AC [14:0] is the updated frequency compensated value.**
**FP [15:0] (Read): LO frequency fractional part setting.**

### 12.5.20 TX Register I (Address: 0x813h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TX I | W | TXSM1 | TXSM0 | TXDI | TME | FS | FDP2 | FDP1 | FDP0 |
| Reset | | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

**TXSM [1:0]: Moving average for non-filter select.**
[00]: not average. [01]: 2 bit average. [10]: 4 bit average. [11]: 8 bit average
**TXDI: TX data invert. Recommend TXDI = [0].**
[0]: Non-invert. [1]: Invert.
**TME: TX modulation enable.**
[0]: Disable. [1]: Enable.
**FS: Filter select.**
**The filter shape is gaussian filter (BT=0.7).**
[0]: disable. [1]: enable.
**FDP [2:0]: Frequency deviation power setting.** Refer to control register (15h).

### 12.5.21 TX Register II (Address: 0x814h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TX II | W | FD7 | FD6 | FD5 | FD4 | FD3 | FD2 | FD1 | FD0 |
| Reset | | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |

**FD [7:0]: Frequency deviation setting.**
**Frequency deviation $F_{DEV} = F_{PFD} * 2^{FDP\ [2:0]} * FD\ [7:0] / 2^{20}$**
**Where $F_{PFD}$, the PLL comparison frequency, is equal to crystal frequency * (DBL+1)/ ((RRC [1:0]+1).**

### 12.5.22 Delay Register I (Address: 0x815h)

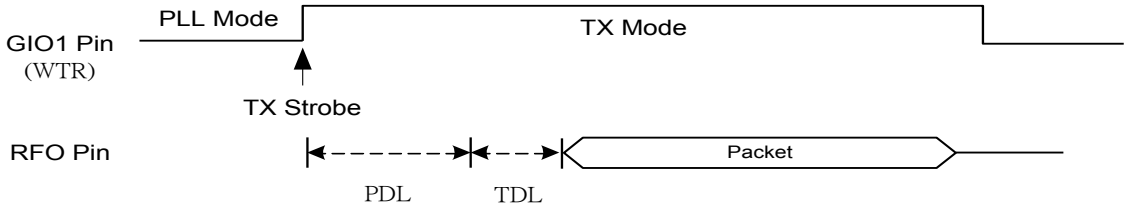
| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Delay | W | DPR2 | DPR1 | DPR0 | TDL1 | TDL0 | PDL2 | PDL1 | PDL0 |
| Reset | | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

**DPR [2:0]: Delay scale. Recommend DPR = [000].**
**TDL [1:0]: Delay for TX settling from WPLL to TX.**
**Delay= 20 * (TDL [1:0]+1)*(DPR [2:0]+1) us.**

| DPR [2:0] | TDL [1:0] | WPLL to TX | Note |
|---|---|---|---|
| 000 | 00 | 20 us | |
| 000 | 01 | 40 us | |
| 000 | 10 | 60 us | **Recommend** |
| 000 | 11 | 80 us | |

**PDL [2:0]: Delay for TX settling from PLL to WPLL.**
**Delay= 10+20 * (PDL [2:0]+1)*(DPR [2:0]+1) us.**

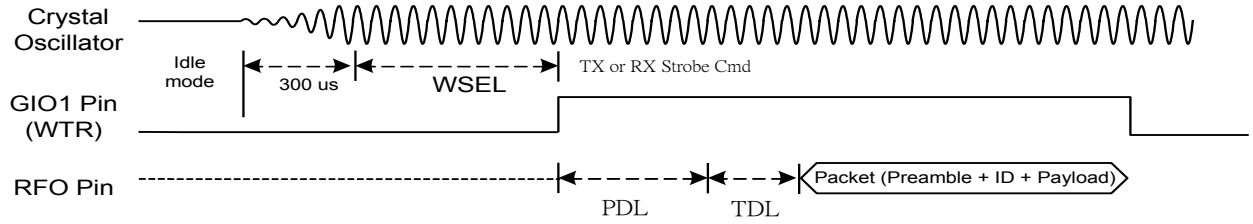
| DPR [2:0] | PDL [2:0] | PLL to WPLL (LO freq. fixed) | PLL to WPLL (LO freq changed) | Note |
|---|---|---|---|---|
| 000 | 001 | 10 us | 50 us | |
| 000 | 010 | 10 us | 70 us | **Recommend** |
| 000 | 011 | 10 us | 90 us | |
| 000 | 100 | 10 us | 110 us | |




### 12.5.23 Delay Register II (Address: 0x816h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Delay | W | WSEL2 | WSEL1 | WSEL0 | RSSC_D1 | RSSC_D0 | RS_DLY2 | RS_DLY1 | RS_DLY0 |
| Reset | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

**WSEL [2:0]: XTAL settling delay setting (200us ~ 2.5ms). Recommend WSEL = [010].**
**[000]:** 200us. **[001]:** 400us. **[010]:** 800us. **[011]:** 600us.
**[100]:** 1ms. **[101]:** 1.5ms. **[110]:** 2ms. **[111]:** No Wait.




**RSSC_D [1:0]: RSSI calibration switching time (10us ~ 40us). Recommend RSSC_D = [00].**
**[00]:** 10us. **[01]:** 20us. **[10]:** 30us. **[11]:** 40us.
**RS_DLY [2:0]: RSSI measurement delay (10us ~ 80us). Recommend RS_DLY = [001].**
**[000]:** 10us. **[001]:** 20us. **[010]:** 30us. **[011]:** 40us.
**[100]:** 50us. **[101]:** 60us. **[110]:** 70us. **[111]:** 80us.

### 12.5.24 RX Register (Address: 0x817h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX | W | QDLS | RXSM1 | RXSM0 | AFC | RXDI | DMG | BWS | ULS |
| Reset | | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

**RXSM0: Reserved for internal usage only. Shall be set to [0].**
**RXSM1: Reserved for internal usage only. Shall be set to [1].**
**AFC: Auto Frequency compensation select.**
**[0]:** Manual compensation. **[1]:** Auto compensation.
Refer to section 14.4 for details.
**RXDI: RX data output invert. Recommend RXDI = [0].**
**[0]:** Non-inverted output. **[1]:** Inverted output.
**DMG: Reserved for internal usage only. Shall be set to [0].**
**BWS:** the IF band pass filter center frequency
**[0]:** 250KHz. **[1]:** 500KHz.

| Data Rate (Kbps) | BWS | Note |
|---|---|---|
| 2~ 500 | 1 | $F_{IF}$= 500KHz |

**ULS: RX Up/Low side band select.**
**[0]:** Up side band, **[1]:** Low side band.
Refer to section 14.2 for details.
**QDLS: limiter amp quick settle select.**
**[0]:** enable, **[1]:** disable.

### 12.5.25 RX Gain Register I (Address: 0x818h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX Gain I | R/W | MVGS | AGLNE | IGC | MGC1 | MGC0 | LGC2 | LGC1 | LGC0 |
| Reset | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**MVGS: Manual VGA setting.**
**[0]:** Auto. **[1]:** Manual.
**AGLNE: Reserved for internal usage only. Shall be set to [0].**
**IGC: Reserved for internal usage only. Shall be set to [0].**
**MGC [1:0]: Mixer gain. Recommend MGS = [00].**
**[00]:** 24dB. **[01]:** 18dB. **[10]:** 12dB. **[11]:** 6dB.
**LGC [2:0]: LNA gain. Recommend LGS = [000].**
**[000]:** 24dB. **[001]:** 18dB. **[010]:** 12dB. **[011]:** 6dB. **[1XX]:** 0dB.

### 12.5.26 RX Gain Register II (Address: 0x819h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX Gain II | R | RHR7 | RHR6 | RHR5 | RHR4 | RHR3 | RHR2 | RHR1 | RHR0 |
| | W | RH7 | RH 6 | RH5 | RH4 | RH3 | RH2 | RH1 | RH0 |
| Reset | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

**RHR [7:0]: RSSI calibration reading for high input power –78dBm.**
**RH [7:0]: Reserved for internal usage only.**

### 12.5.27 RX Gain Register III (Address: 0x81Ah)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX Gain III | R | RLR7 | RLR6 | RLR5 | RLR4 | RLR3 | RLR2 | RLR1 | RLR0 |
| | W | RL7 | RL6 | RL5 | RL4 | RL3 | RL2 | RL1 | RL0 |
| Reset | | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

**RLR [7:0]: RSSI calibration reading for low input power –90dBm.**
**RH [7:0]: Reserved for internal usage only.**

### 12.5.28 RX Gain Register IV (Address: 0x81Bh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX Gain III | W | ENGC | CRCD | MVSEL1 | MVSEL0 | MHC | LHC1 | LHC0 | VGCE |
| Reset | | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |

**ENGC: Reserved for internal usage only.**
**CRCD: CRC package filtering select.**
[0]: disable, [1]: enable.
**MVSEL [1:0]: moving average bits select for RSSI calibration.**
[00]: 8 bit, [01]: 32bit, [10]: 64bit, [11]: 128bit.
**MHC: Reserved for internal usage only. Shall be set to [0].**
**LHC: Reserved for internal usage only. Shall be set to [01].**
**VGCE: Reserved for internal usage only.**

### 12.5.29 RSSI Threshold Register (Address: 0x81Ch)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RSSI Threshold | R | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 |
| | W | RTH7 | RTH6 | RTH5 | RTH4 | RTH3 | RTH2 | RTH1 | RTH0 |
| Reset | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

**RTH [7:0]: Carrier detect threshold.**
Refer to section 17.3 for details.
**ADC [7:0]: ADC output value of temperature, RSSI or external voltage measurement.**
ADC input voltage= 0.3 + 1.2 * ADC [7:0] / 256 V.

### 12.5.30 ADC Control Register (Address: 0x81Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ADC Control | W | RSM1 | RSM0 | ERSS | FSARS | -- | XADS | RSS | CDM |
| Reset | | 0 | 1 | 0 | 1 | -- | 0 | 1 | 1 |

**RSM [1:0]: RSSI margin = RTH – RTL. Recommend RSM = [11].**
**[00]:** 5. **[01]:** 10. **[10]:** 15. **[11]:** 20.
Refer to section 17.3 for details.
**ERSS: end enable for RSSI measurement.**
**[0]:** RSSI measurement continues until leave off RX mode.
**[1]:** RSSI measurement will end when carrier detected and ID code word received.
**FSARS: ADC clock select. Recommend FSARS = [0].**
**[0]:** 4MHz. **[1]:** 8MHz.
**XADS: ADC input signal select.**
**[0]:** Convert internal temperature or RSS signal. **[1]:** Convert external voltage,
**RSS: Temperature/RSSI measurement select.**
**[0]:** Temperature measurement. **[1]:** RSSI or carrier-detect measurement.
**CDM: RSSI measurement mode.**
**[0]:** Single mode. **[1]:** Continuous mode.

### 12.5.31 Code Register I (Address: 0x81Eh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Code I | W | CRC16 | MCS | WHTS | FECS | CRCS | IDL | PML1 | PML0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

**CRC16: CRC-16-CCITT register reset value setting when CRC_MODE=[00]. [0]:** 0x1D0F**. [1]:** 0xFFFF
**WHTS: Data whitening (Data Encryption) select.**
**[0]:** Disable. **[1]:** Enable.
**FECS: FEC select.**
**[0]:** Disable. **[1]:** Enable.
**CRCS: CRC select.**
**[0]:** Disable. **[1]:** Enable.
**IDL: ID code length select. Recommend IDL= [1].**
**[0]:** 2 bytes. **[1]:** 4 bytes.
**PML [1:0]: Preamble length select. Recommend PML= [11].**
**[00]:** 1 byte. **[01]:** 2 bytes. **[10]:** 3 bytes. **[11]:** 4 bytes.

### 12.5.32 Code Register II (Address: 0x81Fh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Code II | W | DCL2 | DCL1 | DCL0 | ETH2 | ETH1 | ETH0 | PMD1 | PMD0 |
| Reset | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

**DCL [2:0]: Demodulator DC estimation average mode. Refer to DCM (2Eh) for details.**
**DCL [2]: payload average mode.**
**[0]:** 128 bits average. **[1]:** 256 bits average.
**DCL [1]: For average and hold mode.**
**[0]:** 32 bits average. **[1]:** 64 bits average.
**DCL [0]: Preamble detection delay. Count from preamble detected signal. Recommend DCL0 = [1].**
**[0]:** 4 bits for DCL1=0, 8 bits for DCL1=1. **[1]:** 8 bits for DCL1=0, 16 bits for DCL1=1.
**ETH [2:0]: ID code error tolerance. Recommend ETH = [01].**
**[000]:** 0 bit, **[001]:** 1 bit. **[010]:** 2 bits. **[011]:** 3 bits. **[100]:** 4 bits. **[101]:** 5 bits. **[110]:** 6 bits. **[111]:** 7 bits.
**PMD [1:0]: Preamble pattern detection length. Recommend PMD = [10].**
**[00]:** 0bit. **[01]:** 4bits. **[10]:** 8bits. **[11]:** 16bits.

### 12.5.33 Code Register III (Address: 0x820h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Code III | W | WHT9 | WS6 | WS5 | WS4 | WS3 | WS2 | WS1 | WS0 |

| Reset | | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|

**WHT9: Whitening with PN9 generator(X^9+X^5+1)**
**WS [6:0]: Data Whitening seed setting (data encryption key).**

### 12.5.34 IF Calibration Register I (Address: 0x821h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| IF Calibration I | R | | | | FBCF | FB3 | FB2 | FB1 | FB0 |
| | W | -- | -- | -- | MFBS | MFB3 | MFB2 | MFB1 | MFB0 |
| Reset | | -- | -- | -- | 0 | 0 | 1 | 1 | 0 |

**MFBS: IF filter calibration value select. Recommend MFBS = [0].**
**[0]:** Auto calibration value. **[1]:** Manual calibration value.
**MFB [3:0]: IF filter manual calibration value.**
**FBCF: IF filter auto calibration flag.**
**[0]:** Pass. **[1]:** Fail.
**FB [3:0]: IF filter calibration value.**
**MFBS= 0: Auto calibration value (AFB),**
**MFBS= 1: Manual calibration value (MFB).**

### 12.5.35 IF Calibration Register II (Address: 0x822h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| IF Calibration II | R | -- | -- | | FCD4 | FCD3 | FCD2 | FCD1 | FCD0 |
| Reset | | -- | -- | -- | -- | -- | -- | -- | -- |

**FCD [4:0]: IF filter calibration deviation from goal.**

### 12.5.36 VCO current Calibration Register (Address: 0x823h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO current Calibration | R | | | | FVCC | VCB3 | VCB2 | VCB1 | VCB0 |
| | W | -- | -- | VCCS | MVCS | VCOC3 | VCOC2 | VCOC1 | VCOC0 |
| Reset | | -- | -- | 0 | 0 | 1 | 0 | 0 | 0 |

**VCCS: Reserved for internal usage only. Shall be set [0].**
**MVCS: VCO current calibration value select. Recommend MVCS = [0].**
**[0]:** Auto calibration value. **[1]:** Manual calibration value.
**VCOC [3:0]: VCO current manual calibration value.**
**FVCC: VCO current auto calibration flag.**
**[0]:** Pass. **[1]:** Fail.
**VCB [3:0]: VCO current calibration value.**
**MVCS= 0: Auto calibration value (VCB).**
**MVCS= 1: Manual calibration value (VCOC).**

### 12.5.37 VCO Single band Calibration Register I (Address: 0x824h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO Single band Calibration I | R | -- | -- | DVT1 | DVT0 | VBCF | VB2 | VB1 | VB0 |
| | W | -- | -- | -- | -- | MVBS | MVB2 | MVB1 | MVB0 |
| Reset | | -- | -- | -- | -- | 0 | 1 | 0 | 0 |

**MVBS: VCO bank calibration value select. Recommend MVBS = [0].**
**[0]:** Auto calibration value. **[1]:** Manual calibration value.
**MVB [2:0]: VCO band manual calibration value.**
**DVT [1:0]: digital VCO tuning voltage output.**
**[00]:** VT<VTL<VTH. **[01]:** VTL<VT<VTH. **[10]:** No used. **[11]:** VTL<VTH<VT.
**VBCF: VCO band auto calibration flag.**
**[0]:** Pass. **[1]:** Fail.
**VB [2:0]: VCO bank calibration value.**
**MVBS= 0: Auto calibration value (AVB).**
**MVBS= 1: Manual calibration value (MVB).**

### 12.5.38 VCO Single band Calibration Register II (Address: 0x825h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO Single band Calibration II | W | -- | -- | VTH2 | VTH1 | VTH0 | VTL2 | VTL1 | VTL0 |
| Reset | | -- | -- | 1 | 1 | 1 | 0 | 1 | 1 |

**VTH [2:0]: VCO tuning voltage upper threshold level setting.**
**[000]:** VDD_A – 0.6V. **[001]:** VDD_A – 0.7V. **[010]:** VDD_A – 0.8V. **[011]:** VDD_A – 0.9V
**[100]:** VDD_A – 1.0V. **[101]:** VDD_A – 1.1V. **[110]:** VDD_A – 1.2V. **[111]:** VDD_A – 1.3V
**VDD_A is on chip analog regulator output voltage.**
**VTL [2:0]: VCO tuning voltage lower threshold level setting.**
**[000]:** 0.1V. **[001]:** 0.2V. **[010]:** 0.3V. **[011]:** 0.4V.
**[100]:** 0.5V. **[101]:** 0.6V. **[110]:** 0.7V. **[111]:** 0.8V

### 12.5.39 Battery detect Register (Address: 0x826h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Battery detect | R | | RGV1 | RGV0 | BDF | BVT2 | BVT1 | BVT0 | BD_E |
| | W | | RGV1 | RGV0 | QDS | BVT2 | BVT1 | BVT0 | BD_E |
| Reset | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**RGV [1:0]: VDD_D and VDD_A voltage setting in non-Sleep mode. Recommend RGV = [11].**
**[00]:** 2.1V. **[01]:** 2.0V. **[10]:** 1.9V. **[11]:** 1.8V.
**QDS: Reserved for internal usage only. Shall be set [0].**
**BVT [2:0]: Battery voltage detect threshold.**
**[000]:** 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V.
**[100]:** 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.
**BD_E: Battery detect enable.**
**[0]:** Disable. **[1]:** Enable. It will be clear after battery detection done.
**BDF: Battery detection flag.**
**[0]:** Battery voltage less than threshold. **[1]:** Battery voltage greater than threshold.
**QDS: analog regulator quick discharge select when enter sleep mode.**
**[0]:** Disable. **[1]:** Enable.

### 12.5.40 TX test Register (Address: 0x827h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TX test | W | FD7 | FD6 | TXCS | PAC1 | PAC0 | TBG2 | TBG1 | TBG0 |
| Reset | | -- | -- | 0 | 1 | 0 | 1 | 1 | 1 |

**TXCS: TX Current Setting.**
**PAC [1:0]: PA Current Setting.**
**TBG [2:0]: TX Buffer Setting.**

| Typical Output Power (dBm) | Recommend setting | | | Typical TX current (mA) |
|---|---|---|---|---|
| | TXCS | TBG | PAC | |
| 1 | 0 | 7 | 3 | 22 |
| 0 | 0 | 7 | 2 | 19 |
| -10 | 0 | 3 | 1 | 14 |
| -20 | 0 | 1 | 0 | 13 |

### 12.5.41 Rx DEM test Register I (Address: 0x828h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Rx DEM test I | W | DMT | DCM1 | DCM0 | MLP1 | MLP0 | SLF2 | SLF1 | SLF0 |
| Reset | | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

**DMT: Reserved for internal usage only. Shall be set to [0].**
**DCM [1:0]: Demodulator DC estimation mode.**

**[00]:** Fix mode (For testing only). DC level is set by DCV [7:0].
**[01]:** Preamble hold mode. DC level is preamble average value.
**[10]:** Average and hold mode. DC level is the average value hold about 8 bit data rate later after preamble is detected.
**[11]:** Payload average mode (For internal usage). DC level is payload data average.
**MLP [1:0]: Reserved for internal usage only. Shall be set to [000].**
**SLF [2:0]: Reserved for internal usage only. Shall be set to [111].**

### 12.5.42 Rx DEM test Register II (Address: 0x829h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Rx DEM test II | W | DCV7 | DCV6 | DCV5 | DCV4 | DCV3 | DCV2 | DCV1 | DCV0 |
| Reset | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**DCV [7:0]: Demodulator fix mode DC value. Recommend DCV = [0x80].**

### 12.5.43 Charge Pump Current Register (Address: 0x82Ah)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Charge Pump Current | W | RCOSCS | | MID | MXD | DBD | LVR | CPC1 | CPC0 |
| Reset | | 0 | | 0 | 0 | 0 | 0 | 0 | 1 |

**CPC [1:0]: Charge pump current setting. Recommend CPC = [11].**
[00]: 0.5mA. [01]: 1.0mA. [10]: 1.5mA. [11]: 2.0mA
**LVR: Reserved for internal usage only. Shall be set to [0].**
**RCOSCS: Reserved for internal usage only. Shall be set to [0].**
**MID: Reserved for internal usage only. Shall be set to [0].**
**MXD: Reserved for internal usage only. Shall be set to [0].**
**DBD: Reserved for internal usage only. Shall be set to [0].**

### 12.5.44 Crystal test Register (Address: 82Bh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Crystal test | W | RSIS | PKT1 | PKT0 | PKS | XCC1 | XCC0 | XCP1 | XCP0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**XCC[1:0]: Reserved for internal usage only. Shall be set to [01].**
**XCP [1:0]: Reserved for internal usage only. Shall be set to [01].**
**PKS: Reserved for internal usage only. Shall be set to [0].**
**PKT [1:0]: Reserved for internal usage only. Shall be set to [0].**
**RSIS [1:0]: Reserved for internal usage only. Shall be set to [00].**

### 12.5.45 PLL test Register (Address: 0x82Ch)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL test | W | PRS | PMPE | PRIC1 | PRIC0 | PRRC1 | PRRC0 | SDPW | NSDO |
| Reset | | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

**PMPE: Reserved for internal usage only. Shall be set to [1].**
**PRRC [1:0]: Reserved for internal usage only. Shall be set to [00].**
**PRIC [1:0]: Reserved for internal usage only. Shall be set to [01].**
**SDPW: Reserved for internal usage only. Shall be set to [0].**
**NSDO: Reserved for internal usage only. Shall be set to [1].**
**PRS: PLL register IV and V reading select.**

### 12.5.46 VCO test Register I (Address: 0x82Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO test I | W | MQDL | FIFOREV | IDREV | TLB1 | TLB0 | RLB1 | RLB0 | VCBS |
| Reset | | 0 | -- | -- | 1 | 1 | 0 | 1 | 0 |

**TLB [1:0]: Reserved for internal usage only. Shall be set to [11].**

**RLB [1:0]: Reserved for internal usage only. Shall be set to [00].**
**VCBS: Reserved for internal usage only. Shall be set to [0].**
**MQDL: Reserved for internal usage only. Shall be set to [0].**
**FIFOREV: FIFO reverse enable.**
**[0]:** Disable. **[1]:** Enable
**IDREV: ID reverse enable.**
**[0]:** Disable. **[1]:** Enable.

### 12.5.47 VCO test Register II (Address: 0x82Eh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO test II | W | BREV | | | XEC | RFT3 | RFT2 | RFT1 | RFT0 |
| Reset | | -- | -- | -- | -- | 0 | 0 | 0 | 0 |

**RFT [3:0]: RF analog pin configuration for testing. Recommend RFT= [0000].**
**BREV: data byte reversion for TX data in the air**
**[0]:** normal. **[1]:** reverted.
**XEC: Reserved. Should set to [1]**

### 12.5.48 IFAT Register (Address: 0x82Fh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO test II | W | IGFI2 | IGFI1 | IGFI0 | IGFQ2 | IGFQ1 | IGFQ0 | IFBC | LIMC |
| Reset | | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

**IGFI [2:0]: Reserved for internal usage only. Shall be set to [111].**
**IGFQ [2:0]: Reserved for internal usage only. Shall be set to [111].**
**IFBC: Reserved for internal usage only. Shall be set to [1].**
**LIMC: Reserved for internal usage only. Shall be set to [1].**

### 12.5.49 RScale Register (Address: 0x830h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RSCALE | R/W | RSC7 | RSC6 | RSC5 | RSC4 | RSC3 | RSC2 | RSC1 | RSC0 |
| Reset | | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**RSC [7:0]: Reserved for internal usage only.**

### 12.5.50 Filter test Register (Address: 0x831h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TMV | W | PRES | TRT2 | TRT1 | TRT0 | ASMV2 | ASMV1 | ASMV0 | AMVS |
| Reset | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**PRES: Preamble detect margin manual setting select by 0x833h PREDN[2:0], PREUP[2:0] . [1]: manual.**
**ASMV [2:0]: TX ramp up timing select.**
**Ramping up time = 4* ASMV.**
[000]: 4us. [001]: 8us. [010]: 12us. [011]: 16us.
[100]: 20us. [101]: 24us. [110]: 28us. [111]: 32us.
**TRT [2:0]: TX ramping time select.**
**Ramping down time = 2*TRT.**
[000]: 4us. [001]: 8us. [010]: 12us. [011]: 16us.
[100]: 20us. [101]: 24us. [110]: 28us. [111]: 32us.

### 12.5.51 RX Gain Register II (Address: 0x832h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| SYNC | W | RNUM1_2 | RNUM1_1 | RNUM1_0 | RCK_sel | CKSEL1 | CKSEL0 | MRCKS | SYNCS |
| | | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

**MRCKS: Clock Recovery reset setting.Recommand MRCKS=[0]**
**[0]:** reset by sync word ok. **[1]:** reset by preamble ok..
**RCK_sel: Clock Recovery timing manual setting. Recommand RCK_sel=[0]**
**RNUM1[2:0]: Clock Recovery timing setting. Recommand RNUM1[2:0]=[010]**
**RNUM0[2:0]: Clock Recovery timing setting manual select. [001]: manual. Recommand RNUM0[2:0]=[001]**
**SYNCS: SYNC word detect select. [1]: sync word. [0]: preamble. Recommand SYNCS=[1]**
**CKSEL[1:0]: Flash Clock delay when MCU wake. [00]: Fxtal*2048. [01]: Fxtal*1024. [10]: Fxtal*512. [11]: Fxtal*256**

### 12.5.52 RX Detection Register (Address: 0x833h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| DET | W | DC_SEL | RXDCS | PREDN2 | PREDN1 | PREDN0 | PREUP2 | PREUP1 | PREUP0 |
| | R | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

**DC_SEL: Initial DC value select when sync word ok.**
[0]: DC set by last pattern DC
[1]: DC set by 0x82Eh DC value.
**RXDCS: RX dc average clock setting. Recommed RXDCS=[0].**
**PREDN[2:0]: Preamble detect low threshold setting.**
**PREUP[2:0]: Preamble detect high threshold setting.**

### 12.5.53 DC_SHIFT (Address: 0x834h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| DC | W | DC_SHIFT[7:0] | | | | | | | |
| | R | DCOUT[7: 0] | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

**dc_shift [7:0]: DC average by ID initial dc value shift setting. (NOTE): DC_SHIFT[7] is signed bit.**
**DCOUT [7:0]: Read demodulator DC value.**

### 12.5.54 ID Register 0 (Address: 0x835h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ID0 | W/R | ID31 | ID30 | ID29 | ID28 | ID27 | ID26 | ID25 | ID24 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ID[31:0]: ID Data.**
**Once this address is accessed, ID Data is input/output in sequence corresponding to Write or Read.**

### 12.5.55 ID Register 1 (Address: 0x836h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ID1 | W/R | ID23 | ID22 | ID21 | ID20 | ID19 | ID18 | ID17 | ID16 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ID[31:0]: ID Data.**
**Once this address is accessed, ID Data is input/output in sequence corresponding to Write or Read.**

### 12.5.56 ID Register 2 (Address: 0x837h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ID2 | W/R | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | ID9 | ID8 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ID[31:0]: ID Data.**
**Once this address is accessed, ID Data is input/output in sequence corresponding to Write or Read.**

### 12.5.57 ID Register 3 (Address: 0x838h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|

| ID3 | W/R | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
|---|---|---|---|---|---|---|---|---|---|
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ID[31:0]: ID Data.**
**Once this address is accessed, ID Data is input/output in sequence corresponding to Write or Read.**

### 12.5.58 DID Register 0 (Address: 0x839h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| DID0 | R | DID31 | DID30 | DID29 | DID28 | DID27 | DID26 | DID25 | DID24 |
| Reset | | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

**DID[31:0]: Device ID.**

### 12.5.59 DID Register 1 (Address: 0x83Ah)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| DID1 | R | DID23 | DID22 | DID21 | DID20 | DID19 | DID18 | DID17 | DID16 |
| Reset | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**DID[31:0]: Device ID.**

### 12.5.60 DID Register 2 (Address: 0x83Bh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| DID2 | R | DID15 | DID14 | DID13 | DID12 | DID11 | DID10 | DID9 | DID8 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**DID[31:0]: Device ID.**

### 12.5.61 DID Register 3 (Address: 0x83Ch)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| DID3 | R | DID7 | DID6 | DID5 | DID4 | DID3 | DID2 | DID1 | DID0 |
| Reset | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

**DID[31:0]: Device ID.**

### 12.5.62 Power Control Register 0 (Address: 0x83Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PWRCTL0 | W | CBG2 | CBG1 | CBG0 | PDNS | STS | ENDL2 | ENDL1 | ENDL0 |
| Reset | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**CBG[2:0]: Reserved for internal usage.**
**PDNS: Power manager to turn on REGOD Recommend PDNS = [0]**
**STS: Reserved for internal usage only. Shall be set to [0].**
**ENDL[2:0]: Reserved for internal usage only**

### 12.5.63 Power Control Register 1 (Address: 0x83Eh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PWRCTL1 | W | EBOD | ENAV | QDSA | ENDV | QDSD | CEL | SVREF | CELA |
| Reset | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

**EBOD: Reserved for internal usage.**
**ENAV: REGOA and REGOD connection. Reserved for internal usage.**
[1]: REGOA is connected to REGOD.
**QDSA: Reserved for internal usage.**
**ENDV: Reserved for internal usage.**
**QDSD: Reserved for internal usage.**

**CEL: Digital voltage select in standby mode. Recommend CEL = [0].**
**SVREF: Reserved for internal usage.**
**CELA: Reserved for internal usage.**

### 12.5.64 Power Control Register 2 (Address: 0x83Fh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PWRCTL2 | W | P3PUNIE | -- | RGS | | | RGC1 | RGC0 | RCHC |
| Reset | | 0 | -- | -- | 0 | 0 | 0 | 1 | 0 |

**RTCPUNIE: Reserved for internal usage. Shall be set to [0].**
**RGS: VDD_D voltage setting in Sleep mode.**
[0]: 1.8V. [1]: 1.6V
**RGC[1:0]: Low power band-gap current select. Recommend RGC = [01]**
**RCHC: Reserved for internal usage.**

### 12.5.65 RC OSC Register IV (Address: 0x840h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RC OSC IV | W | RCOT2 | RCOT1 | RCOT0 | WCKSEL1 | WCKSEL0 | MVS1 | MVS0 | ENCAL |
| | R | NUMLH11 | NUMLH10 | NUMLH9 | NUMLH8 | -- | RCOC9 | RCOC8 | ENCAL |
| Reset | | -- | -- | -- | 0 | 0 | 0 | 0 | 0 |

**RCOT[2:0]: RCOSC current select for RC oscillator calibration.**
**WCKSEL [1:0]: Clock select for internal RC oscillator Calibration.**
[00]: 16 MHz
[01]: 8 MHz
[10]: 4 MHz
[11]: 2MHz
**ENCAL: WOR calibration enable.**
[0]: Disable [1]: Enable.
**RCOC [9:0]: WOR Calibration value.**
**NUMLH[11:0]: WOR calibration latch number.**

### 12.5.66 RC OSC Register V (Address: 0x841h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RC OSC V | W | MRCT9 | MRCT8 | -- | -- | -- | TMRE | MAN | MCALS |
| | R | NUMLH7 | NUMLH6 | NUMLH5 | NUMLH4 | NUMLH3 | NUMLH2 | NUMLH1 | NUMLH0 |
| Reset | | 0 | 0 | -- | -- | -- | -- | 0 | 0 |

**MRCT[9:0]: Manual RC-OSC calibration value setting.**
**MAN: Enable Manual RC-OSC Calibration.**
[0]: Auto [1]: Manual.
**TMRE: RC-oscillator enable.**
[0]: Disable. [1]: Enable.
**MCALS: Enable Continuous RC-OSC Calibration.**
[0]: Continuous mode. [1]: Single mode.
**NUMLH[11:0]: RC-OSC calibration latch number.**

### 12.5.67 RC OSC Register VI (Address: 0x842h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RC OSC VI | W | MRCT7 | MRCT6 | MRCT5 | MRCT4 | MRCT3 | MRCT2 | MRCT1 | MRCT0 |
| | R | RCOC7 | RCOC6 | RCOC5 | RCOC4 | RCOC3 | RCOC2 | RCOC1 | RCOC0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**MRCT [9:0]: Manual RC-OSC calibration value setting.**
**RCOC [9:0]: RC-OSC calibration value.**

### 12.5.68 RC OSC Register VII (Address: 0x843h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RCOSC7 | W | PDNFHR | QDSFHR | PDNFLR | QDSFLR | TGNUM11 | TGNUM10 | TGNUM9 | TGNUM8 |
| Reset | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**TGNUM[11:0]: Target Number for RC OSC Calibration.**
**PDNFHR: Flash power control for VDD_H. Recommend PDNFHR=[1].**
**QDSFHR: Flash power control for VDD_H. Recommend QDSFHR=[0].**
**PDNFLR: Flash power control for VDD_S. Recommend PDNFLR=[1].**
**QDSFLR: Flash power control for VDD_S. Recommend QDSFLR=[0].**

### 12.5.69 RC OSC Register VIII (Address: 0x844h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RCOSC8 | W | TGNUM7 | TGNUM6 | TGNUM5 | TGNUM4 | TGNUM3 | TGNUM2 | TGNUM1 | TGNUM0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**TGNUM[11:0]: Target Number for RC OSC Calibration.**

### 12.5.70 Timer Interval Register 1 (Address: 0x845h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TMRITV1 | W/R | TMR_ITV[15:8] | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**TMR_ITV[15:0]**: Timer interval setting.
**Timer interval can be set to be:**
**TMRCKS[1:0] = 00: 0.15625 ms ~ 10.24 s**
**TMRCKS[1:0] = 01: 0.3125 ms ~ 20.48 s**
**TMRCKS[1:0] = 10: 0.625 ms ~ 40.96 s**
**TMRCKS[1:0] = 11: 1.25 ms ~ 81.92 s**

### 12.5.71 Timer Interval Register 2 (Address: 0x846h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TMRITV2 | W/R | TMR_ITV[7:0] | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**TMR_ITV[15:0]**: Timer interval setting.
**Timer interval can be set to be:**
**TMRCKS[1:0] = 00: 0.15625 ms ~ 10.24 s**
**TMRCKS[1:0] = 01: 0.3125 ms ~ 20.48 s**
**TMRCKS[1:0] = 10: 0.625 ms ~ 40.96 s**
**TMRCKS[1:0] = 11: 1.25 ms ~ 81.92 s**

### 12.5.72 Timer Wake On Radio Register 1 (Address: 0x847h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TMRWOR1 | W/R | TMRWORS | -- | -- | TMR_OFS4 | TMR_OFS3 | TMR_OFS2 | TMR_OFS1 | TMR_OFS0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**TMRWORS: Timer WOR / WOT selection.**
**[0]:** WOR
**[1]:** WOT
**TMR_OFS[4:0]: Interrupt offset for 16-bits Timer.**

### 12.5.73 Timer Control Register (Address: 0x848h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TMRCTL | W | TMRON | TMRIE | TMRIF | TMRCOR | TMRWOR | TMRCKS[1:0] | | TMR_CE |
| | R | -- | TMRIE | TMRIF | -- | -- | TMRCKS[1:0] | | TMR_CE |

| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|---|

**TMRON: Turn on TMR.**
**TMRIE: Timer Interrupt Enable.**
[0]: Disable.
[1]: Enable.
**TMRIF: Timer Interrupt Flag. (Write "1" to clear)**
**TMRCOR : Timer CLK re-correct when sync.**
**[0]:** disable.
**[1]:** enable
**TMRWOR: Timer WOR function enable.**
[0]: Disable.
[1]: Enable.
**TMRCKS[1:0]: Select Timer Source Clock**
[00]: 6.4 kHz
[01]: 3.2 kHz
[10]: 1.6 kHz
[11]: 0.8 kHz
**TMR_CE: Start Timer counting.**
[0]: Stop.
[1]: Start.

### 12.5.74 RFT Test Register IV (Address: 0x849h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RFT4 | W | -- | | | FBG4 | FBG3 | FBG2 | FBG1 | FBG0 |
| | R | -- | -- | -- | FBGR4 | FBGR3 | FBGR2 | FBGR1 | FBGR0 |
| Reset | | -- | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**FBG[4:0]: Bandgap voltage SPI fine trim setting.**

### 12.5.75 RFT Test Register III (Address: 0x84Ah)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RFT3 | W | -- | STMP | STM5 | STM4 | STM3 | STM2 | STM1 | STM0 |
| | R | -- | STMP | STMR5 | STMR4 | STMR3 | STMR2 | STMR1 | STMR0 |
| Reset | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**STMP: Temp voltage ADC reading select.**
**[0]:** 1 scale / degree C. **[1]:** 2 scale/degree C.
**STM [5:0]: ADC voltage fine trim setting.**

### 12.5.76 ADC Control Register (Address: 0x84Bh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ADCCTL | W | BUFS | CKS1 | CKS0 | MODE | MVS2 | MVS1 | MVS0 | ADCE |
| | R | -- | -- | -- | MODE | MVS2 | MVS1 | MVS0 | ADCE |
| Reset | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**BUFS: input buffer select for 12 bit ADC.**
[0]: disable. [1]: enable.
**CKS[1:0]: ADC clock selected.**
[00]: 4 MHz
[01]: 2 MHz
[10]: 1 MHz
[11]: 500 kHz
**MODE: ADC measurement mode.**
[0]: Single mode. [1]: Continuous mode.
**MVS [1:0]: ADC average times (for VCO calibration and RSSI ).**
[00]: Average 8 times. [01]: Average 16 times. [10]: Average 32 times. [11]: Average 64 times.
**ADCE: ADC measurement enable**

### 12.5.77 ADC Value Register 1 (Address: 0x84Ch)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ADCAVG1 | W | ADCIE | -- | -- | -- | ADIVL | ADCYC | ENADC | DTMP |
| | R | MVADC11 | MVADC10 | MVADC9 | MVADC8 | ADC11 | ADC10 | ADC9 | ADC8 |
| Reset | | 0 | -- | -- | -- | 0 | 0 | 0 | 0 |

**ADCIE : 12-bits interrupt enable.**
[0]: disable. [1]: enable.
**ADIVL: Reserved. Should set to [0]**
**ADCYC: Reserved. Should set to [0]**
**ENADC: Enable ADC.**
**MVADC [11:0]: Moving average ADC output value**
**ADC [11:0]: ADC output value**
**MVADC [11:0]: Moving average ADC output value**

### 12.5.78 ADC Value Register 2 (Address: 0x84Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ADCAVG2 | R | MVADC7 | MVADC6 | MVADC5 | MVADC4 | MVADC3 | MVADC2 | MVADC1 | MVADC0 |
| Reset | | -- | -- | -- | -- | -- | -- | -- | -- |

**MVADC [11:0]: Moving average ADC output value.**

### 12.5.79 ADC Value Register 3 (Address: 0x84Eh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ADCAVG3 | R | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 |
| Reset | | -- | -- | -- | -- | -- | -- | -- | -- |

**ADC [11:0]: ADC output value.**

## 13. Auxiliary function

A8108 has built-in 8-bits ADC for RSSI measurement as well as carrier detection function. The ADC clock ($F_{ADC}$) is 4.096MHz. The ADC converting time is 20 x ADC clock periods.

| Bit | | Mode | |
|---|---|---|---|
| XADS | RSS | Standby | RX |
| 0 | 1 | None | RSSI / Carrier detect |

Table 13.1 Setting of ADC function

**Relative Control Register**

Mode Control Register (Address: 0802h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Name | R | PIPOS | ARSSI | AIF | CD | WWSE | FMT | FMS | ADCM |
| | W | PIPOS | ARSSI | AIF | DFCD | WWSE | FMT | FMS | ADCM |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RSSI Threshold Register (Address: 081Ch)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RSSI Threshold | R | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 |
| | W | RTH7 | RTH6 | RTH5 | RTH4 | RTH3 | RTH2 | RTH1 | RTH0 |
| Reset | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

ADC Control Register (Address: 081Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ADC Control | W | RSM1 | RSM0 | ERSS | FSARS | -- | XADS | RSS | CDM |
| Reset | | 0 | 1 | 0 | 1 | -- | 0 | 1 | 1 |

### 13.1 RSSI Measurement

A8102 supports 8-bits digital RSSI to detect RF signal strength. RSSI value is stored in ADC [7:0] (1Ch). Fig 13.2 shows a typical plot of RSSI reading as a function of input power. This curve is based on the current gain setting of A8102 reference code. A8102 automatically averages 8-times ADC conversion a RSSI measurement until A8102 exits RX mode. Therefore, each RSSI measuring time is (8 x 20 x $F_{ADC}$). Be aware RSSI accuracy is about ± 6dBm.

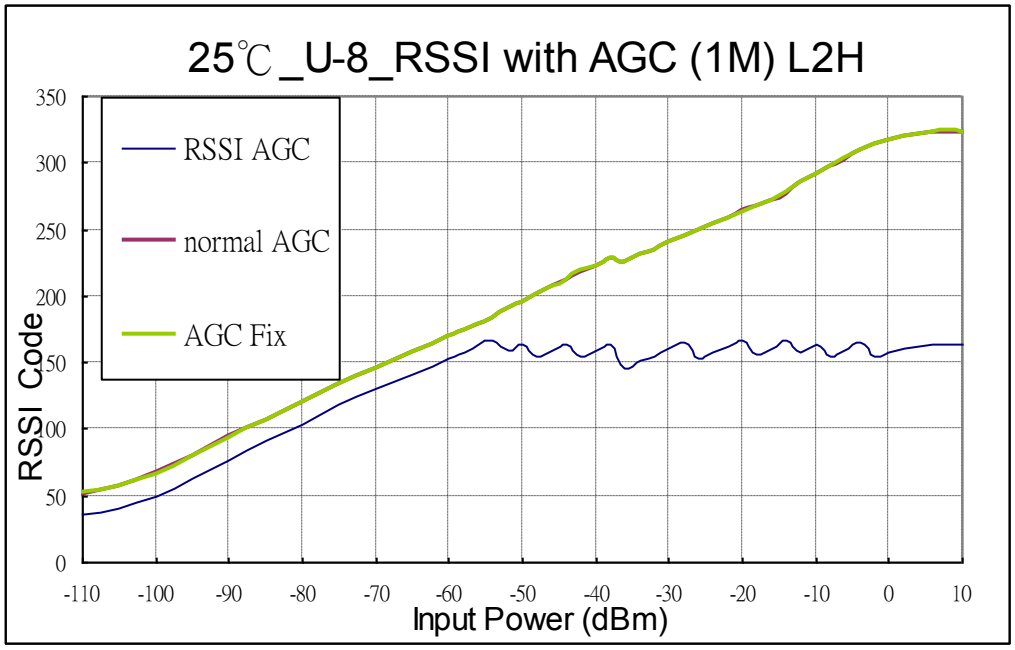
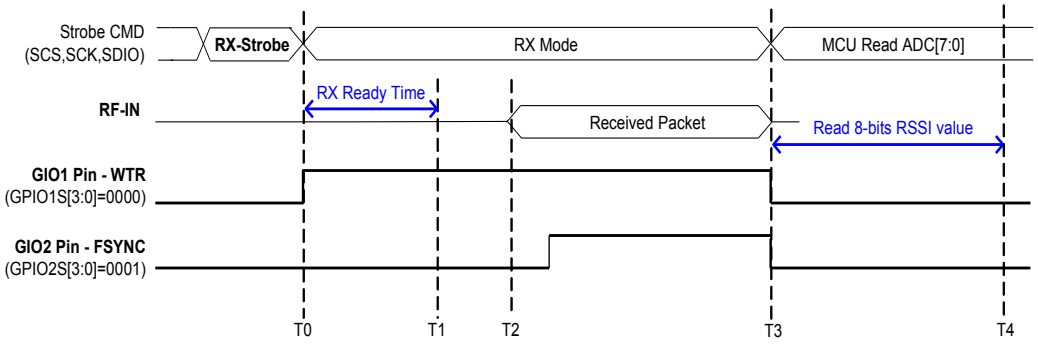



Figure 13.2 Typical RSSI characteristic.

**Auto RSSI measurement for TX Power:**

1. Set wanted $F_{RXLO}$.
2. Set RSS= 1 (081Dh), FSARS= 0 (081Dh, 4.096MHz ADC clock).
3. Enable ARSSI= 1 (0802h).
4. Send RX Strobe command.
5. In RX mode, 8-times average a RSSI measurement periodically.
6. Exit RX mode, user can read digital RSSI value from ADC [7:0] (081Ch) for TX power.

In step 6, if A8102 is set in direct mode, MCU shall let A8102 exit RX mode within 40 us to prevent RSSI inaccuracy.



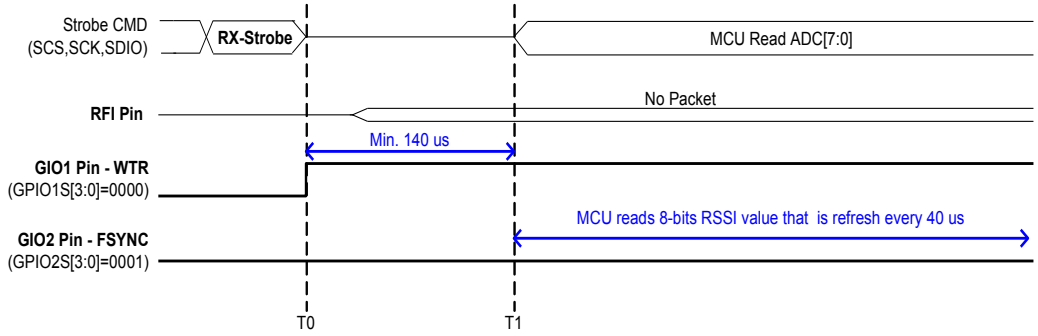

T0-T1: Settling Time
T2-T3: Receiving Packet
T3 : Exit RX mode automatically in FIFO mode
T3-T4: MCU read RSSI value @ ADC [7:0]

Figure 16.2 RSSI Measurement of TX Power.

**Auto RSSI measurement for Background Power:**

1. Set wanted $F_{RXLO}$.
2. Set RSS= 1 (081Dh), FSARS= 0 (081Dh, 4.096MHz ADC clock).
3. Enable ARSSI= 1 (0802h).

4. Send RX Strobe command.
5. MCU delays min. 140us.
6. Read digital RSSI value from ADC [7:0] (081Ch) to get background power.
7. Send other Strobe command to let A8102 exit RX mode.




T0-T1: MCU Delay Loop from PLL to RX mode for RSSI measurment
T1 : Auto RSSI Measurment is done by 8-times average.
MCU can read RSSI value from ADC [7:0]

Figure 16.3 RSSI Measurement of Background Power.

## 13.2 Carrier Detect

Base on RSSI measurement, user can extend its application to do carrier detect (CD). In Carrier Detect mode, RSSI is refresh every 5 us without 8-times average. If RSSI level is below threshold level (RTH), CD is output high to GIO1 or GIO2 pin to inform MCU that current channel is busy.

Below is a reference procedure:

1. Set CDTH (081Ch) for absolute RSSI threshold level (ex. RTH = 80d).
2. Set GIO2S = [0010] (080Bh) for Carrier Detect to GIO2 pin.
   (2-1) Set wanted $F_{RXLO}$.
   (2-2) Set RSM= [11] (081Dh, CDM =0 and hysteresis =6, or CDM =1 and hysteresis =12).
   (2-3) Enable ARSSI= 1 (0802h).
   (2-4) Send RX Strobe command.
   (2-5) MCU enables a timer delay (min. 100 us).
3. MCU checks GIO2 pin.
   (3-1) If ADC $\geqq$ CDTH, GIO2 = 0.
   (3-2) If ADC $\leqq$ CDTH-CDM, GIO2 = 1.
   (3-3) If ADC locates in hysteresis zone, GIO2 = previouse state.
4. Exit RX mode.

## 13.3 Battery Detect

A8108 has a built-in battery detector to check supply voltage (REGI pin). The detecting range is 1.8V ~ 2.5V in 8 levels.

### 13.3.1 Relative Control Register

Battery detect Register (Address: 082Bh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Battery detect | W | RGS | RGV1 | RGV0 | PACTL | BVT2 | BVT1 | BVT0 | BDS |

| | R | -- | RGV1 | RGV0 | BDF | BVT2 | BVT1 | BVT0 | BDS |
|---|---|---|---|---|---|---|---|---|---|
| Reset | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

BVT[1:0]: Battery detection threshold.
[000]: 1.8V. [001]: 1.9V. [010]: 2.0V. [011]: 2.1V.
[100]: 2.2V. [101]: 2.3V. [110]: 2.4V. [111]: 2.5V.
When REGI < Threshold, BDF= low.
When REGI > Threshold, BDF= high.

Below is the procedure to detect low voltage input (ex. below 2.1V):

1. Set A8108 in standby or PLL mode.
2. Set BVT[3:1] (082Bh) = [011] and enable BDS (082Bh) = 1.
3. After 5 us, BDE is auto clear.
4. MCU reads BDF (082Bh).
   If REGI pin > 2.1V,
   BDF = 1 (battery high). Else, BDF = 0 (battery low).

# 14 Power Management

The power consumption of A8108 comes from RF, analog circuit (includes audio codec and audio amplifier) and digital circuit (includes MCU and peripherals). In the RF part, the sleep mode use the minimum power and the TX or RX mode use the maximum power consumptions. To changes RF status by setting the strobe control register (0x0800h). For more detail information, please refer chapter 12.5. In analog circuit, please refer the chapter 17 more details. This chapter only introduces digital parts. Low power operation is enabled through different power modes setting. A8108 has various operating mode are referred as normal mode and PM (power manager mode). Table 14.1 shows the impact of different power modes on systems operation. There are two registers to setting power manager. One is power control register (PCON, 0x87h) and the other is power control extend register (PCONE, 0xB9h).

In normal mode, user selects different clock be MCU core clock.in CLKSEL[2:0] (PCONE, 0xB9h) then enable CKSE (PCON, 0x87h). User adjusts MCU clocks depends on the required power consumption. CLKSEL[2:0] = 001 ~ 110b, the MCU core clock is the clock sources divide 2 ~ 64. User could adjust the MCU speed to trade-off between the performance and the power consumption. **BEWARE, please choice CLKSEL firstly then enable CKSE to avoid glitch. Please refer the reference code or contact AMICCOM's FAE for more details.**

User can enable STOP to freeze MCU core clock and all digital peripherals also stop. MCU can be waked up by hardware reset, wakeup key, KEYINT or sleep timer (WOR /TWOR). User set sleep timer, WOR or TWOR before enter STOP mode. In this condition, it is called PM(power manger mode). In PM, all digital circuitry is stop.

**Note: Please don't enable STOP and CKSE at the same time.**

**PCON (087h) Power control**

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 87h PCON | R/W | SMOD | - | - | PWE | - | SWB | STOP | CKSE |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SWB (Switchback enable)**
[1]: Enable
[0]: Disable
**STOP (Stop mode)**
[1]: Enable
[0]: Disable
**CKSE (Clock select enable )**
[1]: Enable clock select
[0]: Disable clock select

**PCONE(0xB9h) Power control extend**

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| B9h PCONE | R/W | PDN_USB | USB_TM | QD | REGAE | PM2F | CLKSEL2 | CLKSEL1 | CLKSEL0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**PDN_USB (USB power down)**
[1]: normal
[0]: power down
**USB (USB test mode)**
[1]: USB 48MHz clock from the XTAL pad input.
[0]: USB 48MHz clock from the internal PLL generation.
**QD (Quick discharge )**
[1]: Quick discharge enable
[0]: Quick discharge disable
**REGAE(RegA Enable)**
[1]: Enable
[0]: Disable
**PM2F (Power Mode 2 flag)**
[1]: EnablePM2. MCU enter PM2 after STOP mode and VDD_D is off
[0]: Disable PM2
**CLKSEL[2:0] (Clock Select), Select clock source when enable clock select.**
[000]: Clock source div 64 as MCU clock

[001]: Clock source div 2 as MCU clock
[010]: Clock source div 4 as MCU clock
[011]: Clock source div 8 as MCU clock
[100]: Clock source div 16 as MCU clock
[101]: Clock source div 32 as MCU clock
[110]: Clock source div 64 as MCU clock
[111]: Select RTC as CPU clock when CKSE=0; RTC div 2 as CPU clock when CKSE=1

| | MCU speed | 16MHz | RAM | Back to Normal | LVR | RF |
|---|---|---|---|---|---|---|
| Normal CKSE = 0 | 16MHz | ON | ON | X | X | X |
| Normal CKSE = 1 | 8/4/2/1 MHz IRC/RTC | ON | ON | X | X | X |
| PM1 STOP =1 | OFF | OFF | ON | H/W reset / KEYINT / Sleep timer | X | X |
| PM2 STOP=1 PM2F=1 | OFF | OFF | OFF | H/W reset / wakeup key / Sleep timer | OFF | OFF |

Table 14.1 Power manager

X: don't care, it can turn on or off by user setting

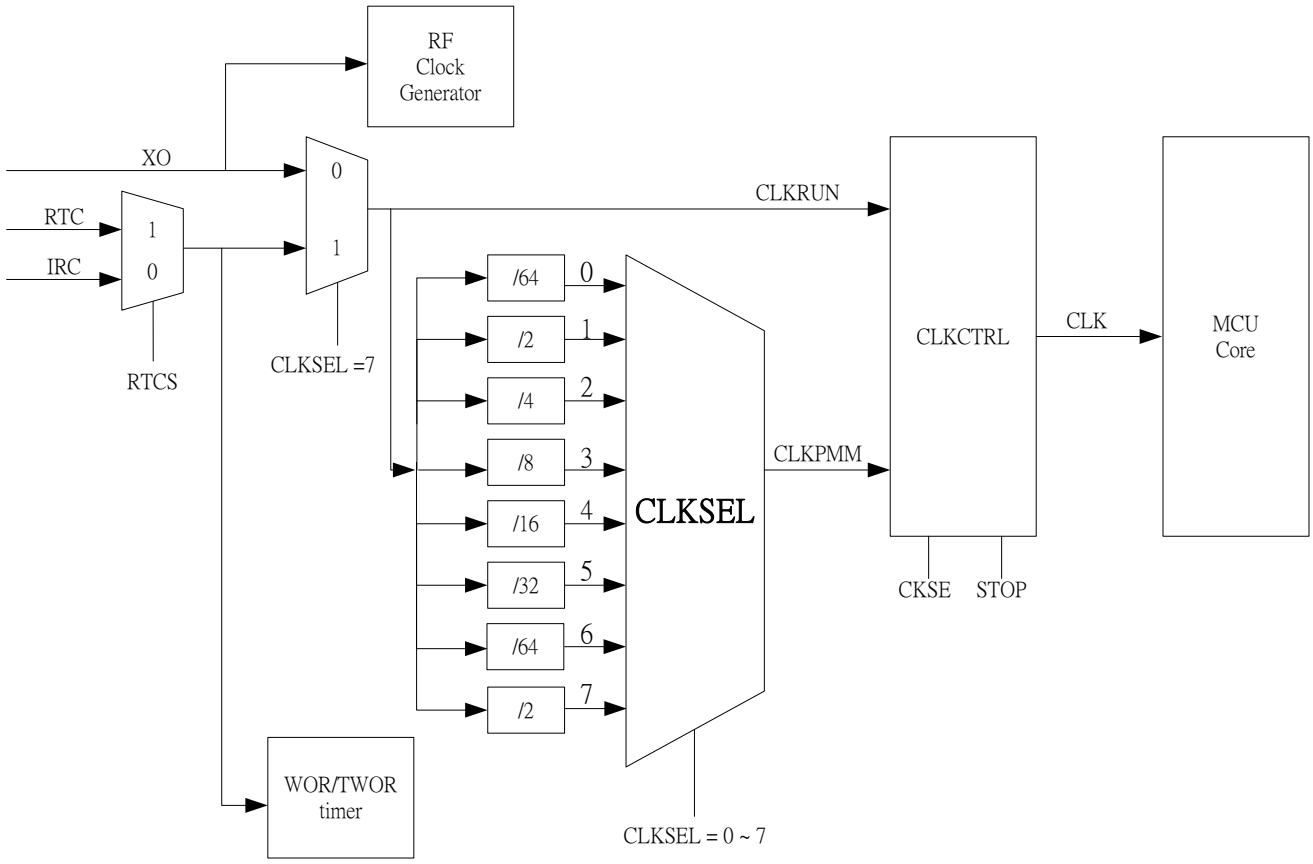



Figure 14.1 Whole chip clock sources

# 15. Flash memory controller

## 15.1 SFR RELATED REGISTERS

FLASH memory is controlled using PCON(0x87)'s PWE bit, FLASHCTRL(0x9A) and FLASHTMR (0x9B). An SFR register named FLASHCTRL (0x9A) is used to control communication between MCU and flash. FLSHCTRL(0x9A) is consisted of 6bits used to control all FLASH related operations. Lower five bits of FLSHTMR (0x9B) named FREQ[4:0] determine real CLK frequency with 1MHz step resolution. FREQ[4:0] after reset is set to 20MHz by default, provides optimal timing for flash macro. Please contact AMICCOM FAE for more details flash operation reference code.

**FLSHCTRL (0x9A)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
|---|---|---|---|---|---|---|---|---|
| - | - | CTRL.5 | CTRL.4 | CTRL.3 | CTRL.2 | CTRL.1 | CTRL.0 | 0x00 |

*Figure 3. FLSHCTRL register*

**FLSHTMR (0x9B)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | FREQ.4 | FREQ.3 | FREQ.2 | FREQ.1 | FREQ.0 | 0x00 |

*Figure 4. FLSHTMR register*

| FREQ[4:0] | Frequency MHz |
|---|---|
| 0x00 | - |
| 0x01 | 1 |
| 0x02 | 2 |
| ... | ... |
| 0x14 | 20 |

*Table 3. FREQ intervals*

Setting higher clock frequency is not supported since given flash macro has limited its clock frequency up to 20MHz by Tkp read cycle time. FLASHCTRL register is write protected by TA enable procedure listed below:

```
CLR   EA ;disable interrupt system
MOV TA, #0xAA
MOV TA, #0x55
MOV FLASHCTRL,#<value> ; Any direct addressing instruction writing FLASHCTRL register.
  SETB   EA   ;Enable interrupt system
```

The Program Write Enable (PWE) bit, located in PCON register, is used to enable/disable PRGROMWR and PRGRRAMWR pin activity during MOVX instructions.

| Address/Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 87h PCON | R/W | SMOD | - | - | PWE | - | SWB | STOP | CKSE |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

When PWE bit is set to logic 1, the MOVX @DPTR,A instruction writes data located in accumulator register into Program Memory addressed by DPTR register (active :DPH:DPL). The MOVX @Rx,A instruction writes data located in accumulator register into program memory addressed by P2 register (bits 15:8) and Rx register(bits 7:0). Program Memory can be read by MOVC only regardless of PWE bit.

CHIP ERASE OPERATION

Chip erase operation is enabled by setting CTRL[5:0]=0x04 of FLSHCTRL register according to MCU TA enable procedure. PCON.PWE bit must be set too, then first MOVX instruction writing to program memory space at address belong to certain FLASH macro begins sector erase operation. During erase operation MCU is halted by asserting FLASHBUSY pin. When FALSH macro has been erased, FLASHBUSY pin id deactivated and FNOP is automatically written. MCU executes next instruction. FLASH macro is blank and ready for new programming. To erase another FLASH macro the whole procedure needs to be repeated with changed MOVX address pointing to certain FLASH macro. Preprograming of whole FLASH macro is executed automatically without any interaction with user, before real chip erase. It extends lifecycle of FLASH macro.

SECTOR ERASE OPERATION

The 16kB FLASH macro has 128 sectors (128B each) which can be erased separately. Sector erase operation is enabled by setting CTRL[5:0]=0x02 of FLSHCTRL register according to MCU TA enable procedure . PCON.PWE bit must be also set. The first MOVX instruction writing to program memory space at selected sector address begins sector erase operation. During sector erase operation MC U is halted by asserting FLASHBUSY pin. When sector has been erased FLASHBUSY pin is deactivated and FNOP is automatically written. MCU executes next instruction. Selected FLASH macro sector(s) is blank and ready for new programming. To erase another sectors whole procedure needs to be repeated. Preprograming of whole sector is executed automatically without any interaction with user, before real sector erase. It extend lifecycle of FLASH macro.

PROGRAM OPERATION

Word program operation is enabled by setting CTRL[5:0]=0x01 of FLSHCTRL register according to MCU TA enable procedure. PCONE.PWE bit must be set too, then each write to program memory space by MOVX instruction addressing odd bytes begins word program operation. During program operation MCU is halted by asserting FLASHBUSY pin. When word has been programmed FLASHBUSY pin is deactivated. MCU executes next instruction which can be (i) programming of next memory word (ii) CTRL[5:0] = 0x00 according to MCU TA enable procedure. Number of programmed by bytes must be always even number(2,4,6…) . For example to program byte at address 0x003, first must be written byte at address 0x002 then second MOVX instruction write at address 0x003 begins physical write to FLASH macro. When number of programmed bytes is not even then it must be filled with extra neutral byte. The neutral bytes does not program any bit in a FLASH macro. Note: Flash memory can programmed once. Please erase sector firstly if change the content in the flash memory.

## 16. In Circuit Emulator (ICE)

A8108 support In Circuit Emulator on chip. It is a real-time hardware debugger as a non-intrusive system. It doesn't need to occupy any hardware resource such as the UART and Timer. User develops firmware complete producing code without any modification using ICE. It helps user to track down hidden bugs within the application running with microcontroller. The ICE with Hardware USB dongle provides a powerful SOC development tool with silicon using 2-wire protocol. The ICE fully supports Keil uVision2/3/4 interface to hardware debuggers. It allows Keil software user to work with uvision2/3/4. For more detail information, please reference Application note.

### 16.1 PIN define

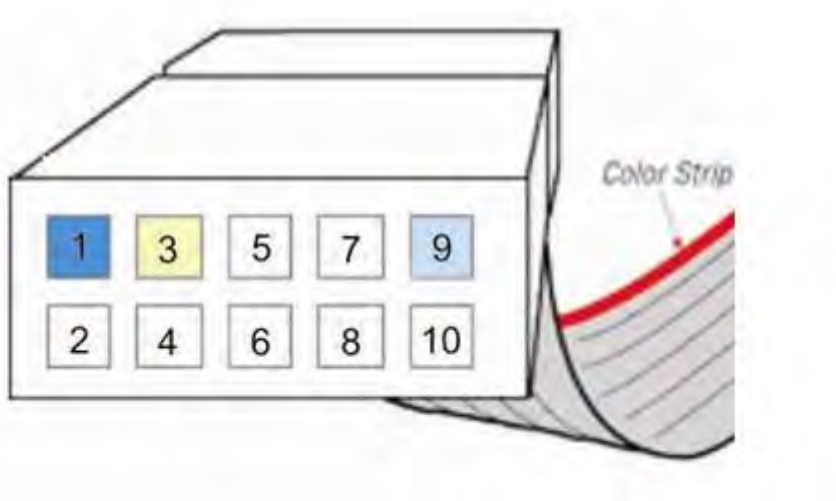



Fig 16.1 The USB connectors

| Pin | Signal name | Description | Pin | Signal name | Description |
|---|---|---|---|---|---|
| 1 | ttck | Clock signal (in) | 2 | GND | Signal Ground |
| 3 | ttdio | Data (io) | 4 | VCCIO | Used to VCCIO detection |
| 5 | NU | Do not use | 6 | NU | Do not use or connect |
| 7 | NU | Do not use | 8 | NU | Do not use or connect |
| 9 | rsto | Reset output (od) | 10 | GND | Signal Ground |

Fig16.2 The Pin define within USB connector

Note: RSTO pin is open drain (od) type active low. It forces logic zero to issue reset. When RSTO is inactive its output is floating, and should be connected to global system reset with pull-up resistor. This pin can be left unconnected.

There are 10 pin in the ICE connectors. 2-wire ICE only use 2 pins (PIN1 and PIN3). The PIN9 is optional and it can connect reset signal. PIN2 and PIN10 are GND pin. PIN4 is VCCIO pin. The recommended circuit shows as the below figure. (Fig16.3). There is a resister (100 ohm) between A8510 and pin connected the connector.

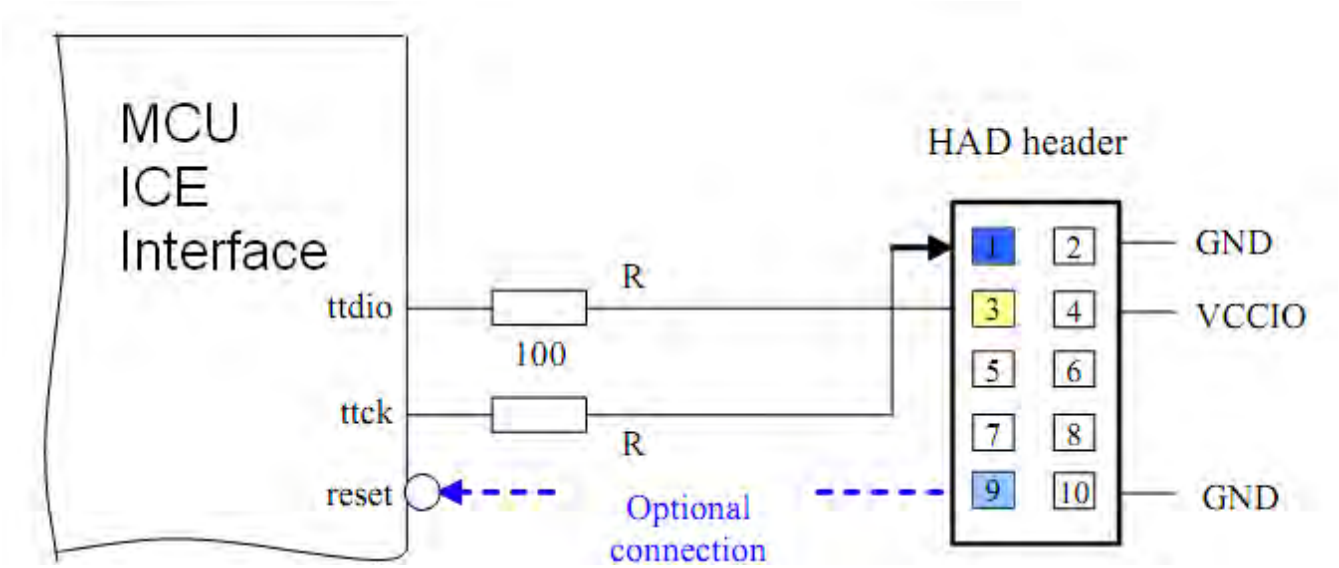


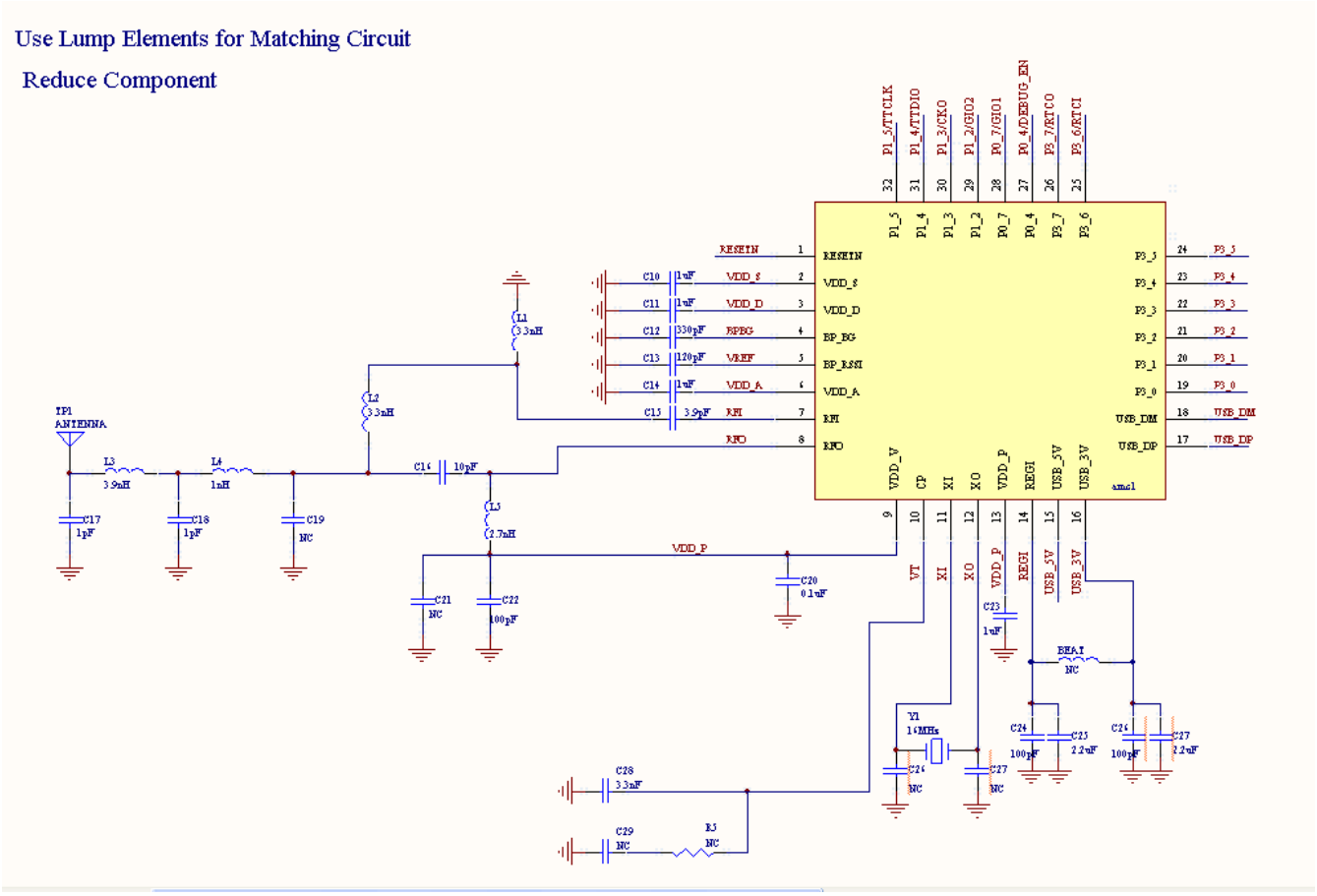

Fig 16.3 The connections between A8108 and USB connectors

## 16.2 ICE Key feature

The ICE supports source level debugging, 2 hardware breakpoint, auto refresh of all register and In system programming (ISP). User can use ICE to download firmware by Keil software or AMICCOM tool.

## 17. Application circuit

**Below are AMICCOM's ref. design module, MD8102, circuit example and its PCB layout.**
**TBD**



## 18. Abbreviations

| | |
|---|---|
| ADC | Analog to Digital Converter |
| AIF | Auto IF |
| FC | Frequency Compensation |
| AGC | Automatic Gain Control |
| BER | Bit Error Rate |
| BW | Bandwidth |
| CD | Carrier Detect |
| CHSP | Channel Step |
| CRC | Cyclic Redundancy Check |
| DC | Direct Current |
| FEC | Forward Error Correction |
| FIFO | First in First out |
| FSK | Frequency Shift Keying |
| ID | Identifier |
| ICE | In Circuit Emulator |
| IF | Intermediate Frequency |
| ISM | Industrial, Scientific and Medical |
| LO | Local Oscillator |
| MCU | Micro Controller Unit |
| PFD | Phase Frequency Detector for PLL |
| PLL | Phase Lock Loop |
| POR | Power on Reset |
| PWM | Pulse width modulation |
| RX | Receiver |
| RXLO | Receiver Local Oscillator |
| RSSI | Received Signal Strength Indicator |
| SPI | Serial to Parallel Interface |
| SYCK | System Clock for digital circuit |
| TX | Transmitter |
| TXRF | Transmitter Radio Frequency |
| VCO | Voltage Controlled Oscillator |
| XOSC | Crystal Oscillator |
| XREF | Crystal Reference frequency |
| XTAL | Crystal |

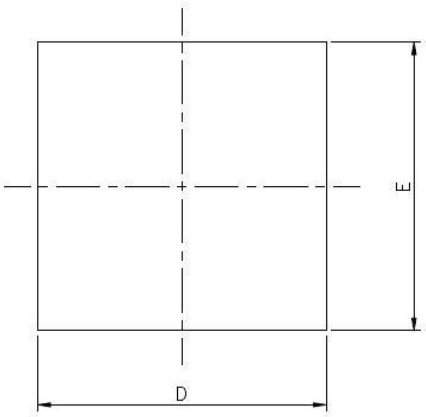
## 19. Ordering Information

| Part No. | Package | Units Per Reel / Tray |
|---|---|---|
| A81X08F6004AQ58/Q | QFN32L , Pb Free, Tape & Reel, -40℃～85℃ | 3K |
| A81X08F6004AQ58 | QFN32L, Pb Free, Tray, -40℃～85℃ | 490EA |
| A81X08F6004AH | Die form, -40℃～85℃ | 100EA |

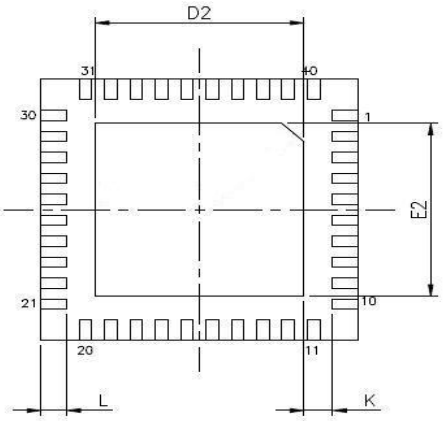
## 20. Package Information

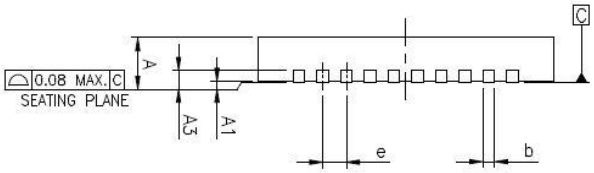
**QFN 32L (5 X 5 X 0.8mm) Outline Dimensions**

Top View




Bottom View

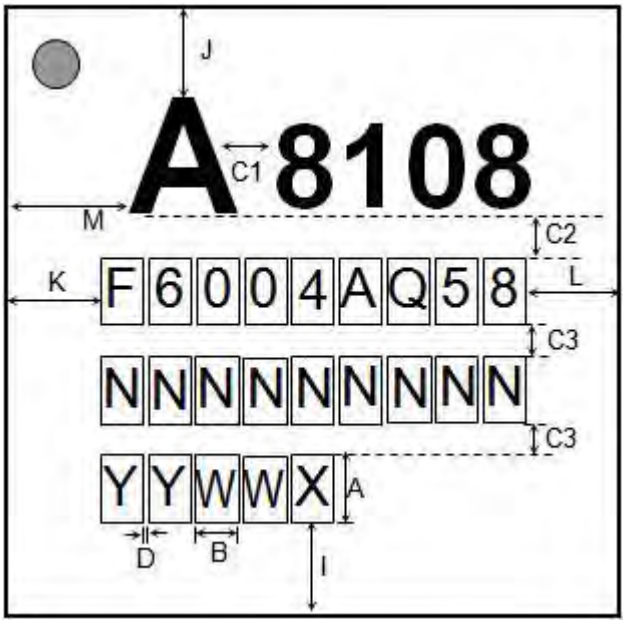



| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.028 | 0.030 | 0.031 | 0.70 | 0.75 | 0.80 |
| $A_1$ | 0.000 | 0.001 | 0.002 | 0.00 | 0.02 | 0.05 |
| $A_3$ | | 0.008 REF | | | 0.20 REF | |
| b | 0.006 | 0.008 | 0.010 | 0.15 | 0.20 | 0.25 |
| D | 0.194 | - | 0.200 | 4.924 | - | 5.076 |
| $D_2$ | 0.126 | - | 0.138 | 3.20 | - | 3.50 |
| E | 0.194 | | 0.200 | 4.924 | | 5.076 |
| $E_2$ | 0.126 | - | 0.138 | 3.20 | - | 3.50 |
| e | | 0.016 | | | 0.40 | |
| L | 0.013 | 0.016 | 0.019 | 0.324 | 0.40 | 0.476 |
| k | | 0.008 | | | 0.2 | |

## 21. Top Marking Information

- Part No. : **A81X08F6004AQ58**
- Pin Count : **32**
- Package Type : **QFN**
- Dimension : **5*5 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**




❖ CHARACTER SIZE : (Unit in mm)

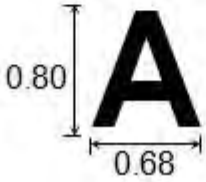
**A : 0.55**
**B : 0.36**
**C1 : 0.25  C2 : 0.3  C3 : 0.2**
**D : 0.03**
**M : 1.5**

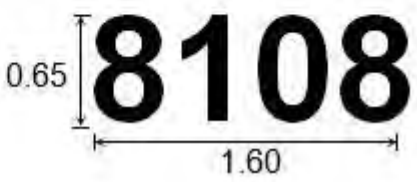
**I=J**
**K=L**

Y Y W W : DATECODE

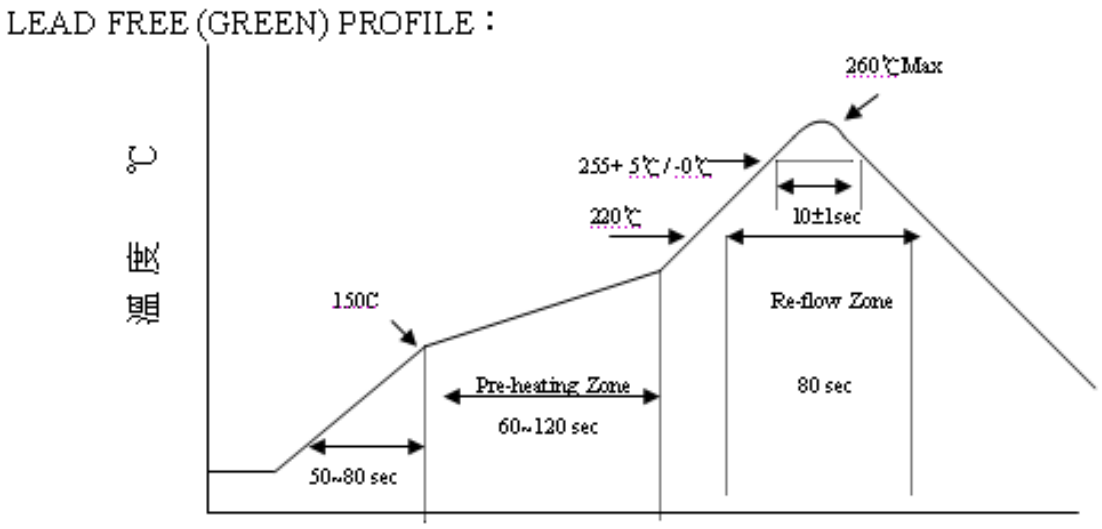
X : PKG HOUSE ID

N N N N N N N N N : LOT NO. (max. 9 characters)

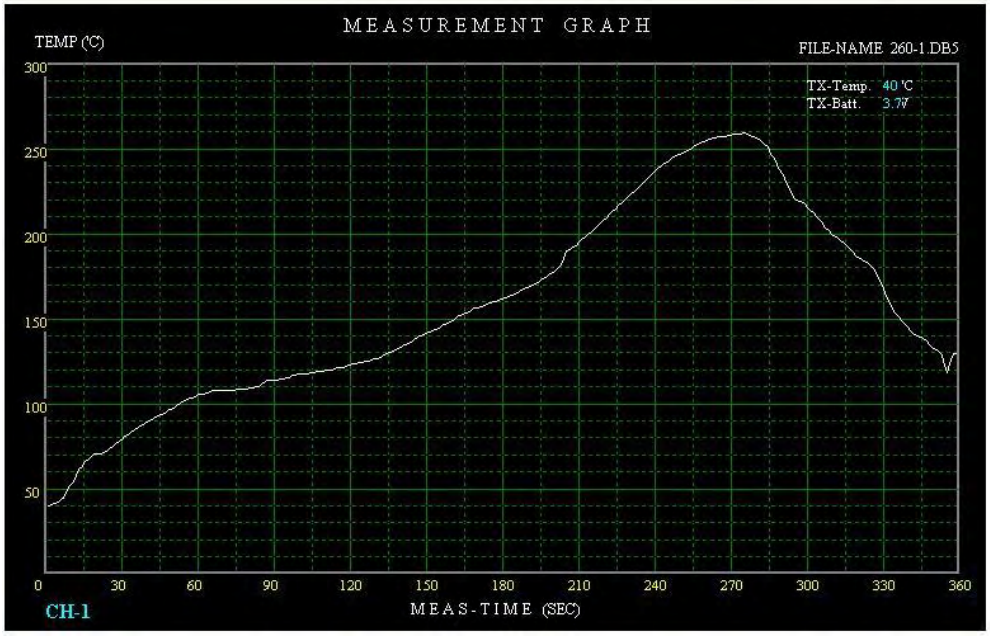


## 22. Reflow Profile

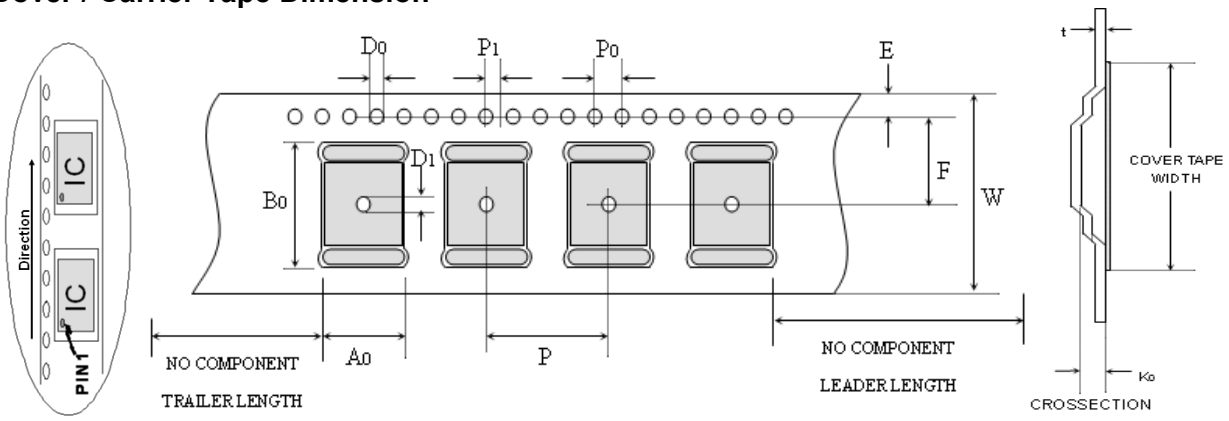



**Actual Measurement Graph**



## 23. Tape Reel Information

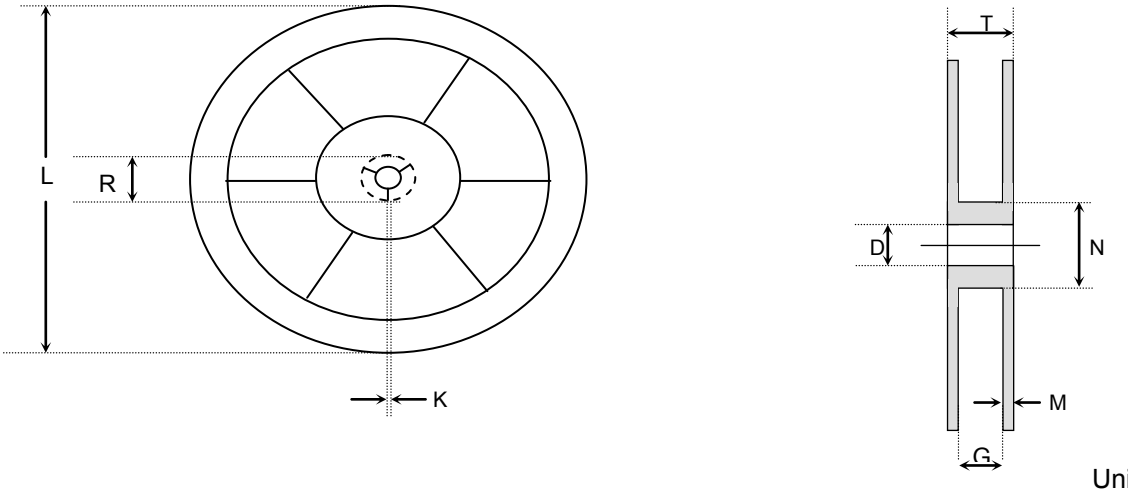
### Cover / Carrier Tape Dimension




Unit: mm

| TYPE | P | A0 | B0 | P0 | P1 | D0 | D1 | E | F | W | K0 | t | Cover tape width |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| QFN3*3 | 8±0.1 | 3.2 5±0.1 | 3.25 ±0.1 | 4±0.2 | 2±0.1 | 1.5±0.1 | 1.5 | 1.75 ±0.1 | 5.5 ±0.05 | 12±0.3 | 1.25 ±0.1 | 0.3 ±0.05 | 9.3±0.1 |
| QFN 4*4 | 8±0.1 | 4.35 ±0.1 | 4.35 ±0.1 | 4±0.2 | 2±0.1 | 1.5±0.1 | 1.5 | 1.75 ±0.1 | 5.5 ±0.05 | 12±0.3 | 1.2 5±0.1 | 0.3 ±0.05 | 9.3±0.1 |
| QFN 5*5 | 8±0.1 | 5.25 ±0.1 | 5.25 ±0.1 | 4±0.2 | 2±0.1 | 1.5±0.1 | 1.5 | 1.75 ±0.1 | 5.5 ±0.05 | 12±0.3 | 1.25 ±0.1 | 0.3 ±0.05 | 9.3±0.1 |
| SSOP | 12±0.1 | 8.2±1 | 8.8±1.5 | 4.0±0.1 | 2.0±0.1 | 1.5±0.1 | 1.5±0.1 | 1.75 ±0.1 | 7.5±0.1 | 16±0.1 | 2.1±0.4 | 0.3 ±0.05 | 13.3 ±0.1 |

### REEL DIMENSIONS




Unit: mm

| TYPE | G | N | M | D | K | L | R |
|---|---|---|---|---|---|---|---|
| QFN | 12.9±0.5 | 102 REF±2.0 | 2.3±0.2 | 13.15±0.35 | 2.0±0.5 | 330±3.0 | 19.6±2.9 |
| SSOP | 16.3±1 | 102 REF±2.0 | 2.3±0.2 | 13.15±0.35 | 2.0±0.5 | 330±3.0 | 19.6±2.9 |

## 24. Product Status

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| Objective | Planned or Under Development | This data sheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | Engineering Samples and First Production | This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| No Identification | Noted Full Production | This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Obsolete | Not In Production | This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only. |

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