Document Title

A8125 Data Sheet, 2.4GHz FSK/GFSK SoC

Revision History

Rev. No.	History	Issue Date	Remark
0.1	Initial issue.	Aug. 2014	Preliminary

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1. General Description

A8125 is a high performance and low cost 2.4GHz ISM band FSK/GFSK system-on-chip (SOC) wireless transceiver chip. This device integrates high speed pipeline 8051 MCU, 16KBytes In-system programmable flash memory, 256Bytes internal data RAM, 256Byte external data RAM, various powerful functions and excellent performance of 2.4GHz RF transceiver. A8125 has various operating modes, making it highly suited for systems where ultra-low power consumption is required.

A8125 supports 2.4GHz IEEE 802.15.4 MAC layers and physical layers except RF modulation. A8125 does not support DSSS and choice GFSK/ FSK modulation. Besides, A8125 also supports preparatory data frame (protocol) to communicate with AMICCOM 2.4GHz RFIC, like A7125 and A7137.

A8125 has excellent RF performance with maximum 5dBm output power and good sensitivity (-90dBm @ 2Mbps). The data rate is adjustable by Data Rate Registers from 1M ~ 2Mbps. A8125 supports fast settling time (90 us) for frequency hopping system. For packet handling, A8125 has built-in separated 64-bytes TX/RX FIFO for data buffering and burst transmission, auto-ack and auto-resend, CRC for error packet filtering, FEC for 1-bit data correction per code word, RSSI for clear channel assessment, thermal sensor for monitoring relative temperature, WOR (Wake on RX) function to support periodically wake up from sleep mode to RX mode and listen for incoming packets without MCU interaction, data whitening for data encryption / decryption. Those functions are very easy to use while developing a wireless system.

2. Typical Applications

- Wireless sensor network
- 2.4GHz active RFID
- 2400 ~ 2483.5 MHz ISM system
- Smart remote controller
- Home and building automation
- Wireless toys and game controllers

3. Feature

- Package size (QFN5 X5, 40 pins and 32 pins).
- High performance pipeline complicated 8051
- Operation clock: 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of crystal oscillator.
- 16KByte Flash memory with copy protection, 256Byte internal data RAM, 256Byte external data RAM
- UART, I^2C, SPI serial communication
- 3 16/8-bit counter/timers
- 2 Channel PWM
- Watchdog timer
- Sleep timer
- In-Circuit Debugger
- In-System programming/ In-Application programming
- Key wake-up
- 24 GPIO
- Support 2.4GHz FSK/GFSK modulation.
- Low RX current consumption (24mA)
- Low TX current consumption (25mA @ 5 dBm).
- PM3 current (0.6 uA)
- On chip regulator, support input voltage 2.0 ~ 3.6 V.
- Programmable TX power level from -20 dBm to 5 dBm.
- High sensitivity: -90dBm at 2Mbps on-air data rate
- Fast settling time (90 us) for frequency hopping system.
- Support low cost crystal (16 MHz).
- Support RTC clock (32.768KHz)
- ONE register setting for new channel frequency.
- 8-bits Digital RSSI for clear channel indication.
- Auto Calibrations.
- Auto IF function.
- Clear channel assessment (CCA).
- Auto-ACK and Auto-resend scheme.
- Auto RSSI measurement.
- Auto CSMA-CA.
- Auto FCS (CRC) and Filtering.
- Separated 64 bytes FIFO for RX and TX.

- Support ED (Energy Detect) for CCA.
- Integrated RC Oscillator for WOR /TWOR function.
- Built-in Battery Detect, Thermal Sensor and Crystal load capacitors.

4. Pin Configurations

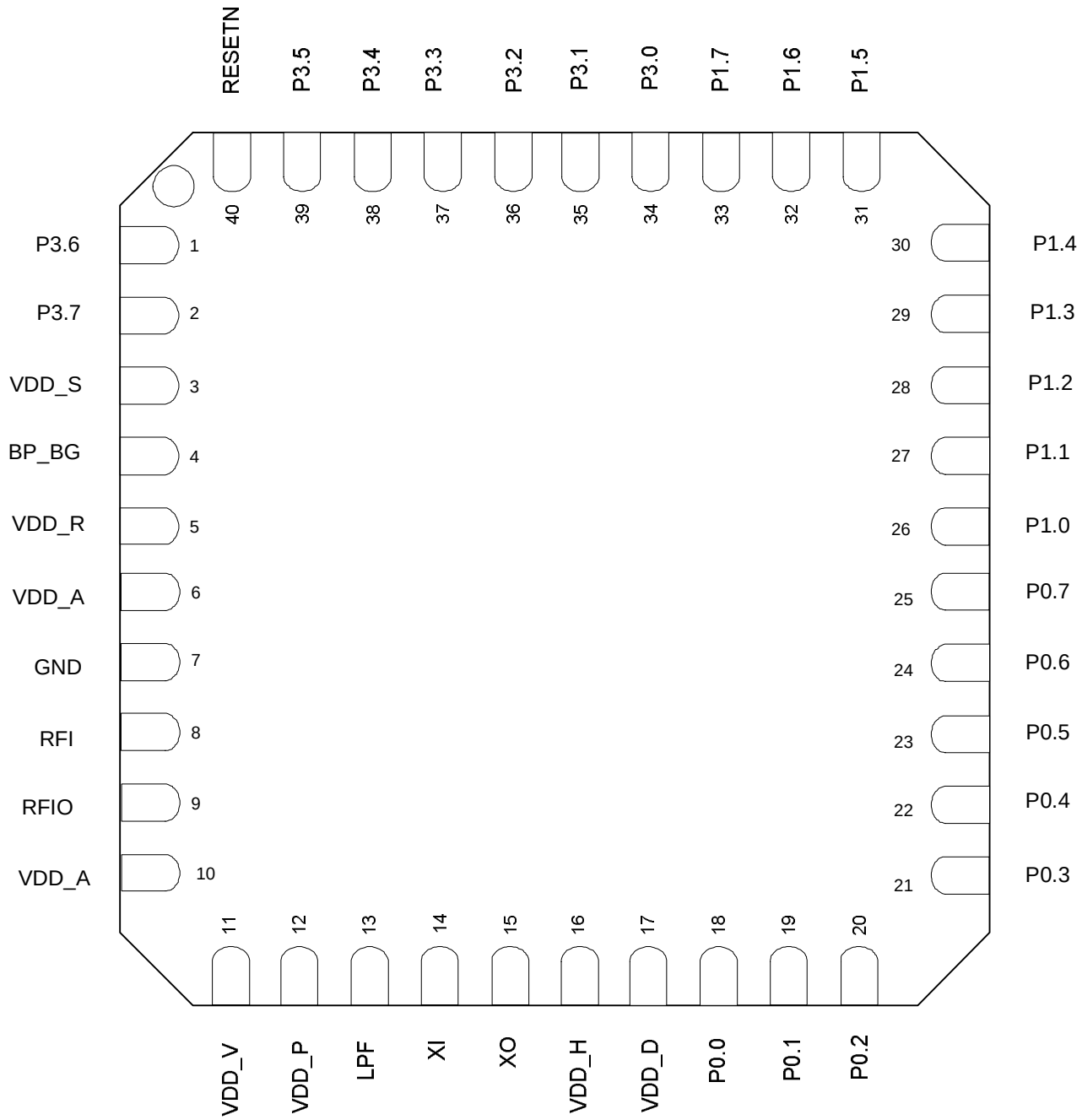


Fig 4-1. A8125 QFN 5x5 40 pin Package Top View

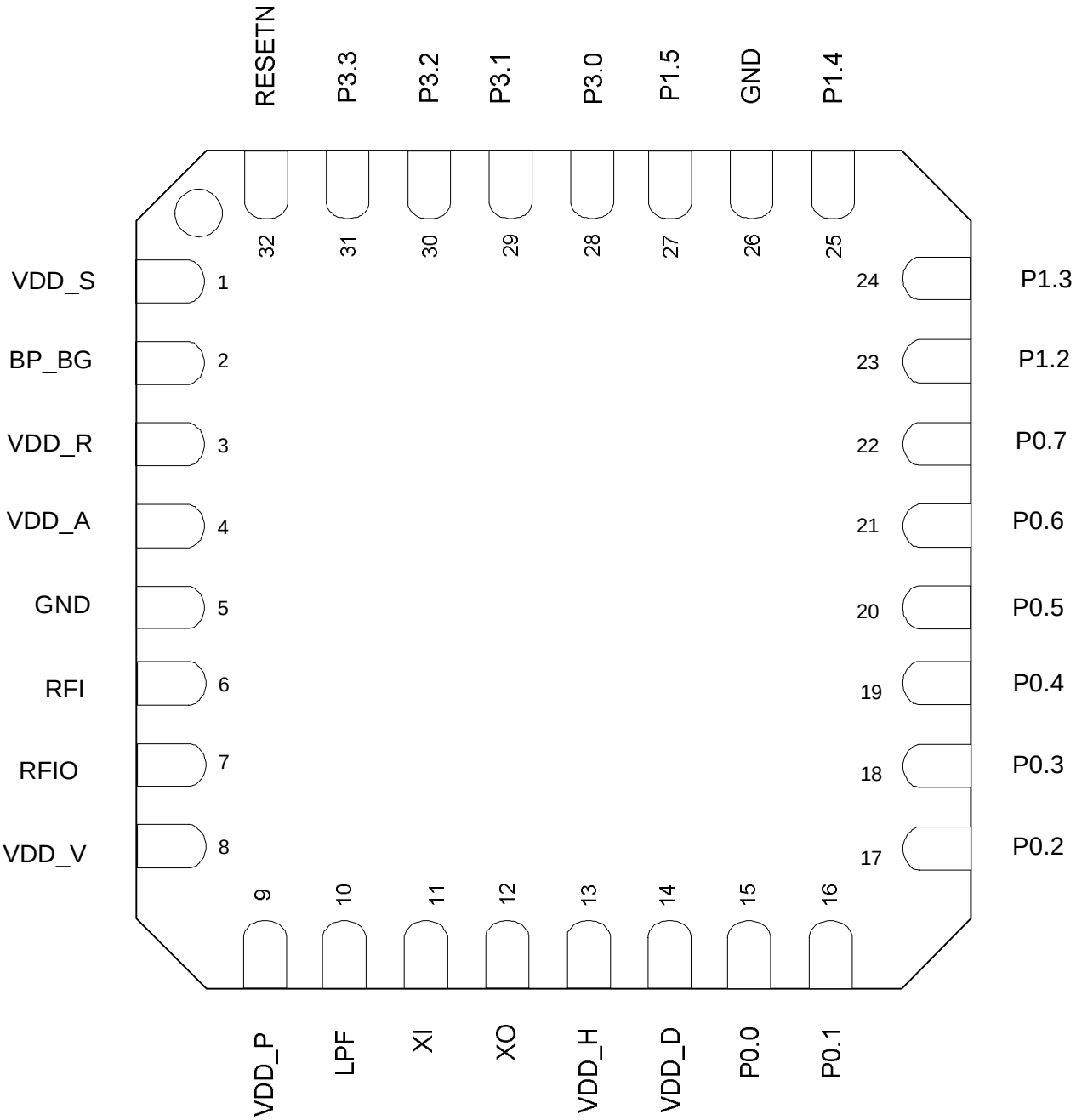


Fig 4-2. A8125 QFN 5x5 32 pin Package Top View

5. Pin Description (I: input; O: output, I/O: input or output)

Pin No.	Symbol	I/O	Function Description
1	P3.6	DIO/AI	**RTC_I**
2	P3.7	DIO/AO	**RTC_O**
3	VDD_S	AO	VDD_S supply voltage output.
4	BP_BG	AO	Band gap output.
5	VDD_R	AO	Auxiliary supply for 8 bit ADC input circuit.
6	VDD_A	AO	VDD_A supply voltage output.
7	GND	G	
8	RFI	AI	**RF input.**
9	RFIO	AO	**RF output/input.**
10	VDD_A	AO	VDD_A supply voltage output.
11	VDD_V	AI	**VCO supply voltage input.**
12	VDD_P	AO	**PLL supply voltage output.**
13	LPF	AO	PLL loop filter output. Connect to loop filter.
14	XI	AI	Crystal oscillator input.
15	XO	AO	Crystal oscillator output.
16	VDD_H	AI	**Regulator input.**
17	VDD_D	AO	**VDD_D supply voltage output.**
18	P0.0	DIO	**SPI_SCLK**
19	P0.1	DIO	**SPI_MOSI**
20	P0.2	DIO	**SPI_MISO**
21	P0.3	DIO	**SPI_SSEL**
22	P0.4	DIO	**GPIO/ ICE mode**
23	P0.5	DIO	**I2C_SCL**
24	P0.6	DIO	**I2C_SDA**
25	P0.7	DIO	**INT2 /GIO1**
26	P1.0	DIO	**Timer2_T2**
27	P1.1	DIO	**Timer2_T2EX**
28	P1.2	DIO	**INT3 /GIO2**
29	P1.3	DIO	**INT4/ CKO**
30	P1.4	DIO	**TTAG_TTDIO**
31	P1.5	DIO	**TTAG_TTCK**
32	P1.6	DIO	**PWM0**
33	P1.7	DIO	**PWM1**
34	P3.0	DIO	**UART0_RX**
35	P3.1	DIO	**UART0_TX**
36	P3.2	DIO/AI	**INT0/Gate0/ADC0**
37	P3.3	DIO/AI	**INT1/Gate1/ADC1**
38	P3.4	DIO/AI	**Timer0_T0/ADC2**
39	P3.5	DIO/AI	**Timer1_T1/ADC3**
40	RESETN	DI	**RESETN**

	Back side plate	G	**Ground.** **Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

Pin No.	Symbol	I/O	Function Description
1	VDD_S	AO	VDD_S supply voltage output.
2	BP_BG	AO	Band gap output.
3	VDD_R	AO	Auxiliary supply for 8 bit ADC input circuit.
4	VDD_A	AO	VDD_A supply voltage output.
5	GND	G	
6	RFI	AI	**RF input.**
7	RFIO	AO	**RF output/input.**
8	VDD_V	AI	**VCO supply voltage input.**
9	VDD_P	AO	**PLL supply voltage output.**
10	LPF	AO	PLL loop filter output. Connect to loop filter.
11	XI	AI	Crystal oscillator input.
12	XO	AO	Crystal oscillator output.
13	VDD_H	AI	**Regulator input.**
14	VDD_D	AO	**VDD_D supply voltage output.**
15	P0.0	DIO	**SPI_SCLK**
16	P0.1	DIO	**SPI_MOSI**
17	P0.2	DIO	**SPI_MISO**
18	P0.3	DIO	**SPI_SSEL**
19	P0.4	DIO	**GPIO/ ICE mode**
20	P0.5	DIO	**I2C_SCL**
21	P0.6	DIO	**I2C_SDA**
22	P0.7	DIO	**INT2 /GIO1**
23	P1.2	DIO	**INT3 /GIO2**
24	P1.3	DIO	**INT4/ CKO**
25	P1.4	DIO	**TTAG_TTDIO**
26	GND	G	
27	P1.5	DIO	**TTAG_TTCK**
28	P3.0	DIO	**UART0_RX**
29	P3.1	DIO	**UART0_TX**
30	P3.2	DIO/AI	**INT0/Gate0/ADC0**
31	P3.3	DIO/AI	**INT1/Gate1/ADC1**
32	RESETN	DI	**RESETN**
	Back side plate	G	**Ground.** **Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

6. Chip Block Diagram

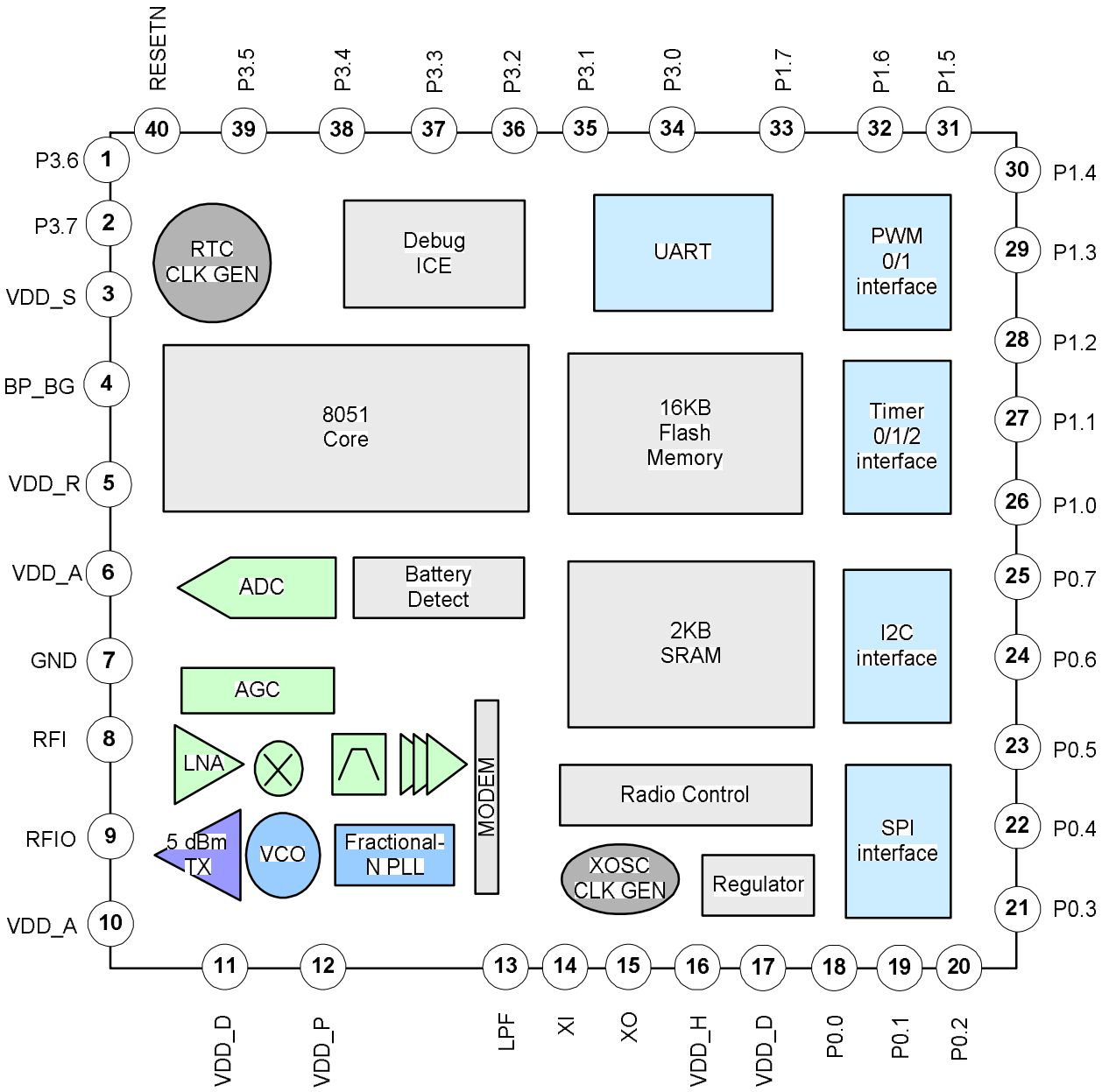


Fig 6-1. A8125 QFN40L Block Diagram

7. Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 2.1	V
Input RF level		10	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	+/- 2KV*	V
	MM	+/- 100V*	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).
* RFIO PIN is HBM ± 1500V and MM ± 75V.

8. Electrical Specification

(Ta=25℃, VDD=3.3V, data rate= 2Mbps, F_{XTAL} =16MHz, On Chip Regulator = 1.8V, PN9 pattern, with matching network and low pass filter, unless otherwise noted.)

Parameter	Description	Minimum	Typical	Maximum	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage (VDD)	Regulator supply input	2.0	3.3	3.6	V
Current Consumption (Digital only and RF in sleep mode)	Normal		4.5		mA
	PM1 with sleep timer		3.3		uA
	PM2 with sleep timer		3.3		uA
	PM3 with sleep timer		1.2		uA
	PM3 without sleep timer		0.6		uA
Current Consumption (MCU in normal mode,no peripheral active)	Standby Mode		6		mA
	PLL Mode		12		mA
	RX Mode (AGC On)		24		mA
	TX Mode (@5dBm output)		25		mA
Phase Locked Loop					
X'TAL Settling Time[1]	49S DIP Xtal		0.5		ms
X'TAL Frequency (F_{XTAL})			**16**		MHz
X'TAL Load Capatitance			18		pF
X'TAL ESR				80	ohm
PLL Setting Time	@Loop BW = 200 KHz		30		μs
Transmitter					
Carrier Frequency		2400		2483.5	MHz
Data rate		1M	2M	2M	bps
TX Power Control Range	With external LPF	-20	0	5	dBm
Out Band Spurious Emission [2]	30MHz~1GHz			-36	dBm
	1GHz~12.75GHz			-30	
	1.8GHz~ 1.9GHz			-47	
	5.15GHz~ 5.3GHz			-47	
TX Settling Time	@ Loop BW = 200KHz		60		μs
Receiver					
Sensitivity	BER = 0.1% @ 2Mbps		-90		dBm
IF Frequency (F_{IF})	1Mbps		1		MHz
	2Mbps		2		MHz
Channel rejection Channel space is 2MHz.	Co-Channel (C/Io)		11		dB
	1st Adjacent Channel (C/I_1)		2		dB
	2nd Adjacent Channel (C/I_2)		-18		dB
	3rd Adjacent Channel (C/I_3)		-28		dB
	Image (C/I_{IM})		-12		dB
Maximum Operating Input Power	@RF input (BER = 0.1%)			3	dBm
Spurious Emission [2]	30MHz~1GHz			-57	dBm
	1GHz~12.75GHz			-47	
RSSI Range	@RF input	-100		-20	dBm
RX Settling Time	@ Loop BW =200 KHz		60		μs
SPI					

SCK period			4		MHz
MISO setup		10			ns
MISO hold		10			ns
8bit SAR ADC					
SAR Conversion clock rate			4		MHz
Conversion time in SAR clocks		20			clock
Input voltage range		0.3		1.5	V
Regulator					
Regulator settling time	Connected to 0.2uF		200		µs
Band-gap reference voltage			1.2		V
Regulator output voltage			1.8		V
Digital I/O DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Source current	@VOH = 2.4V		8		mA
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V
Sink current	@VOL = 0.4V		5		mA

9. SFR & RFR(Radio Frequency Register)

A8125 contains standard 8051 SFRs(special function registers) and RFR (RF control registers). A8051's SFR location is almost the same as the standard 8052 SFR location. RFR is Radio Frequency Registers are located in XDATA spaces and located in 0x0800 ~ 0x08FF. For more detail information, please reference Section 9.2.

9.1 SFR Overview

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	EIP	OSCCON						
0xF0	B	I2CSADR	I2CSCR	I2CSBUF	I2CMSA	I2CMCR	I2CMBUF	I2CMTP
0xE8	EIE			TA	SPCR	SPSR	SPDR	SSCR
0xE0	ACC	P3OE	P3PUN	P3WUN	SPCR1	SPSR1	SPDR1	SSCR1
0xD8	WDCON	P1OE	P1PUN	P1WUN				
0xD0	PSW	P0OE	P0PUN	P0WUN				
0xC8	T2CON	T2IF	RCAP2L	RCAP2H	TL2	TH2		DEVICR
0xC0								
0xB8	IP	PCONE	RSFLAG	IOSEL				
0xB0	P3	PWM1CON	PWM1H	PWM1L				
0xA8	IE	PWM0CON	PWM0H	PWM0L				
0xA0	P2							
0x98	SOCN0	SBUF	FLASHCTRL	FLASHMR				
0x90	P1	EIF					ENSPADDR	ENSPDATA
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	DPSADDR
0x80	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON

Table 9.1 A8125 Special Function Registers (SFRs) table

: It means bit-addressable

: It means reserved.

Following are description of SFRs related to the operation of A8125 System Controller. Detailed descriptions of the remaining SFRs are including the sections of the datasheet associated with their corresponding system function. The arithmetic section of the processor performs extensive data manipulation and is comprised of the 8-bit arithmetic logic unit (ALU), an ACC(0xE0) register, B(0xF0) register and PSW(0xD0) register.

PSW (Address: D0h)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D0h PSW	R/W	CY	AC	F0	RS1	RS2	OV	F1	P
Reset		0	0	0	0	0	0	0	0

Program Status Word register

The ALU performs typical arithmetic operations as: addition, subtraction, multiplication, division and additional operations such as: increment, decrement, BCD-decimal-add-adjust and compare. Within logic unit are performance: AND, OR, Exclusive OR, complement and rotation. The Boolean processor performance the bit operations as: set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry.

CY - Carry flag

AC - Auxiliary carry
F0 - General purpose flag 0
RS[1:0] - Register bank select bits

RS[1:0]	Function description
00	- Bank 0, data address 0x00-0x07
01	- Bank 1, data address 0x08-0x0F
10	- Bank 2, data address 0x10-0x17
11	- Bank 3, data address 0x18-0x1F

OV - Overflow flag
F1 - General purpose flag 1
P - Parity flag
The PSW contains several bits that reflect the current state of the MCU.

ACC (Address: E0h)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E0h ACC	R/W								
Reset		0	0	0	0	0	0	0	0

Accumulator ACC Register

B (Address: F0h)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F0h B	R/W								
Reset		0	0	0	0	0	0	0	0

B Register

The B register is used during multiply and divide operations. In other cases may be used as normal SFR.

9.2 RFR Overview

Address / Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0800h Strobe control	W	Strobe3	Strobe2	Strobe1	Strobe0	--	--	--	--
	R	--	P_GO1	P_GO2	P_CKO	FPEN	RFSTATE2	RFSTATE1	RFSTATE0
0801h RESET control	W	RESETN	FWPRN	FRPRN	--	FIFORN	BFCRN	--	--
	R	CSMAF	CCAF	CRCF	CER	XER	PLLER	TRER	TRSR
0802h Mode control	W	DFCRC	--	**WOT**	DFCD	WORE	FMT	FMS	ADCM
	R	FECF	FPF	--	CD	WORE	FMT	FMS	ADCM
0803h Mode select	W	--	DLS	PNS	PNIVS	ACKS	ARTS	CSMAS	SLOT
0804h Calc	R/W	--	ADCC	RCC	VCC	VBC	VDC	FBC	RSSC
0805h PHR	R/W	PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
0806h TWUNF	R/W	RNTWUN	RNTWUN	RNTWUN	RNTWUN	RNTWUN	RNTWUN	RNTWUN	TWUNF
0807h RC OSC I	W	RCKS1	RCKS0	WUS1	WUS0	RTCS	IRCHC	ROE	TWWS
0808h RC OSC II	W	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
	R	RCT7	RCT6	RCT5	RCT4	RCT3	RCT2	RCT1	RCT0
0809h	W	TGNUM11	TGNUM10	TGNUM9	TGNUM8	MVS1	MVS0	MRCT9	MRCT8

RC OSC III	R	NUMLH11	NUMLH10	NUMLH9	NUMLH8	--	--	RCT9	RCT8
080Ah RC OSC IV	W	TGNUM7	TGNUM6	TGNUM5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0
	R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
080Bh RC OSC V	W	RCOT2	RCOT1	RCOT0	CX4	CX3	CX2	CX1	CX0
080Ch CKO Pin	W	FIFOSS	TRDC	CKOS2	CKOS1	CKOS0	CKOI	MRC	DCKS
080Dh GIO1 Pin I	W	--	--	GIOS3	GIOS2	GIO1S1	GIO1S0	GIO1I	--
080Eh GIO2 Pin II	W	--	--	GIO2S3	GIO2S2	GIO2S1	GIO2S0	GIO2I	--
080Fh STM	W	--	--	STM5	STM4	STM3	STM2	STM1	STM0
0810h Data Rate Clock	W	MDR1	MDR0	GRC3	GRC1	GRC1	GRC0	CGFS1	CGFS0
0811h PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
0812h PLLII	W	--	--	--	--	--	--	--	BIP8
0813h PLL III	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
0814h PLL IV	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
0815h PLL V	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
0816h PLL VI	W	-	CHR14	CHR13	CHR12	CHR11	CHR10	CHR9	CHR8
0817h PLL VII	W	CHR7	CHR6	CHR5	CHR4	CHR3	CHR2	CHR1	CHR0
0818h Channel Group I	W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
0819h Channel Group II	W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
081Ah TX I	W	TCPS	PADL	TXDI	TME	--	FDP2	FDP1	FDP0
081Bh TX II	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
081Ch RX	W	IGCR	LGCR	MGCR	RCP2	RCP1	RCP0	DMG	RXDI
081Dh RX Gain I	R/W	IGS1	IGS0	LGS2	LGS1	LGS0	MGS2	MGS1	MGS0
081Eh RX Gain II	R/W	PKIS1	PKIS0	VTHS2	VTHS1	VTHS0	VTLS2	VTLS1	VTLS0
		RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
081Fh RX Gain III	W	LMS	RSSL6	RSSL5	RSSL4	RSSL3	RSSL2	RSSL1	RSSL0
	R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
0820h RX Gain IV	W	AGS1	AGS0	IFAS	IFPK	MHC	LHC1	LHC0	AGCE
	R	RU7	RU6	RU5	RU4	RU3	RU2	RU1	RU0
0821h ADC	W	CDTH7	CDTH6	CDTH5	CDTH4	CDTH3	CDTH2	CDTH1	CDTH0
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
0822h ADC Control	W	--	CDM	ADCOM1	ADCOM0	MRHL	--	AVGS1	AVGS0
0823h IF Calibration I	W	IFHCM	IFTS	--	MFBS	MFB3	MFB2	MFB1	MFB0
	R	VTB1	VTB0	--	FBCF	FB3	FB2	FB1	FB0
0824h IF Calibration II	R				FCD4	FCD3	FCD2	FCD1	FCD0
0825h VCO current Calibration	W	--	VCCS1	VCCS0	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0

0826h VCO band Calibration I	W	LPFT1	LPFT0	LPFS	MDAGS	MVBS	MVB2	MVB1	MVB0
	R	--	--	--	--	VBCF	VB2	VB1	VB0
0827h VCO band Calibration II	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
0828h VCO deviation Calibration I	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
0829h VCO deviation Calibration II	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
082Ah VCO modulation Delay	W	DEVCM	--	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
082Bh Channel Offset	W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
082Ch Battery detect	W	ATP1	ATP0	BLE	BDV2	BDV1	BDV0	BGS	BDE
	R	--	--	--	--	--	--	--	BDF
082Dh CBG	W	PD_LVD	PDNR	REGCL	CBG4	CBG3	CBG2	CBG1	CBG0
082Eh TX test	W	SLF1	SLF0	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
082Fh Rx DEM test I	W	ULS	SLF2	DCM1	DCM0	LQICE	ARSSI	AIF	LQIS
	R	LQIV7	LQIV6	LQIV5	LQIV4	LQIV3	LQIV2	LQIV1	LQIV0
0830h Rx DEM test II	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
	R	DCO7	DCO6	DCO5	DCO4	DCO3	DCO2	DCO1	DCO0
0831h Charge Pump Current	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
0832 Crystal test	W	CGS	XS	XCL3	XCL2	XCL1	XCL0	XCC	XCP
0833 PLL test	W	XEC	CPS	PRRC1	PRRC0	PRIC1	PRIC0	SDPW	NSDO
0834 VCO test	W	TLB1	TLB0	CPCH1	CPCH0	RLB1	RLB0	VCBS1	VCBS0
0835 Delay	W	--	WSEL1	WSEL0	PDL1	PDL0	TDL2	TDL1	TDL0
0836 AGC DLY	W	AGC_DLY 1	AGC_DLY 0	RS_DLY1	RS_DLY0	AGCKS1	AGCKS0	--	--
0837 ART DLY1	W	RTRTD3	RTRTD2	RTRTD1	RTRTD0	RTTRD3	RTTRD2	RTTRD1	RTTRD0
0838 ART DLY2	W	RTRAT7	RTRAT6	RTRAT5	RTRAT4	RTRAT3	RTRAT2	RTRAT1	RTRAT0
0839 CSMA DLY	W	ATLP2	ATLP1	ATLP0	CST1	CST0	MaxNB2	MaxNB1	MaxNB0
083Ah BE	W	MaxBE3	MaxBE2	MaxBE1	MaxBE0	MinBE3	MinBE2	MinBE1	MinBE0
083Bh PTRS	W	ACKD3	ACKD2	ACKD1	ACKD0	PTRS3	PTRS2	PTRS1	PTRS0
083Ch INTST	W	ISTRN	--	CCAM1	CCAM0	ERX	EDS	CCAS	--
	R	INT	IST3	IST2	IST1	IST0	EDS	CCAS	FLAG
083Dh ADFC I	W	FADDE	ACBEN	ACDAT	ACACK	ACCMD	ACRES	PCORR	MAXVER1
083Eh ADFC II	W	MAXVER0	RESMUX2	RESMUX1	RESMUX0	--	SLT2	SLT1	SLT0
083Fh ADFF 1	W	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8

0840h ADFF 2	W	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
0841h ADFF 3	W	SADD15	SADD14	SADD13	SADD12	SADD11	SADD10	SADD9	SADD8
0842h ADFF 4	W	SADD7	SADD6	SADD5	SADD4	SADD3	SADD2	SADD1	SADD0
0843h ADFF 5	W	LADD63	LADD62	LADD61	LADD60	LADD59	LADD58	LADD57	LADD56
0844h ADFF 6	W	LADD55	LADD54	LADD53	LADD52	LADD51	LADD50	LADD49	LADD48
0845h ADFF 7	W	LADD47	LADD46	LADD45	LADD44	LADD43	LADD42	LADD41	LADD40
0846h ADFF 8	W	LADD39	LADD38	LADD37	LADD36	LADD35	LADD34	LADD33	LADD32
0847h ADFF 9	W	LADD31	LADD30	LADD29	LADD28	LADD27	LADD26	LADD25	LADD24
0848h ADFF 10	W	LADD23	LADD22	LADD21	LADD20	LADD19	LADD18	LADD17	LADD16
0849h ADFF 11	W	LADD15	LADD14	LADD13	LADD12	LADD11	LADD10	LADD9	LADD8
084Ah ADFF 12	W	LADD7	LADD6	LADD5	LADD4	LADD3	LADD2	LADD1	LADD0
084Bh ACK FIFO I	W	AFCF7	AFCF6	AFCF5	AFCF4	AFCF3	AFCF2	AFCF1	AFCF0
084Ch ACK FIFO II	W	AFCF15	AFCF14	AFCF13	AFCF12	AFCF11	AFCF10	AFCF9	AFCF8
084Dh PN I	W	PNIV15	PNIV14	PNIV13	PNIV12	PNIV11	PNIV10	PNIV9	PNIV8
	R	PNO15	PNO14	PNO13	PNO12	PNO11	PNO10	PNO9	PNO8
084Eh PN II	W	PNIV7	PNIV6	PNIV5	PNIV4	PNIV3	PNIV2	PNIV1	PNIV0
	R	PNO7	PNO6	PNO5	PNO4	PNO3	PNO2	PNO1	PNO0
084Fh RBTO I	W	RBTO7	RBTO6	RBTO5	RBTO4	RBTO3	RBTO2	RBTO1	RBTO0
	R	RBTD7	RBTD6	RBTD5	RBTD4	RBTD3	RBTD2	RBTD1	RBTD0
0850h RBTO II	W	RBTO15	RBTO14	RBTO13	RBTO12	RBTO11	RBTO10	RBTO9	RBTO8
	R	RBTD15	RBTD14	RBTD13	RBTD12	RBTD11	RBTD10	RBTD9	RBTD8
0851h RBT I	W	RBT7	RBT6	RBT5	RBT4	RBT3	RBT2	RBT1	RBT0
	R	BFCNT7	BFCNT6	BFCNT5	BFCNT4	BFCNT3	BFCNT2	BFCNT1	BFCNT0
0852h RBT II	W	RBT15	RBT14	RBT13	RBT12	RBT11	RBT10	RBT9	RBT8
	R	BFCNT15	BFCNT14	BFCNT13	BFCNT12	BFCNT11	BFCNT10	BFCNT9	BFCNT8
0853h RBT III	W	RBT23	RBT22	RBT21	RBT20	RBT19	RBT18	RBT17	RBT16
	R	BFCNT23	BFCNT22	BFCNT21	BFCNT20	BFCNT19	BFCNT18	BFCNT17	BFCNT16
0854h TXG	W	TMDE	FS	GDR	HFR	XDS	DEVGD2	DEVGD1	DEVGD0
0855h TXG1	W	PA_HCS	PWORS	PACTL	TRT2	TRT1	TRT0	TXUDS1	TXUDS0
0856h VMG	W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
0857h CODE	W	FPM1	FPM0	FPFIS	--	CRCIV	CRCS	FECS	WHTS
0858h CRCRIV1	W	CRCRIV15	CRCRIV14	CRCRIV13	CRCRIV12	CRCRIV11	CRCRIV10	CRCRIV9	CRCRIV8
0859h CRCRIV2	W	CRCRIV7	CRCRIV6	CRCRIV5	CRCRIV4	CRCRIV3	CRCRIV2	CRCRIV1	CRCRIV0
085Ah CRCTIV1	W	CRCTIV15	CRCTIV14	CRCTIV13	CRCTIV12	CRCTIV11	CRCTIV10	CRCTIV9	CRCTIV8
085Bh CRCTIV2	W	CRCTIV7	CRCTIV6	CRCTIV5	CRCTIV4	CRCTIV3	CRCTIV2	CRCTIV1	CRCTIV0
085Ch CRCPL1	W	CRCPL15	CRCPL14	CRCPL13	CRCPL12	CRCPL11	CRCPL10	CRCPL9	CRCPL8
085Dh CRCPL2	W	CRCPL7	CRCPL6	CRCPL5	CRCPL4	CRCPL3	CRCPL2	CRCPL1	CRCPL0

085Eh WS	W		WS6	WS5	WS4	WS3	WS2	WS1	WS0
085Fh TH	W	PPS	IDL	PTH2	PTH1	PTH0	ETH2	ETH1	ETH0
0860h CTR	W	--	--	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
0861h BDC	W	**WTLP3**	**WTLP2**	**WTLP1**	**WTLP0**	BDC3	BDC2	BDC1	BDC0
0862h~0869h SID	W	SID	SID	SID	SID	SID	SID	SID	SID
086Ah AD CAL I	R	ADH7	ADH6	ADH5	ADH4	ADH3	ADH2	ADH1	ADH0
086Bh AD CAL II	R	ADL7	ADL6	ADL5	ADL4	ADL3	ADL2	ADL1	ADL0
086Ch SDR	W	**SDR7**	**SDR6**	**SDR5**	**SDR4**	**SDR3**	**SDR2**	**SDR1**	**SDR0**
08FBh FPC	W	**--**	**--**	**--**	**--**	**PDNFH**	**QDSFH**	**PDNFL**	**QDSFL**
08FCh~08FFh USID	R	USID	USID	USID	USID	USID	USID	USID	USID

9.2.1 Strobe Control Register (Address: 0800h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	P_GO1	P_GO2	P_CKO	FPEN	RFSTATE2	RFSTATE1	RFSTATE0
	W	Strobe3	Strobe2	Strobe1	Strobe0	--	--	--	--
Write Reset Value		0	0	0	0	0	0	0	0

Use strobe command control RF state.
Strobe[3:0] = 4'b1000: Sleep mode.
Strobe[3:0] = 4'b1001: Idle mode.
Strobe[3:0] = 4'b1010: Standby .
Strobe[3:0] = 4'b1011: PLL mode.
Strobe[3:0] = 4'b1100: RX mode
Strobe[3:0] = 4'b1101: TX mode

P_GO1, P_GO2, P_CKO: P_GIO1, P_GIO2, and P_CKO pin state read out.

FPEN: Frame pending bit.
RFSTATE[2:0]: RF state flag.
RFSTATE[2:0] = 3'b000: Sleep mode.
RFSTATE[2:0] = 3'b001: Idle mode.
RFSTATE[2:0] = 3'b010: standby mode.
RFSTATE[2:0] = 3'b011: PLL mode.
RFSTATE[2:0] = 3'b100: TX mode
RFSTATE[2:0] = 3'b101: RX mode

Please refer Chapter 21.1 for more detail information.

9.2.2 Reset Control Register (Address: 0801h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	CSMAF	CCAF	CRCF	CER	XER	PLLER	TRER	TRSR
	W	RESETN	FWPRN	FRPRN	--	FIFORN	BFCRN	--	--
Write Reset Value		0	0	0	0	0	0	0	0

RESETN: Soft reset. (Write only)
[1]: Soft reset this device. Auto clear when done.

FWPRN: FIFO write point reset. (Write only)
[1]: reset FIFO write pointer. Auto clear when done.

FRPRN: FIFO read point reset. (Write only)
[1]: reset FIFO read pointer. Auto clear when done.

FIFORN: FIFO data reset. (Write only)
[1]: Reset FIFO Data to all zero. Auto clear when done.

BFCRN: Back-off counter reset. (Write this register to 1 to issue reset command, then it is auto clear.)
[1]: Reset Back-off counter to zero. Auto clear when done.

CSMAF: CSMA function flag.
[0]: CSMA pass. [1]: CSMA Fail.

CCAF: CCA flag.
[0]: CCA pass. [1]: CCA fail.

CRCF: CRC flag. (Read only and updated for each valid packet.)
[0]: CRC pass. [1]: CRC error.

CER: Chip Status. (Read only)
[0]: Chip is disabled. [1]: Chip is enabled.

XER: Xtal Status. (Read only)
[0]: Crystal oscillator is disabled. [1]: Crystal oscillator is enabled.

PLLE: PLL Status. (Read only)
[0]: PLL is disabled. [1]: PLL is enabled after PLL strobe command.

TRER: TRX Status I. (Read only)
[0]: TRX is disabled. [1]: TRX is enabled.

TRSR: TRX Status II. (Read only)
[0]: RX mode. [1]: TX mode.
Serviceable when TRER=1 (TRX is enable).

9.2.3 Mode Control Register (Address: 0802h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	FECF	FPF	--	CD	WORE	FMT	FMS	ADCM
	W	DFCRC	--	WOT	DFCD	WORE	FMT	FMS	ADCM
Reset		1	1	0	0	0	0	1	0

DFCRC: Filter RX packet with CRC check.
[0]: Disable. **[1]:** Enable.

WOT: Wake On TX enable.
[0]: Disable. **[1]:** Enable.

DFCD (Data Filter by CD): The received packet will be filtered out.
[0]: Disable. **[1]:** Enable.

CD: Carrier detector (Read only).
[0]: Input power below threshold. **[1]:** Input power above threshold.

WORE: Wake On RX enable.
[0]: Disable. **[1]:** Enable.

FMT: Reserved for internal usage only.

FMS: Direct/FIFO mode select.
[0]: Direct mode. **[1]:** FIFO mode.

ADCM: ADC measurement (Auto clear when done).
[0]: Disable. **[1]:** Enable.

ADCM	Standby mode	RX mode
[0]	Disable ADC	Disable ADC
[1]	Measure temperature or external voltage	Measure RSSI, carrier detect

XADC: Refer to ADC control register (0820h)

FECF: FEC flag. (Read only and updated for each valid packet.)
[0]: FEC pass. [1]: FEC error.

FPF: FIFO pointer flag

9.2.4 Mode Select Register (Address: 0803h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	DLS	PNS	PNIVS	ACKS	ARTS	CSMAS	SLOT
Reset		0	0	0	0	1	0	1	0

DLS: Dynamic length select.
[0]: deselect. **[1]:** select.

PNS: Reserved.

PNIVS: PN initial seed select. Recommend PNIVS = [0].
[0]: Use RF calibration value. **[1]:** Manual setting by PNIV (35h).

ACKS: Auto ACK enable.
[0]: Disable. **[1]:** Enable.

ARTS: Auto Resend enable.
[0]: Disable. **[1]:** Enable.

CSMAS: CSMA-CA enable.
[0]: Disable. **[1]:** Enable.

SLOT: CSMA_CA algorithm type.
[0]: Un-slotted. **[1]:** Slotted.

9.2.5 Calibration Control Register (Address: 0804h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	--	ADCC	ROBC	VCC	VBC	VDC	FBC	RSSC
Reset		--	0	0	0	0	0	0	0

ADCC: ADC calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

ROBC: RO bank calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VCC: VCO current calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VBC: VCO bank calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VDC: VCO deviation calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

FBC: IF filter bank Calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

RSSC: RSSI calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

9.2.6 PHR Register (Address: 0805h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Name	R/W	PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
Reset		0	0	0	0	0	0	0	0

PHR [7:0] : Physical Header of IEEE 802.15.4.
It contains length of frame.
Write : TX FIFO Length.
Read : RX FIFO received length.
Payload length is programmable by PHR [7:0]. The physical FIFO depth is 64 bytes. A8125 also supports logical FIFO extension up to 256 bytes.

9.2.7 TWUN Register (Address: 0806h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0806h	R	--	--	--	--	--	--	--	TWUNF
	W	RNTWUNF	RNTWUNF	RNTWUNF	RNTWUNF	RNTWUNF	RNTWUNF	RNTWUNF	RNTWUNF
Reset		0	0	0	0	0	0	0	0

RNTWUNF: Reset TWUN flag.
TWUNF: TWUN flag.

9.2.8 RO Register I (Address: 0807h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	RCKS1	RCKS0	WUS1	WUS0	RTCS	IRCHC	ROE	TWWS
Reset		0	1	1	1	0	1	1	0

RCKS [1:0]: RO calibration clock select:
[00]: 32XMDR **[01]:** 16MHz **[10]:** 8XMDR **[11]:** 4XMDR

WUS [1:0]: Wake up select when WOR is enabled.
[00]: Detect carrier.
[01]: Detect IEEE 802.15.4 Sync word.
[10]: Detect IEEE 802.14.4 Beacon.
[11]: CRC pass.

RTCS: Sleep timer select.
[0]: RC oscillator (Internal). **[1]:** RTC crystal oscillator (External).

IRCHC: RC oscillator high current mode select.

ROE: Enable Internal RC oscillator.
[0]: Disable. **[1]:** Enable.

TWWS: Timer wake up enable.
[0]: Disable. **[1]:** Enable.

9.2.9 RO Register II (Address: 0808h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	RCT7	RCT6	RCT5	RCT4	RCT3	RCT2	RCT1	RCT0
	W	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
Reset		0	0	1	1	1	0	1	0

MRCT [7:0]: RO Bank manual calibration value (write only).
Manual setting when MRC =1.

RCT [7:0]: RO Bank auto calibration value (read only).

9.2.10 RO Register III (Address: 0809h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	NUMLH11	NUMLH10	NUMLH9	NUMLH8	--	--	RCT9	RCT8
	W	TGNUM11	TGNUM10	TGNUM9	TGNUM8	MVS1	MVS0	MRCT9	MRCT8
Reset		1	0	0	0	1	1	1	0

MVS [1:0]: RO calibration moving average mode.

[00]: 1 [01]: 2 [10]: 4 [11]: 8

9.2.11 RO Register IV (Address: 080Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
	W	TGNUM7	TGNUM6	TGNUM5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0
Reset		0	0	0	0	0	0	0	0

NUMLH [11:0]: RO N Counter calibration result (read only).

TGNUM [11:0]: RO N Counter target (write only).
RO N Counter calibration goal or manual setting.

9.2.12 RO Register V (Address: 080Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	RCOT2	RCOT1	RCOT0	CX4	CX3	CX2	CX1	CX0
Reset		1	0	0	0	0	1	0	0

RCOT[2:0]: Reserved for internal usage only.

CX[4:0]: Reserved for internal usage only.

9.2.13 CKO Pin Control Register (Address: 080Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FIFOSS	TRDC	CKOS2	CKOS1	CKOS0	CKOI	MRC	DCKS
Reset		0	0	0	0	0	0	0	0

FIFOSS: FIFO sequence order select.
[0]: LSB first. **[1]:** MSB first.

TRDC: RFIO pin and RFO pin control.
[0]: Internal Combined.
RFIO pin is Input/Output (bi-directional for PA output and LNA input).
RFO pin is NC.

[1]: External Combined.
RFIO pin is Input (single-directional for LNA input).
RFO pin is Output (single-directional for PA output).

CKOS [2:0]: CKO pin output select.
[000]: INTF (refer to 30h).
[001]: BDF (Low battery detection output).
[010]: XRDY.
[011]: SDO (4 wires SPI data output).
[100]: BBCK (4XDR).
[101]: RO 320us. (20 symbols).
[110]: RO frequency.
[111]: Data clock (2M or 250K).

CKOI: CKO pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

MRC: RO bank manual calibration.
[0]: Disable. **[1]:** Enable.

DCKS: RX data clock select.
[0]: Virtual clock. **[1]:** Recovery clock.

9.2.14 GIO1 Pin Control Register (Address: 080Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	--

Reset		--	--	0	0	1	1	0	--

GIO1S [3:0]: GIO1 pin function select.

GIO1S	TX state	RX state
[0000]	INT (Interrupt)	
[0001]	WTR (Wait until TX or RX finished)	
[0010]	WOR	
[0011]	EOAC (end of access code)	FSYNC (frame sync)
[0100]	TMEO (TX modulation enable)	CD (carrier detect)
[0101]	Preamble Detect Output (PMDO)	
[0110]	RXD (Direct mode)	
[0111]	TXD (Direct mode)	
[1000]	PDN_RX	
[1001]	PDN_TX	
[1010]	PASW	
[1011]	VTB[0]	
[1100]	DMII	
[1101]	EOFF	
[1110]	FPF	
[1111]	CKE	

INT: Interrupt sources (refer to 083Ch).

GIO1I: GIO1 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

9.2.15 GIO2 Pin Control Register (Address: 080Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	**GIO2S3**	**GIO2S2**	**GIO2S1**	**GIO2S0**	**GIO2I**	
Reset		--	--	0	0	0	1	0	

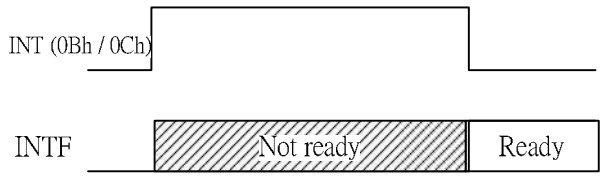
GIO2S [2:0]: GIO2 pin function select.

GIO2S	TX state	RX state
[0000]	INT	
[0001]	WTR (Wait until TX or RX finished)	
[0010]	Wake up signal	
[0011]	EOAC (end of access code)	FSYNC (frame sync)
[0100]	TMEO (TX modulation enable)	CD (carrier detect)
[0101]	Preamble Detect Output (PMDO)	
[0110]	RXD (Direct mode)	
[0111]	TXD (Direct mode)	
[1000]	PDN_RX	
[1001]	PDN_TX	
[1010]	PASW	
[1011]	VTB[1]	
[1100]	DMIQ	
[1101]	EOFF	
[1110]	FPF	
[1111]	CKE	

INT: Interrupt Sources (refer to 083Ch).

IST (30h)	INT	INTF (30h)	Note
IST[3:0]=0	none	none	
IST[3:0]=1	**WTR**	**CRCF**	
IST[3:0]=2	CSMA_CA	CSMAF	
IST[3:0]=3	CCA	CCAF	
IST[3:0]=4	ART	Reserved	

IST[3:0]=5	**ED**	none	
IST[3:0]=6	FPFINT	FPF	
IST[3:0]=7	ADCM	Reserved	
IST[3:0]=8	WOR	**CRCF**	
IST[3:0]=9	WOT	none	
IST[3:0]=10	TWOR	none	



GIO2I: GIO2 pin output invert.
[0]: Non-inverted output. **[1]:** Inverted output.

EOFF: EOP, EOVBC, EOFBC, EOADC, EOVCC, EOVDC, EORSSC, OKADC, EOAGC (Internal usage only).

9.2.16 STM (Address: 080Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	STM5	STM4	STM3	STM2	STM1	STM0
	R	--	--	STMR5	STMR5	STMR3	STMR2	STMR1	STMR0
Reset		0	0	1	0	0	0	0	0

Reserved for internal usage.

9.2.17 Data Rate Clock Register (Address: 0810h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	MDR1	MDR0	GRC3	GRC2	GRC1	GRC0	CGFS1	CGFS0
Reset		1	0	0	1	1	1	0	1

MDR [1:0]: Main Data rate setting.

MDR [1:0]	Data Rate
[00]	Reserved
[01]	1 Mbps
[10]	2 Mbps
[11]	Reserved

GRC [3:0]: Generator Reference Counter
GRC is used to get internal 2 MHz Clock Generator Reference (F_{CGR}) for different Xtal frequency.

External Crystal (F_{XREF})	Clock Generation Reference (CGR)	GRC [3:0]
16 MHz	Must be 2 MHz	[0111]
12 MHz	Must be 2 MHz	[0101]
8 MHz	Must be 2 MHz	[0011]

CGFS [1:0]: Clock generator frequency select. Recommed CGFS = [01].
[00]: 16MHz. **[01]:** 32MHz. **[10]:** 48MHz. **[11]:** 64MHz.

9.2.18 PLL Register I (Address: 0811h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset		0	1	1	0	0	1	0	0

CHN [7:0]: RF Channel Number.

9.2.19 PLL Register II 、III (Address: 0812h~0813h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0812h	W	--	--	--	--	--	--	--	BIP8
Reset		--	--	--	--	--	--	--	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0813h	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
Reset		1	0	0	1	0	1	1	0

BIP [8:0]: LO frequency integer part setting.

Xtal	Data Rate	BIP [8:0]
16MHz	2Mbps	0x0096
18MHz	3Mbps	0x0085

9.2.20 PLL Register IV、V (Address: 0814h~0815h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0814h	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
Reset		0	0	0	0	0	0	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0815h	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
Reset		0	0	0	0	0	1	0	0

BFP [15:0]: LO frequency floating part setting.

Xtal	Data Rate	BFP [15:0]
16MHz	2Mbps	0x0004
18MHz	3Mbps	0x5558

9.2.21 PLL Register VI、VII (Address: 0816h~0817h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0816h	W	--	CHR14	CHR13	CHR12	CHR11	CHR10	CHR9	CHR8
Reset		--	0	0	0	1	0	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0817h	W	CHR7	CHR6	CRH5	CHR4	CHR3	CHR2	CHR1	CHR0
Reset		0	0	0	0	0	0	0	0

CHR [14:0]: Channel resolution setting.

Xtal	Data Rate	CHR [14:0]
16MHz	2Mbps	0x0800
18MHz	3Mbps	0x071C

Remark: The above setting is used for 500KHz channel spacing.

9.2.22 Channel Group Register I、II (Address: 0818h~0819h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0818h	W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
Reset		0	0	1	1	1	1	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0819h	W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
Reset		0	1	1	1	1	0	0	0

CHGL [7:0]: PLL channel group low boundary setting. Recommend CHGL = [0x3C].

CHGH [7:0]: PLL channel group high boundary setting. Recommend CHGH = [0x78].

PLL frequency is divided into 3 groups:

	Channel
Group1	0 ~ CHGL-1
Group2	CHGL ~ CHGH-1
Group3	CHGH ~ 255

9.2.23 TX Register I (Address: 081Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	TCPS	PADL	TXDI	TME	--	FDP2	FDP1	FDP0
Reset		0	0	0	1	--	1	1	1

TCPS: TX delay fit carrier or preamble select(turbo mode).
[0]: Fit TX carrier. **[1]:** Fit preamble data.

PADL: Embedded PA off delay.
[0]: 8us. **[1]:** 0us.

TXDI: TX data invert. Recommend TXDI = [0].
[0]: Non-invert. **[1]:** Invert.

TME: TX modulation enable.
[0]: Disable. **[1]:** Enable.

FDP [2:0]: Frequency deviation power setting. Recommend FDP = [111].

9.2.24 TX Register II (Address: 081Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset		0	1	0	0	0	0	0	0

FD [7:0]: Frequency deviation setting. Recommend FD = [0x40]
Frequency deviation:
$_{DEV}= F_{PFD}$ x 127 x (FD [7:0] + 1) x $2^{(FDP\ [2:0]\ +\ 1)}$ / 2^{25}

Recommend F_{DEV} = 500 KHz.

9.2.25 RX Register (Address: 081Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	IGCR	LGCR	MGCR	RCP2	RCP1	RCP0	DMG	RXDI
Reset		0	0	1	0	1	0	0	0

IGCR: IF gain control range. Recommend IGCR = [0].
[0]: 0dB to -18dB. **[1]:** -6dB to -18dB.

LGCR: LNA gain control range. Recommend IGCR = [0].
[0]: 0dB to -30dB. **[1]:** -6dB to -30dB.

MGCR: Mixer gain control range. Recommend MGCR = [1].
[0]: 0dB to -24dB. **[1]:** 0dB to -18dB.

RCP [2:0]: Turbo mode recovery clock position. Recommend RCP = [010].

DMG: Reserved for internal usage only.

RXDI: RX data output invert. Recommend RXDI = [0].
[0]: Non-inverted output. **[1]:** Inverted output.

9.2.26 RX Gain Register I (Address: 081Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	IGS1	IGS0	LGS2	LGS1	LGS0	MGS2	MGS1	MGS0
Reset		0	0	0	0	0	0	0	0

IGS [1:0]: IF gain select.
[00]: 0dB. **[01]:** -6dB. **[10]:** -12dB. **[11]:** -18dB.

MGS [2:0]: Mixer gain attenuation select. Recommend MGS = [000].

[000]: 0dB. **[001]:** -6dB. **[010]:** -12dB. **[011]:** -18dB. **[1XX]:** -24dB.

LGS [2:0]: LNA gain attenuation select. Recommend LGS = [000].
[000]: 0dB. **[001]:** -6dB. **[010]:** -12dB. **[011]:** -18dB. **[100]:** -24dB. **[101]** ~ **[111]:** -30dB.

9.2.27 RX Gain Register II (Address: 081Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
	W	PKIS1	PKIS0	VTHS2	VTHS1	VTHS0	VTLS2	VTLS1	VTLS0
Reset		0	0	0	0	1	0	0	1

PKIS[1:0]: AGC Peak Detect Current Select. Recommend PKIS = [00].
VTHS: AGC target upper limit. Recommand value= [001].
VTLS: AGC target lower limit. Recommand value= [001].

RH [7:0]: RSSI high level calibration value.

9.2.28 RX Gain Register III (Address: 081Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
	W	LMS	RSSL6	RSSL5	RSSL4	RSSL3	RSSL2	RSSL1	RSSL0
Reset		0	0	0	1	1	0	0	1

RL [7:0]: RSSI low level calibration value (read only).

LMS: AGC order select. [0]: Mixer [1]: LNA.

RSSL [6:0]: RSSI slope (write only).

9.2.29 RX Gain Register IV (Address: 0820h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	RU7	RU6	RU5	RU4	RU3	RU2	RU1	RU0
	W	AGCS1	AGCS0	IFAS	IFPK	MHC	LHC1	LHC0	AGCE
Reset		1	0	0	0	1	0	1	1

RU [7:0]: RSSI upper level calibration value.

AGCS [1:0]: AGC stop mode. Recommend AGCS = [00].
[00]: Non-stop. **[01]:** Stop by PRAOK. **[10]:** Stop by FSYNC. **[11]:** AGC test mode.

IFAS: IF amplifier current setting. Recommend IFAS = [0].

IFPK: AGC Amplifier Current Select. Recommend IFPK = [0].

MHC: Mixer Current Control.

LHC[1:0]: LNA Current Control.

AGCE: AGC enable. Recommend AGCE = [1].
[0]: Disable. **[1]:** Enable.

9.2.30 ADC Register (Address: 0821h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	W	CDTH7	CDTH6	CDTH5	CDTH4	CDTH3	CDTH2	CDTH1	CDTH0
Reset		0	0	0	0	0	0	0	0

CDTH [7:0]: Carrier detect threshold (write only).

ADC [7:0]: ADC digital output value (read only).

ADC input voltage = 1.2 * ADC [7:0] / 256 V.

9.2.31 ADC Control Register (Address: 0822h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	CDM	ADCOM1	ADCOM0	MRSSL	--	AVGS1	AVGS0
Reset			1	1	1	0	--	1	1

CDM: CD margin = CDTH – CDTL. Recommend CDM = [1].
[0]: 6 LSB. **[1]:** 12 LSB.

ADCOM: ADC output mode. Recommend ADCOM = [10].
[00]: Single mode.
[01]: Average mode (2, 4, 8, 16 average is according to AVGS [1:0].
[10]: ED. No hold.
[11]: ED. Hold after sync 128us.

MRSSL: Reserved for internal usage only.

AVGS [1:0]: ADC average mode. Recommend AVGS = [11].
[00]: 2. **[01]:** 4. **[10]:** 8. **[11]:** 16.

Please note that AVGS = [11] during VBC, VDC and RSSI calibration.

9.2.32 IF Calibration Register I (Address: 0823h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	VTB1	VTB0	--	FBCF	FB3	FB2	FB1	FB0
	W	IFHCM	IFTS	--	MFBS	MFB3	MFB2	MFB1	MFB0
Reset		0	0	--	0	0	1	1	1

IFHCM: Reserved for internal usage only.

IFTS: Reserved for internal usage only.

MFBS: IF filter calibration select. Recommend MFBS = [0].
[0]: Auto. **[1]:** Manual.

MFB [3:0]: IF filter manual calibration value.

VTB: AGC status from Peak detect

FBCF: IF filter calibration flag.
[0]: Pass. **[1]:** Fail.

FB [3:0]: IF filter calibration result (read only).
Auto calibration result when MFBS = 0.
Manual calibration result when MFBS = 1.

9.2.33 IF Calibration Register II (Address: 0824h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	FCD4	FCD3	FCD2	FCD1	FCD0
Reset		--	--	--	0	0	1	0	0

FCD [4:0]: IF filter calibration difference.

9.2.34 VCO Current Calibration Register (Address: 0825h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
	W	--	VCCS1	VCCS0	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
Reset		--	1	0	0	0	1	0	0

VCCS [1:0]: VCO current calibration value select.
[00]: 0.6mA. **[01]:** 0.8mA. **[10]:** 1.0mA. [**11]:** 1.2mA.

MVCS: VCO current calibration select. Recommend MVCS = [0].

[0]: Auto. **[1]:** Manual.

VCOC [3:0]: VCO current manual calibration value.
VCO current manual setting when MVCS = 1.

VCCF: VCO current calibration flag.
[0]: Pass. **[1]:** Fail.

VCB [3:0]: VCO current calibration value (read only).
Auto calibration result when MVCS = 0.
Manual calibration result when MVCS = 1.

9.2.35 VCO Bank Calibration Register I (Address: 0826h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	--	VBCF	VB2	VB1	VB0
	W	LPFT1	LPFT0	LPFS	MDAGS	MVBS	MVB2	MVB1	MVB0
Reset		0	1	0	0	0	1	0	0

LPFT [1:0]: Loop Filter.
[00]: R1=22.0K, C1=21.5pF.
[01]: R1=11.0K, C1=43.0pF.
[10]: R1= 7.3K, C1=64.5pF.
[11]: R1= 5.5K, C1=86.0pF.

LPFS: Loop Filter Select.
[0]: Internal. **[1]:** External.

MDAGS: DAG calibration select. Recommend MDAGS = [0].
[0]: Auto. **[1]:** Manual.

MVBS: VCO bank calibration select. Recommend MVBS = [0].
[0]: Auto. **[1]:** Manual.

MVB [2:0]: VCO band manual calibration value.
VCO band manual setting when MVBS = 1.

VBCF: VCO band calibration flag.
[0]: Pass. **[1]:** Fail.

VB [2:0]: VCO bank calibration value (read only).
Auto calibration result when MVBS = 0.
Manual calibration result when MVBS = 1.

9.2.36 VCO Bank Calibration Register II (Address: 0827h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
Reset		1	0	0	0	0	0	0	0

MDAG [7:0]: DAG manual calibration value. Recommend MDAG = [0x80].

ADAG [7:0]: DAG auto calibration result (read only).

9.2.37 VCO Deviation Calibration Register I (Address: 0828h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
Reset		0	0	1	1	0	0	0	0

DEVS [3:0]: Deviation output scaling. Recommend DEVS = [0011].

DAMR_M: DAMR manual enable. Recommend DAMR_M = [0].
[0]: Disable. **[1]:** Enable.

VMTE_M: VMT manual enable. Recommend VMTE_M = [0].

[0]: Disable. **[1]:** Enable.

VMS_M: VM manual enable. Recommend VMS_M = [0].
[0]: Disable. **[1]:** Enable.

MSEL: VCO control select. Recommend MSEL = [0].
[0]: Auto control for VMS /VMTE / DAMR. **[1]:** Manual control for VMS /VMTE / DAMR.

DEVA [7:0]: VCO Deviation result.
Auto calibration result when MVDS = 0. (1Fh)
Manual calibration result when MVDS = 1. (1Fh)
Where auto calibration result is ((ADEV / 8) × (DEVS + 1)).

9.2.38 VCO Deviation Calibration Register II (Address: 0829h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
Reset		0	0	0	1	1	0	1	1

MVDS: VCO deviation calibration select. Recommend MVDS = [0].
[0]: Auto. **[1]:** Manual.

MDEV [6:0]: VCO deviation manual calibration value.

ADEV [7:0]: VCO deviation auto calibration value.

9.2.39 VCO Modulation Delay Register (Address: 082Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	DEVCM	--	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
Reset		0	--	0	0	0	0	1	1

DEV CAL mode:
[0]: one side calibration mode. [1]: two side calibration mode.

DEVFD [2:0]: Reserved for internal usage only.

Xtal	Date Rate	DEVFD [2:0]
16MHz	2Mbps	000
18MHz	3Mbps	000

DEVD [2:0]: Reserved for internal usage only.

Xtal	Data Rate	DEVD [2:0]
16MHz	2Mbps	011
18MHz	3Mbps	011

9.2.40 Channel Select Register (Address: 082Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
Reset		0	0	1	1	0	1	1	1

CHI [3:0]: Auto IF offset channel number setting.
If F_{CHSP} = 500 KHz, recommend **CHI = [0011]**.
F_{CHSP} × (CHI + 1) = 2MHz.

Xtal	Data Rate	CHI [3:0]
16MHz	2Mbps	0011
18MHz	3Mbps	0101

CHD [3:0]: Channel frequency offset for deviation calibration.
If F_{CHSP} = 500 KHz, recommend **CHD = [0111]**.
Where Offset channel number = +/- (CHD + 1).

Xtal	Data Rate	CHD [3:0]

16MHz	2Mbps	0111
18MHz	3Mbps	1011

9.2.41 Battery Detect Register (Address: 082Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	--	--	--	--	BDF
	W	ATP1	ATP0	BLE	BDV2	BDV1	BDV0	BGS	BDE
Reset		0	1	0	0	0	1	0	0

ATP [1:0]: Analog Test Pin. Recommend ATP= [01].

ATP [1:0]	VDD_R
[00]	1.2 voltage regulator out
[01]	Analog temperature voltage
[10]	BPF positive in phase output
[11]	BPF negative in phase output

BLE: Battary life extension. Reserved for internal usage.

BDV[2:0]: Battery detection voltage.
[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V. **[100]:** 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

BGS: Bangap (BG) select:
[0]: Low currect BG. [1]: High currect BG.

BDE: Battery detection enable.
[0]: Disable. **[1]:** Enable.

BDF: Battery detection flag.
[0]: Low Battery. **[1]:** High Battery.

9.2.42 CBG Register (Address: 082Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	PD_LVD	PDNR	REGCL	CBG4	CBG3	CBG2	CBG1	CBG0
Reset		0	1	0	1	0	0	0	0

PD_LVD: LVD circuit power down.
When PD_LVD=0 and REGI voltage less than 1.8v, the LVD circuit will generate a low voltage reset signal.
[0]: Power on. [1]: Power down.

PDNR: 1.2 Voltage regulator power down.
[0]: Power down. [1]: Power on.

REGCL: Reserved for internal usage.

CBG [4:0]: Vref calibration.

9.2.43 TX test Register (Address: 082Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	SLF1	SLF0	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
Reset		1	1	0	0	0	1	1	0

SLF [2:0]: Reserved for internal usage only.

TXCS: TX Current Setting.

PAC [1:0]: PA Current Setting.

TBG [2:0]: TX Buffer Setting.

9.2.44 RX LQI Register I (Address: 082Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	LQI7	LQI6	LQI5	LQI4	LQI3	LQI2	LQI1	LQI0
	W	ULS	SLF2	DCM1	DCM0	LQICE	ARSSI	AIF	LQIE
Reset		0	1	0	1	0	1	1	0

ULS: RX Up/Low side band select. Recommend ULS = [0].
[0]: Up side band. **[1]:** Low side band.

DCM[1:0] : Demodulator DC estimation mode. Recommend DCM = [01].
[00]: Fix mode (For ±10 ppm crystal accuracy only). DC level is set by DCV [7:0].
[01]: 32 bits average before frame sync, hold after frame sync.
[1X]: 32 bits average before frame sync and then become 128 bits average after frame sync.

LQICE: LQI Counter enable for WOR, ATRE, RX timeout.
[0]: Disable. **[1]:** Enable.

ARSSI: Auto RSSI measurement whenever in RX mode. Recommend ARSSI = [1].
[0]: Disable. **[1]:** Enable.

AIF: Auto IF. Recommend AIF = [1].
[0]: Disable. [1]: Enable.
RF LO frequency will auto offset one IF frequency whenever entering to RX mode.

LQIE: LQI enable. Recommend LQIE = [1].
[0]: Disable. **[1]:** Enable.

LQI [7:0]: Link quality indication (read only).
LQI=0x00, low link quality.
LQI=0xFF, high link quality.

A8125's LQI calculation is implemented by 32-Packets Moving Average.
LQI = (1 – PER) x 256, where LQI initial value is 0xFF and PER stands for Packet Error Rate.

9.2.45 RX DEM DC Register II (Address: 0830h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
	R	DCO7	DCO6	DCO5	DCO4	DCO3	DCO2	DCO1	DCO0
Reset		1	0	0	0	0	0	0	0

DCV [7:0]: Demodulator fix mode DC value. Recommend DCV = [0x80].

DCO[7:0]: DC average output (read only).

9.2.46 Charge Pump Current Register (Address: 0831h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
Reset		1	1	1	1	0	0	1	1

CPM [3:0]: Charge pump current setting for VM loop. Recommend CPM = [1111].
Charge pump current = (CPM + 1) / 16 mA.

CPT [3:0]: Charge pump current setting for VT loop. Recommend CPT = [0011].
Charge pump current = (CPT + 1) / 16 mA.

9.2.47 Crystal test Register (Address: 0832h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CGS	XS	XCL3	XCL2	XCL1	XCL0	XCC	XCP
Reset		1	1	1	0	1	0	1	1

CGS: Clock generator select. Recommend CGS = [1].

[0]: By pass clock generator. **[1]:** Use clock generator.

XS: Crystal oscillator select. Recommend XS = [1].
[0]: Use external clock. **[1]:** Use external crystal.

XCL [3:0]: Reserved for internal usage only.

XCC: Reserved for internal usage only.

XCP: Reserved for internal usage only.

9.2.48 PLL test Register (Address: 0833h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	XEC	CPS	PRRC1	PRRC0	PRIC1	PRIC0	SDPW	NSDO
Reset		1	1	0	1	0	0	0	1

XEC: Crystal enable control.
[0]: Control by RF state. [1]: Control by MCU and RF state.

CPS: Reserved for internal usage only.

PRRC [1:0]: Reserved for internal usage only.

PRIC [1:0]: Reserved for internal usage only.

SDPW: Reserved for internal usage only.

NSDO: Reserved for internal usage only.

9.2.49 VCO test Register (Address: 0834h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	TLB1	TLB0	CPCH1	CPCH0	RLB1	RLB0	VCBS1	VCBS0
Reset		0	0	0	0	0	0	1	0

TLB [1:0]: LO TX Buffer current.
[00]:1.2mA. **[01]:**1.5mA. **[10]:** 1.8mA. **[11]:** 2.1mA.

CPCH [1:0]: Charge pump high current.

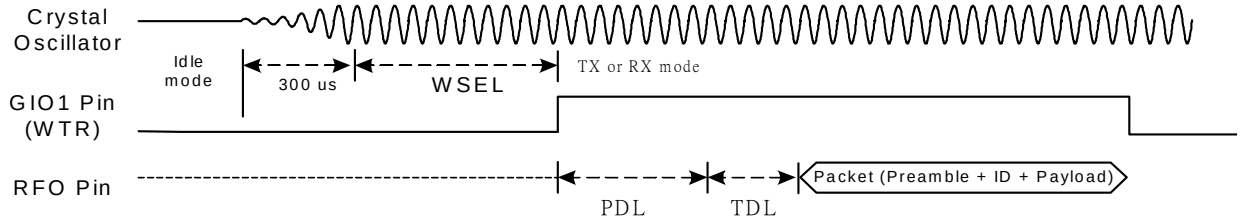
RLB [1:0]: LO RX Buffer current.
[00]:1.2mA. **[01]:**1.5mA. **[10]:** 1.8mA. **[11]:** 2.1mA.

VCBS [1:0]: VCO Buffer current Select. Recommend VCBS = [10].
[00]: 0.6mA. **[01]:** 0.8mA. **[10]:** 1.0mA. **[11]:** 1.2mA.

9.2.50 Delay Register (Address: 0835h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	WSEL1	WSEL0	PDL1	PDL0	TDL2	TDL1	TDL0
Reset		0	1	0	1	0	1	0	0

WSEL [1:0]: XTAL settling delay (0us ~ 840us). Recommend WSEL = [11].
[00]: 0us. **[01]:** 400us. **[10]:** 600us. **[11]:** 800us.
Remark :
In slotted mode or WOR mode: recommend WSEL= [00].
In un-slotted mode and non-WOR mode: recommend WSEL= [11].



PDL [1:0]: PLL Settling Delay. Recommend PDL = [10].
[00]: 0us. **[01]:** 16us. **[10]:** 32us. **[11]:** 48us.

TDL [2:0]: TRX Settling Delay. Recommend TDL = [100].
[000]: 0us. **[001]:** 16us. **[010]:** 32us. **[011]:** 48us. **[100]:** 64us. **[101]:** 80us. **[110]:** 96us. **[111]:** 112us.

9.2.51 AGC Delay Register (Address: 0836h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	AGC_DLY 1	AGC_DLY 0	RS_DLY1	RS_DLY0	AGCKS1	AGCKS0	--	--
Reset		0	0	0	1	1	1	--	--

AGC_DLY [1:0]: AGC Settling Delay (4us ~ 16us). Recommend AGC_DLY = [00].
[00]: 4us. **[01]:** 8us. **[10]:** 12us. **[11]:** 16us.

RS_DLY [1:0]: AGC Measurement Delay . Recommend RS_DLY = [01].
[00]: 2XAGCK count. **[01]:** 3XAGCK count. **[10]:** 4XAGCK count. **[11]:** 5XAGCK count.

AGCKS [1:0]: AGC clock seleck.
[00]: 4XMDR [01]: 2XMDR [10]: 1XMDR [11]: 1/2XMDR

9.2.52 ART Delay Register I (Address: 0837h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	RTD 3	RTD 2	RTD 1	RTD 0	TRD 3	TRD 2	TRD 1	TRD 0
Reset		0	0	0	0	1	0	0	0

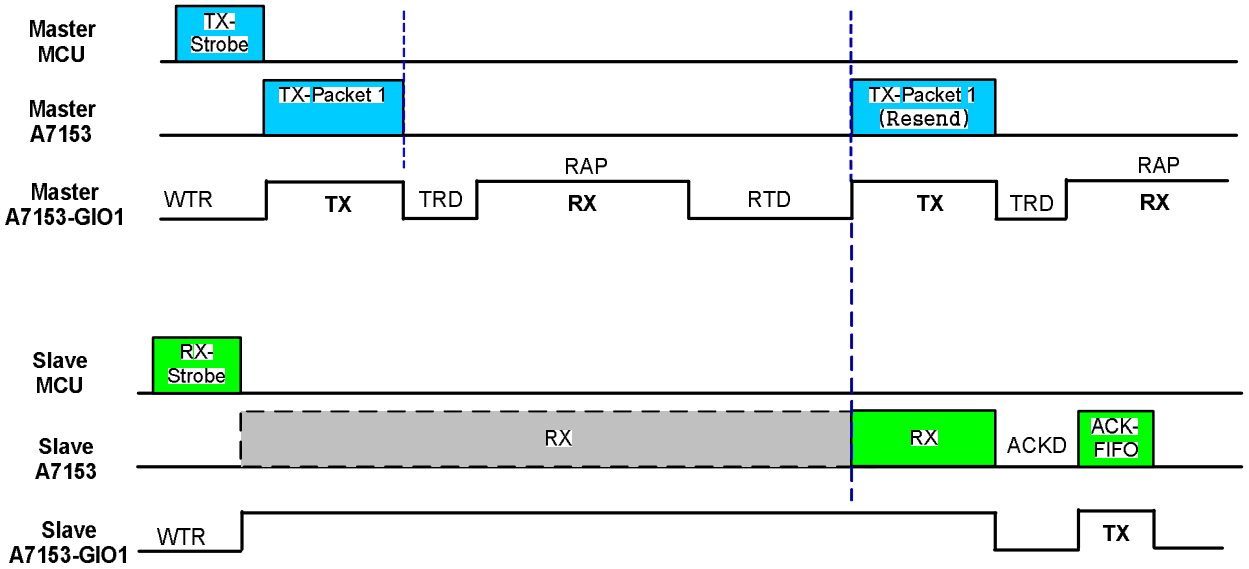
RTD [3:0]: Delay from TX to RX of Auto-resend function. Recommend RTD = [0000].
Delay= 16 * (RTD [3:0]) us.

TRD [3:0]: Delay from RX to TX of Auto-resend function. Recommend RTD = [1000].
Delay= 16 * (TRD [3:0]) us.

9.2.53 ART Delay Register II (Address: 0838h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	RAP 7	RAP 6	RAP 5	RAP 4	RAP 3	RAP 2	RAP 1	RAP 0
Reset		0	0	0	1	1	1	0	1

RAP [7:0]: RX Active Period of Auto-resend function.
Delay= 16 * (**RAP** [7:0]) us.



9.2.54 CSMA Register I (Address: 0839h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	ATLP2	ATLP1	ATLP0	CST1	CST0	MaxNB2	MaxNB1	MaxNB0
Reset		0	1	1	0	0	1	0	0

ATLP [2:0]: Loop times for auto resend algorithm. Recommend ATLP = [011].

CST[1:0]: Carrier sense time. Recommend CST = [00].
[00]:128us. **[01]:**160us. **[10]:** 192us. **[11]:**224us.

MaxNB [2:0]: Loop times for CSMA-CA algorithm. Recommend MaxNB = [100].

9.2.55 CSMA Register II (Address: 083Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	MaxBE3	MaxBE2	MaxBE1	MaxBE0	MinBE3	MinBE2	MinBE1	MinBE0
Reset		0	1	0	1	0	0	1	1

MaxBE [3:0]: Maxmum back-off exponent in CSMA-CA algorithm. Recommend MaxBE = [0101].

MinBE [3:0]: Minimum back-off exponent in CSMA-CA algorithm. Recommend MinBE = [0011].

9.2.56 Pre_TRX setting Register (Address: 083Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	ACKD3	ACKD2	ACKD1	ACKD0	PTRS3	PTRS2	PTRS1	PTRS0
Reset		1	0	0	0	0	0	0	0

PTRS [3:0]: Pre_TRX setting. Recommend PTRS = [0000].

ACKD [3:0]: Auto-ACK Delay. Recommend ACKD = [1000] for 128 us.
Delay= 16 * (ACKD [3:0]) us.

Based on IEEE802.15.4, ACK Packet shall be replied within **192 us** after receiving the ACK request package.

9.2.57 Interrupt State Register (Address: 083Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	ISTRN	--	CCAM1	CCAM0	ERX	EDS	CCAS	--

	R	INT	IST3	IST2	IST1	IST0	EDS	CCAS	INTF
Reset		0	--	0	1	0	0	0	--

ISTRN: Interrupt state reset. (write only). Recommend ISTRN = [0].
[1]: Reset interrupts sources. Auto clear when done.

CCAM[1:0]: CCA mode. Recommend CCAM = [01].
[00]: CCAF=1, when RSSI > RTH, and detect preamble frame.
[01]: CCAF=1, when RSSI > RTH.
[10]: CCAF=1, when detect preamble frame.
[11]: CCAF=1, when RSSI > RTH or detect preamble frame.

EDS: Energy detect. (Auto clear when done).
[0]: Disable. **[1]:** Enable.

CCAS: CCA function. (Auto clear when done).
[0]: Disable. **[1]:** Enable.

ERX: RX Behavior.
[0]: Normal RX.
[1]: For CCA and ED. When CCA or ED is done, auto back to previous state (i.e. Standby or PLL mode).

INT: Interrupt source state.
[0]: None. **[1]:** Busy.

IST[3:0]: Interrupt source select.

INTF: Interrupt flag.
INTF status is shown as the respective function as the below table.

IST[3:0]	Interrupt source	INTF (Bit 0)	Note
0000	none	none	
0001	WTR	CRCF	
0010	CSMA_CA	CSMAF	
0011	CCA	CCAF	
0100	ART	Reserved	
0101	EDM	None	
0110	FPFINT	FPF	
0111	ADCM	None	
1000	WOR	CRCF	
1001	WOT	None	
1010	TWOR	None	

9.2.58 ADF control Register I、II (Address: 083Dh~083Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
083Dh	W	**FADDE**	**ACBEN**	**ACDAT**	**ACACK**	**ACCMD**	**ACRES**	**PCORR**	**MAXVER1**
Reset		1	1	1	1	1	1	0	0
083Eh	W	**MAXVER0**	**RESMUX2**	**RESMUX1**	**RESMUX0**	**--**	**SLT2**	**SLT1**	**SLT0**
Reset		1	0	0	0	--	1	0	0

FADDE: MAC Address Filtering.
[0]: Disable. **[1]:** Enable.

ACBEN: Accept Beacon frame type (0)
[0]: Reject. **[1]:** Accept.

ACDAT: Accept Data frame type (1)
[0]: Reject. **[1]:** Accept.

ACACK: Accept Ack frame type (2)
[0]: Reject. **[1]:** Accept.

ACCMD: Accept MAC command frame type (3)

[0]: Reject. **[1]:** Accept.

ACRES: Accept Reserved frame type (4,5,6,7)
[0]: Reject. **[1]:** Accept.

PCORR: PAN Coordinator.
[0]: End device. **[1]:** Coordinator.

MAXVER: Max frame version. Recommend MAXVER = [01].

RESMUX: FCF reserved bit mask. Recommend RESMUX = [000].

SLT[2:0]: TRX lead time in slotted mode.
[000]: 2 slot time. **[001]:** 3 slot time. **[010]:** 4 slot time. **[011]:** 5 slot time. **[100]:** 6 slot time. **[101]:** 7 slot time.
[110]: 8 slot time. **[111]:** 9 slot time.

9.2.59 ADF Frame Register 1~12 (Address: 083Fh~084Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
083Fh	w	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
0840h	w	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
0841h	w	SADD15	SADD14	SADD13	SADD12	SADD11	SADD10	SADD9	SADD8
0842h	w	SADD7	SADD6	SADD5	SADD4	SADD3	SADD2	SADD1	SADD0
0843h	w	LADD63	LADD62	LADD61	LADD60	LADD59	LADD58	LADD57	LADD56
0844h	w	LADD55	LADD54	LADD53	LADD52	LADD51	LADD50	LADD49	LADD48
0845h	w	LADD47	LADD46	LADD45	LADD44	LADD43	LADD42	LADD41	LADD40
0846h	w	LADD39	LADD38	LADD37	LADD36	LADD35	LADD34	LADD33	LADD32
0847h	w	LADD31	LADD30	LADD29	LADD28	LADD27	LADD26	LADD25	LADD24
0844h	w	LADD23	LADD22	LADD21	LADD20	LADD19	LADD18	LADD17	LADD16
0849h	w	LADD15	LADD14	LADD13	LADD12	LADD11	LADD10	LADD8	LADD8
084Ah	w	LADD7	LADD6	LADD5	LADD4	LADD3	LADD2	LADD1	LADD0
Reset		1	1	1	1	1	1	1	1

PID[15:0]: PAN ID Storage.
PID [15:0]: Store PAN_ID for frame filtering.
Default : 0xFFFF.

SADD[15:0]: Short Address Storage.
SADD [15:0]: Store Short address for frame filtering.
Default : 0xFFFF.

LADD[63:0]: Long Address Storage.
LADD [63:0]: Store Long address for frame filtering.
Default : 0xFFFF-FFFF-FFFF-FFFF.

Refer to Chapter 13 for frame filtering.

9.2.60 ACK Frame Control Register I、II (Address: 084Bh~084Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
084Bh	W	AFCF7	AFCF6	AFCF5	AFCF4	AFCF3	AFCF2	AFCF1	AFCF0
Reset		0	0	0	0	0	0	1	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
084Ch	W	AFCF15	AFCF14	AFCF13	AFCF12	AFCF11	AFCF10	AFCF9	AFCF8
Reset		0	0	0	0	0	0	0	0

AFCF[15:0]: ACK Frame Control Field.
AFCF [15:0] shall be filled in advance based on IEEE 802.15.4 Frame Control Field when ACKS =1 (02h).

9.2.61 PNG Register I、II(Address: 084Dh~084Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
084Dh	R	PNO15	PNO14	PNO13	PNO12	PNO11	PNO10	PNO9	PNO8
	W	PNIV15	PNIV14	PNIV13	PNIV12	PNIV11	PNIV10	PNIV9	PNIV8

Reset		0	1	1	1	0	0	0	1
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
084Eh	R	PNO7	PNO6	PNO5	PNO4	PNO3	PNO2	PNO1	PNO0
Reset	W	PNIV7	PNIV6	PNIV5	PNIV4	PNIV3	PNIV2	PNIV1	PNIV0
Reset		0	1	0	1	0	0	1	1

PNO [15:0]: 16-bits Random number generator output.

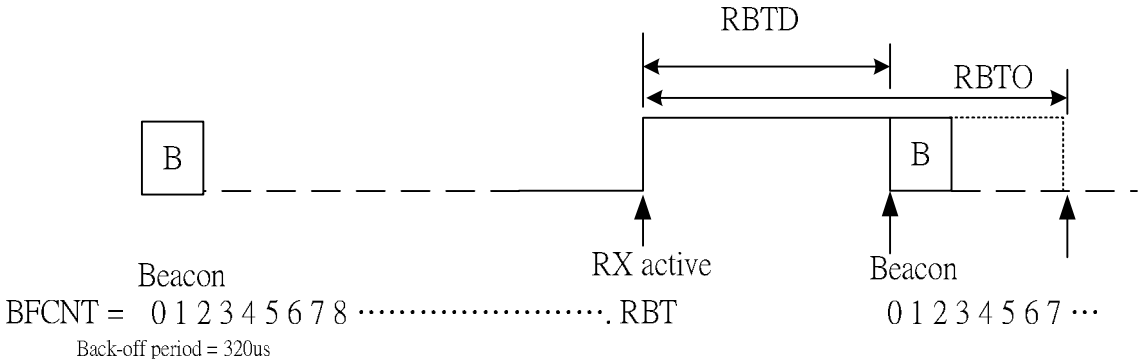
PNIV [15:0]: Initial value of 16-bits Random number generator.

9.2.62 Random Back Off Time-Out Register I、II(Address: 084Fh~0850h)

Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
084Fh	R	RBTD7	RBTD6	RBTD5	RBTD4	RBTD3	RBTD2	RBTD1	RBTD0
	W	RBTO7	RBTO6	RBTO5	RBTO4	RBTO3	RBTO2	RBTO1	RBTO0
Reset		0	0	0	0	0	0	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0850h	R	RBTD15	RBTD14	RBTD13	RBTD12	RBTD11	RBTD10	RBTD9	RBTD8
Reset	W	RBTO15	RBTO14	RBTO13	RBTO12	RBTO11	RBTO10	RBTO9	RBTO8
Reset		0	0	0	0	0	0	0	0

RBTO [15:0]: Random back off time-out in RX.
Time-out = (RBTO+1) X 320 us.

RBTD [15:0]: Random back off difference.
The difference is the value between the active position and the beacon position.



9.2.63 Random Back Off Register Ⅰ、II、III(Address: 0851h~0853h)

Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0851h	R	BFCNT7	BFCNT6	BFCNT5	BFCNT4	BFCNT3	BFCNT2	BFCNT1	BFCNT0
	W	RBT7	RBT6	RBT5	RBT4	RBT3	RBT2	RBT1	RBT0
Reset		0	0	0	0	0	0	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0852h	R	BFCNT15	BFCNT14	BFCNT13	BFCNT12	BFCNT11	BFCNT10	BFCNT9	BFCNT8
	W	RBT15	RBT14	RBT13	RBT12	RBT11	RBT10	RBT9	RBT8
Reset		0	0	0	0	0	0	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0853h	R	BFCNT23	BFCNT22	BFCNT21	BFCNT20	BFCNT19	BFCNT18	BFCNT17	BFCNT16
Reset	W	RBT23	RBT22	RBT21	RBT20	RBT19	RBT18	RBT17	RBT16
Reset		0	0	0	0	0	0	0	0

RBT [23:0]: Random back off active position. (write only)
Active time = (**RBT**+1) X 320us.

BFCNT [23:0]: Random back off counter. (read only)
It could show the position after enable back-off counter or received the beacon frame.
Each back off period is **320us**.
Use the **BFCNT** to calculate the active position (**RBT**).

9.2.64 TXG Register (Address: 0854h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	TMDE	FS	GDR	HFR	XDS	DEVGD2	DEVGD1	DEVGD0
Reset		1	0	1	0	0	0	0	0

TMDE: TX Modulation Enable for VCO Modulation. Recommend TMDE = [1].
[0]: Disable. **[1]:** Enable.

FS: Gaussian Filter Select.
[0]: Disable. **[1]:** Enable.

GDR: Gaussian Filter Over-sampling Rate Select.
[0]: BT= 0.7
[1]: BT= 0.5

HFR: Helf frequency rate select. Recommend HFR = [1].
[0]: 32x. **[1]:** 16x.

XDS: VCO Modulation Data Sampling Clock selection. Recommend XDS = [1].
[0]: 8x over-sampling Clock. **[1]:** XCPCK Clock.

DEVGD [2:0]: Sigma Delta Modulator Data Delay Setting. Recommend DEVGD = [000].

9.2.65 TXG1 Register (Address: 0855h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	PA_HCS	PWORS	PACTL	TRT2	TRT1	TRT0	TXUDS1	TXUDS0
Reset		0	0	1	0	0	0	0	0

PA_HCS: Reserved for internal usage only.

PWORS: Reserved for internal usage only.

PACTL: Reserved for internal usage only.

TRT [2:0]: Reserved for internal usage only.

TXUDS [1:0]: TX ramp up/down clock select.
[00]: 4M [01]: 2M [10]: 1M [11]: 0.5M.

9.2.66 VMG Register (Address: 0856h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
Reset		1	0	1	0	0	0	0	0

VMG [7:0]: VM Center Value for Deviation Calibration. Recommend VMG [7:0] = [0x80].

9.2.67 Code Register (Address: 0857h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FPM1	FPM0	FPFIS	--	CRCIV	CRCS	FECS	WHTS
Reset		0	0	0	--	0	1	0	0

FPM [1:0]: FIFO Pointer Margin
TX: 8, 12, 16, 32 byte; RX: 56, 52, 48, 32 byte

FPFIS: FPF interrupt select.

CRCIV: CRC format invert.
[0]:normal **[1]**:invert.

CRCS: CRC select.
[0]: Disable. **[1]:** Enable.

FECS: FEC select.
[0]: Disable. **[1]:** Enable.

WHTS: Data whitening (Data Encryption) select.
[0]: Disable. **[1]:** Enable.

9.2.68 CRC RX initial value Register 1~2(Address: 0858h~0859h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0859h	W	CRCRIV15	CRCRIV14	CRCRIV13	CRCRIV12	CRCRIV11	CRCRIV10	CRCRIV9	CRCRIV8
085Ah	W	CRCRIV7	CRCRIV6	CRCRIV5	CRCRIV4	CRCRIV3	CRCRIV2	CRCRIV1	CRCRIV0

CRCRIV[15:0]: CRC RX initial value.

9.2.69 CRC TX initial value Register 1~2(Address: 085Ah~085Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
085Ah	W	CRCTIV15	CRCTIV14	CRCTIV13	CRCTIV12	CRCTIV11	CRCTIV10	CRCTIV9	CRCTIV8
085Bh	W	CRCTIV7	CRCTIV6	CRCTIV5	CRCTIV4	CRCTIV3	CRCTIV2	CRCTIV1	CRCTIV0

CRCTIV[15:0]: CRC TX initial value.

9.2.70 CRC polynorminal value Register 1~2(Address: 085Ch~085Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
085Ch	W	CRCPL15	CRCPL14	CRCPL13	CRCPL12	CRCPL11	CRCPL10	CRCPL9	CRCPL8
085Dh	W	CRCPL7	CRCPL6	CRCPL5	CRCPL4	CRCPL3	CRCPL2	CRCPL1	CRCPL0

CRCPL[15:0]: CRC polynorminal value.

9.2.71 WS Register (Address: 085Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	WS6	WS5	WS4	WS3	WS2	WS1	WS0
Reset		--	0	1	0	1	0	1	0

WS [6:0]: Data Whitening seed setting (data encryption key).
Refer to chapter 16 for details.

9.2.72 TH Register (Address: 085Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	PPS	IDL	PTH2	PTH1	PTH0	ETH2	ETH1	ETH0
Reset		0	1	0	1	1	0	1	0

PPS: TX delay fit data select.
[0]: Fit preamble carrier. **[1]:** Fit SID data.

IDL: ID code length select. Recommend IDL= [1].
[0]: 2 bytes. **[1]:** 4 bytes.

PTH [1:0]: Received SID1 Code Error Tolerance. Recommend PTH = [010].
[000]: 0 bit, **[001]:** 1 bit. **[010]:** 2 bit. **[011]:** 3 bit. **[100]:** 4 bit, **[101]:** 5 bit. **[110]:** 6 bit. **[111]:** 7 bit.

ETH [2:0]: Received SID2 Code Error Tolerance. SID2 is only valid if ID length is 8bytes. Recommend ETH = [011].
[000]: 0 bit, **[001]:** 1 bit. **[010]:** 2 bit. **[011]:** 3 bit. **[100]:** 4 bit, **[101]:** 5 bit. **[110]:** 6 bit. **[111]:** 7 bit.

9.2.73 CTR Register (Address: 0860h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
Reset		--	--	1	0	0	0	0	0

CTR [5:0]: Reserved for internal usage only.

9.2.74 BDC Register (Address: 0861h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
name	W	WTLP3	WTLP2	WTLP1	WTLP0	BCD3	BCD2	BCD1	BCD0
Reset		0	0	0	0	1	0	0	0

WTLP[3:0]: WOT loop time.

BDC[3:0]: Battery detector current option select.

9.2.75 SID Register 1~8(Address: 0862h~0869h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0862h	W	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
0863h	W	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8
0864h	W	SID23	SID22	SID21	SID20	SID19	SID18	SID17	SID16
0865h	W	SID31	SID30	SID29	SID28	SID27	SID26	SID25	SID24
0866h	W	SID39	SID38	SID37	SID36	SID35	SID34	SID33	SID32
0867h	W	SID47	SID46	SID45	SID44	SID43	SID42	SID41	SID40
0868h	W	SID55	SID54	SID53	SID52	SID51	SID50	SID49	SID48
0869h	W	SID63	SID62	SID61	SID60	SID59	SID58	SID57	SID56

SID: Serial Packet ID.

9.2.76 ADHL Register Ⅰ、Ⅱ(Address: 086Ah~086Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
086Ah	R	ADH7	ADH6	ADH5	ADH4	ADH3	ADH2	ADH1	ADH0
Reset		0	0	0	0	0	0	0	0
Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
086Bh	R	ADL7	ADL6	ADL5	ADL4	ADL3	ADL2	ADL1	ADL0
Reset		0	0	0	0	0	0	0	0

ADH[7:0]: AD high level calibration result.

ADL[7:0]: AD low level calibration result.

9.2.77 Data Rate Setting Register (Address: 086Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
Reset		0	0	0	0	0	0	0	0

SDR [7:0]: Data Rate Setting. On-air Data rate = MDR / (SDR+1).

9.2.78 FPC Register (Address: 08FBh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0869h	R	--	--	--	--	--	--	--	--
	W					PDNFH	QDSFH	PDNFL	QDSFL
Reset		0	0	0	0	1	0	1	0

PDNFH, QDSFH, PDNFL, QDSFL: Flash power control. Use for PM mode.

9.2.79 USID (Address: 08FCh~08FFh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08FCh	W	USID 7	USID 6	USID 5	USID 4	USID 3	USID 2	USID 1	USID 0
08FDh	W	USID 15	USID 14	USID 13	USID 12	USID 11	USID 10	USID 9	USID 8
08FEh	W	USID 23	USID 22	USID 21	USID 20	USID 19	USID 18	USID 17	USID 16

08FFh	W	USID 31	USID 30	USID 29	USID 28	USID 27	USID 26	USID 25	USID 24

USID [31:0]: USID
USID [7:0] = 8'hA1
USID [15:8] = 8'h81
USID [23:16] = 8'h37
USID [31:24] = 8'h04

10.SOC Architectural Overview

A8125 microcontroller is instruction set compatible with the industry standard 8051. Besides FSK/GFSK modulation RF transceiver, A8125 integrates many features, three 8/16bit counters/timers, watchdog timer, RTC, UART, SPI interface, I^2C interface, 2 channels PWM, 4 channels ADC, battery detector and AES engine. The interrupt controller is extended to support 6 interrupt sources. A8125 includes TTAG (2-wire) debug circuitry that provides full time, real-time, in-circuit debugging.

10.1 Pipeline 8051 MCU

A8125 microcontroller has pipelined architecture 10 times faster compared to standard 8051 architecture. The pipeline 8051 is fully compatible with the MCS-51™ instruction set. User can use standard 8051 assemblers and compilers to develop software. The pipelined architecture 8051 has greatly increases its instruction throughput over the standard 8051 architecture. A8125 has a total of 110 instructions. The table below shows the total number of instructions that require each execution time. For more detail information of instruction, please refer Table 10.1.

Clock to Execute	1	2	3	4	5	6
Number of instructions	24	38	29	11	8	1

10.2 Memory Organization

The memory organization of A8125 is similar to the standard 8051. The memory organization is shown as figure 10.1

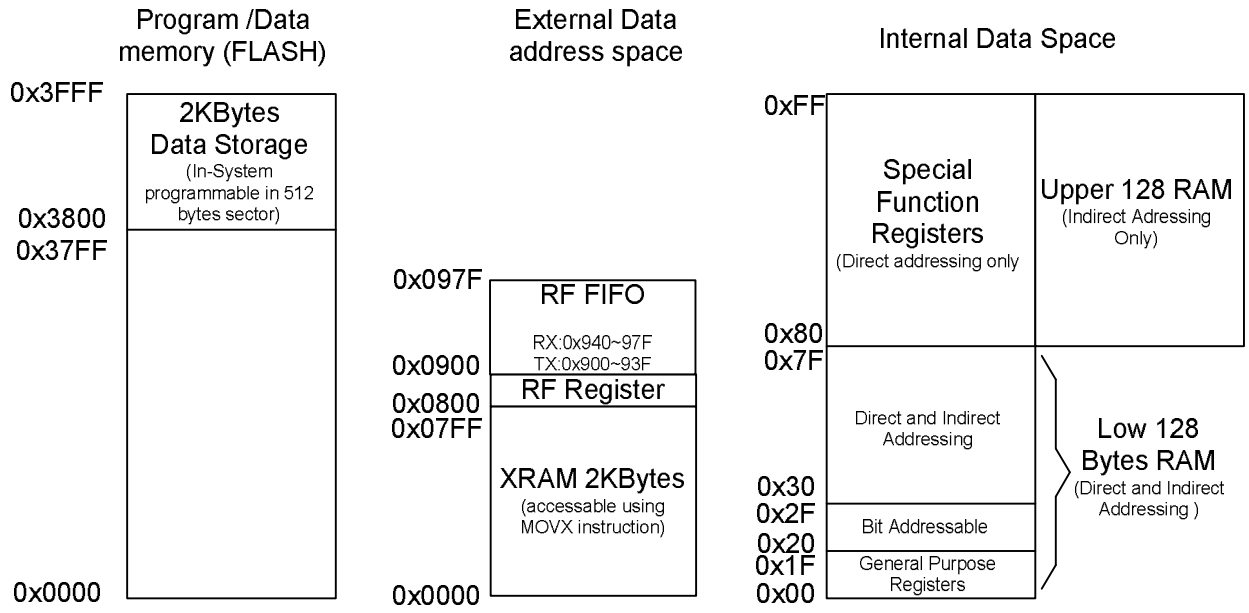


Figure 10.1 Memory Organization

10.2.1 Program memory

The standard 8051 core has 64KB program memory space. A8125 implement 16KB flash. The last 2KB program memory space (0x 3800 ~ 0x3FFF) supports IAP (In-Application Programming) function. The each block size in this area is 128Bytes. User has 16 blocks in 2KB program memory space to storage data. Program memory is normally assumed to be read-only. However, A8125 can write to program memory by IAP function call. Please reference Application note to write program memory for more details.

10.2.2 Data memory

The A8125 includes 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode. The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the MCU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 10.1 illustrates the data memory organization of the A8125.

10.2.3 General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 9.1). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

10.2.4 Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination). The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte.
For example, the instruction:
MOV C, 22.3h moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

10.2.5 Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the MCU resources and peripherals. The MCU duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the MCU. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 9.2 lists the SFRs implemented in the MCU.
The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, SCON, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided.

10.2.6 Stack

A8125 has 8-bit stack point called SP (0x81) located in the internal RAM space. It is incremented before data is stored during PUSH and CALL execution and decremented after data is popped during POP, RET and RETI execution. In the other words it always points to the last valid stack byte. The SP is accessed as any other SFRS.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
81h SP Reset	R/W	0	0	0	0	0	1	1	1

Stack pointer register

10.2.7 Data Pointer Register

A8125 are implemented dual data pointer registers, auto increment and auto decrement to speed up data block copying. DPTR0 and DPTR1 are located at four SFR addresses. Active DPTR register is selected by SEL bit (0x86.0). If SEL = 0 the DPTR0 is selected otherwise DPTR1.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
82h	R/W								

DPL Reset		0	0	0	0	0	0	0	0

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
83h DPH Reset	R/W	0	0	0	0	0	0	0	0

Data Pointer Register DPTR0

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
84h DPL1 Reset	R/W	0	0	0	0	0	0	0	0

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
85h DPH1 Reset	R/W	0	0	0	0	0	0	0	0

Data Pointer 1 Register DPTR1

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
86h DPS Reset	R/W	ID1 0	ID0 0	TSL 0	AU 0		- 0	- 0	SEL 0

Data Pointers Select Register

ID[1:0] - Increment/decrement function select. See table below.
TSL - Toggle select enable. When set, this bit allows the following DPTR related instruction to toggle the SEL bit following execution of the instruction:

```
MOVC A, @A+DPTR
INC DPTR
MOVX @DPTR, A
MOVX A, @DPTR
MOV DPTR, #data16
```

When TSL=0, DPTR related instructions do not affect state of SEL bit.

AU -When set to '1' performs automatic increment(0)/ decrement(1) of selected DPTR according to IDx bits, after each MOVX @DPTR, MOVC @DPTR instructions
SEL - Select active data pointer – see table below

ID1	ID0	SEL=1	SEL=0
0	0	INC DPTR1	INC DPTR
0	1	INC DPTR1	DEC DPTR
1	0	DEC DPTR1	INC DPTR
1	1	DEC DPTR1	DEC DPTR

Table10.1　DPTR0, DPTR1 operations

Selected data pointer register in used in the following instructions:

```
MOVX @DPTR,A
MOVX A,@DPTR
MOVC A,A+DPTR
JMP @A+DPTR
INC DPTR
MOV DPTR,#data16
```

10.2.8 RF Registers and RF FIFO

RF registers are RF radio control registers and located in 0x0800 ~ 0x08ff. Please refer the section 9.2 and the related function setting in the datasheet. A8125 has 128 Bytes FIFO located from 0x0900 to 0x097F. There are 64 bytes FIFO from 0x0900 ~ 0x093F for data transmitting. There are 128 bytes FIFO from 0x0940 ~ 0x097F for data receiving.

10.3 Instruction set

A8125 use a high performance, pipeline 8051 core and it is fully compatible with the standard MCS-51™ instruction set. Standard 8051 development tools can used to develop software for A8125. All A8125 instruction sets are the binary and functional equivalent of the MCS-51™. However, instruct timing is different with the standard 8051. All instruction timings are specified in the terms of clock cycles as shown in the table 10.1

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	4
ADD A,#data	Add immediate data to accumulator	0x24	2	2
ADD A,@Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A,direct	Add direct byte to accumulator	0x25	2	2
ADD A,Rn	Add register to accumulator	0x28-0x2F	1	1
ADDC A,#data	Add immediate data to A with carry flag	0x34	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A,direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A,Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
AJMP addr11	Absolute jump	0x01-0xE1	2	3
ANL C,/bit	AND complement of direct bit to carry	0xB0	2	2
ANL A,#data	AND immediate data to accumulator	0x54	2	2
ANL A,@Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A,direct	AND direct byte to accumulator	0x55	2	2
ANL A,Rn	AND register to accumulator	0x58-0x5F	1	1
ANL C,bit	AND direct bit to carry flag	0x82	2	2
ANL direct,#data	AND immediate data to direct byte	0x53	3	3
ANL direct,A	AND accumulator to direct byte	0x52	2	3
CJNE @Ri,#data	Compare immediate to ind. and jump if not equal	0xB6-0xB7	3	5
CJNE A,#datare	Compare immediate to A and jump if not equal	0xB4	3	4
CJNE A,directre	Compare direct byte to A and jump if not equal	0xB5	3	5
CJNE Rn,#datar	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4
CLR A	Clear accumulator	0xE4	1	1
CLR bit	Clear direct bit	0xC2	2	3
CLR C	Clear carry flag	0xC3	1	1
CPL A	Complement accumulator	0xF4	1	1
CPL bit	Complement direct bit	0xB2	2	3
CPL C	Complement carry flag	0xB3	1	1

DA A	Decimal adjust accumulator	0xD4	1	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	2	3
DEC A	Decrement accumulator	0x14	1	1
DEC direct	Decrement direct byte	0x15	1	3
DEC Rn	Decrement register	0x18-0x1F	1	2
DIV A,B	Divide A by B	0x84	1	6
DJNZ direct,rel	Decrement direct byte and jump if not zero	0xD5	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	0xD8-0xDF	2	4
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
INC A	Increment accumulator	0x04	1	1
INC direct	Increment directbyte	0x05	2	3
INC Rn	Increment register	0x08-0x0F	1	2
INC DPTR	Increment data pointer	0xA3	1	1
JB bit,rel	Jump if direct bit is set	0x20	3	5
JBC bit,directre	Jump if direct bit is set and clear bit	0x10	3	5
JC rel	Jump if carry flag is set	0x40	2	3
JMP@A+DPTR	Jump indirect relative to the DPTR	0x73	1	5
JNB bit,rel	Jumpifdirectbitisnotset	0x30	3	5
JNC	Jump if carry flag is not set	0x50	2	3
JNZ rel	Jump if accumulator is not zero	0x70	2	4
JZ rel	Jump if accumulator is zero	0x60	2	4
LCALL addr16	Long subroutine call	0x12	3	4
LJMP addr16	Long jump	0x02	3	4
MOV A,@Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV bit,C	Move carry flag to direct bit	0x92	2	3
MOV @Ri,#data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV @Ri,A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri,direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV A,#data	Move immediate data to accumulator	0x74	2	2
MOV A,direct	Move direct byte to accumulator	0xE5	2	2
MOV A,Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV C,bit	Move direct bit to carry flag	0xA2	2	2
MOV direct,#data	Move immediate data to direct byte	0x75	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct,A	Move accumulator to direct byte	0xF5	2	2
MOV direct,Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1,direct2	Move direct byte to direct byte	0x85	3	3

MOV DPTR,#data16	Load 16-bit constant in to active DPTR	0x90	3	3
MOV Rn,#data	Move immediate data to register	0x78-0x7F	2	2
MOV Rn,A	Move accumulator to register	0xF8-0xFF	1	1
MOV Rn,direct	Move direct byte to register	0xA8-0xAF	2	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	0x93	1	5
MOVC A,@A+PC	Move code byte relative to PC to accumulator	0x83	1	4
MOVX @DPTR,A	Move A to external SRAM (16-bitaddress)	0xF0	1	1
MOVX @Ri,A	Move A to external RAM (8-bitaddress)	0xF2-0xF3	1	1*
MOVX A,@DPTR	Move external RAM (16-bitaddress) to A	0xE0	1	2*
MOVX A,@Ri	Move external RAM (8-bitaddress) to A	0xE2-0xE3	1	2*
MUL A,B	Multiply A and B	0xA4	1	2
NOP	No operation	0x00	1	1
ORL direct,A	OR accumulator to direct byte	0x42	2	3
ORL A,#data	OR immediate data to accumulator	0x44	2	2
ORL A,@Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A,direct	OR direct byte to accumulator	0x45	2	2
ORL A,Rn	OR register to accumulator	0x48-0x4F	1	1
ORL C,/bit	OR complement of direct bit to carry	0xA0	2	2
ORL C,bit	OR direct bit to carry flag	0x72	2	2
ORL direct,#data	OR immediate data to direct byte	0x43	3	3
POP direct	Pop direct byte from internal ram stack	0xD0	2	2
PUSH direct	Push direct byte on to internal ram stack	0xC0	2	3
RET	Return from subroutine	0x22	1	4
RETI	Return from interrupt	0x32	1	4
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
SJMP rel	Short jump (relative address)	0x80	2	3
SUBB A,@Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A,direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A,#data	Subtract immediate data from A with borrow	0x94	2	2
SUBB A,Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	1
XCH A,@Ri	Exchange indirect RAM with accumulator	0xC6-0xC7	1	3

XCH A,direct	Exchange direct byte with accumulator	0xC5	2	3
XCH A,Rn	Exchange register with accumulator	0xC8-0xCF	1	2
XCHD A,@Ri	Exchange low-order nibble indirect RAM with A	0xD6-0xD7	1	3
XRL direct,#data	ExclusiveOR immediate data to direct byte	0x63	3	3
XRL A,#data	ExclusiveOR immediate data to accumulator	0x64	2	2
XRL A,@Ri	ExclusiveOR indirect RAM to accumulator	0x66-0x67	1	2
XRL A,direct	ExclusiveOR direct byte to accumulator	0x65	2	2
XRL A,Rn	ExclusiveOR register to accumulator	0x68-0x6F	1	1
XRL direct,A	ExclusiveOR accumulator to direct byte	0x62	2	3

Table 10.2 Instruction set sorted by alphabet

10.4 Interrupt handler

This section describes 8051 interrupts and their functionality. For peripherals related interrupts, please refer to an appropriate peripheral section. The external interrupts symbol is shown in figure above. And the pins functionality is described in the following table. All pins are one directional. There are no three-state output pins and internal signals.

Name	ACTIVE	TYPE	DESCRIPTION
INT0(P3.2)	low/falling	Input	External interrupt 0 line
INT1(P3.3)	low/falling	Input	External interrupt 1 line
INT2(P0.7)	low	Input	External interrupt 2 line

Table 10.3 External interrupts pins description

10.4.1 FUNCTIONALITY

The interrupt system has implemented two levels interrupt priority control. Each external interrupt can be in high or low level priority group by setting or clearing a bit in the IP(0xB8) and EIP(0xF8) registers. External interrupt pins are activated at low level or by a falling edge. Interrupt requests are sampled each system clock at the rising edge of CLK.

Interrupt flag	Function	Active level/edge	Flag resets	Vector[1]	Natural priority
IE0	Device pin INT0	Low/falling	Hardware	0x03	1
TF0	Internal, Timer 0	-	Hardware	0x0B	2
IE1	Device pin INT1	Low/falling	Hardware	0x13	3
TF1	Internal, Timer 1	-	Hardware	0x1B	4
TI & RI	Interrupt, UART	-	Software	0x23	5
TF2	Interrupt, Timer 2	-	Software	0x2B	6
Reserved	Reserved	-	Software	0x33	7
INT2F	Device pin INT2	Low	Hardware	0x3B	8
Reserved	Reserved	-	-	0x43	9
Reserved	Reserved	-	-	0x4B	10
RFINTF	Interrupt, RFINT	-Falling	Software	0x53	11
KEYINTF	Interrupt, KeyINT	-Falling	Software	0x5B	12
WDIF	Internal, Watchdog	-	Software	0x63	13
I2CMIF	Internal, I2C MASTER MODULE	-	Software	0x6B	14
I2CSIF SPIIF	Internal, DI2CS/ Internal, SPI	-	Software	0x73	15

Table10.4 8051 interrupts summary

1- This is a default location when IRQ_INTERVAL = 8, in other case is equal to (IRQ_INTERVAL* n) + 3, when n = (natural Priority - 1)

2- The recommend start address of program is 08Bh. It can avoid the program crash by the exception or interrupts happens.

Each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the IE(0xA8), and EIE(0xE8). The IE contains global interrupt system disable (0) / enable (1) bit called EA.

IE register (0xA8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8h IE	R/W	EA	-	ET2	ES	ET1	EX1	ET0	EX0
Reset		0	0	0	0	0	0	0	0

EA：Enable global interrupts
EX0：Enable INT0 interrupts
ET0：Enable Timer 0 interrupts
EX1：Enable INT1 interrupts
ET1：Enable Timer 1 interrupts
ES：Enable UART interrupts
ET2：Enable Timer 2 interrupts

All of bits that generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software. The exceptions of this rule are the request flags IE0 and IE1. If the external interrupts 0 or 1 are programmed to be level activated, IE0 and IE1 are controlled by the external source via pin INT0 and INT1, respectively. Thus, writing a one to these bits will not set the request flag IE0 and/or IE1. The same exception is related to INT2F, INT3F, INT4F, RFINTF, and KEYINTF – external interrupts number 2, 3, 4, 5, 6.

IP register (0xB8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B8h IP	R/W	-	-	PT2	PS	PT1	PX1	PT0	PX0
Reset		0	0	0	0	0	0	0	0

PX0：INT0 priority level control (at 1-high-level)
PT0：Timer 0 priority level control (at 1-high-level)
PX1：INT1 priority level control (at 1-high-level)
PT1：Timer 1 priority level control (at 1-high-level)
PS：UART priority level control (at 1-high-level)
PT2：Timer 2 priority level control (at 1-high-level)

TCON register (0x88)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
88h TCON	R/W	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Reset		0	0	0	0	0	0	0	0

IT0：INT0 level (at 0) / edge (at 1) sensitivity
IT1：INT1 level (at 0) / edge (at 1) sensitivity
IE0：INT0 interrupt flag
Cleared by hardware when processor branches to interrupt routine
IE1：INT1 interrupt flag
Cleared by hardware when processor branches to interrupt routine
TF0：Timer 0 interrupt (overflow) flag
Cleared by hardware when processor branches to interrupt routine
TF1：Timer 1 interrupt (overflow) flag
Cleared by hardware when processor branches to interrupt routine

SCON register (0x98)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
98h SCON	R/W	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Reset		0	0	0	0	0	0	0	0

RI：UART receiver interrupt flag
TI：UART transmitter interrupt flag

EIE register (0xE8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8h EIE	R/W	EI2CS ESPI	EI2CM	EWDI	EKEYINT	ERFINT	EINT4	EINT3	EINT2
Reset		0	0	0	0	0	0	0	0

EINT2：Enable INT2 interrupts
EINT3：Enable INT3
EINT4：Enable INT4
ERFINT：Enable RF INT
EKEYINT：Enable KEY INT
EWDI：Enable Watchdog interrupts
EI2CM：Enable I2C MASTER MODULE interrupts
EI2CS：Enable DI2CS interrupts
ESPI：Enable SPI MODULE interrupts

EIP register (0xF8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F8h EIP	R/W	PI2CS PSPI	PI2CM	PWDI	PKEYINT	PRFINT	PINT4	PINT3	PINT2
Reset		0	0	0	0	0	0	0	0

PINT2：INT2 priority level control (at 1-high-level)
PINT3：INT3/Compare 0 priority level control (at 1-high-level)
PINT4：INT4/Compare 1 priority level control (at 1-high-level)
PRFINT：RFINT priority level control (at 1-high-level)
PKEYINT：KEYINT priority level control (at 1-high-level)
PWDI：Watchdog priority level control (at 1-high-level)
PI2CM：I2C MASTER MODULE priority level control (at 1-high-level)
PI2CS：I2C MODULE priority level control (at 1-high-level)
PSPI：SPI MODULE priority level control (at 1-high-level)

EIF register (0x91)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
91h EIF	R/W	I2CSF SPIF	I2CMF	-	KEYINTF	RFINTF	INT4F	INT3F	INT2F
Reset		0	0	0	0	0	0	0	0

INT2F：INT2 interrupt flag

Should be cleared by external hardware when processor branches to interrupt routine. This bit is a copy of INT2 pin updated every CLK period. It cannot be set by software.

INT3F*：INT3/Compare 0 interrupt flag

Should be cleared by external hardware when processor branches to interrupt routine. t cannot be set by software.

INT4F*：INT4/Compare 1 interrupt flag

Should be cleared by external hardware when processor branches to interrupt routine.　It cannot be set by software.

RFINTF：RFINT interrupt flag

Must be cleared by software writing 0x08 when controlled by RFINT.

KEYINTF：KEYINT interrupt flag

Must be cleared by software writing 0x10 when controlled by KEYINT.

I2CMIF：I2C MASTER MODULE interrupt flag. It must be cleared by software writing 0x40. It cannot be set by software

I2CSIF：I2C MODULE interrupt flag

SPIIF：SPI MODULE interrupt flag

Software should determine the source of interrupt by checking both modules' interrupt related bits. It must be cleared by software writing 0x80. It cannot be set by software.

10.5 Reset source

Reset circuitry allows A8125 to be easily placed in a predefined default confition. LVD, Reset, POR, and Watchdog signal will reset 8125 when they happen.

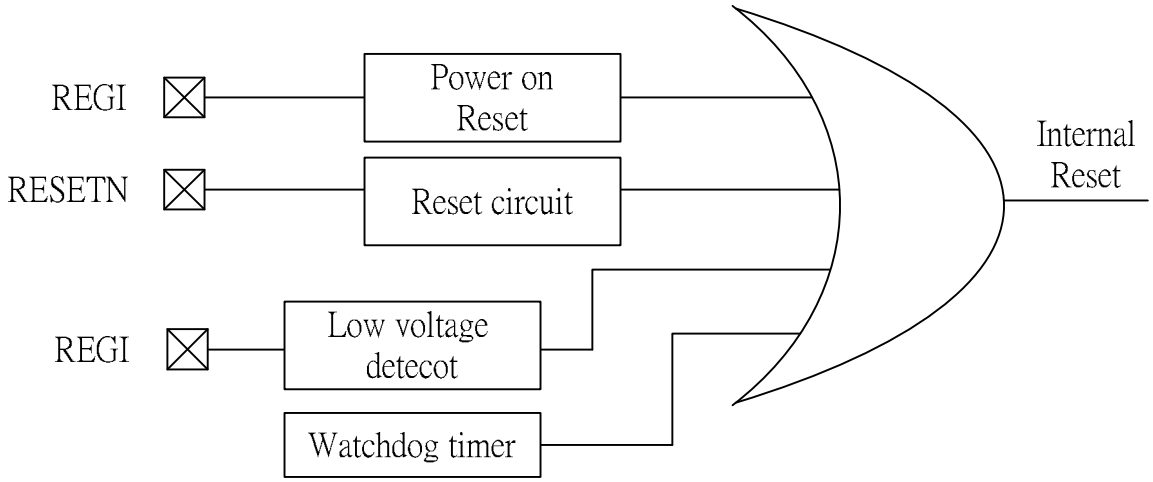


Figure 10.2 Reset source

RSFLAG: Reset Flag(0xBA):

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BAh RSFLAG	R	-	-	-	-	-	LVDF	RESETNF	PORF
Reset		0	0	0	0	0	0	0	1

Write any data to RSFLAG to clear all bits.

PORF (power-on reset flag)

= 1: Occurred Power-on Reset

= 0: No Power-on Reset

RESETNF (resetn flag)

= 1: Occurred ResetN reset

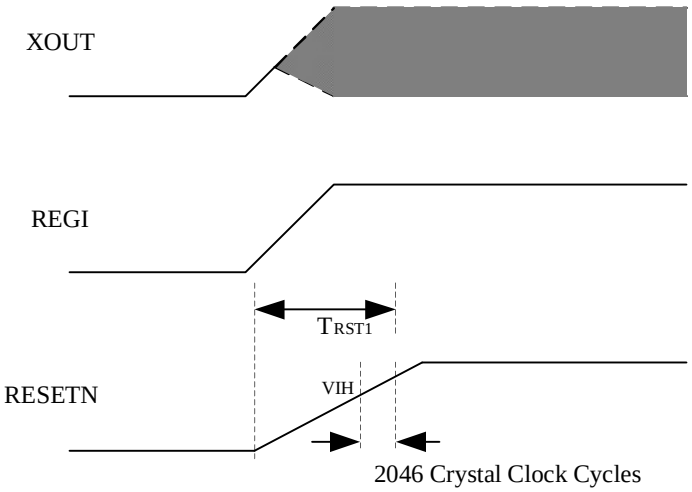
= 0: No ResetN resetno resetn reset

LVDF (Low voltage detect) flag

= 1: Occurred Low Voltage Reset

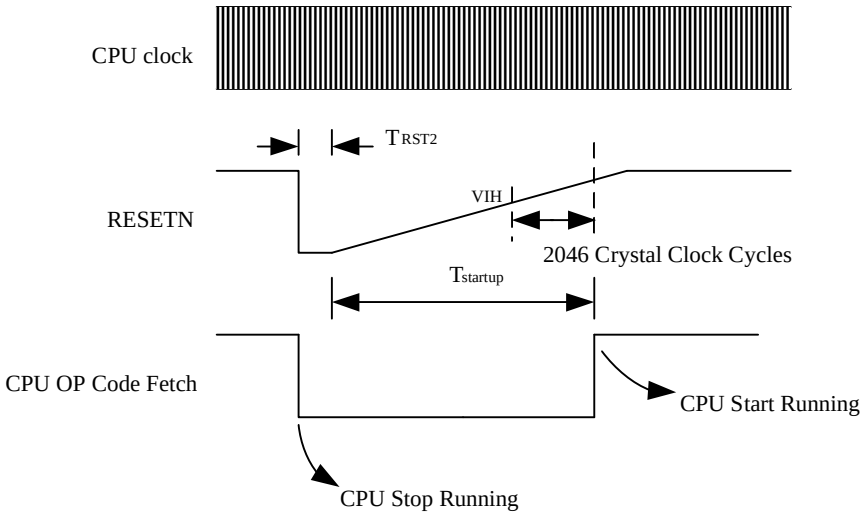
= 0: No Low Voltage reset

Please refer the figure 10.3 and 10.4 for the timing diagram for stable power of reset signal and internal behavior of CPU.



T_{RST1} : According to RESETN's RC delay (standard module is about 50ms)

Figure 10.3 Timing Diagram for stable power to the release of RESETN



T_{RST2} : 2 Crystal Clock Cycles (min)

$T_{startup}$: 2046 Crystal Clock Cycles + RESETN's RC delay (standard module is about 50ms)

Figure 10.4 Timing Diagram for RESETN control sequence

10.6 Clock source

A8125 has three clock source, crystal oscillator (pin 13,14/ Xi, XO), RTC crystal (pin 1,2/ P3.6, P3.7/ RTC_I, RTC_O) and internal RC oscillator. In the MCU part (digital peripherals), user choices the suitable clock source by power consumptions and performance. In the RF part, the clock source only comes from XO..

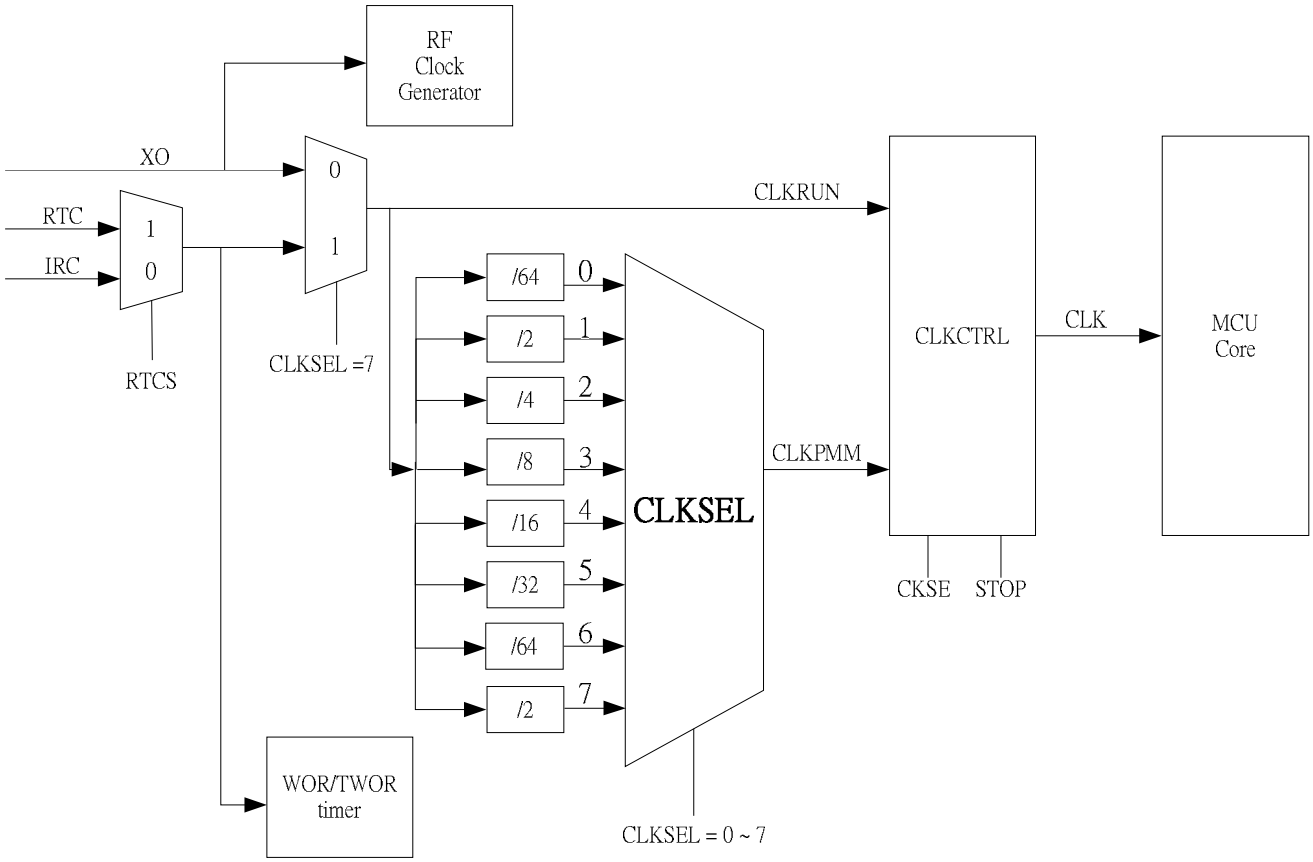


Figure 10.3 Whole chip clock

11. I/O Ports

A8125 has 24 Digital I/O Pins. There are separated to 3 Ports (Port0, Port1 and Port3) and each of the Port pin can be defined as general-purpose I/O (GPIO) or peripheral I/O signals connected to the timers, UART, I2C and SPI functions. Thus, each pin can also be used to wake A8125 up from sleep mode. User can select each pin function by setting register. Each port has itself port register like P0 (0x80), P1 (0x90) and P3 (0xB0) that are both byte addressable and bit addressable. When reading, the logic levels of the Port's input pins are returned. Each port has three registers to setting Pull-up (PUN), Output-enable (OE) and Wake-up enable (WUN). As shown the bellow block diagram, Fig. 11.1. Unused I/O pins should have a defined level and not be left floating. One way to do this is to leave the pin unconnected and configure the pin as a general-purpose I/O input with pull-up resistor.

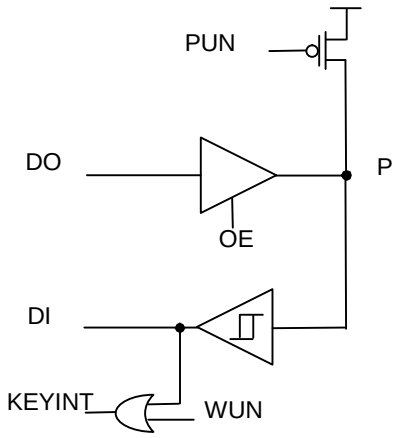


Figure11.1 Ports I/O block diagram

OE	PUN	P	DI
0	0	1	1
0	1	HZ	INH
1	X	DO	DO

Table 11.1 OE and PUN setting and Output(P) and Input(DI)

WUN	KEYINT
0	Enable
1	Disable

Table 11.2 WUN setting and KEYINT source

11.1 FUNCTIONALITY

It has three 8-bit full bi-directional ports, P0, P1 and P3. Each port bit can be individually accessed by bit addressable instructions.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h P0	R/W								
Reset		0	0	0	0	0	0	0	0

Port 0 register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
90h P1	R/W								

Reset		0	0	0	0	0	0	0	0

Port 1 register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B0h P3	R/W								
Reset		0	0	0	0	0	0	0	0

Port 3 register

Read and write accesses to the I/O port are performed via their corresponding SFRs P0(0x80), P1(0x90), and P3(0xB0). Some port-reading instructions read the data register and others read the port's pin. The "Read-Modify-Write" instructions are directed to the data registers and are shown below. All the other instructions used to read a port exclusively read the port's pin.

Instruction	Function description
ANL	Logic AND
ORL	Logic OR
XRL	Logic eXclusive OR
JBC	Jump if bit is set and clear
CPL	Complement bit
INC, DEC	Increment, decrement byte
DJNZ	Decrement and jump if not zero
MOV Px.y, C	Move carry bit to y of port x
CLR Px.y	Clear bit y of port x
SETB Px.y	Set bit y of port x

Table11.3 Read-modify-write instructions

According the Table 11.1, all Port pins can be configured as Output, Input with the pull-up resistor (around 100 Kohm) or Input. Please refer the following truth table to know every function setting. When OE=1, this pin is configured as Output. Otherwise OE =0, this pin is configured as Input. User can set PUN =1 or 0 depending on application. When OE =0, PUN=0 is recommended for saving power.

All Port pins can wake A8125 up when WUEN=0 and configured GPIO. All Port pins' WUN signals connect one OR gate to KEYINT. It means pin wake up function needs KEYINT ISR to take care this interrupt event.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D1h P0OE	R/W								
Reset		0	0	0	0	0	0	0	0

Port 0 Output Enable Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D2h P0PUN	R/W								
Reset		0	0	0	0	0	0	0	0

Port 0 Pull Up Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D3h P0WUN	R/W								
Reset		1	1	1	1	1	1	1	1

Port 0 Wake Up Enable Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D9h P1OE	R/W								
Reset		0	0	0	0	0	0	0	0

Port 1 Output Enable Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAh P1PUN	R/W								
Reset		0	0	0	0	0	0	0	0

Port 1 Pull Up Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DBh P1WUN	R/W								
Reset		1	1	1	1	1	1	1	1

Port 1 Wake Up Enable Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E1h P3OE	R/W								
Reset		0	0	0	0	0	0	0	0

Port 3 Output Enable Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E2h P3PUN	R/W								
Reset		0	0	0	0	0	0	0	0

Port 3Pull Up Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E3h P3WUN	R/W								
Reset		1	1	1	1	1	1	1	1

Port 3 Wake Up Enable Register

IOSEL Register (0xBB)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BBh IOSEL	R/W	ADCIOS2	ADCIOS1	ADCIOS0	RTCIOS	BBIOS	-	I2CIOS	UARTIOS
Reset		0	0	0	0	0	0	0	0

ADCIOS[2:0] (ADC I/O select)
ADCIOS[2:1]
[00]: Select P3.2 as the ADC analog input
[01]: Select P3.3 as the ADC analog input
[10]: Select P3.4 as the ADC analog input
[11]: Select P3.5 as the ADC analog input
ADCIOS0
[1]: Enable ADC analog input
[0]: Disable ADC analog input
RTCIOS (Real-time clock I/O select)
[1]: The pad is for RTC clock
[0]: The pad is normal I/O
BBIOS (Base band I/O select)
[1]: P0.7, P1.2, P1.3 are selected for RF GPIO1,GPIO2,CKO function pin
[0]: P0.7, P1.2, P1.3 are normal I/O
I2CIOS (I2C I/O select)
[1]: The pad is selected for I2C (open drain I/O)
[0]: The pad is normal I/O
UARTIOS (UART0 I/O select)
[1]: Port 3.0 and Port3.1 are selected for UART0 mode0 (open drain I/O)

[0]: Port 3.0 and Port3.1 are normal I/O

11.2 Key interrupt

User can use P0, P1 or P3 port as key input and meanwhile these key are clicked to event a key interrupt to wake up A8125 or enter key process flow. It is a helpful use to design a remote controller and low power consumption with power saving mode setting. The KEY INT vector is located on 0x5B. User can put an interrupt service routine in 0x5B.

The KEY interrupts can wake up A8125 back to normal mode in PM1 and PM2. In PM3, Port 3.2~Port 3.5 and RESETN PIN will reset A8125 and A8125 need to initial all needed peripherals and take care key interrupt event.

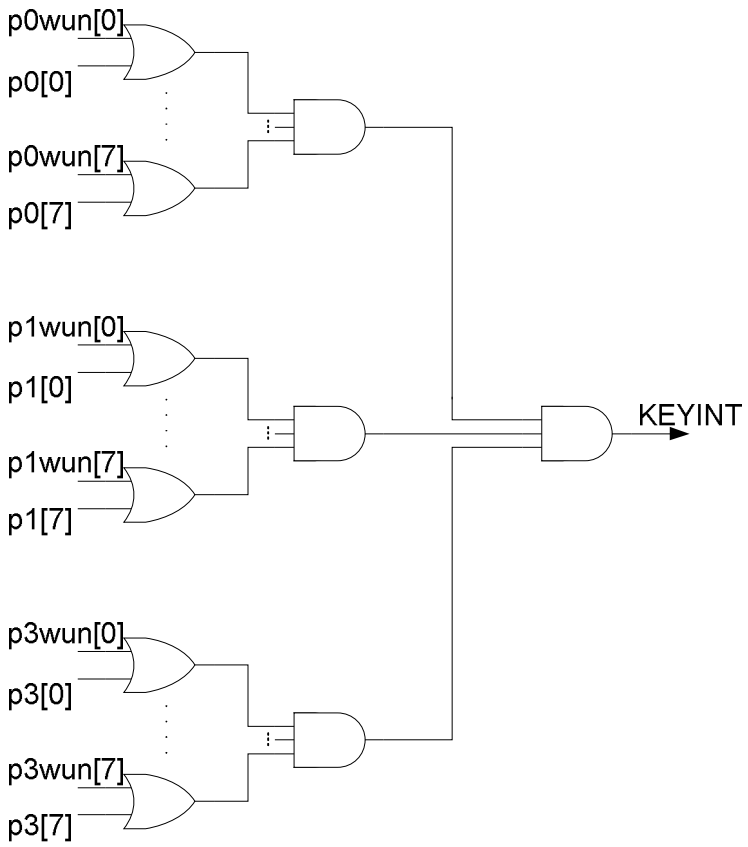


Figure11.2 Key interrupt block diagram

12. Timer 0, 1 and Timer 2

A8125 contains three 16-bit timer/counters, Timer 0, Timer 1 and Timer 2. Timer 0 and Timer 1 in the “timer mode“, timer registers are incremented every 4/12/CLK periods depends on CKCON (0x8E) setting, when appropriate timer is enabled. In the “counter mode” the timer registers are incremented every falling transition on theirs corresponding input pins: T0 or T1. The input pins are sampled every CLK period.

The Timer 2 is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc.

12.1 Timer 0 & 1 PINS DESCRIPTION

The pins functionality is described in the following table. All pins are one directional.

PIN	ACTIVE	TYPE	DESCRIPTION
T0(P3.4)	Falling	Input	Timer 0 clock line
GATE0(P3.2)	High	Input	Timer 0 clock line gate control
T1(P3.5)	Falling	Input	Timer 1 clock line
GATE1(P3.3)	High	Input	Timer 1clock line gate control

Table12.1 Timer 0, 1 pins description

12.2 Timer 0 & 1 FUNCTIONALITY

12.2.1 OVERVIEW

Timer 0 and Timer 1 are fully compatible with the standard 8051 timers. Each timer consists of two 8-bit registers TH0 (0x8C), TL0 (0x8A), TH1 (0x8D), TL1 (0x8B). Timers 0, 1 work in the same four modes. The modes are described below.

M1	M0	Mode	Function description
0	0	0	THx operates as 8-bit timer/counter with a divide by 32 prescaler served by lower 5-bit of TLx.
0	1	1	16-bit timer/counter. THx and TLx are cascaded.
1	0	2	TLx operates as 8-bit timer/counter with 8-bit auto-reload by THx.
1	1	3	TL0 is configured as 8-bit timer/counter controlled by the standard Timer 0 bits. TH0 is an 8-bit timer controlled by the Timer 1 controls bits. Timer 1 holds its count.

Table12.2 Timer 0 and 1 modes

12.2.2 Timer 0 & 1 Registers

TMOD register (0x89)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
89h TMOD	R/W	GATE1	CT	M1	M0	GATE0	CT	M1	M0
		Timer 1 control bits				Timer 0 control bits			
Reset		0	0	0	0	0	0	0	0

GATE：Gating control

=1, Timer x enabled while GATEx pin is high and TRx control bit is set.

=0, Timer x enabled while TRx control bit is set.

CT：Counter or timer select bit

=1, Counter mode, Timer x clock from Tx pin.

=0, Timer mode, internally clocked.

M[1：0]：Mode select bits

TCON register (0x88)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
88h TCON	R/W	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Reset		0	0	0	0	0	0	0	0

TR0：Timer 0 run control bit

=1, enabled.

=0, disabled.

TR1：Timer 1 run control bit
=1, enabled.
=0, disabled.
TF0：Timer 0 interrupt (overflow) flag.
Cleared by hardware when processor branches to interrupt routine.
TF1：Timer 1 interrupt (overflow) flag.
Cleared by hardware when processor branches to interrupt routine.

CKCON register (0x8E)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8Eh CKCON	R/W	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
Reset		0	0	0	0	0	0	0	0

T2M：This bit controls the division of the system clock that drives Timer 2.
=1, Timer 2 uses a divided-by-4 of the system clock frequency.
=0, Timer 2 uses a divided-by-12 of the system clock frequency.

T1M：This bit controls the division of the system clock that drives Timer 1.
=1, Timer 1 uses a divided-by-4 of the system clock frequency.
=0, Timer 1 uses a divided-by-12 of the system clock frequency.

T0M：This bit controls the division of the system clock that drives Timer 0.
=1, Timer 0 uses a divided-by-4 of the system clock frequency.
=0, Timer 0 uses a divided-by-12 of the system clock frequency.

IE register (0xA8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8h IE	R/W	EA	-	ET2	ES	ET1	EX1	ET0	EX0
Reset		0	0	0	0	0	0	0	0

EA：Enable global interrupts.
ET0：Enable Timer 0 interrupts.
ET1：Enable Timer 1 interrupts.

IP register (0xB8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B8h IP	R/W	-	-	PT2	PS	PT1	PX1	PT0	PX0
Reset		0	0	0	0	0	0	0	0

PT0：Timer 0 priority level control (at 1-high level)
PT1：Timer 1 priority level control (at 1-high level)

Timer 0, 1 related bits that generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Natural priority
TF0	Internal, Timer 0	-	Hardware	0x0B	2
TF1	Internal, Timer 1	-	Hardware	0x1B	4

Table12.3　Timer 0, 1 interrupts

12.2.3 Timer 0 – Mode 0

In this mode, the Timer 0 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s. Timer 0 interrupt flag TF0 is set. The counted input is enabled to the Timer 0 when TCON.4 = 1 and either TMOD.3 = 1 or GATE0 = 1. (Setting TMOD.3 = 1 allows the Timer 0 to be controlled by external input GATE0, to facilitate pulse width measurement). The 13-bit register consists of all 8-bit of TH0 and lower 5 bits of TL0.The upper 3 bits of TL0 are indeterminate and should be ignored.

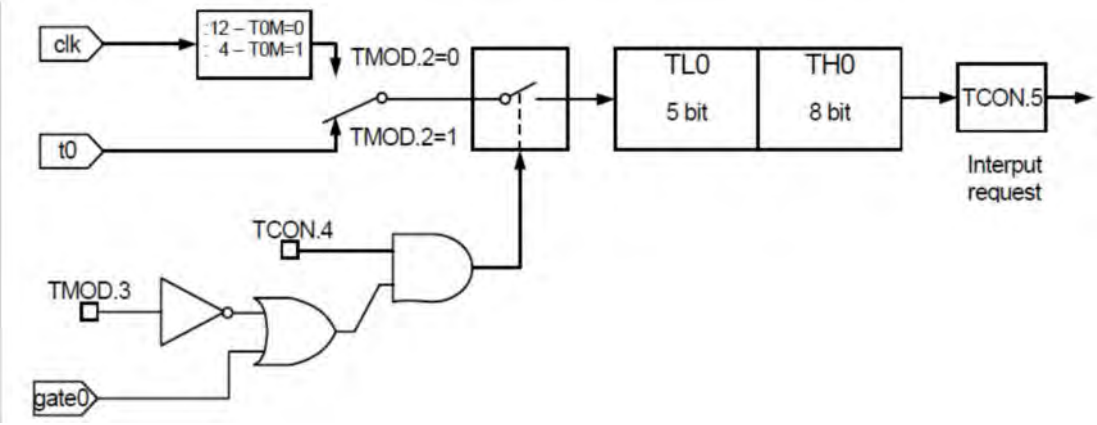


Figure12.1　Timer/Counter 0, Mode 0：13-Bit Timer/Counter

12.2.4 Timer 0 – Mode 1

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. Mode 1 is shown in figure below.

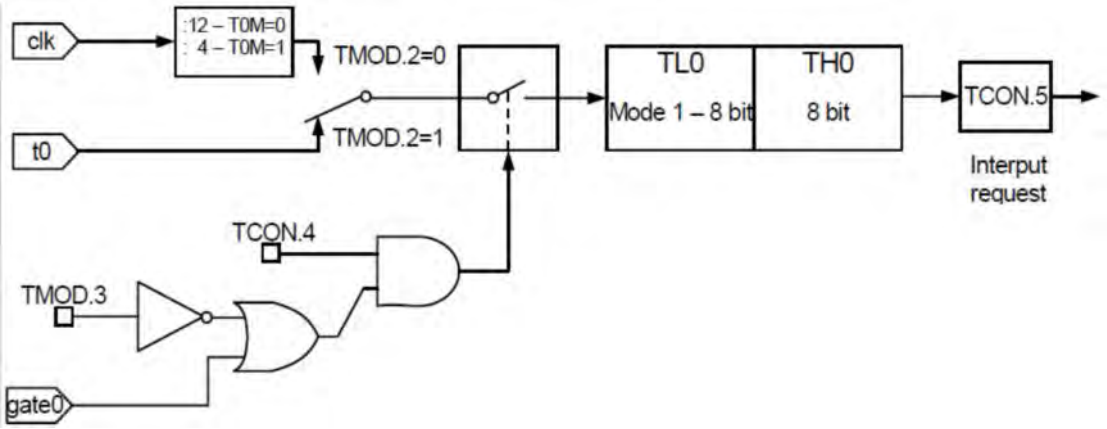


Figure12.2　Timer/Counter 0, Mode 1：16-Bit Timer/Counter

12.2.5 Timer 0 – Mode 2

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reloads, as shown in figure below. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is loaded by software. The reload leaves TH0 unchanged.

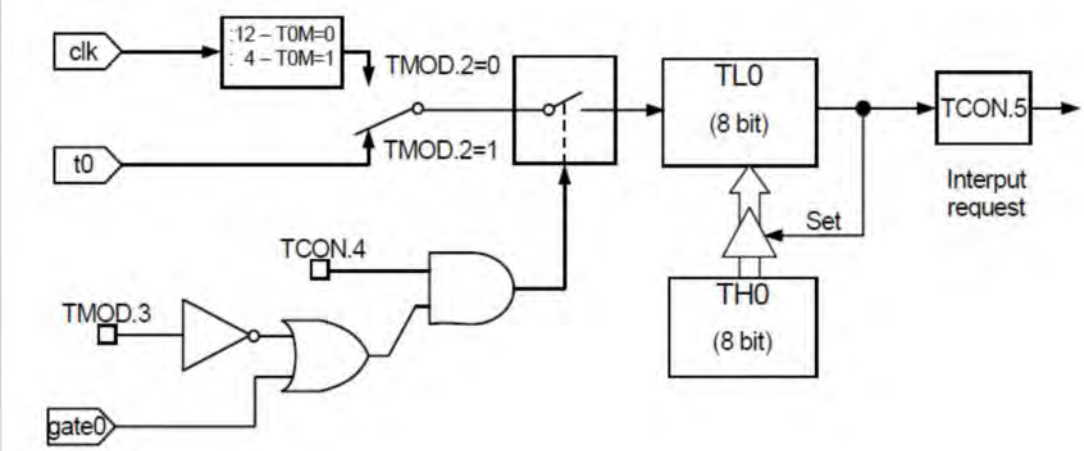


Figure12.3　Timer/Counter 0, Mode 2：8-Bit Timer/Counter with Auto-Reload

12.2.6 Timer 0 – Mode 3

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in figure below. TL0 uses the Timer 0 control bits：C/T, GATE, TR0, GATE0 and TF0. TH0 is locked into a timer function and use the TR1 and TF1 flag from Timer1 and controls Timer1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer/counter. When Timer 0 is in Mode 3, Timer 1 can be turned off by switching it into its own Mode 3, or can still be used by the serial channel as a baud rate generator, or in any application where interrupt from Timer 1 is not required.

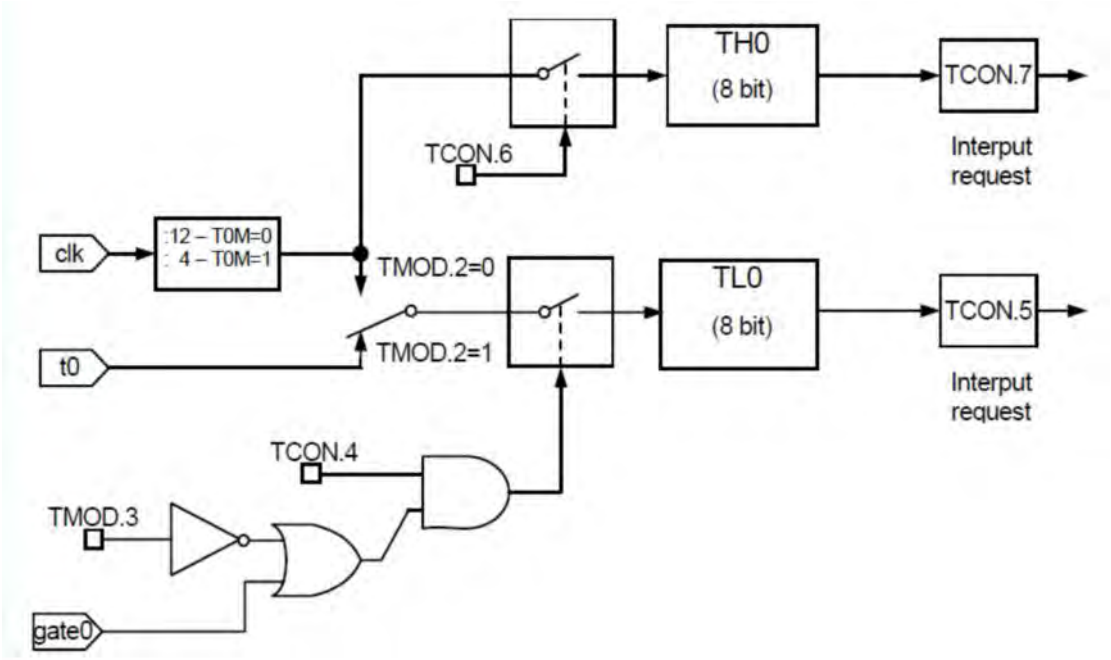


Figure12.4　Timer/Counter 0, Mode 3：Two 8-Bit Timers/Counters

12.2.7 Timer 1 – Mode 0

In this Mode, the Timer1 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer1 interrupt flag TF1 is set. The counted input is enabled to the Timer1 when TCON.6 = 1 and either TMOD.6 = 0 or GATE1 = 1. (Setting TMOD.7 = 1 allows the Timer1 to be controlled by external input GATE1, to facilitate pulse width measurements). The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored.

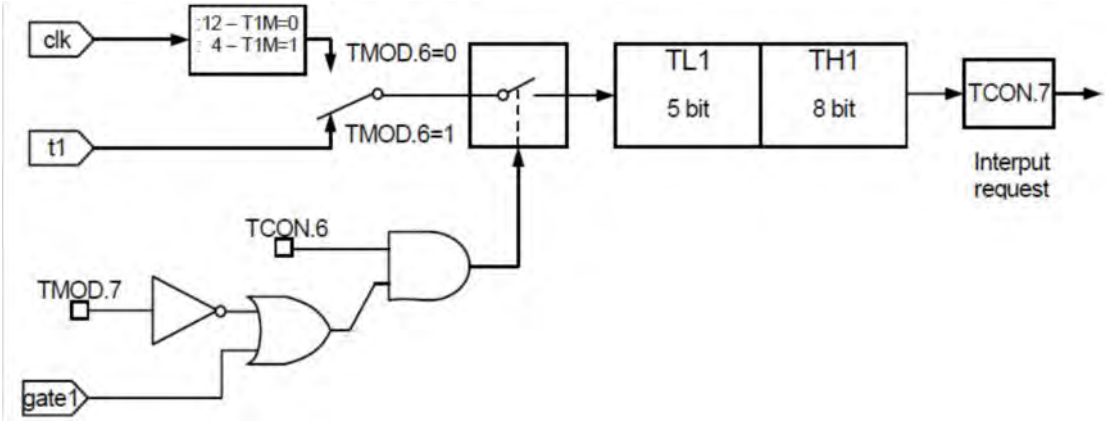


Figure12.5 Timer/Counter 1, Mode 0：13-Bit Timers/Counters

12.2.8 Timer 1 – Mode 1

Mode 1 is the same as Mode 0, except that timer register is running with all 16 bits. Mode 1 is shown in figure below.

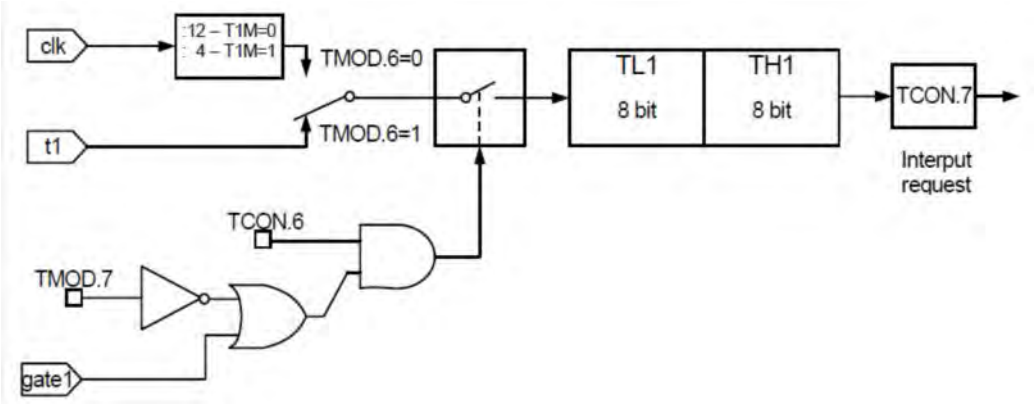


Figure12.6　Timer/Counter 1, Mode 0：16-Bit Timers/Counter

12.2.9 Timer 1 – Mode 2

Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reloads, as shown in figure below. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is loaded by software. The reload leaves TH1 unchanged.

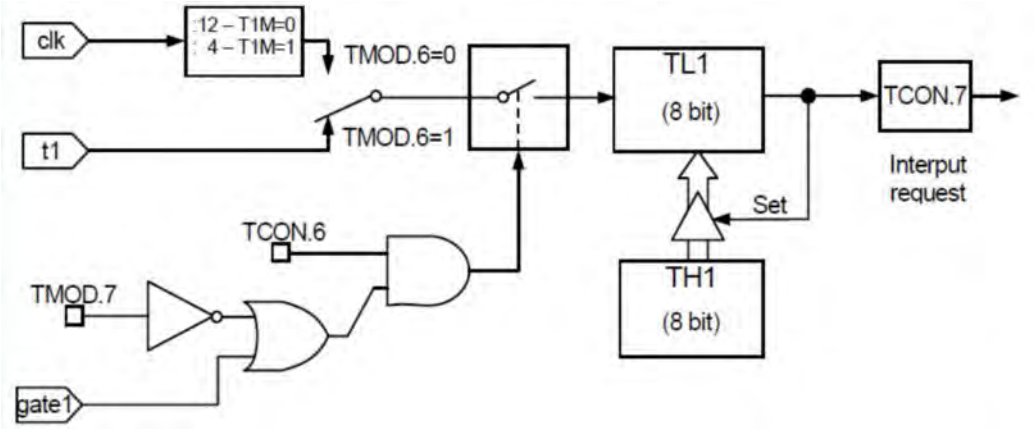


Figure12.7　Timer/Counter 1, Mode 2：8-Bit Timer/Counter with Auto-Reload

12.2.10 Timer 1 – Mode 3

Timer 1 in Mode 3 is held counting. The effect is the same as setting TR1=0.

12.3 Timer2 PINS DESCRIPTION

The Timer 2 pins functionality is described in the following table. All pins are one directional.

PIN	ACTIVE	TYPE	DESCRIPTION
t2(P1.0)	falling	INPUT	Timer 2 clock line
t2ex(P1.1)	high	INPUT	Timer 2 control

Table12.4 Compare/Capture pins description

12.4 Timer2 FUNCTIONALITY

12.4.1 OVERVIEW

Timer 2 is fully compatible with the standard 8052 Timer 2. It is up counter. Totally five SFRs control the Timer 2 operation: TH2/TL2(0xCD/0xCC) counter registers, RCAP2H/RCAP2L (0xCB/0xCA) capture registers and T2CON(0xC8) control register. Timer 2 works in the three modes selected by T2CON bits as shown in table below.

RCLK, TCLK	CPRL2	TR2	Function description
0	0	1	16-bit auto-reload mode. The Timer 2 overflow sets TF2 bit and the TH2,TL2 registers reloaded 16-bit value from RCAP2H, RCAP2L.
0	1	1	16-bit capture mode. The Timer 2 overflow sets TF2 bit. When the EXEN2 = 1, the TH2, TL2 register values are stored into RCAP2H, RCAP2Lwhile falling edge is detected on T2EX pin.
1	X	1	Baud rate generator for the UART0 interface. It auto-reloads its counter with RCAP2H, RCAP2Lvalues each overflows.
X	X	0	Timer 2 is off

Table12.5　　Timer 2 modes

12.4.2 Timer 2 Registers

T2CON register　　(0xC8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C8h	R/W	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2
APOL									
Reset		0	0	0	0	0	0	0	0

EXF2：Falling edge indicator on T2EX pin when EXEN = 1. Must be cleared by software.

RCLK：Receiver clock enable

=1, UART0 receiver is clocked by Timer 2 overflow pulses

=0, UART0 receiver is clocked by Timer 2 overflow pulses

TCLK：Transmit clock enable

=1, UART0 transmitter is clocked by Timer 2 overflow pulses

=0, UART0 transmitter is clocked by Timer 2 overflow pulses

EXEN2：Enable T2EX pin functionality.

=1, Allows capture or reload as a result of T2EX pin falling edge.

=0, ignore T2EX events

TR2：Start / Stop Timer 2

=1, start

=0, stop

CT2：Timer / counter select

=1, external event counter. Clock source is T2 pin.

=0, timer 2 internally clocked

CPRL2：Capture / Reload select

=1, T2EX pin falling edge causes capture to occur when EXEN2 = 1

=0, automatic reload occurs on Timer 2 overflow or falling edge T2EX pin when EXEN2 = 1. When RCLK or TCLK is set this bit is ignored and automatic reload on Timer 2 overflow is forced.

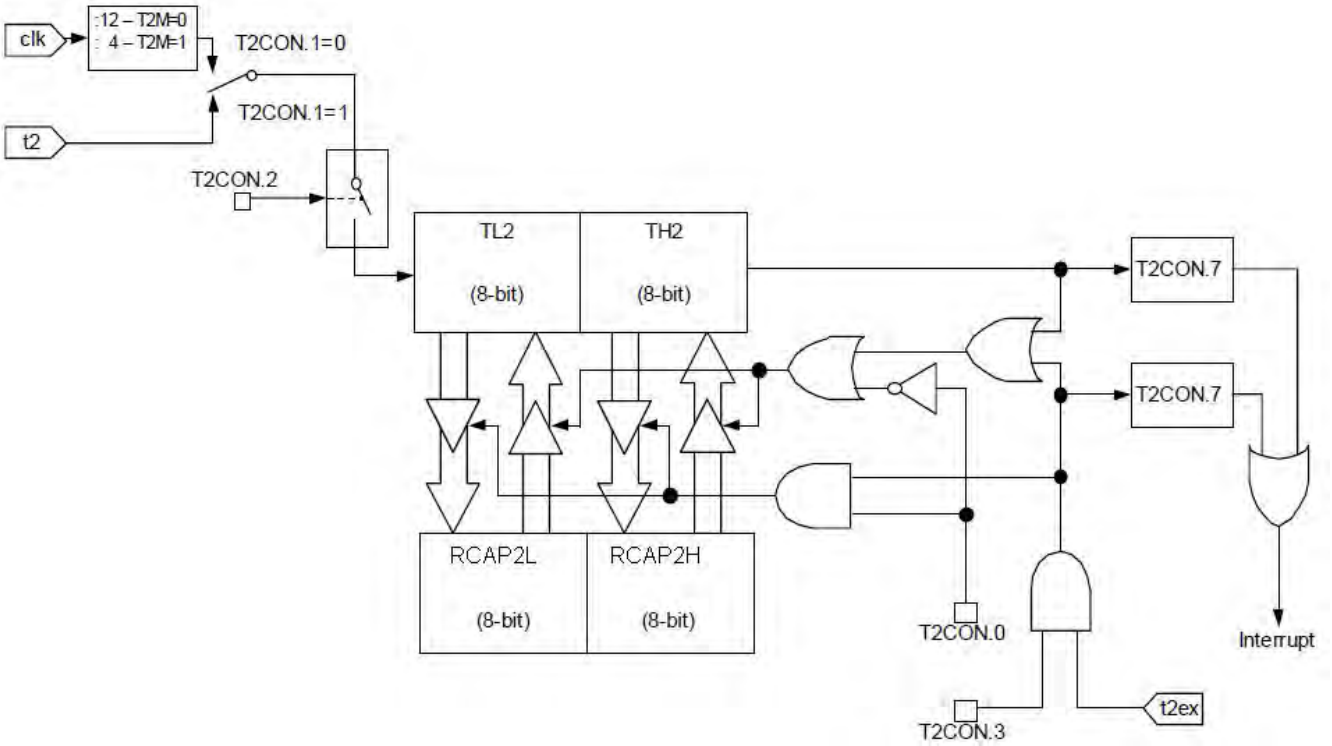


Figure12.8　Timer 2 block diagram in timer mode

CKCON register (0x8E)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8Eh CKCON Reset	R/W	WD1 0	WD0 0	T2M 0	T1M 0	T0M 0	MD2 0	MD1 0	MD0 0

T2M：This bit controls the division of the system clock that drives Timer 2. This bit has no effect when the timer is in baud rate generator mode.

=1, Timer 2 uses a divide-by-4 of the system clock frequency.

=0, Timer 2 uses a divide-by-12 of the system clock frequency.

Timer 2 interrupt related bits are shown below. An interrupt can be turned on/off by IE (0xA8) register, and set into high/low priority group by IP register.

IE register (0xA8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8h IE Reset	R/W	EA 0	- 0	ET2 0	ES 0	ET1 0	EX1 0	ET0 0	EX0 0

EA：Enable global interrupts.

ET2：Enable Timer 2 interrupts.

IP register (0xB8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B8h IP Reset	R/W	- 0	- 0	PT2 0	PS 0	PT1 0	PX1 0	PT0 0	PX0 0

PT2：Timer 2 priority level control (at 1-high level)

T2CON register (0xC8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C8h T2CON Reset	R/W	TF2 0	EXF2 0	RCLK 0	TCLK 0	EXEN2 0	TR2 0	CT2 0	CPRL2 0

TF2：Timer 2 interrupt (overflow) flag. It must be cleared by software.
The flag will not be set when either RCLK or TCLK is set.

All Timer 2 related bits generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software.

Interrupt flag	Function	Active level / edge	Flag resets	Vector	Natural priority
TF2	Internal, Timer2	-	Software	0x2B	6

Table12.6 Timer2 interrupt

Interrupt is also generated at falling edge of T2EX pin, while EXEN2 bit is set. This interrupt doesn't set TF2 flag, but EXF2 only and also uses 0x2B vector. Please see picture below. Timer2 internal logic configured as baud-rate generator is shwon below.

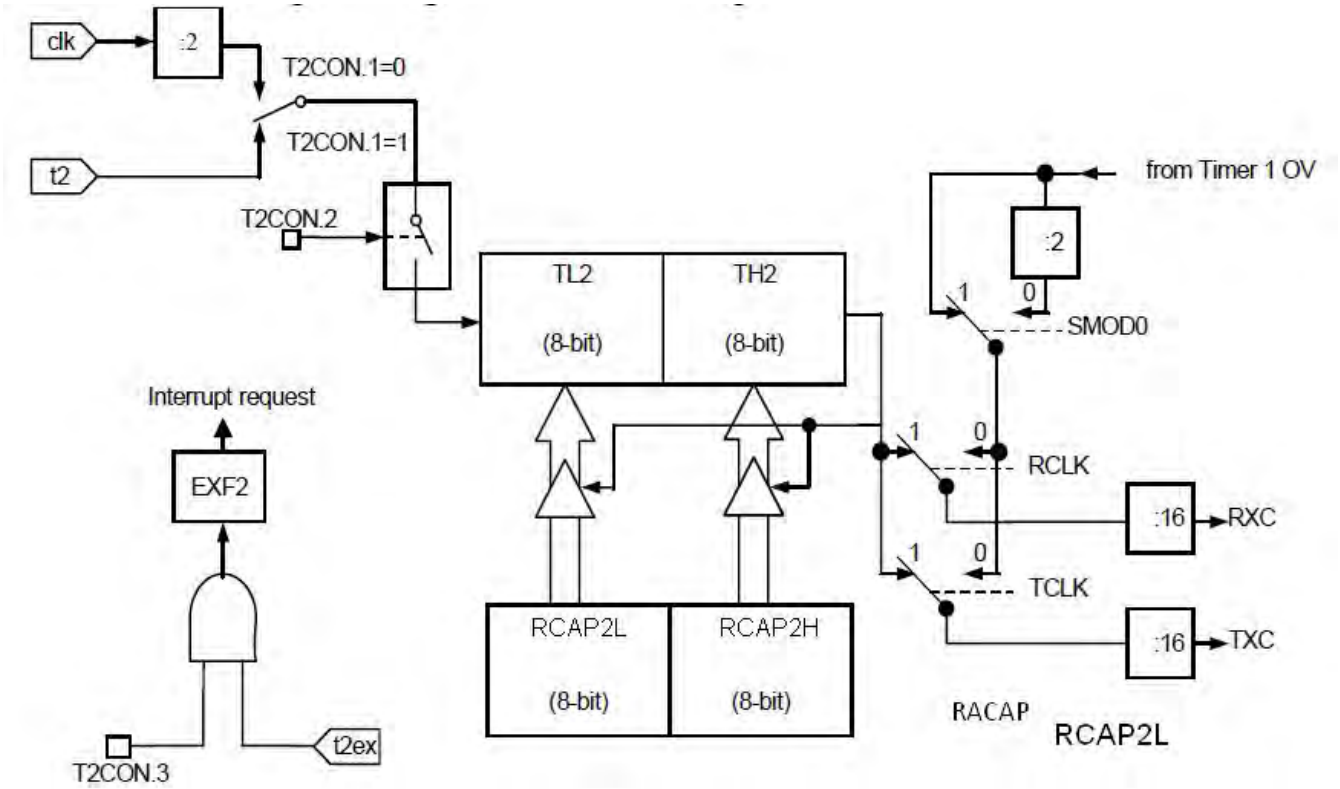


Figure12.9 Timer 2 block diagram as UART0 baud rate generator

Please note that SMODbit is ignored by UART when clocked by Timer2. The RLCK/TCLK frequency is equal to：

$$xCLK = \frac{CLK}{2 \cdot (65536 - RLD)}$$

$$where\ xCLK = TCLK, RCLK$$

13. UART

UART is full duplex, meaning it can transmit and receive concurrently. It is receive double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF loads the transmit register, and reading SBUF reads a physically separate receive register. The serial port can operate in 4 modes: one synchronous and three asynchronous modes. Mode 2 and 3 has a special feature for multiprocessor communications. This feature is enabled by setting SM2 bit in SCON register. The master processor first sends out an address byte, which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte will interrupt all slaves. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that were not being addressed leave their SM2 set and ignoring the incoming data.

13.1 UART PINS DESCRIPTION

The UART pins functionality is described in the following table. All pins are one directional. There are no three-state output pins and internal signals.

PIN	ACTIVE	TYPE	DESCRIPTION
Rxd_0(P3.0)	-	Input / Output	Serial receiver I_0 / O_0
Txd_0(P3.1)	-	Output	Serial transmitter line 0

Table13.1　UART pins description

13.2 FUNCTIONALITY

The UART has the same functionality as a standard 8051 UART. The UART related registers are: SBUF(0x99), SCON (0x98), PCON(0x87), IE(0xA8) and IP(0xB8). The UART data buffer (SBUF) consists of two separate registers: transmit and receive registers. A data writes into the SBUF sets this data in UART output register and starts a transmission. A data reads from SBUF, reads data from the UART receive register.

SBUF register　　(0x99)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
99h SBUF	R/W								
Reset		0	0	0	0	0	0	0	0

SBUF[7:0]：UART buffer

SCON register　　(0x98)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
98h SCON	R/W	SM00	SM01	SM02	REN	TB8	RB8	TI	RI
Reset		0	0	0	0	0	0	0	0

SM2：Enable a multiprocessor communication feature

SM [1:0]：Sets baud rate

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Shift register	$F_{CLK}/12$
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	$F_{CLK}/32$ or $F_{CLK}/64$
1	1	3	9-bit UART	Variable

Timer 2 cannot be used as baud rate generator when Compare Capture unit is present in the system. The UART baud rates are presented in the table below.

Mode　　Baud Rate

Mode 0　FCLK/12
Mode 1, 3　Timer 1 overflow rate – $T1_{ov}$
SMOD= 0　$T1_{ov}/32$
SMOD= 1　$T1_{ov}/16$
Timer 2 overflow rate – $T2_{ov}$
SMOD= x　$T2_{ov}/16$
Mode 2　SMOD= 0　$F_{CLK}/64$
SMOD= 1　$F_{CLK}/32$
The SMOD bit is located in PCON register.

REN：If set, enable serial reception. Cleared by software to disable reception.
TB8：The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the MCU, depending on the function it performs (parity check, multiprocessor communication etc.)
RB8：In Modes 2 and 3 it is the 9th data bit received. In Mode 1, if SM2 is 0, RB8 is the stop bit. In Mode 0 this bit is not used.

PCON register　(0x87)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
87h PCON	R/W	SMOD	-	-	PWE	-	SWB	STOP	CKSE
Reset		0	0	0	0	0	0	0	0

SMOD：UART double baud rate bit when clocked by Timer 1 only.

UART interrupt related bits are shown below. An interrupt can be turned on / off by IE register, and set into high / low priority group by IP register.

IE register　(0xA8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8h IE	R/W	EA	-	ET2	ES	ET1	EX1	ET0	EX0
Reset		0	0	0	0	0	0	0	0

ES：RI & TI interrupt enable flag

IP register　(0xB8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B8h IP	R/W	-	-	PT2	PS	PT1	PX1	PT0	PX0
Reset		0	0	0	0	0	0	0	0

PS：RI & TI interrupt priority flag

SCON register　(0x98)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
98h SCON	R/W	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Reset		0	0	0	0	0	0	0	0

TI：Transmit interrupt flag, set by hardware after completion of a serial transfer. It must be cleared by software.
RI：Receive interrupt flag, set by hardware after completion of a serial reception. It must be cleared by software.

All of bits that generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software.

Interrupt flag	Function	Active level / edge	Flag resets	Vector	Natural priority
TI & RI	Internal, UART	-	Software	0x23	5

Table13.3　UART interrupt

13.3 OPERATING MODES

13.3.1 UART MODE 0, SYNCHRONOUS

Pin RXD0I serves as input and RXD0O as output. TXD0 output is a shift clock. The baud rate is fixed at 1/12 of the CLK clock frequency. Eight bits are transmitted with LSB first. Reception is initialized by setting the flags in SCON as follows: RI=0 and REN=1.

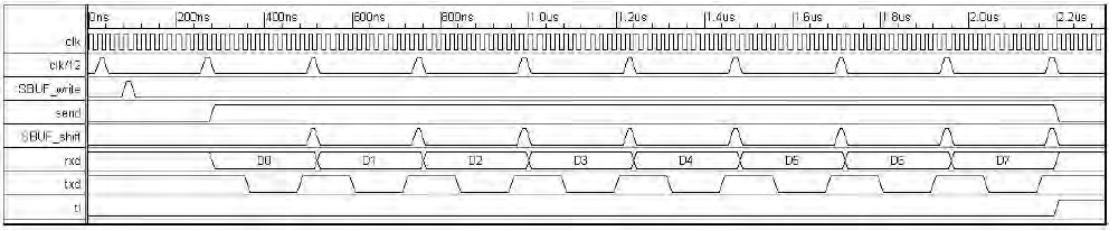


Figure13.3　UART transmission mode 0 timing diagram

13.3.2 UART MODE 1, 8-BIT UART, VARIABLE BAUD RATE, TIMER CLOCK SOURCE

Pin RXD0I serves as input, and TXD0 serves as serial output. 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading SBUF, and stop bit sets the flag RB8 in the SFR SCON. The baud rate is variable and depends from Timer 1 or Timer 2 mode. To enable Timer 2 clocking set the TCLK, RCLK bits located in T2CON (0xC8) register. SMOD bit is ignored when UART is clocked by Timer2.

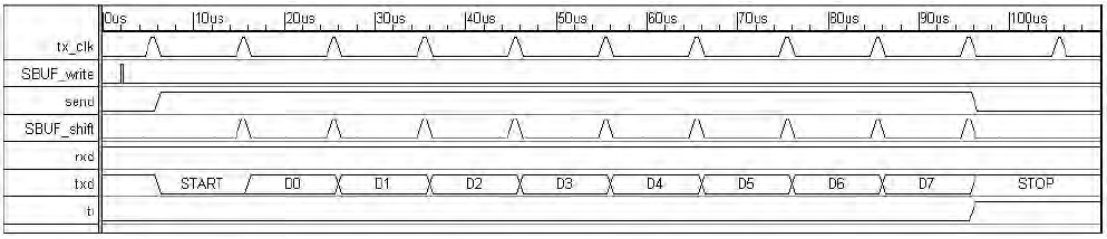


Figure13.4　UART transmission mode 1 timing diagram

13.3.3 UART MODE 2, 9-BIT UART, FIXED BAUD RATE

This mode is similar to Mode 1 with two differences. The baud rate is fixed at 1/32 or 1/64 of CLK clock frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the UART interface: at transmission, bit TB8 in SCON is output as the 9th bit, and at receive, the 9th bit affects RB8 in SCON.

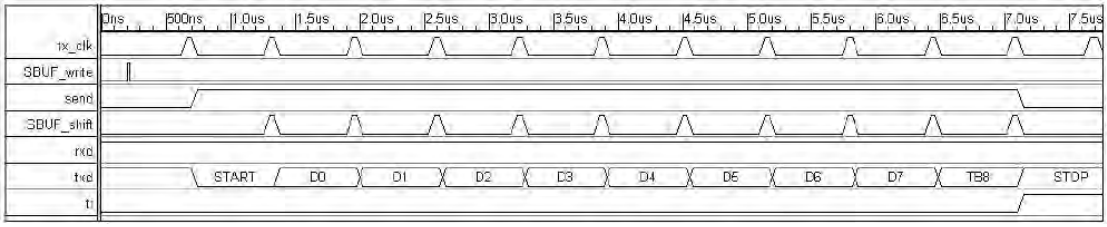


Figure13.5　UART transmission mode 2 timing diagram

13.3.4 UART MODE 3, 9-BIT UART, VARIABLE BAUD RATE, TIMER CLOCK SOURCE

The only difference between Mode 2 and Mode 3 is that the baud rate is a variable in Mode 3. When REN=1 data receiving is enabled. The baud rate is variable and depends from Timer 1 or Timer 2 mode. To enable Timer 2 clocking set the TCLK, RCLK bits located in T2CON (0xC8) register. SMOD bit is ignored when UART is clocked by Timer2.

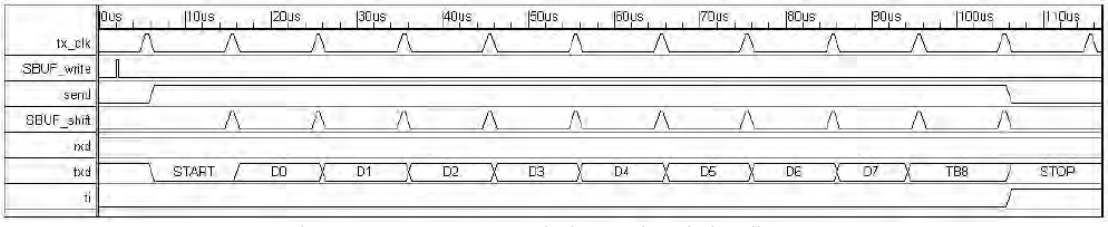


Figure13.6　UART transmission mode 3 timing diagram

14. IIC interface

A8125's I²C peripheral provides two-wire interface between the device and I²C -compatible device by the two-wire I²C serial bus. The I²C peripheral supports the following functions.

- Conforms to v2.1 of the I²C specification (published by Philips Semiconductor)
- Master transmitter / receiver
- Slave transmitter / receiver
- Flexible transmission speed modes: Standard (up to 100 Kb/s) and Fast (up to 400Kb/s)
- Multi-master systems supported
- Supports 7-bit addressing modes on the I²C bus
- Interrupt generation
- Allows operation from a wide range of input clock frequencies (build-in 8-bit timer)

P0.5 (PIN 23) and P0.6 (PIN 24) are I2C Interface in A8125. The alternate function is Port 0.5 and Port 0.6. User can set IOSEL (BBh) to set up the PIN function. Please refer the Chapter 11 for more detail information.

PIN	TYPE	DESCRIPTION
SCL(P0.5)	INPUT /OUTPUT	I²C clock input /output
SDA(P0.6)	INPUT/ OUTPUT	I²C data input /output

Table14.1 I2C interface pins description

14.1 Master mode I²C

The I²C master mode provides an interface between a microprocessor and an I²C bus. It can be programmed to operate with arbitration and clock synchronization to allow it to operate in multi-master systems. Master mode I²C supports transmission speeds up to 400Kb/s.

14.1.1 I²C REGISTERS

There are six registers used to interface to the host: the Control, Status, Slave Address, Transmitted Data, Received Data and Timer Period Register.

Register	Address
Slave address – I2CMSA	0xF4
Control – I2CMCR	0xF5
Transmitted data I2CBUF	0xF6
Timer period - I2CMTP	0xF7

Table14.3 I²C Registers for writing

Register	Address
Slave address – I2CMSA	0xF4
Status – I2CMSR	0xF5
Received data - I2CBUF	0xF6
Timer period - I2CMTP	0xF7

Table14.4 I²C Registers for reading

■ **I²C Master mode Timer Period Register**

To generate wide range of SCL frequencies the core have built-in 8-bit timer. Programming sequence must be done at least once after system reset. After reset, register have 0x01 value by default.

SCL_PERIOD = 2 x (1+TIMER_PRD) x (SCL_LP + SCL_HP) x CLK_PRD
For example： - CLK_PRD = 62.5ns (CLK_FRQ = 16MHz)； - TIMER_PRD =3； - SCL_LP = 6；(fixed) - SCL_HP = 4; (fixed)
SCL_PERIOD = 2 x (1 + 3) x (6 + 4) x 62.5ns = 5000ns = 5us
SCL_FREQUENCY = 1 / 5us = 200 KHz
SCL_PRD - SCL line period (I2C clock line)
TIMER PRD -Timer period register value (range 1 to 255)

CLK_PRD - System clock period ($1/f_{clk}$)

I2CMTP (0xE7)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E7h I2CMTP	R/W	0	P.6	P.5	P.4	P.3	P.2	P.1	P.0
Reset		0	0	0	0	0	0	0	1

■ I²C CONTROL AND STATUS REGISTERS

The Control Register consists of eight bits: the RUN, START, STOP, ACK, HS, ADDR, SLRST and RSTB bit. The RSTB bit performs reset of whole I²C controller and behaves identically as external reset provided by RST pin. Using this bit software application can reinitialize I²C mater module when some problem is encountered on I²C bus. In case when I²C Slave device blocks I²C bus, then SLRST bit should be set along with RUN bit (just after issuing the RSTB). SLRST bit causes that I²C master module generates 9 SCK clocks (no START is generated) to recover Slave device to known state and issues at the end STOP. This bit is automatically cleared by I2C MASTER MODULE, thus, it is always read as '0'. The BUSY bit should be checked to know when this transmission is ended.

The START bit will cause the generation of the START, or REPEATED START condition. The STOP bit determines if the cycle will stop at the end of the data cycle, or continue on to a burst. To generate a single send cycle, the Slave Address register is written with the desired address, the R/S bit is set to '0', and Control Register is written with HS=0, ACK=x, STOP=1, START=1, RUN=1 (binary xxx0x111 x-mean 0 or 1) to perform the operation and stop. When the operation is completed (or aborted due an error), the interrupt is generated. The data may be read from Received Data Register. When I2C MASTER MODULE core operates in Master receiver mode the ACK bit must be set normally to logic 1. This cause the I2C MASTER MODULE bus controller to send acknowledge automatically after each byte. This bit must be reset when the I2C MASTER MODULE bus controller requires no further data to be sent from slave transmitter.

The ADDR bit along with RUN bit cause the generation of the START condition and transmission of Slave Address. Next STOP can end transmission, or REPEATED START generates the START and ADDRRESS sequence once again. In both cases STOP can ends transmission. See I²C MASTER MODULE ACK Polling chapter for details.

I2CMCR (0xF5)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F5h I2CMCR	R/W	RSTB	SLRST	ADDR	HS	ACK	STOP	START	RUN
Reset		0	0	0	0	0	0	0	0

RSTB	SLRST	ADDR	HS	R/S	ACK	STOP	START	RUN	OPERATION
0	0	0	0	0	-	0	1	1	START condition followed by SEND (Master remains in Transmitter mode)
0	0	0	0	0	-	1	1	1	START condition followed by SEND and STOP condition
0	0	0	0	1	0	0	1	1	START condition followed by RECEIVE operation with **negative Acknowledge** (Master remains in Receiver mode)
0	0	0	0	1	0	1	1	1	START condition followed by RECEIVE and STOP condition
0	0	0	0	1	1	0	1	1	START condition followed by RECEIVE (Master remains in Receiver mode)
0	0	0	0	1	1	1	1	1	**forbidden sequence**
0	0	0	1	0	0	0	0	1	Master Code sending and switching to High-speed mode
1	0	0	-	-	-	-	-	-	I2CM module software reset
0	1	0	0	0	0	0	0	1	Reset slaves connected to I2C bus by generating 9 SCK clocks followed by STOP
0	0	1	0	0	0	0	0	1	START condition followed by Slave Address

Table14.5 Control bits combinations permitted in IDLE state *

RSTB	SLRST	ADDR	HS	R/S	ACK	STOP	START	RUN	OPERATION

0	0	0	0	-	-	0	0	1	SEND operation (Master remains in Transmitter mode)
0	0	0	0	-	-	1	0	0	STOP condition
0	0	0	0	-	-	1	0	1	SEND followed by STOP condition
0	0	0	0	0	-	0	1	1	Repeated START condition followed by SEND (Master remains in Transmitter mode)
0	0	0	0	0	-	1	1	1	Repeated START condition followed by SEND and STOP condition
0	0	0	0	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with **negative Acknowledge** (Master remains in Receiver mode)
0	0	0	0	1	0	1	1	1	Repeated START condition followed by SEND and STOP condition
0	0	0	0	1	1	0	1	1	Repeated START condition followed by RECEIVE (Master remains in Receiver mode)
0	0	0	0	1	1	1	1	1	**forbidden sequence**
1	0	0	-	-	-	-	-	-	I2CM module software reset
0	0	1	0	0	-	0	1	1	Repeated START condition followed by Slave Address

Table14.6 Control bits combinations permitted in Master Transmitter mode

RSTB	SLRST	ADDR	HS	R/S	ACK	STOP	START	RUN	OPERATION
0	0	0	0	-	0	0	0	1	RECEIVE operation with **negative Acknowledge** (Master remains in Receiver mode)
0	0	0	0	-	-	1	0	0	STOP condition**
0	0	0	0	-	0	1	0	1	RECEIVE followed by STOP condition
0	0	0	0	-	1	0	0	1	RECEIVE operation (Master remains in Receiver mode)
0	0	0	0	-	1	1	0	1	**forbidden sequence**
0	0	0	0	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with **negative Acknowledge** (Master remains in Receiver mode)
0	0	0	0	1	0	1	1	1	Repeated START condition followed by RECEIVE and STOP condition
0	0	0	0	1	1	0	1	1	Repeated START condition followed by RECEIVE (Master remains in Receiver mode)
0	0	0	0	0	-	0	1	1	Repeated START condition followed by SEND (Master remains in Transmitter mode)
0	0	0	0	0	-	1	1	1	Repeated START condition followed by SEND and STOP condition
1	0	0	-	-	-	-	-	-	I2CM module software reset

Table14.7 Control bits combinations permitted in Master Receiver mode

The status Register is consisted of six bits：the BUSY bit, the ERROR bit, the ADDR_ACK bit, the DATA_ACK bit, the ARB_LOST bit, and the IDLE bit.

I2CMSR (0xF5)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F5h I2CMSR	R/W	-	BUS_ BUSY	IDLE	ARB_ LOST	DATA_ ACK	ADDR_ ACK	ERROR	BUSY
Reset	0x20	0	0	1	0	0	0	0	0

IDLE：This bit indicates that I2C BUS controller is in the IDLE state。

BUSY：This bit indicates that I2C BUS controller receiving, or transmitting data on the bus, and other bits of Status register are no valid;

BUS_BUSY：This bit indicates that the Bus is Busy, and access is not possible. This bit is set / reset by START and STOP conditions;
ERROR：This bit indicates that due the last operation an error occurred: slave address wasn't acknowledged, transmitted data wasn't acknowledged, or I2C Bus controller lost the arbitration;
ADDR_ACK：This bit indicates that due the last operation slave address wasn't acknowledged;
ARB_LOST：This bit indicates that due the last operation I2C Bus controller lost the arbitration;

■ **SLAVE ADDRESS REGISTER**

The Slave address Register consists of eight bits：Seven address bits (A6-A0), and Receive/ not send bit R/S. The R/S bit determines if the next operation will be a Receive (high), or Send (low).

I2CMSA (0xF4)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F4h I2CMCA	R/W	A.6	A.5	A.4	A.3	A.2	A.1	A.0	R/S
Reset		0	0	0	0	0	0	0	0

■ **I²C Buffer – RECEIVER AND TRANSMITTER REGISTERS**

I2C module has two separated 1 byte buffer in receiver and transmitter and these are located in the same address (0xF6). The Transmitted Data Register consists of eight data bits which will be sent on the bus due the next Send, or Burst Send operation. The first send bit is D.7 (MSB).

I2CBUF (0xF6)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F6h I2CBUF	R/W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
Reset		0	0	0	0	0	0	0	0

The Receiver Data Register consists of eight data bits which have been received on the bus due the last receive, or Burst Receive operation.

I2CBUF (0xF6)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F6h I2CBUF	R/W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
Reset		0	0	0	0	0	0	0	0

14.2.4 I2C MASTER MODULE AVAILABLE SPEED MODES

Default transmission parameter/constant values are shown in sections below. SCL clock frequency can be changed by modification of timer period values as show in the table below.

■ **I2C MASTER MODULE STANDARD MODE**

Typical configuration values for Standard speed mode：

The following table gives an example parameters for standard I2C speed mode.

System clock	TIMER_PERIOD	Transmission speed
4 MHz	1 (01h)	100kb/s
6 MHz	2 (02h)	100kb/s
10 MHz	4 (04h)	100kb/s
16 MHz	7 (07h)	100kb/s
20 MHz	9 (09h)	100kb/s

Table14.8 I2C MASTER MODULE Timer period values for standard speed mode

■ **I2C MASTER MODULE FAST MODE**

Typical configuration values for Fast speed mode：

The following table gives example parameters for Fast I2C speed mode.

System clock	TIMER_PERIOD	Transmission speed
10 MHz	1 (01h)	250 Kb/s
16 MHz	1 (01h)	400 Kb/s
20 MHz	2 (02h)	333 Kb/s

Table14.8　I2C MASTER MODULE Timer period values for Fast speed mode

14.2.5 I2C MASTER MODULE AVAILABLE COMMAND SEQUENCES

- **I2C MASTER MODULE SINGLE SEND**

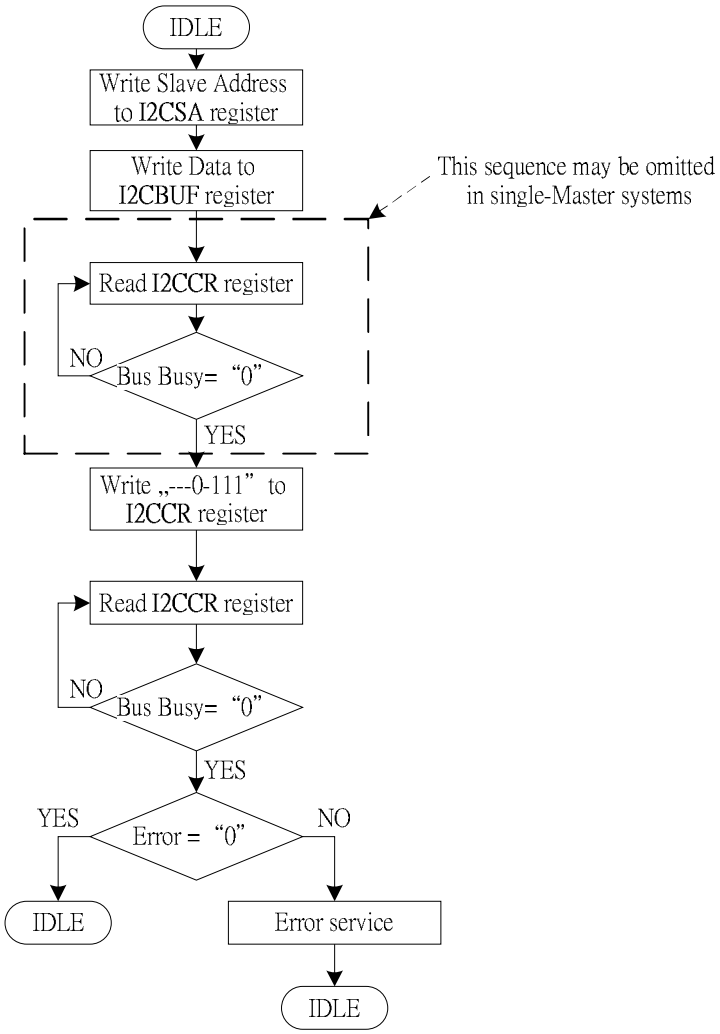


Figure14.4　I2C MASTER MODULE Single SEND flowchart

■ **I2C MASTER MODULE SINGLE RECEIVE**

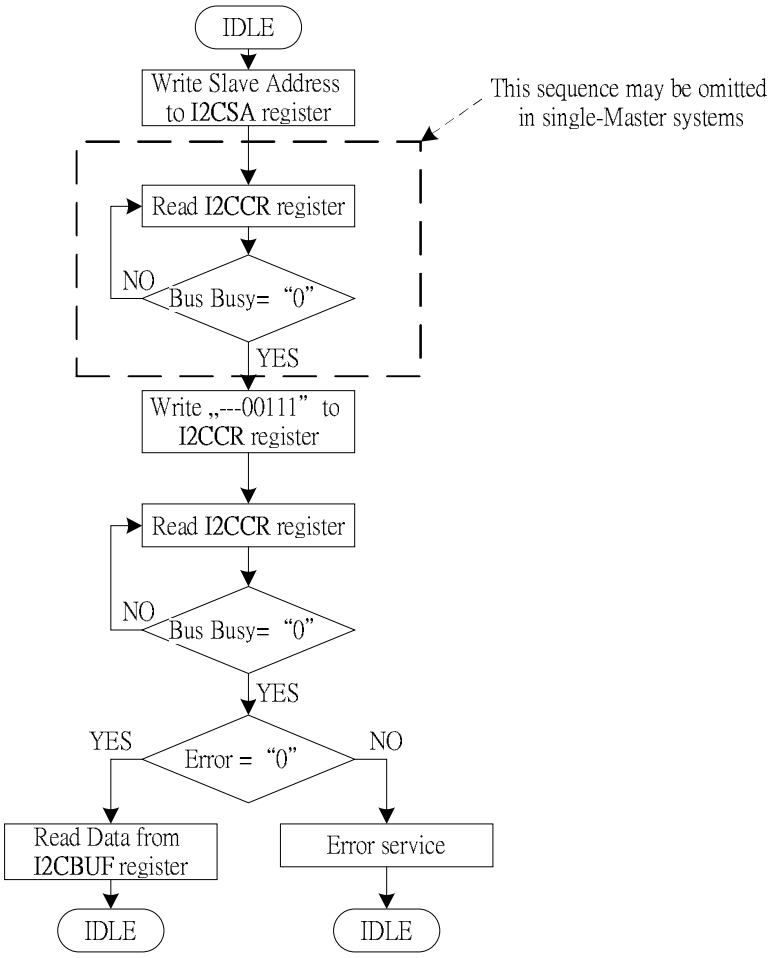


Figure14.5　Single RECEIVE flowchart

■ I2C MASTER MODULE BURST SEND

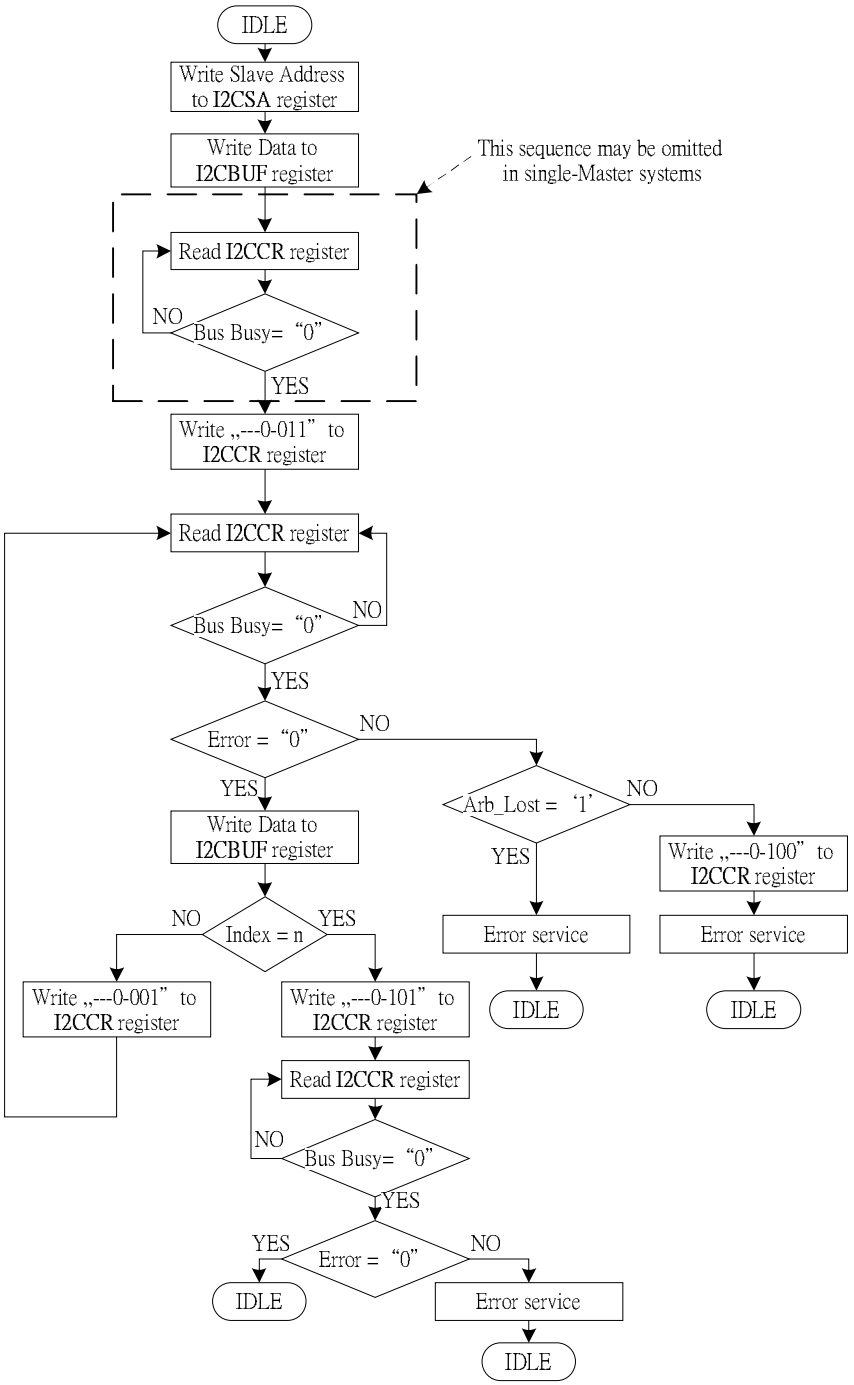


Figure14.6　I2C MASTER MODULE Sending n bytes flowchart

■ **I2C MASTER MODULE BURST RECEIVE**

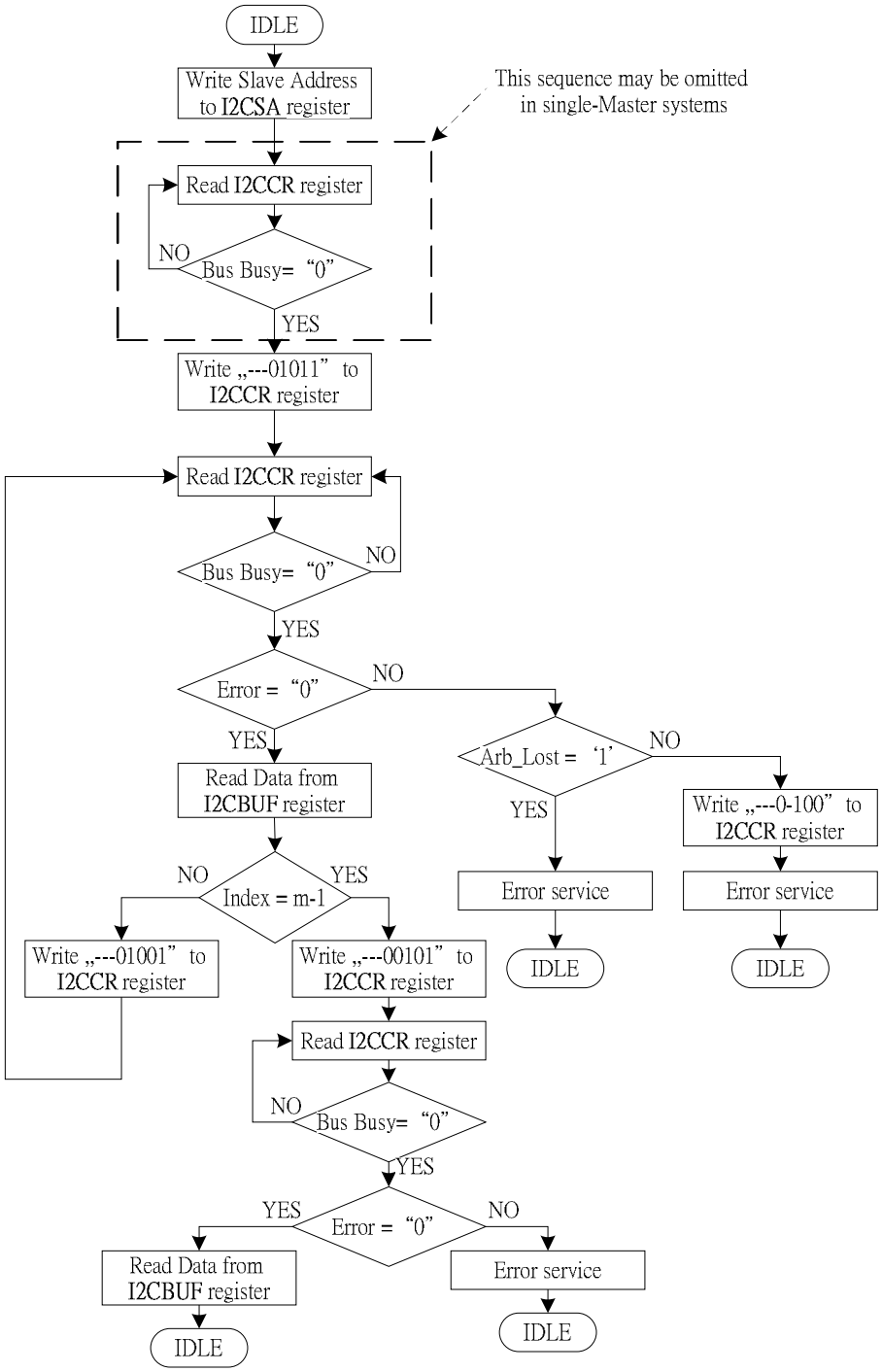


Figure14.7　I2C MASTER MODULE Receiving m bytes flowchart

■ I2C MASTER MODULE BURST RECEIVE AFTER BURST SEND

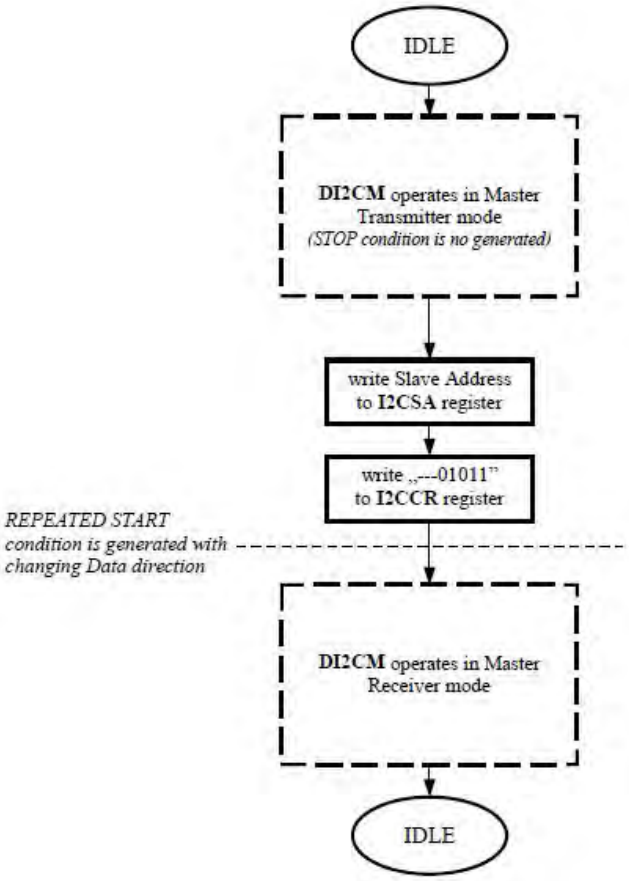


Figure14.8　I2C MASTER MODULE Sending n bytes then Repeated Start and Receiving m bytes flowchart

■ I2C MASTER MODULE BURST SEND AFTER BURST RECEIVE

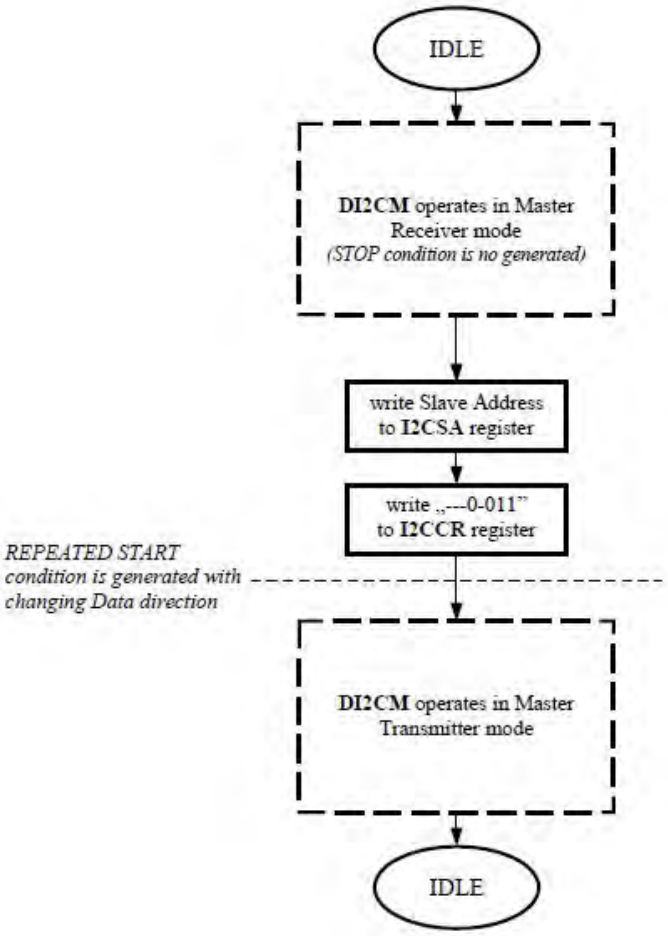


Figure14.9　I2C MASTER MODULE Receiving m bytes then Repeated Start and Sending n bytes flowchart

Figure14.10　I2C MASTER MODULE Single RECEIVE with 10-bit addressing flowchart

■ I2C MASTER MODULE ACK POLLING

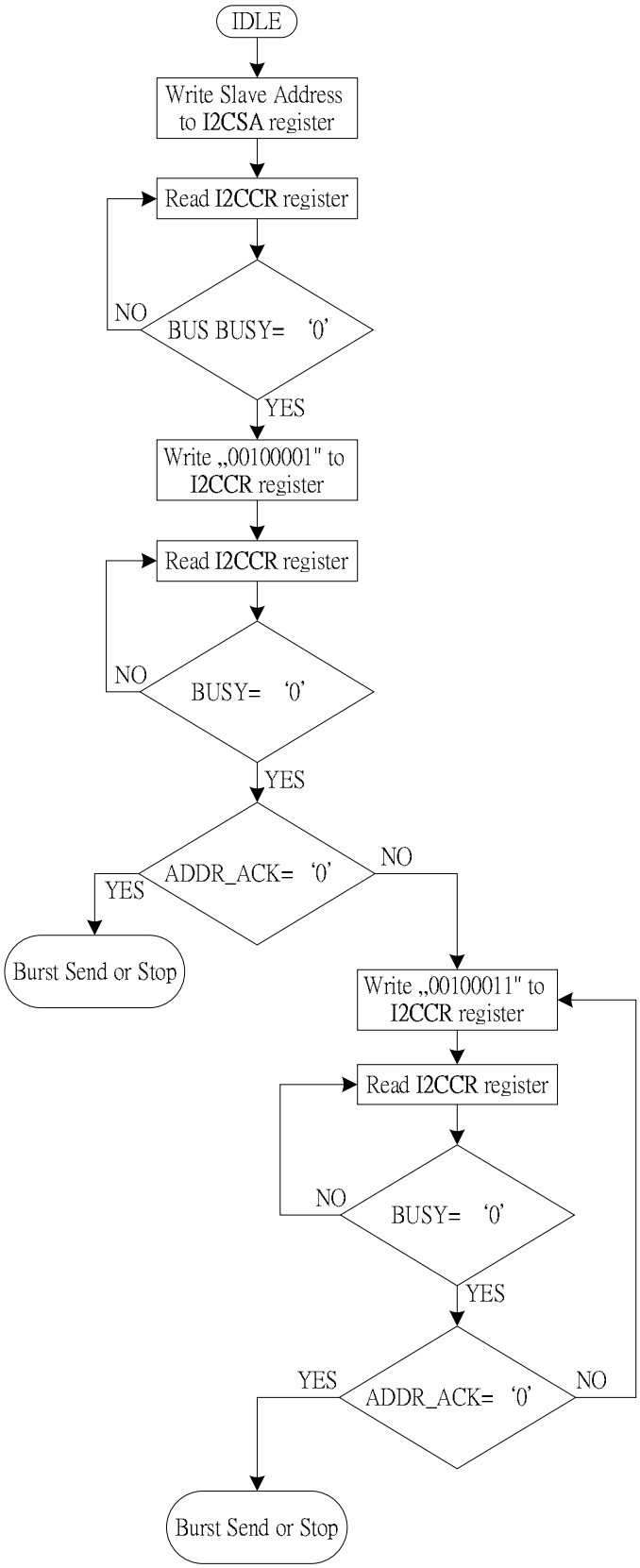


Figure14.11 I2C MASTER MODULE ACK Polling flowchart

14.3 I2C MASTER MODULE INTERRUPT GENERATION

I2C MASTER MODULE interrupt flag is automatically asserted when I2C transfer (send or receive a byte) is completed or transfer error has occurred. I2CMIF flag has to be cleared by software.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Natural priority
I2CMIF	Internal, I2C MASTER MODULE	-	Software	0x6B	14

Table14.11 I2C MASTER MODULE interrupt summary

I2C MASTER MODULE related interrupt bits have been summarized below. The IE (0xA8) contains global interrupt system disable (0) / enable (1) bit called EA.

EIE (0xE8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8h EIE Reset	R/W	EI2CSESPI 0	EI2CM 0	EWDI 0	EKEYINT 0	ERFINT 0	EINT4 0	EINT3 0	EINT2 0

EI2CM：Enable I2C MASTER MODULE interrupts

EIP (0xF8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F8h EIP Reset	R/W	PI2CSPSPI 0	PI2CM 0	PWDI 0	PKEYINT 0	PRFINT 0	PINT4 0	PINT3 0	PINT2 0

PI2CM：I2C MASTER MODULE priority level control (at 1-high-level)

EIF (0x91)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
91h EIF Reset	R/W	I2CSFSPIF 0	I2CMF 0	- 0	KEYINTF 0	RFINTF 0	INT4F 0	INT3F 0	INT2F 0

I2CMIF：I2C MASTER MODULE interrupt flag

It must be cleared by software writing logic '1'. Writing '0' does not change its content.

14.5 Slave mode I^2C

The I^2C module provides an interface between a microprocessor and I^2C bus. It can works as a slave receiver or transmitter depending on working mode determined by microprocessor/microcontroller. The core incorporates all features required by I^2C specification. The I^2C module supports all the transmission modes: Standard and Fast.

14.5.1 I2C MODULE INTERNAL REGISTERS

There are five registers used to interface to the target device：The Own Address, Control, Status, Transmitted Data and Received Data registers.

Register	Address
Own address – I2CSOA	0xF1
Control – I2CSCR	0xF2
Transmitted data – I2CSBUF	0xF3

Table14.12 I2C MODULE Registers for writing

Register	Address
Own address – I2CSOA	0xF1

Control – I2CSSR	0xF2
Received data – I2CSBUF	0xF3

Table14.13 I2C MODULE Registers for reading

■ **I2CSOA – OWN ADDRESS REGISTER**

The Own Address Register consists of seven address bits which identify I^2C module core on I^2C Bus. This register can be read and written at the address 0xF1.

I2CSOA (0xF1)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F1h I2CSOA	R/W	-	A.6	A.5	A.4	A.3	A.2	A.1	A0
Reset		0	0	0	0	0	0	0	0

■ **I2CSCR – CONTROL AND STATUS REGISTERS**

The Control Register consists of the bits：The RSTB and DA bit. The RSTB bit performs reset of whole I^2C controller and behaves identically as external reset provided by RST pin. Using this bit software application can reinitialize I^2C module when some problem is encountered on I^2C bus. The DA bit enables (‘1’) and disable (‘0’) the I^2C module device operation. DA is set immediately to ‘1’ when MCU write DA=1. This register can be only written at address 0xF2. Reading this address puts status register on data bus – see below.

I2CSCR (0xF2)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F2h I2CSCR	R/W	RSTB	DA	-	-	RECFINCLR	SENDFINCLR	-	-
Reset		0	0	0	0	0	0	0	0

DA：Device Active – enable or disable the I^2C module device operation;
RSTB：Reset of whole I^2C controller by writing ‘1’ to this bit. It behaves identically as RST pin
RECFINCLR：Writing ‘1’ to this bit clears RECFIN bit from the I2C MODULE status register.
SENDFINCLR：Writing ‘1’ to this bit clears SENDFIN bit from the I2C MODULE status register.

The Status Register consists of five bits: the DA, BUSACTIVE, RECFIN, SENDFIN bit, RREQ bit, TREQ bit. The receive finished RECFIN bit indicates that Master I2C controller has finished transmitting of data during single or burst receive operations. It also causes generation of interrupt on IRQ pin. The send finished SENDFIN bit indicates that Master I2C controller has finished receiving of data during single or burst send operations. It also causes generation of interrupt on IRQ pin. The Receive Request RREQ bit indicates that I^2C module device has received data byte from I2C master. I^2C module host device (usually MCU) should read one data byte from the Received Data register I2CSBUF. The Transmit Request TREQ bit indicates that I2C MODULE device is addressed as Slave Transmitter and I^2C module host device (usually MCU) should write one data byte into the Transmitted Data register I2CSBUF. The BUSACTIVE ‘1’ signalizes that any transmission (send, receive or own address detection) is in progress. BUSACTIVE is cleared (‘0’) automatically by I^2C module in case when there is no any transmission. This is read only bit.

The DA bit should be polled (read) when MCU wrote DA=0. The DA bit is not immediately cleared when any I2C transmission (send, receive or own address detection) is in progress. When current transmission has completed then this bit is cleared to ‘0’ and I^2C module become inactive.

I2CSSR (0xF2)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F2h I2CSSR	R/W		DA	-	BUSACTIVE	RECFIN	SENDFIN	TREQ	RREQ
Reset		0	0	0	0	0	0	0	0

DA：Device Active – enable (‘1’) or disable (‘0’) the I2C MODULE device operation;
BUSACTIVE：Bus ACTIVE – ‘1’ signalizes that any transmission: send, receive or own address detection is in progress;
RREQ：Indicates that I^2C module device has received data byte from I^2C master;
It is automatically cleared by read of I2CSBUF.
TREQ：Indicates that I^2C module device is addressed as transmitter and requires data byte from host device;
It is automatically cleared by write data I2CSBUF.

RECFIN：Indicates that Master I2C controller has ended transmit operation. It means that no more RREQ will be set during this single or burst I²C module receive operation. It is cleared by writing '1' to the RECFINCLR bit in the I²C module control register.

SENDFIN：Indicates that Master I2C controller has ended receive operation. It means that no more TREQ will be set during this single or burst I²C module send operation. It is cleared by writing '1' to the SENDFINCLR bit in the I2C control register.

NOTE：All bits are active at HIGH level ('1').

■ **I2CSBUF – RECEIVER AND TRANSMITTER REGISTERS**

The Transmitter Data Register consists of eight Data bits which will be sent on the bus due the next Send operation. The first send bit is the D.7(MSB).

I2CSBUF (0xF3)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F3h I2CSBUF Reset	R/W	D.7 0	D.6 0	D.5 0	D.4 0	D.3 0	D.2 0	D.1 0	D.0 0

The Receiver Data Register consists of eight data bits which have been received on the bus due the last Receive operation.

I2CSBUF (0xF3)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F3h I2CSBUF Reset	R/W	D.7 0	D.6 0	D.5 0	D.4 0	D.3 0	D.2 0	D.1 0	D.0 0

14.7 AVAILABLE I2C MODULE TRANSMISSION MODES

This chapter describes all available transmission modes of the I²C module core. Default I2C own address for all presented waveforms is 0x39 ("0111001").

14.7.1 I²C module SINGLE RECEIVE

The figure below shows a set of sequences during Single data Receive by I2C MODULE. Single receive sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I2C Master as receiver
- ✧ Address is acknowledged by I²C module
- ✧ Data is received by I²C module
- ✧ Data is acknowledged by I²C module
- ✧ Stop condition

14.7.2 I²C module SINGLE SEND

The figure below shows a set of sequences during Single data Send by I2C MODULE. Single send sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I2C Master as transmitter
- ✧ Address is acknowledged by I²C module
- ✧ Data is transmitted by I²C module
- ✧ Data is not acknowledged by I2C Master
- ✧ Stop condition

14.7.3 I²C module BURST RECEIVE

The figure below shows a set of sequences during Burst data Receive by I²C module. Burst receive sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I2C Master as receiver
- ✧ Address is acknowledged by I²C module
- ✧ (1)Data is received by I²C module
- ✧ (2)Data is acknowledged by I²C module
- ✧ STOP condition

Sequences (1) and (2) are repeated until Stop condition occurs.

14.7.4 I²C module BURST SEND

The figure below shows a set of sequences during Burst Data Send by I²C module. Burst send sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I2C Master as transmitter
- ✧ Address is acknowledged by I²C module
- ✧ (1)Data is transmitted by I²C module
- ✧ (2)Data is acknowledged by I2C Master
- ✧ (3)Last data is not acknowledged by I2C Master
- ✧ Stop condition

Sequences (1) and (2) are repeated until last transmitted data is not acknowledged (3) by I2C Master.

14.7.5 AVAILABLE I²C module COMMAND SEQUENCES FLOWCHART

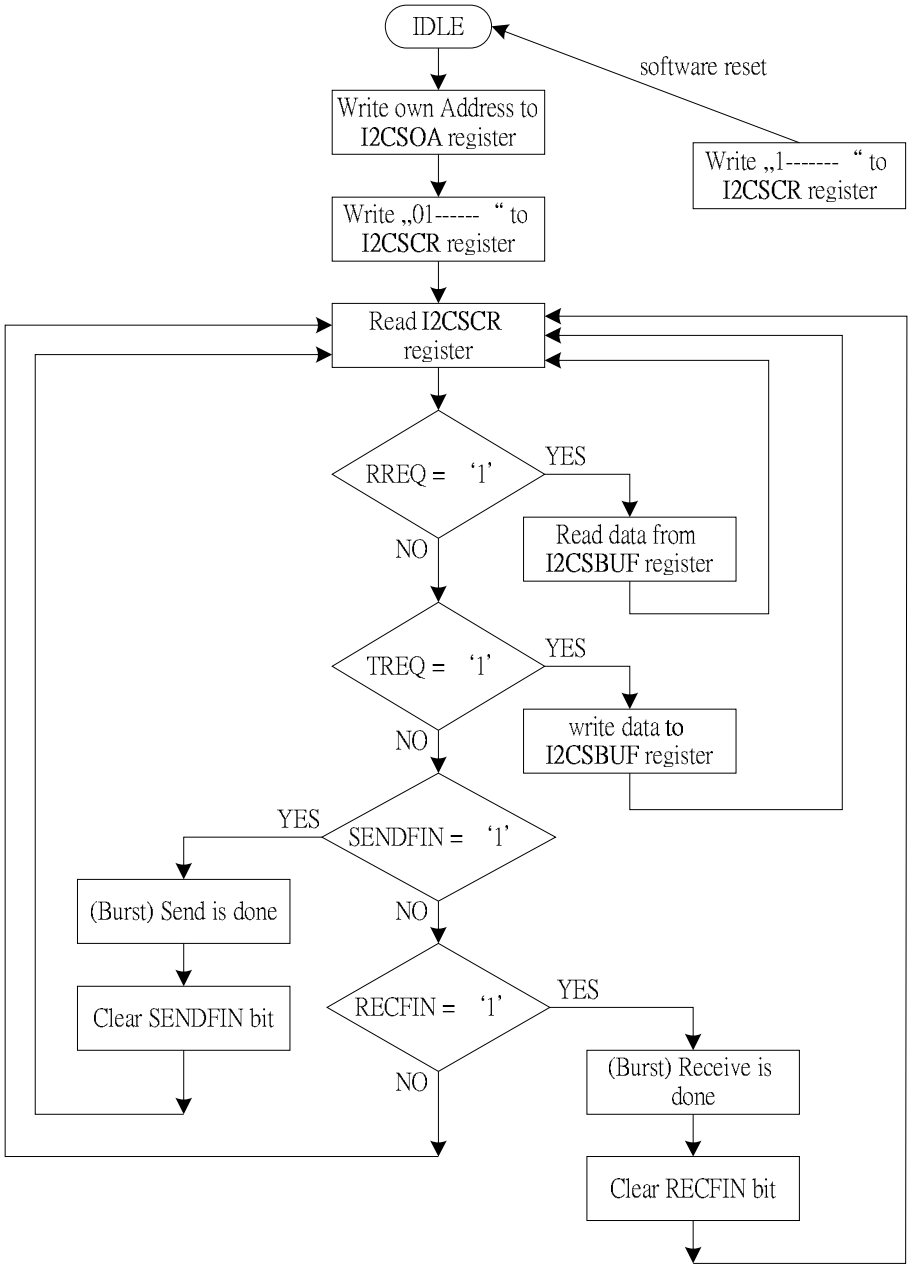


Figure14.20 Available I2C MODULE command sequences flowchart

14.8 I2C MODULE INTERRUPT GENERATION

I2C MODULE interrupt flag is automatically asserted when I2C transfer (send or receive a byte) is completed or transfer error has occurred. I2CSIF flag has to be cleared by software.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Natural priority
I2CSIF	Internal, DI2CS	-	Software	0x73	15

Table14.16 I2C MODULE interrupt summary

I2C MODULE related interrupt bits have been summarized below. The IE (0xA8) contains global interrupt system disable (0) / enable (1) bit called EA.

EIE (0xE8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8h EIE	R/W	EI2CS ESPI	EI2CM	EWDI	EKEYINT	ERFINT	EINT4	EINT3	EINT2
Reset		0	0	0	0	0	0	0	0

EI2CS：Enable I2C MODULE interrupts

EIP (0xF8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F8h EIP	R/W	PI2CS PSPI	PI2CM	PWDI	PKEYINT	PRFINT	PINT4	PINT3	PINT2
Reset		0	0	0	0	0	0	0	0

PI2CS：I2C MODULE priority level control (at 1-high-level)

EIF (0x91)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
91h EIF	R/W	I2CSF SPIF	I2CMF	-	KEYINTF	RFINTF	INT4F	INT3F	INT2F
Reset		0	0	0	0	0	0	0	0

I2CSIF：I2C MODULE interrupt flag

Software should determine the source of interrupt by check both modules' interrupt related bits. It must be cleared by software writing 0x80. It cannot be set by software.

15. SPI interface

The SPI is a fully configurable SPI master/slave device, which allows user to configure polarity and phase of serial clock signal SCK.

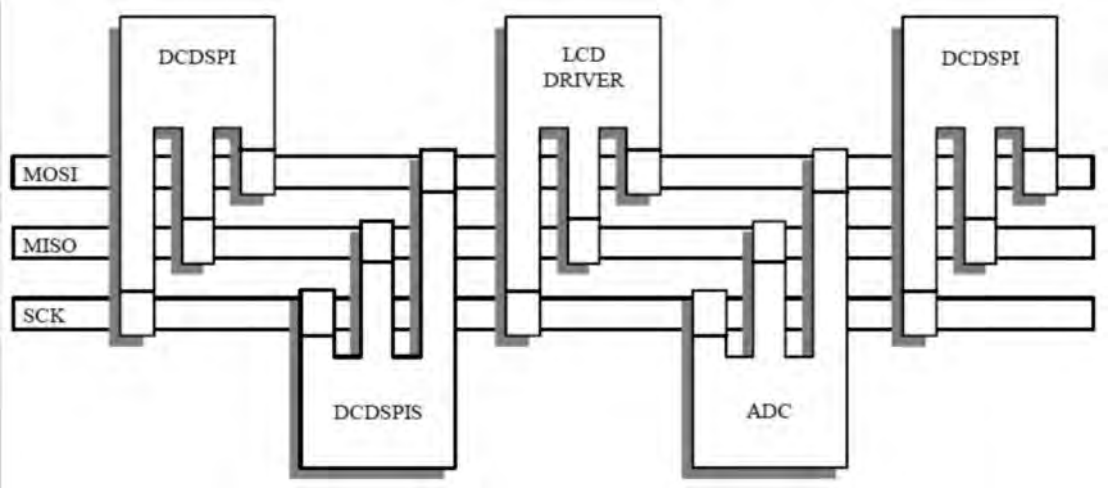
The SPI allows the microcontroller to communicate with serial peripheral devices. It is also capable of inter-processor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received.

The SPI is a technology independent design that can be implemented in a variety of process technologies.

The SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. The system can be configured as a master or a slave device. Data rates as high as System clock divided by four (CLK/4). Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock.

The SPI automatically drive selected by SSCR (Slave Select Control Register) slave select outputs (SS7O – SS0O), and address SPI slave device to exchange serially shifted data.

Error-detection logic is included to support inter-processor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to be become bus master.



15.1 KEY FEATURES

All features listed below are included in the current version of SPI core.

- SPI Master
  - Full duplex synchronous serial data transfer
  - Master operation
  - Multi-master system supported
  - Up to 8 SPI slaves can be addressed
  - System error detection
  - Interrupt generation
  - Supports speeds up to 1/4 up to CLK
  - Bit rates generated 1/4, 1/8, 1/32, 1/64, 1/128, 1/512 of CLK
  - Four transfer formats supported
  - Simple interface allows easy connection to microcontrollers
- SPI Slave
  - Full duplex synchronous serial data transfer
  - Slave operation
  - System error detection
  - Interrupt generation
  - Supports speeds up to 1/4 of system clock
  - Simple interface allows easy connection to microcontrollers

- Four transfer formats supported
- Fully synthesizable, static synchronous design with no internal tri-states

15.2 SPI PINS DESCRIPTION

PIN	TYPE	ACTIVE	DESCRIPTION
Scki_Scko (P0.0)	INPUT / OUTPUT	-	SPI clock input / output
MOSI (P0.1)	INPUT / OUTPUT	-	Master serial data input / Slave serial data output
MISO (P0.2)	INPUT / OUTPUT	-	Slave serial data input / Master serial data output
SSO (P0.3)	OUTPUT	low	Slave select output

Table15.1　SPI pins description

15.3 SPI HARDWARE DESCRIPTION

15.3.1 BLOCK DIAGRAM

When an SPI transfer occurs, an 8-bit character is shifted out on data pin while a different 8-bit character is simultaneously shifted in a second data pin. Another way to view this transfer is that an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in the master and slave are effectively exchanged.

The central element in the SPI system is the block containing the shift register and the read data buffer. The system is single buffered in the transmit direction and double buffered in the receive direction. This fact means new data for transmission cannot be written to the shifter until the previous transaction is complete; however, received data is transferred into a parallel read data buffer so the shifter is free to accept a second serial character. As long as the first character is read out of the read data buffer before the next serial character is ready to be transferred, no overrun condition will occur.

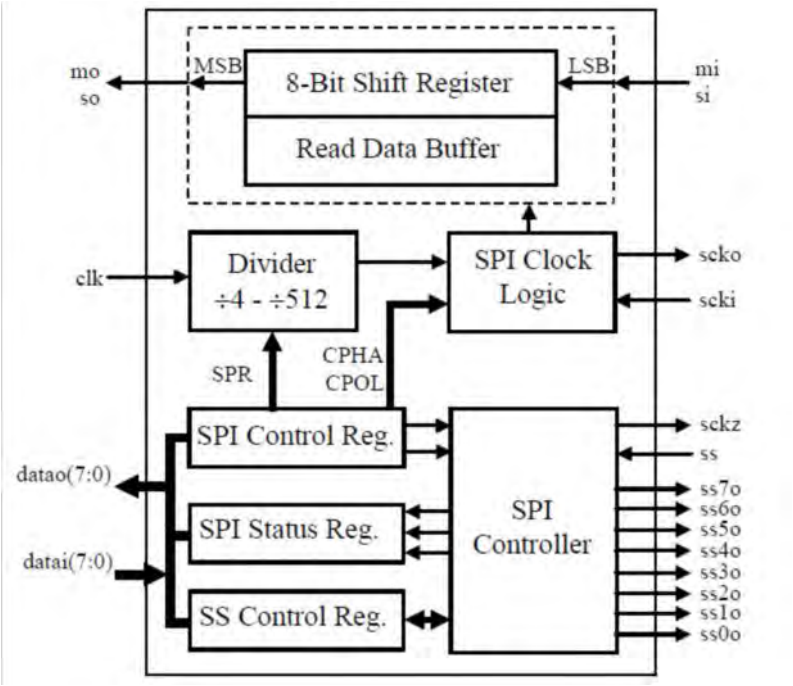


Figure 15.2　SPI Block Diagram

The eight pins are associated with the SPI: the SS, clock pins SCKI, SCKO and SCKEN, master pins MI and MO and slave pins SOEN, SI and SO.

The SS input pin in a master mode is used to detect mode-fault errors. A low on this pin indicates that some other device in a multi-master system has become a master and trying to select the SPI MODULE as a slave. The SS input pin in a slave mode is used to enable transfer.

The SCKI pin is used when the SPI is configured as a slave. The input clock from a master synchronizes data transfer between a master and the slave devices. The slave device ignore the SCKI signal unless the SS (slave select) pin is active low.

The SCKO and SCKEN pins are used as the SPI clock signal reference in a master mode. When the master initiates a transfer eight clock cycles is automatically generated on the SCKO pin.

When the SPI is configured as a slave the SI pin is the slave input data line, and the SO is the slave output data line.

When the SPI is configured as a master, the MI pin is the master input data line, and the MO is the master output data line.

15.3.2 INTERNAL REGISTERS

- **SPI Control Register**

The control register may be read or written at any time, is used to configure the SPI System.

SPCR (0xEC)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECh EIE	R/W	SPIE	SPE	SPR2	MSTR	CPOL	CPHA	SPR1	SPR0
Reset		0	0	0	0	0	1	0	0

SPIE：SPI interrupt enable

= 0, interrupts are disabled, polling mode is used

= 1, interrupts are enabled

SPE：SPI system enable

= 0, system is off

= 1, system is on

MSTR：Master/Slave mode select

= 0, slave

= 1, master

CPOL：Clock polarity select

= 0, high level; SCK idle low

= 1, low level; SCK idle high

CPHA：Clock phase.. Select one of two different transfer formats

SPR[2:0]：SPI clock rate select bits. See the table below

SPR2	SPR1	SPR0	System clock divided by
0	0	0	4
0	0	1	8
0	1	0	16
0	1	1	32
1	0	0	64
1	0	1	128
1	1	0	256
1	1	1	512

- **Slave Select Control Register**

The control register may be read or written at any time. It is used to configure which slave select output should be driven while SPI master transfer. Contents of SSCR register is automatically assigned on SS7O-SS0O pins when SPI master transmission starts.

SSCR (0xEF)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EFh SSCR	R/W	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0
Reset		1	1	1	1	1	1	1	1

SS7 – SS0

= 0, Pin SSxO assigned while Master Transfer

= 1, Pin SSxO is forced to logic 1

- **SPI Status Register**

SPSR (0xED)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EDh EIE	R/W	SPIF	WCOL	-	MODF	-	-	-	SSCEN
Reset		0	0	0	0	0	1	0	0

SPIF：SPI interrupt request. The flag is automatically set to one at the end of an SPI transfer.
WCOL：Write collision error status flag. The flag is automatically set if the SPDR is written while a transfer is in process.
MODF：SPI mode-fault error status flag
This flag is set if SS pin goes to active low while the SPI is configured as a master (MSTR = 1)
SSCEN：
= 1, auto SS assertions enabled
= 0, auto SS assertions disabled – SSO always shows contents of SSCR

SPI status register (SPSR) contains flags indicating the completion of transfer or occurrence of system errors. All flags are set automatically when the corresponding event occur and cleared by software sequence. SPIF and WCOL are automatically cleared by reading SPSR followed by an access of the SPDR. MODF flag is cleared by reading SPSR with MODF set followed by a write to SPCR.

The SSCSEN bit is a enable bit of automatic Slave Select Outputs assertion. When SSCEN is set ('1') then during master transmission the SSXO lines are automatically loaded with contents of SSCR register before each byte transfer, and deasserted when byte is transferred. When SSCEN bit is cleared the SSXO lines always shows contents of the SSCR register, regardless of the transmission is in progress or SPI MODULE is in IDLE state.

- Receiver and Transmitter Registers

The Transmitted Data Register consists of eight data bits, which will be sending on the bus due the next Send operation. The first send bit is the D.7 (MSB).

SPDR (0xEE)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEh SPDR	R/W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.0
Reset		0	0	0	0	0	1	0	0

The Received Data Register consists of eight data bits, which were received on the bus due the last Receive operation.

SPDR (0xEE)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEh SPDR	R/W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.0
Reset		0	0	0	0	0	1	0	0

15.4 MASTER OPERATIONS

When the SPI MODULE core is configured as a SPI master, the transfer is initiated by write to the SPDR register. When the new byte is written to the SPDR register, SPI MODULE begins transfer on the nearest BAUD timer overflow. The serial clock SCK is generated by the SPI MODULE. In master mode the SPI MODULE activates the SCKEN to enable the SCK output driver.

The SPI MODULE in master mode can select one of the eight SPI slave devices, through the SSxO lines. The SSxO lines – Slave Select output lines are loaded with contents of the SSCR register (0x03). The SSCEN bit from the SPSR register select between automatic SSxO lines control and software control. When set the automatic Slave Select outputs assertion is enabled. With SSCEN bit set in master mode the SSXO lines are automatically loaded with contents of SSCR register before each byte transfer, and deasserted when byte is transferred. When SSCEN bit is cleared the SSXO lines are controlled by the software, and always shows contents of the SSCR register, regardless of the transmission is in progress or the SPI MODULE is in IDLE state.

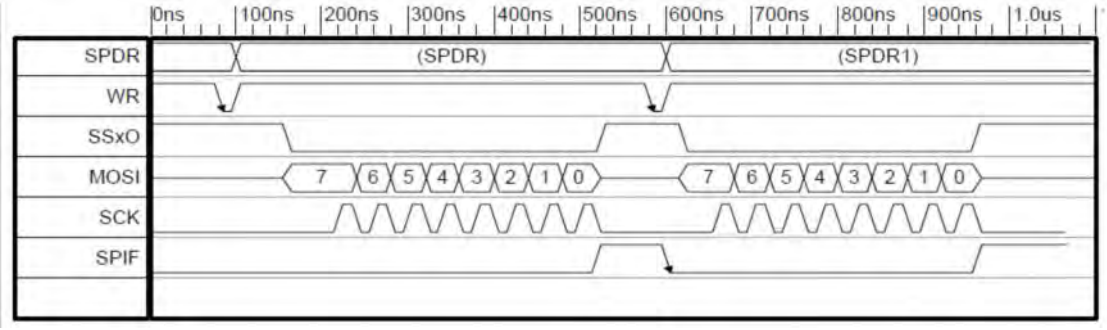


Figure15.3　Automatic slave select lines assertion

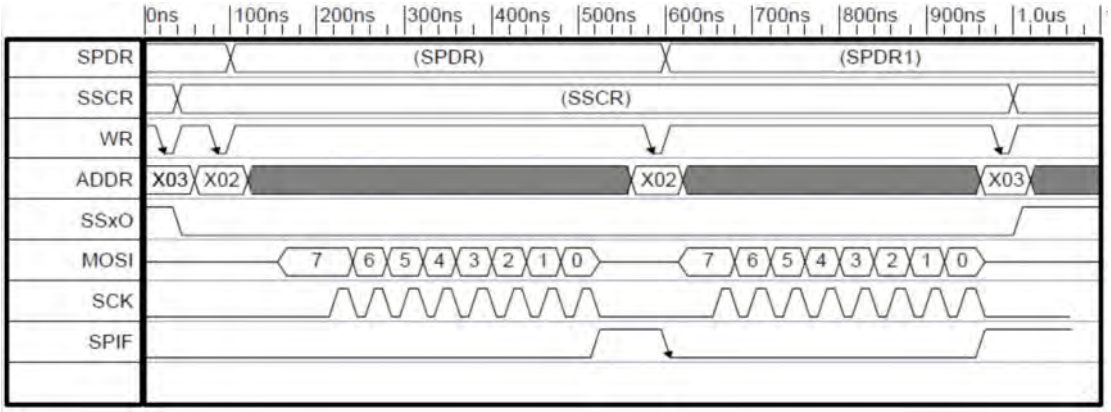


Figure15.4　Software controlled SSxO lines

15.4.1 MASTER MODE ERRORS

In master mode two system errors can be detected by the SPI MODULE. The first type of error arises in multiple-master system when more than one SPI device simultaneously tries to be a master. This error is called a Mode Fault. The second error type, a Write Collision, indicates that MCU tried to write the SPDR register while transfer was in progress.

◆ **MODE FAULT ERROR**

Mode fault error occurs when the SPI MODULE is configured as a master and some other SPI master device will select this device as if it were a slave. If a Mode Fault Error occur：

- ✧ The MSTR bit is forced to zero to reconfigure the SPI MODULE as a slave.
- ✧ The SPE bit is forced to zero to disable the SPI MODULE system
- ✧ The MODF status flag is set and an interrupt request is generated

The MODF flag is cleared by reading SPSR with MODF set followed by a write to SPCR

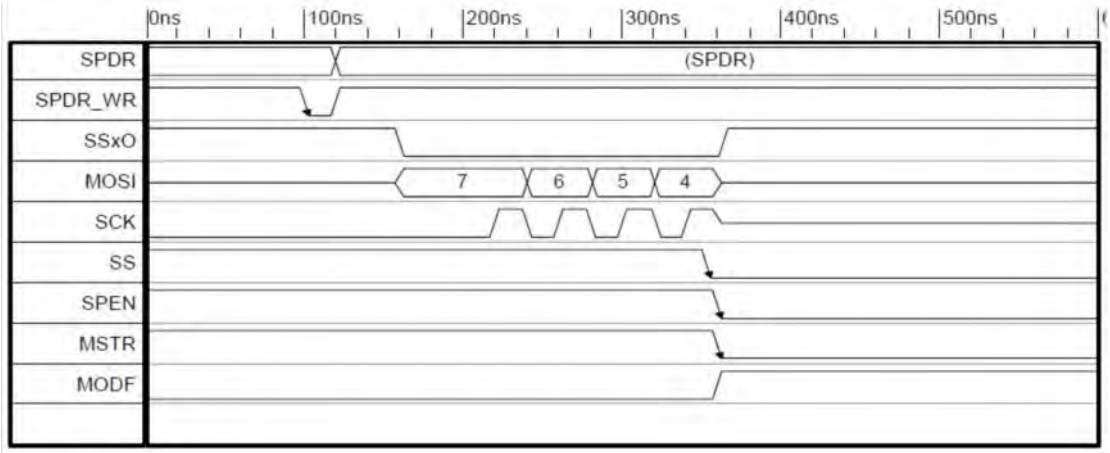


Figure15.5　Mode Fault Error generation

◆ **WRITE-COLLISION ERROR**

A write collision occurs if the SPI MODULE data register is written while a transfer is in progress. The transfer continues undisturbed, and the write data that caused the error is not written to the shifter. The Write Collision is indicated by the WCOL flag in SPSR (3) register.

The WCOL flag is set automatically by hardware, when the WCOL error condition occurs. To clear the WCOL bit, user should execute the following sequence:

- ✧ Read contents of the SPSR register
- ✧ Perform access to the SPDR register (read or write)

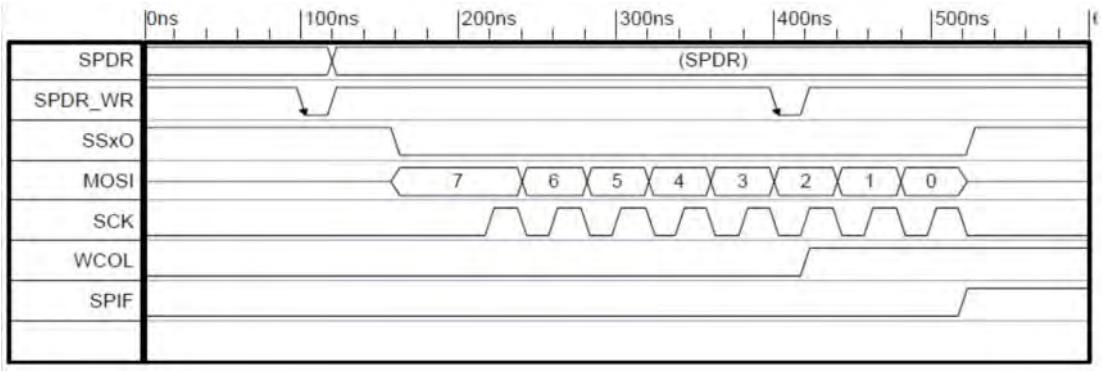


Figure15.6　Write Collision Error in SPI Master mode

15.5 SLAVE OPERATIONS

When configured as SPI Slave the SPI MODULE transfer is initiated by external SPI master module by assertion of the SPI MODULE Slave Select input, and generation of the SCK serial clock.

Before transfer starts, the SPI master has to assert the Slave Select line to determine which SPI slave will be used to exchange data. The SS is asserted (cleared = 0), the clock signal connected to the SXCK line will cause the SPI MODULE slave to shift into receiver shift register contents of the MOSI line, and drives the MISO line with contents of the Transmitter Shift register. When all eight bits are shifted in/out the SPI MODULE generates the Interrupt request by setting the IRQ output.

In SPI MODULE slave mode only one transfer error is possible – Write Collision Error.

15.5.1 SLAVE MODE ERRORS

In slave mode, only the Write Collision Error can be detected by the SPI MODULE.

The Write Collision Error occurs when the SPDR register write is performed while the SPI MODULE transfer is in progress.

In SLAVE mode when the CPHA is cleared, the write collision error may occur as long as the SS Slave Select line is driven low, even if all bits are already transferred. This is because there is not clearly specified the transfer beginning, and SS driven low after full byte transfer may indicate beginning of the next byte transfer.

◆ **WRITE-COLLISION ERROR**

A write collision occurs if the SPI MODULE data register is written while a transfer is in progress. The transfer continues undisturbed, and the write data that caused the error is not written to the shifter. The Write Collision is indicated by the WCOL flag in SPSR (3) register.

The WCOL flag is set automatically by hardware, when the WCOL error condition occurs. To clear the WCLO bit, user should execute the following sequence:

- ✧ Read contents of the SPSR register
- ✧ Perform access to the SPDR register (read or write)

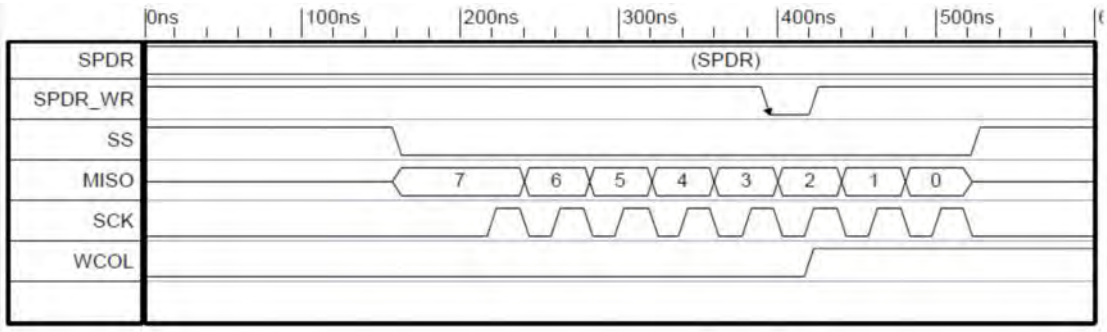


Figure15.7 Write Collision Error – SPI Slave mode – SPDR write during transfer

Figure below shows the WCOL generation, in case that the CPHA is cleared. As it is shown the WCOL generation is cause by any S{DR register write with SS line cleared. It is done even if the SPI master didn't generate the serial clock SCK. This is because there is not clearly specified the transfer beginning, and SS driven low after full byte transfer may indicate beginning of the next byte transfer.

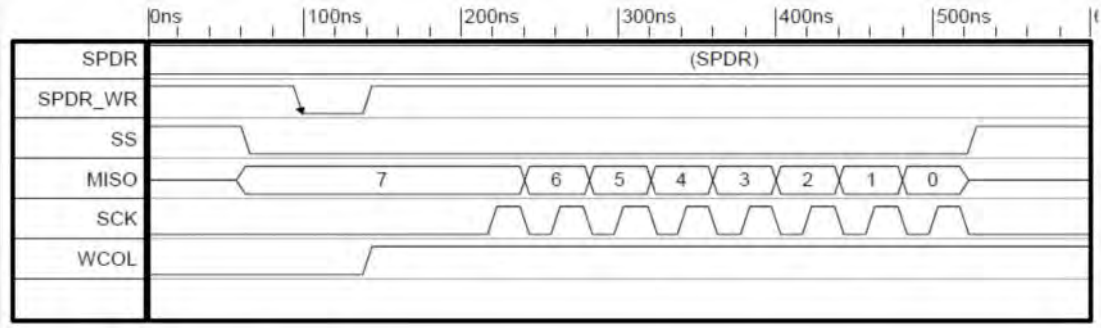


Figure15.8 WCOL Error-SPI Slave mode-SPDR write when CPHA = 0 and SS = 0

15.6 CLOCK CONTROL LOGIC

15.6.1 SPI CLOCK PHASE AND POLARITY CONTROLS

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the SPI MODULE allows direct interface to almost any existing synchronous serial peripheral.

15.6.2 SPI MODULE TRANSFER FORMATS

During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device; slave devices that are not selected do not interfere with SPI bus activities. On a master SPI device, the slave select line can optionally be used to indicate a multiple-master bus contention.

15.6.3 CPHA EQUALS ZERO TRANSFER FORMAT

Figure below shows a timing diagram of an SPI transfer where CPHA is 0. Two waveforms are shown for SCK: one for CPOL equals 0 and another for CPOL equals 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, master in/slave out (MISO), and master out/slave in (MOSI) pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The SS line is the slave select input to the slave; the SS pin of the master is not shown but is assumed to be inactive. The SS pin of the master must be high. This timing diagram functionally depicts how a transfer takes place; it should not be used as a replacement for data-sheet parametric information.

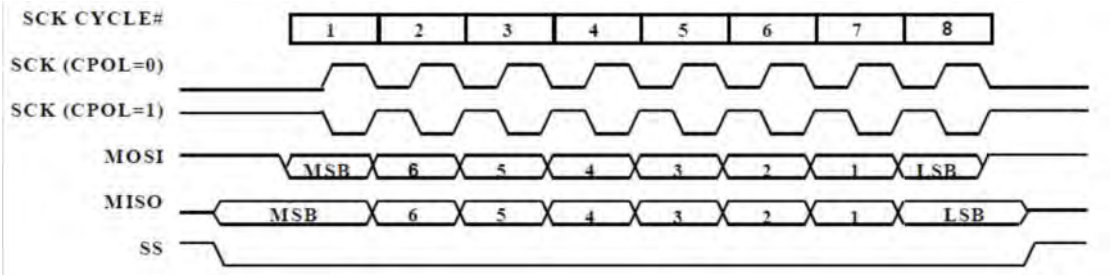


Figure15.9 CPHA Equals Zero SPI Transfer Format

When CPHA = 0, the SS line must be disserted and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while SS is active low, a write-collision error results. When CPHA = 1, the SS line may remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave driving the MISO data line.

15.6.4 CPHA EQUALS ONE TRANSFER FORMAT

Figure below is a timing diagram of an SPI transfer where CPHA = 1. Two waveforms are shown for SCK: one for CPOL = 0 and another for CPOL = 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, MISO, and MOSI pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The SS line is the slave select input to the slave; the SS pin of the master is not shown but is assumed to be inactive. The SS pin of the master must be high or must be reconfigured as a general-purpose output not affecting the SPI.

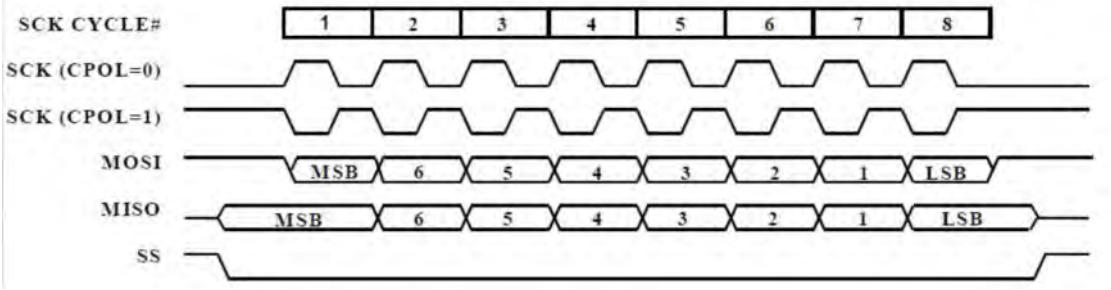


Figure15.10 CPHA Equals One SPI Transfer Format

15.7 SPI DATA TRANSFER

15.7.1 TRANSFER BEGINNING PERIOD (INITIATION DELAY)

All SPI transfers are started and controlled by a master SPI device. As a slave, the SPI MODULE considers a transfer to begin with the first SCK edge or the falling edge of SS, depending on the CPHA format selected. When CPHA = 0, the falling edge of SS indicates the beginning of a transfer. When CPHA = 1, the first edge on the SCK indicates the start of the transfer. In either CPHA format, a transfer can be aborted by taking the SS line high, which causes the SPI slave logic and bit counters to be reset. The SCK rate selected has no effect on slave operations since the clock from the master is controlling transfers.

When the SPI is configured as a master, transfers are started by a software write to the SPDR.

15.7.2 TRANSFER ENDING PERIOD

An SPI transfer is technically complete when the SPIF flag is set, but, depending on the configuration of the SPI system, there may be additional tasks. Because the SPI bit rate does not affect timing of the ending period, only the fastest rate is considered in discussions of the ending period. When the SPI is configured as a master, SPIF is set at the end of the eighth SCK cycle. When CPHA equals 1, SCK is inactive for the last half of the eighth SCK cycle.

When the SPI is operating as a slave, the ending period is different because the SCK line can be asynchronous to the MCU clocks of the slave and because the slave does not have access to as much information about SCK cycles as the master. For example, when CPHA = 1, where the last SCK edge occurs in the middle of the eighth SCK cycle, the slave has no way of knowing when the end of the last SCK cycle is. For these reasons, the slave considers the transfer complete after the last bit of serial data has been sampled, which corresponds to the middle of the eighth SCK cycle.

The SPIF flag is set at the end of a transfer, but the slave is not permitted to write new data to the SPDR while the SS line is still low.

15.8 TIMING DIAGRAMS

15.8.1 MASTER TRANSMISSION

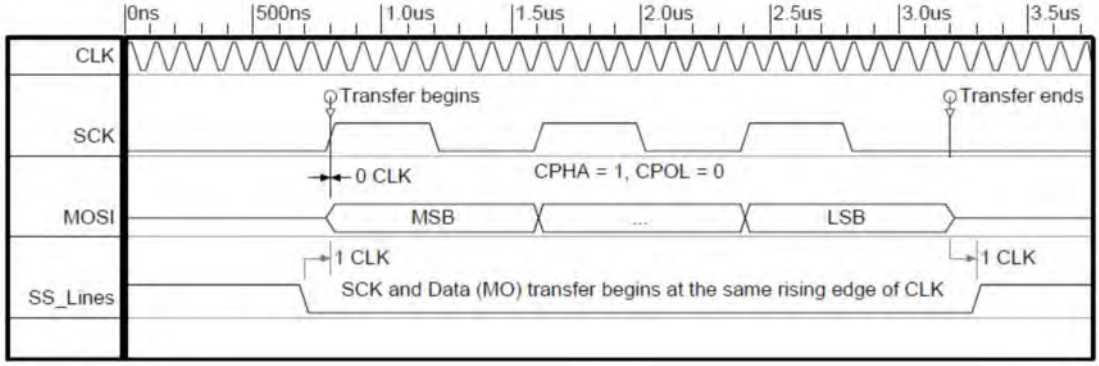


Figure15.11 Master mode timing diagram

15.8.2 SLAVE TRANSMISSION

At a beginning of transfer in Slave mode, the data on serial output (MISO) appears on first rising edge after falling edge on Slave Select (SS) line. Next bits of serial data are driving into MISO line on first rising edge of CLK after SKC active edge (in this case rising edge of SCK).

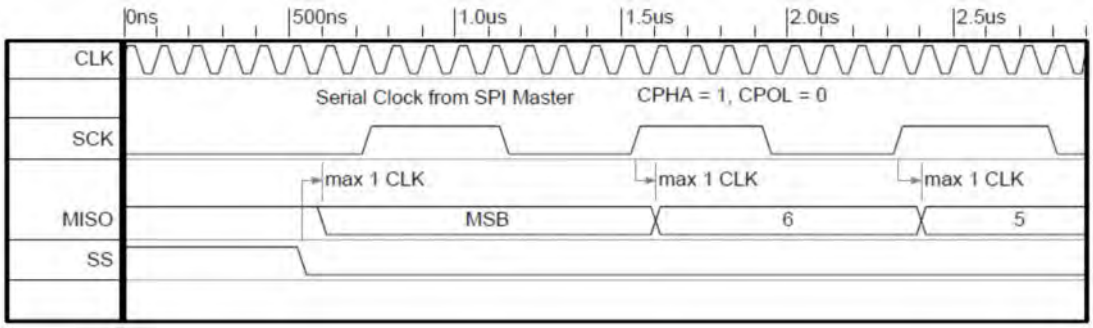


Figure15.12 Slave mode timing diagram

15.9 SPI MODULE INTERRUPT GENERATION

When interrupt is enabled (SPIE bit in SPCR=1), SPI interrupt flag is automatically asserted when SPI transfer is completed or transfer error has occurred. SPIIF flag has to be cleared by software.

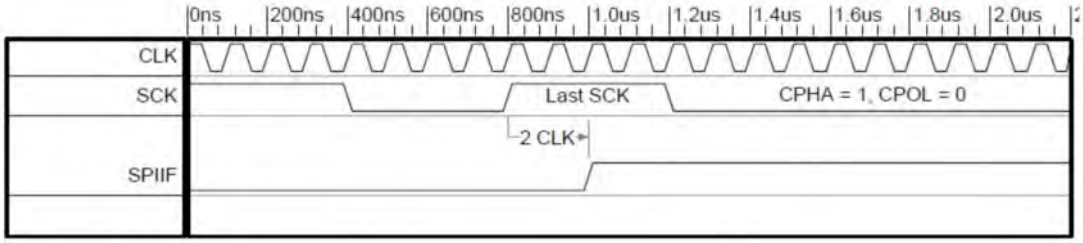


Figure15.13 Interrupt generation

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Natural priority
SPIIF	Internal, SPI	-	Software	0x73	15

Table15.2 SPI interrupt summary

SPI related interrupt bits have been summarized below. The IE (0xA8) contains global interrupt system disable (0) / enable (1) bit called EA.

EIE　(0xE8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8h EIE	R/W	EI2CS ESPI	EI2CM	EWDI	EKEYINT	ERFINT	EINT4	EINT3	EINT2
Reset		0	0	0	0	0	0	0	0

ESPI：Enable SPI Interrupts

EIP　(0xF8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F8h EIP	R/W	PI2CS PSPI	PI2CM	PWDI	PKEYINT	PRFINT	PINT4	PINT3	PINT2
Reset		0	0	0	0	0	0	0	0

PSPI：SPI priority level control (at 1-high-level)

EIF　(0x91)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
91h EIF	R/W	I2CSF SPIF	I2CMF	-	KEYINTF	RFINTF	INT4F	INT3F	INT2F
Reset		0	0	0	0	0	0	0	0

SPIIF：SPI interrupt flag

It must be cleared by software

16. PWM

A8125 has two channels Pulse width modulator (PWM) output. Every channel PWM has an 8-bit counter with comparator, a control register (PWMxCON) and two setting registers (PWMxH and PWMxL). User can select clock source by setting PWMxCON. Enable PWM output and function by setting PWMxEN = 1; otherwise disable PWM output and function by setting PWMxEN =0. When user set PWMxEN=0, it output LOW single and reload the PWMxL to itself. When the counter is enabled and matches the content of PWMxH, its output is asserted HIGH; when the counter is overflow, its output is asserted LOW and reload PWMxL to itself. The pulse frequency and the duty cycle for 8-bit PWM is given by the below equation

$$\text{Pulse frequency} = \text{System clock} / 2^{\text{pwxclk}+1} / (255\text{-PWMxL})$$
$$\text{Duty cycle} = (255\text{-PWMxH}) / 255\text{-PWMxL})$$

Noted: PWMxH must be larger then PWMxL. Otherwise, PWM output always is LOW.

16.1 PWM FUNCTIONALITY

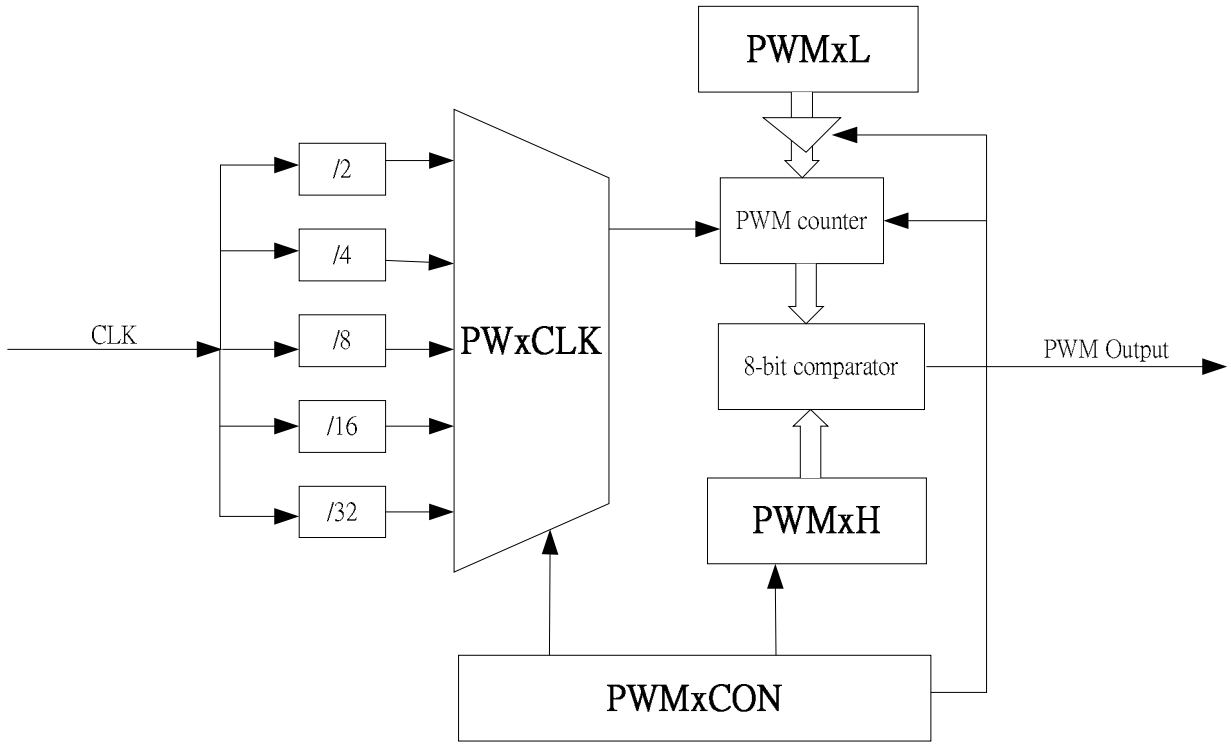


Figure16.1 PWM block diagram

The PWM pins functionality is described in the following table. All pins are one directional.

PIN	ACTIVE	TYPE	DESCRIPTION
PWM0(P1.6)		OUTPUT	PWM 0 output
PWM1(P1.7)		OUTPUT	PWM 1 output

Table16.1 PWM PIN define

16.1.1 PWM Registers

PWM0/1 is new design from AMICCOM. They can output pulse width modulation. User adjusts to duty cycle by setting PWMxH. PWM counter is up counter. PWM counter is not access directly by MCU. User can set or reset PWM counter by setting PWMxCON. When PWMxEN =1, PWM counter start to count. When PWMxEN=0, PWM counter stop counting and reload PWMxL to itself. PWxCLK is clock divider. It divide system clock to 2,4,8,16 ,32 and 64 by setting PWxCLK.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A9h	R/W	PWM0EN	-	-	-	-	PW0CLK2	PW0CLK1	PW0CLK0

PWM0CON									
Reset		0	0	0	0	0	0	0	0

PWM0CON: PWM channel 0 control register

PWM0EN: PWM Channel 0 Enable,
[0]: Disable. **[1]**: Enable.

PWM0CLK[2:0]: PWM Channel 0 Clock select
[000]: MCU Clock /2
[001]: MCU Clock / 4
[010]: MCU Clock / 8
[011]: MCU Clock / 16
[100]: MCU Clock / 32
[101]: MCU Clock / 64

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AAh PWM0H	R/W								
Reset		0	0	0	0	0	0	0	0

PWM0H: PWM channel 0 output HIGH register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ABh PWM0L	R/W								
Reset		0	0	0	0	0	0	0	0

PWM0L: PWM channel 0 frequency setting register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B0h PWM1CON	R/W	PWM1EN	-	-	-	-	PW1CLK2	PW1CLK1	PW1CLK0
Reset		0	0	0	0	0	0	0	0

PWM1CON: PWM channel 1 control register

PWM1EN: PWM Channel 1 Enable,
[0]: Disable. **[1]**: Enable.

PWM1CLK[2:0]: PWM Channel 1 Clock select
[000]: MCU Clock / 2
[001]: MCU Clock / 4
[010]: MCU Clock / 8
[011]: MCU Clock / 16
[100]: MCU Clock / 32
[101]: MCU Clock / 64

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B1h PWM1H	R/W								
Reset		0	0	0	0	0	0	0	0

PWM1H: PWM channel 1 output HIGH register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B2h PWM1L	R/W								
Reset		0	0	0	0	0	0	0	0

PWM1L: PWM channel 1 frequency setting register

17. Watchdog Timer

A8125 has a special timer, called Watchdog Timer. It is a useful programmable clock counter that serves as a time-base generator, an event timer or system supervisor. User can use be a very long timer with disabled reset function.

17.1 Watchdog timer overview

As can be seen in the figure below, the watchdog timer is driven by the main system clock that is supplied to a series of dividers. The divider output is selectable and determines interval between timeouts. When the timeout is reached, an interrupt flag will cause an interrupt to occur if its individual enable bit is set and the global interrupt enable is set. The reset and interrupt are discrete functions that may be acknowledged or ignored, together or separately for various applications.

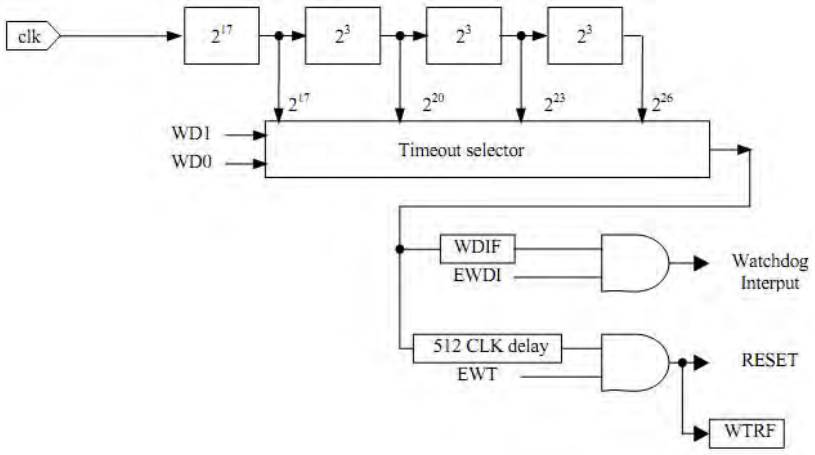


Figure 17.1 Watchdog Timer architecture

17.2 Watchdog interrupt

WATCHDOG interrupt related bits are shown below. An interrupt can be turned on/off by EIE register, and set into high/low priority group by EIP register. The IE contains global interrupt system disable (0) / enable (1) bit called EA.

IE register (0xA8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8h IE	R/W	EA	-	ET2	ES	ET1	EX1	ET0	EX0
Reset		0	0	0	0	0	0	0	0

EA：Enable global interrupts.

EIE (0xE8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8h EIE	R/W	EI2CS ESPI	EI2CM	EWDI	EKEYINT	ERFINT	EINT4	EINT3	EINT2
Reset		0	0	0	0	0	0	0	0

EWDI：Enable Watchdog interrupts

EIP (0xF8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F8h EIP	R/W	PI2CS PSPI	PI2CM	PWDI	PKEYINT	PRFINT	PINT4	PINT3	PINT2
Reset		0	0	0	0	0	0	0	0

PWDI：Enable Watchdog priority level control (at 1-high-level)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D8h WDCON	R/W	-	-	-	-	WDIF	WTRF	EWT	RWT
Reset		0	0	0	0	0	0	0	0

WDIF：Watchdog Interrupt Flag. WDIF in conjunction with the Enable Watchdog Interrupt bit (EXIE.5), and EWT, indicates if watchdog timer event has occurred and what action should be taken. This bit must be cleared by software before exiting the interrupt service routine, or another interrupt is generated. Setting WDIF in software will generate a watchdog interrupt if enabled. Timed access registers procedure can be used to modify this bit.

All of bits that generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software. The Watchdog interrupt vector is located in 0x63. User can put interrupt service routine to take care watchdog interrupt event.

17.3 Watchdog Timer reset

The Watchdog Timer Reset function works as follows. After initializing the correct timeout interval, software first restarts the Watchdog using RWT and then enables the reset mode by setting the Enable Watchdog Timer Reset (WDCON.1) bit. At any time prior to reaching its user selected terminal value, software can set the Reset Watchdog Timer (WDCON.0) bit. If RWT is set before the timeout is reached, the timer will start over. If the timeout is reached without RWT being set, the Watchdog will reset the MCU. Hardware will automatically clear RWT after software sets it. When the reset occurs, the Watchdog Timer Reset Flag (WDCON.2) will automatically be set to indicate the cause of the reset, however software must clear this bit manually.

17.4 SIMPLE TIMER

The Watchdog Timer is a free running timer. When used as a simple timer with both the reset (EWT=0) and interrupt functions disabled (EWDI=0), the timer will continue to set the Watchdog Interrupt flag each time the timer completes the selected timer interval as programmed by WD[1:0]. Restarting the timer using the RWT bit, allows software to use the timer in a polled timeout mode. The WDIF bit is cleared by software or any reset. The Watchdog Interrupt is also available for applications that do not need a true Watchdog Reset but simply a very long timer. The interrupt is enabled using the Enable Watchdog Timer Interrupt (EIE.4) bit. When the timeout occurs, the Watchdog Timer will set the WDIF bit (WDCON.3), and an interrupt will occur if the global interrupt enable (EA) is set. **A potential Watchdog Reset is executed 512 clocks after setting of WDIF flag**. The Watchdog Interrupt Flag indicates the source of the interrupt, and software must clear WDIF flag. Proper use of the Watchdog Interrupt with the Watchdog Reset allows interrupt software to survey the system for errant conditions.

17.5 SYSTEM MONITOR

When using the Watchdog Timer as a system monitor, the Watchdog Reset function should be used. If the Interrupt function were used, the purpose of the watchdog would be defeated. For example, assume the system is executing errant code prior to the Watchdog Interrupt. The interrupt would temporarily force the system back into control by vectoring the MCU to the interrupt service routine. Restarting the Watchdog and exiting by an RETI or RET, would return the processor to the lost position prior to the interrupt. By using the Watchdog Reset function, the processor is restarted from the beginning of the program, and therefore placed into a known state.

17.6 WATCHDOG RELATED REGISTERS

The watchdog timer has several SFR bits that contribute to its operation. It can be enabled to function as either a reset source, interrupt source, software polled timer or any combination of the three. Both the reset and interrupt have status flags. The watchdog also has a bit that restarts the timer. A summary table showing the bit locations is below. A description follows.

Bit name	Register	Bit position	Description
EWDI	EIE	EIE.5	Enable Watchdog Timer Interrupt
PWDI	EIP	EIP.5	Priority of Watchdog Timer Interrupt
WD[1:0]	CKCON	CKCON.7-6	Watchdog Interval
RWT	WDCON	WDCON.0	Reset Watchdog Timer
EWT		WDCON.1	Enable Watchdog Timer Reset
WTRF		WDCON.2	Watchdog Timer Reset flag
WDIF		WDCON.3	Watchdog Interrupt flag

A Watchdog timeout reset will not disable the Watchdog Timer, but restarts the timer. In general, software should set the Watchdog to whichever state is desired, just to be certain of its state. Control bits that support Watchdog operation are described in next subchapters.

17.6.1. WATCHDOG CONTROL

Watchdog control bits are described below. Please note that access (write) to this register has to be performed using Timed access registers procedure.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D8h WDCON	R/W	-	-	-	-	WDIF	WTRF	EWT	RWT
Reset		0	0	0	0	0	0	0	0

WDIF：Watchdog Interrupt Flag.

WDIF in conjunction with the Enable Watchdog Interrupt bit (EXIE.5), and EWT, indicates if watchdog timer event has occurred and what action should be taken. This bit must be cleared by software before exiting the interrupt service routine, or another interrupt is generated. Setting WDIF in software will generate a watchdog interrupt if enabled. Timed access registers procedure can be used to modify this bit.

WTRF：Watchdog Timer Reset Flag.

When set by hardware, indicates that a watchdog timer reset has occurred. Set by software do not generate a watchdog timer reset. It is cleared by RESET pin, but otherwise must be cleared by software. The watchdog timer has no effect on this bit, when EWT bit is cleared.

EWT：Enable Watchdog Timer Reset.

The reset of microcontroller by watchdog timer is controlled by this bit. This bit has no effect on the ability of the watchdog timer to generate a watchdog interrupt. Timed Access procedure must be used to modify this bit.
0: watchdog timer timeout doesn't reset microcontroller
1: watchdog timer timeout resets microcontroller

RWT：Reset Watchdog Timer.

Setting RWT resets the watchdog timer count. Timed Access procedure must be used to set this bit before the watchdog timer expires, or a watchdog timer reset and/or interrupt will be generated if enabled.

17.6.2 CLOCK CONTROL

The Watchdog timeout selection is made using bits WD[1:0] as shown in the figure.

CKCON register (0x8E)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8Eh CKCON	R/W	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
Reset		0	0	0	0	0	0	0	0

Clock control register CKCON(0x8E) contains WD[1:0] bits select Watchdog timer timeout period. The Watchdog is clocked directly from CLK pin, and CKSE mode directly affects its timeout period. It is increased 256 times slower when the core is in CKSE mode. This allows the watchdog period to remain synchronized with device operation. Number of clocks needed for timeout does not depend on CKSE, and is constant as shown in table below. The Watchdog has four timeout selections based on the input CLK clock frequency as shown in the figure. The selections are a pre-selected number of clocks. Therefore, the actual timeout interval is dependent on the CLK frequency.

WD[1:0]	Watchdog interval	Number of clocks
00	2^{17}	131072
01	2^{20}	1048576
10	2^{23}	8388608
11	2^{26}	67108864

Note that the periods shown above are for the interrupt events. The Reset, when enabled, is generated 512 clocks later regardless of whether the interrupt is used. Therefore, the actual Watchdog timeout period is the number shown above plus 512 clocks (always CLK pin).

17.7 TIMED ACCESS REGISTERS

Timed Access registers have built in mechanism preventing them from accidental writes. TA is located at 0xEB SFR address. To do a correct write to such register the following sequence has to be applied:

```
  CLR EA ;disable interrupt system
  MOV TA, #0xAA
  MOV TA, #0x55
; Any direct addressing instruction writing timed access register.
  SETB EA ;Enable interrupt system
```

The time elapsed between first, second, and third operation does not matter (any number of Program Wait Sates is allowed). The only correct sequence is required. Any third instruction causes protection mechanism to be turned on. This means that time protected register is opened for write only for single instruction. Reading from such register is never protected. WDCON (D8h) is Timed Access register.

18. ADC (Analog to Digital Converter)

A8125 has built-in 8-bits ADC do RSSI measurement as well as carrier detection function. And It also use a general ADC and selects input source from P3.2 (PIN36), P3.3 (PIN37), P3.4 (PIN38) or P3.5 (PIN39).The ADC clock (F_{ADC}) is 4MHz. The ADC converting time is 20 x ADC clock periods.

Bit		Mode	
ADCIOS0	ARSSI	Standby	RX
0	1	None	RSSI / Carrier detect
1	x	External Input	External Input

Table 18.1 Setting of ADC function

Relative Control Register

IOSEL Register (0xBB)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BBh IOSEL	R/W	ADCIOS2	ADCIOS1	ADCIOS0	RTCIOS	BBIOS	-	I2CIOS	UARTIOS
Reset		0	0	0	0	0	0	0	0

ADCIOS[2:0] (ADC I/O select)
ADCIOS[2:1]
[00]: Select P3.2 as the ADC analog input
[01]: Select P3.3 as the ADC analog input
[10]: Select P3.4 as the ADC analog input
[11]: Select P3.5 as the ADC analog input
ADCIOS0
[1]: Enable ADC analog input
[0]: Disable ADC analog input

RX LQI Register I (Address: 082Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	LQI7	LQI6	LQI5	LQI4	LQI3	LQI2	LQI1	LQI0
	W	ULS	SLF2	DCM1	DCM0	LQICE	ARSSI	AIF	LQIE
Reset		1	1	0	1	0	1	1	0

ARSSI: Auto RSSI measurement whenever in RX mode. Recommend ARSSI = [1].
[0]: Disable. **[1]:** Enable.

ADC Register (Address: 0821h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	W	CDTH7	CDTH6	CDTH5	CDTH4	CDTH3	CDTH2	CDTH1	CDTH0
Reset		0	0	0	0	0	0	0	0

CDTH [7:0]: Carrier detect threshold (write only).

ADC [7:0]: ADC digital output value (read only).
ADC input voltage = 1.2 * ADC [7:0] / 256 V.

ADC Control Register (Address: 0822h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	CDM	ADCOM1	ADCOM0	MRSSL	--	AVGS1	AVGS0
Reset			1	1	1	0	--	1	1

--

18.1 External Input

User can use ADC to measure the external input. The input voltage range is from 0.3V ~ 1.5V. Please take care the input voltage if set the input source from exteral input. User can set ADCIOS[2 :1 (0Bh)] to select input source. Set ADCIOS0 to 1 to enable external input. Refer the following fouma, user calculate the input voltage from ADC[7 :0] (0821h)

ADC input voltage = 1.2 * ADC [7:0] / 256 V.

18.2 RSSI Measurement

A8125 supports 8-bits digital RSSI to detect RF signal strength. RSSI value is stored in ADC [7:0] (0821h). Fig 18.1 shows a typical plot of RSSI reading as a function of input power. This curve is base on the current gain setting of A8125 reference code. A8125 automatically averages 2/4/8/16-times (by AVGS setting) ADC conversion a RSSI measurement until A8125 exits RX mode. Therefore, maximum RSSI measuring time is (16 x 20 x F_{ADC}). Be aware RSSI accuracy is about ± 6dB.

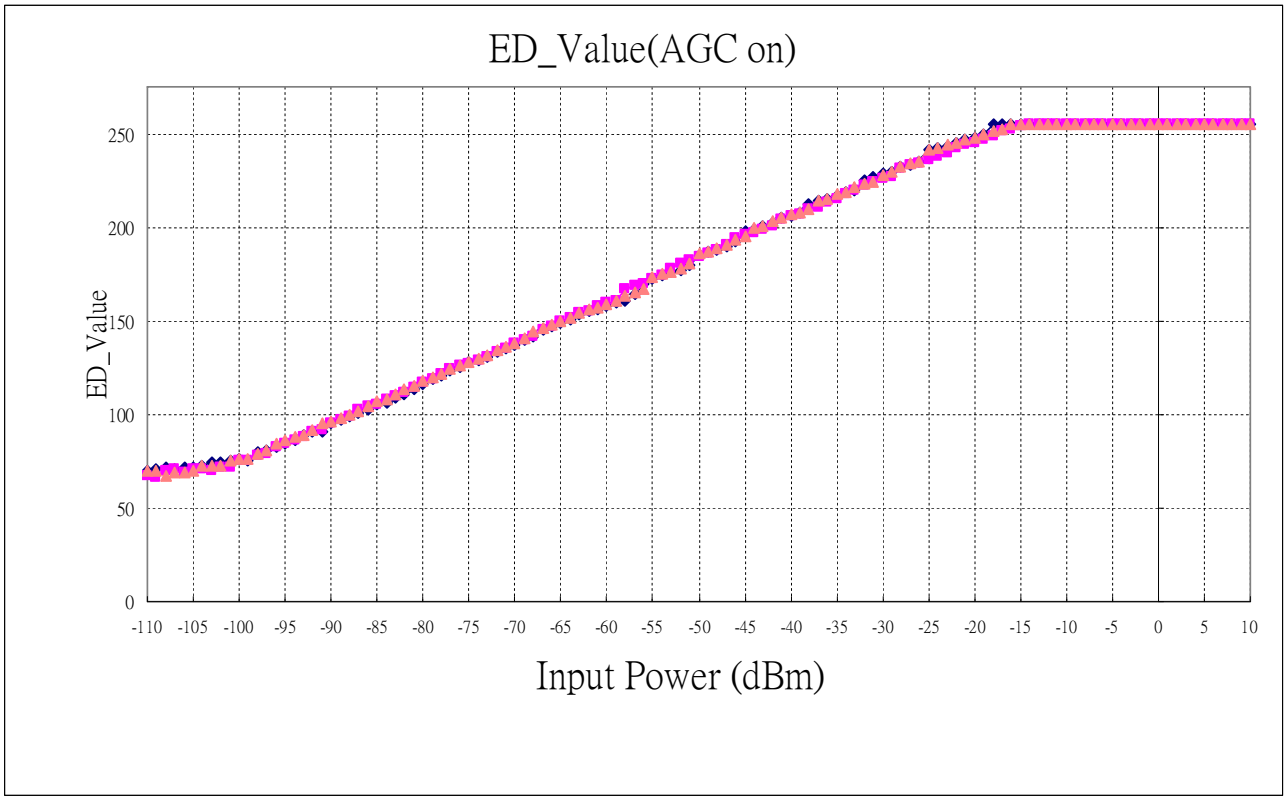


Figure 18.1 Typical RSSI characteristic.

Auto RSSI measurement for TX Power:

1. Enable ARSSI= 1 (082Fh).
2. Send RX Strobe command.
3. In RX mode, 8-times average a RSSI measurement periodically.
4. Exit RX mode, user can read digital RSSI value from ADC [7:0] (0821h) for TX power.

In step 6, if A8125 is set in direct mode, MCU shall let A8125 exit RX mode within 40 us to prevent RSSI inaccuracy.

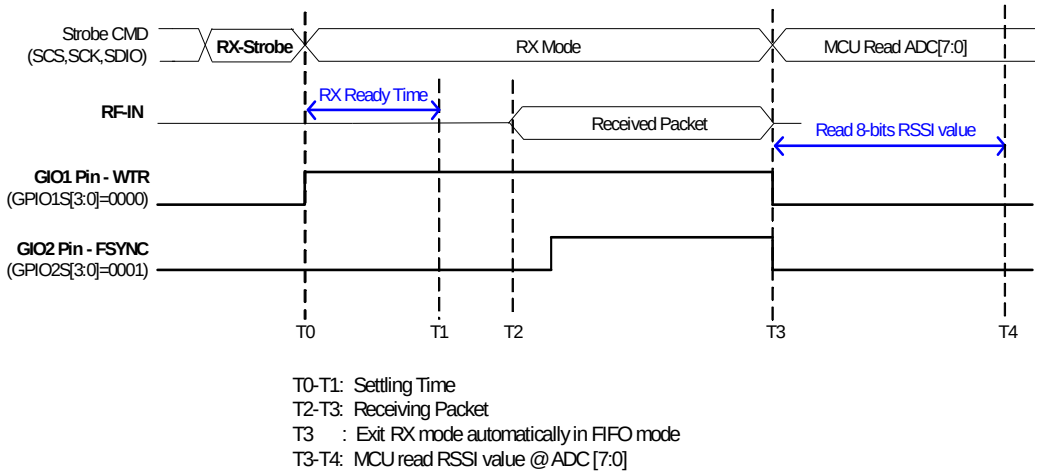


Figure 18.2 RSSI Measurement of TX Power.

Auto RSSI measurement for Background Power:

1. Enable ARSSI= 1 (082Fh).
2. Send RX Strobe command.
3. MCU delays min. 140us.
4. Read digital RSSI value from ADC [7:0] (0821h) to get background power.
5. Send other Strobe command to let A8125 exit RX mode.

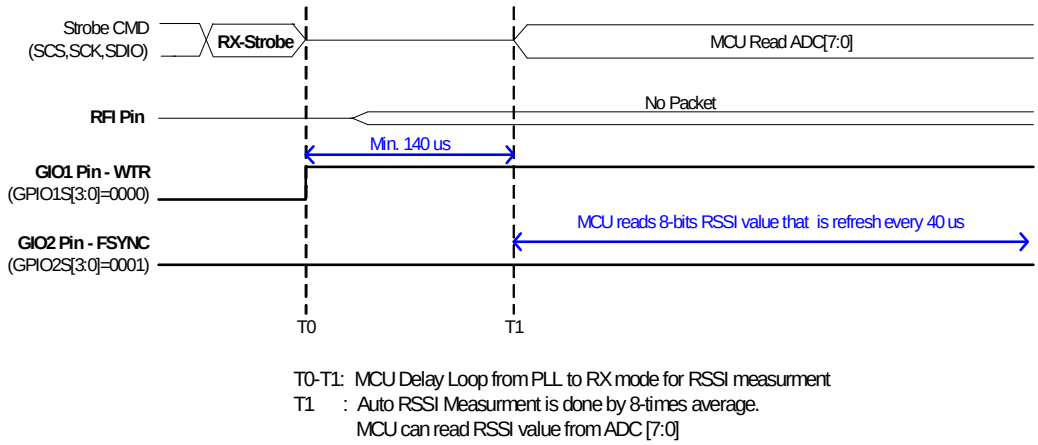


Figure 18.3 RSSI Measurement of Background Power.

18.3 Carrier Detect

Base on RSSI measurement, user can extend its application to do carrier detect (CD). In Carrier Detect mode, RSSI is refresh every 5 us without 8-times average. If RSSI level is below threshold level (RTH), CD is output high to GIO1 or GIO2 pin to inform MCU that current channel is busy.

Below is a reference procedure:

1. Set CDTH (0821h) for absolute RSSI threshold level (ex. RTH = 80d).

2. Set GIO2S = [0010] (080Eh) for Carrier Detect to GIO2 pin.
   (2-1) Set wanted F_{RXLO} (Refer to chapter 14).
   (2-2) Set CDM (0822h, CDM =0 and hysteresis =6, or CDM =1 and hysteresis =12).
   (2-3) Enable ARSSI= 1 (082Fh).
   (2-4) Send RX Strobe command.
   (2-5) MCU enables a timer delay (min. 100 us).
3. MCU checks GIO2 pin.
   (3-1) If ADC ≧ CDTH, GIO2 = 0.
   (3-2) If ADC ≦ CDTH-CDM, GIO2 = 1.
   (3-3) If ADC locates in hysteresis zone, GIO2 = previous state.
4. Exit RX mode.

19. Battery Detect

A8125 has a built-in battery detector to check supply voltage (REGI pin). The detecting range is 2.0V ~ 2.7V in 8 levels.

Relative Control Register

Battery detect Register (Address: 082Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Battery detect	R	--	--	--	--	--	--	--	BDF
	W	ATP1	ATP0	--	BDV2	BDV1	BDV0	BGS	BDE
Reset		0	0	0	--	0	1	1	0

BDV[2:0]: Battery detection threshold.
[000]: 2.0V. **[001]:** 2.1V. [**010]:** 2.2V. **[011]:** 2.3V. **[100]:** 2.4V. **[101]:** 2.5V. [**110]:** 2.6V. **[111]:** 2.7V.

When REGI < Threshold, BDF= low.
When REGI > Threshold, BDF= high.

Below is the procedure to detect low voltage input (ex. below 2.1V):

1. Set A8125 in standby or PLL mode.
2. Set BDV[2:0] (082Ch) = [001] and enable BDE (082Ch) = 1.
3. After 5 us, BDE is auto clear.
4. MCU reads BDF (082Ch).
   If REGI pin > 2.1V,
   BDF = 1 (battery high). Else, BDF = 0 (battery low).

20. Power Management

The power consumption of A8125 comes from two parts. One is RF part and the other is digital part (includes MCU core and peripherals). In the RF part, the sleep mode use the minimum power and the TX or RX mode use the maximum power consumptions. Use changes RF status by setting the strobe control,register(0800h). For more detail information, please refer chapter 21.1. Chapter 20 only introduces digital parts. Low power operation is enabled through different power modes setting. A8125 has various operating mode are referred as normal mode and PM (power manager mode). Table 20.1 shows the impact of different power modes on systems operation. There are two registers to setting power manager. One is power control register (PCON, 0x87h) and the other is power control extend register (PCONE, 0xB9h).

In CKSE mode, user selects different clock be MCU core clock.in CLKSEL[2:0] (PCONE, 089h) then enable CKSE (PCON, 087h). User adjusts MCU clocks depends on the required power consumption. CLKSEL[2:0] = 001 ~ 110b, the MCU core clock is the clock sources divide 2 ~ 64. User could adjust the MCU speed to trade-off between the performance and the power consumption. **BEWARE, please choice CLKSEL firstly then enable CKSE to avoid glitch. Please refer the following reference code or contacts AMICCOM's FAE.**

User can enable STOP to freeze MCU core clock and all digital peripherals also stop. MCU can be waked up by hardware reset, KEY wake up, KEYINT or sleep timer (WOR /TWOR). User set sleep timer, WOR or TWOR before enter STOP mode. In this condition, it is called PM1. In PM1, all digital circuitry is stop and RF circuitry is active by WOR

Note: Please don't enable STOP and CKSE at the same time.

PCON (087h) Power control

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
87h PCON	R/W	SMOD	-	-	PWE	-	SWB	STOP	CKSE
Reset		0	0	0	0	0	0	0	0

SWB (Switchback enable)
[1]: Enable
[0]: Disable
STOP (Stop mode)
[1]: Enable
[0]: Disable
CKSE (Clock select mode)
[1]: Enable power manager mode
[0]: Disable power manager mode

PCONE(089h) Power control extend

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B9h PCONE	R/W	-	PM1S	QD	REGAE	PM3S	CLKSEL2	CLKSEL1	CLKSEL0
Reset		0	0	0	0	0	0	0	0

PM1S (Power Mode 1 select)
It is valid during CPU enter power mode (STOP = 1) and REGAE = 0.
[1]: Select PM1 mode.
[0]: Select PM2 mode.
QD (Quick discharge)
[1]: Quick discharge enable
[0]: Quick discharge disable
REGAE (Analog Regulator Enable)
It is valid during CPU enter power mode (STOP = 1).
[1]: Enable
[0]: Disable
PM3S (Power Mode 3 select)
It is valid during CPU enter power mode (STOP = 1).
[1]: Enable PM3 then VDD_D is off.
[0]: Disable PM3
CLKSEL[2:0] (Clock Select), Select CKSE (Power manager mode) clock source
[000]: Clock source div 64 as MCU clock
[001]: Clock source div 2 as MCU clock
[010]: Clock source div 4 as MCU clock
[011]: Clock source div 8 as MCU clock

[100]: Clock source div 16 as MCU clock
[101]: Clock source div 32 as MCU clock
[110]: Clock source div 64 as MCU clock
[111]: Select RTC as CPU clock when CKSE=0; RTC div 2 as CPU clock when CKSE=1

	MCU speed	16MHz	RAM retainance	Back to Normal	LVR	RF
Normal CKSE = 0	16MHz	ON	ON	X	X	X
Normal CKSE = 1	8/4/2/1 MHz IRC/RTC	ON	ON	X	X	X
PM1 STOP =1 REGAE = 0 PM1S = 1 PM3S = 0	OFF	OFF	ON	H/W reset / KEYINT / Sleep timer	X	OFF
PM2 STOP =1 REGAE = 0 PM1S = 0 PM3S = 0	OFF	OFF	ON	H/W reset / KEYINT / Sleep timer	X	OFF
PM3 STOP =1 REGAE=x PM1S = x PM3S = 1	OFF	OFF	OFF	H/W reset / wakeup key / Sleep timer	OFF	OFF

Table 20.1 Power manager

X: don't care, it can turn on or off by user setting

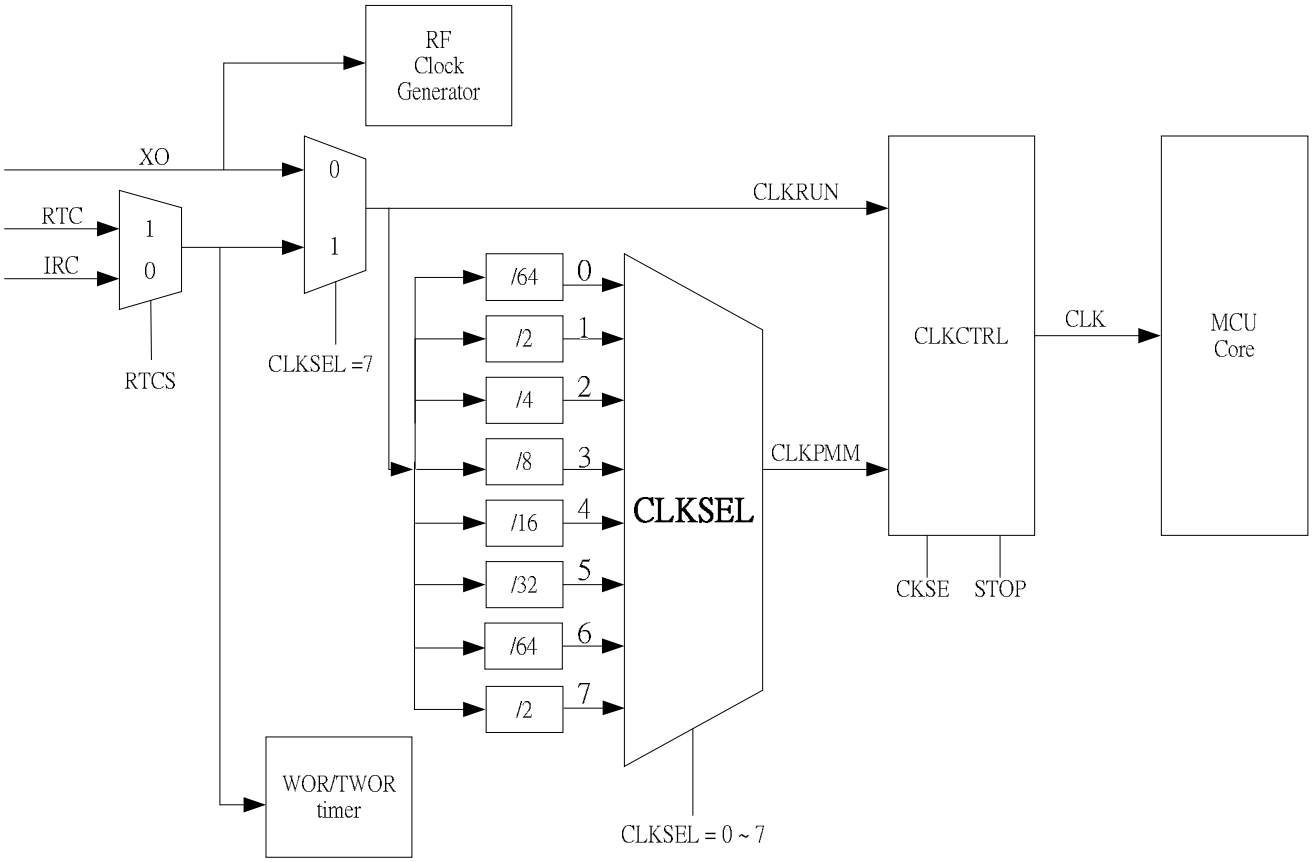


Figure 20.1 Whole chip clock sources

21. A8125 RF

A8125 has high speed (up to 2Mbps) transceiver and use Strobe control register (0800h) to control RF state. There are 6 Strobe commands to control internal state machine for RF operations. These modes include Sleep mode, Idle mode, Standby mode, PLL mode, RX mode and TX mode. There are three 128Bytes FIFO for data transmitting, receiving and AES encrypt/decrypt. Sleep timer is used for WOR (Wake On Rx) and time-slotted mode operation.

21.1 Strobe Command

Strobe Control Register (Address: 0800h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R					FPEN	RFSTATE2	RFSTATE1	RFSTATE0
	W	Strobe3	Strobe2	Strobe1	Strobe0			--	--
Write Reset Value		0	0	0	0	0	0	0	0

Use strobe command control RF state.
Strobe[3:0] = 4'b1000: Sleep mode.
Strobe[3:0] = 4'b1001: Idle mode.
Strobe[3:0] = 4'b1010: Standby .
Strobe[3:0] = 4'b1011: PLL mode.
Strobe[3:0] = 4'b1100: RX mode
Strobe[3:0] = 4'b1101: TX mode

RFSTATE[2:0]: RF state flag.
RFSTATE[2:0] = 3'b000: Sleep mode.
RFSTATE[2:0] = 3'b001: Idle mode.
RFSTATE[2:0] = 3'b010: standby mode.
RFSTATE[2:0] = 3'b011: PLL mode.
RFSTATE[2:0] = 3'b100: TX mode
RFSTATE[2:0] = 3'b101: RX mode

In A8125, user control RF mode as well as read/write ram. By DPTR access and MOVX instruction, user change RF mode and know RF status.

21.1.1 Strobe Command - Sleep Mode
Refer to Strobe Control Register, user can write 0x80 to Strobe Control Register directly to set RF into Sleep mode.

21.1.2 Strobe Command - Idle Mode
Refer to Strobe Control Register, user can write 0x90 to Strobe Control Register directly to set RF into Idle mode.

21.1.3 Strobe Command - Standby Mode
Refer to Strobe Control Register, user can write 0xA0 to Strobe Control Register directly to set RF into Standby mode.

21.1.4 Strobe Command - PLL Mode
Refer to Strobe Control Register, user can write 0xB0 to Strobe Control Register directly to set RF into PLL mode.

21.1.5 Strobe Command - RX Mode
Refer to Strobe Control Register, user can write 0xC0 to Strobe Control Register directly to set RF into RX mode.

21.1.6 Strobe Command - TX Mode
Refer to Strobe Control Register, user can write 0xD0 to Strobe Control Register directly to set RF into TX mode.

21.2 RF Reset Command

In addition to power on reset (POR), A8125 could issue software reset (80h) to RF by setting Mode Register (0801h). A8125 generates an internal signal "RESETN" to initial RF circuit. After reset command, RF state is in standby mode and re-calibration is necessary.

21.3 FIFO Accessing Command

Before TX delivery, user only needs to write wanted data into TX FIFO (0x900 ~ 0x9FFF) in advance. Similarly, user can read RX FIFO (0XA00 ~ 0xAFFF) once payload data is received. It is easy to delivery data to air. Below is the procedure of writing TX FIFO.
Payload length is programmable by PHR [7:0](0805h). The physical FIFO depth is 64 bytes. A8125 also supports logical FIFO extension up to 256 bytes.

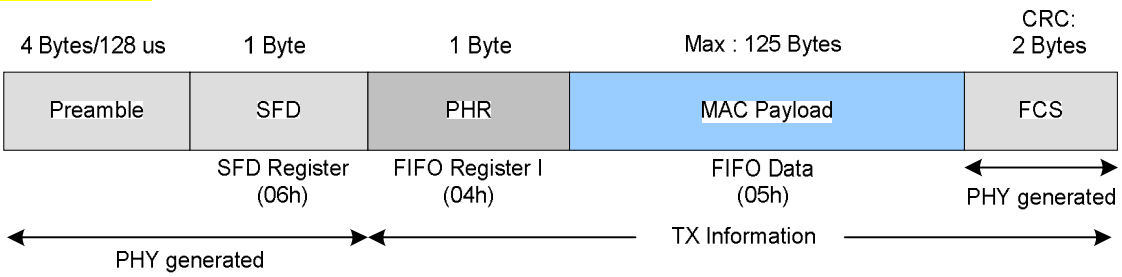
Step1: Send (n+1) bytes TX data in sequence by Data Byte 0, 1, 2 to n.
Step2: Send TX Strobe command for transmitting.

There are similar steps to read RX FIFO.
Step1: Send RX Strobe command for receiving data.
Step2: Read RX data from RX FIFO in sequence by Data Byte 0, 1, 2 to n.

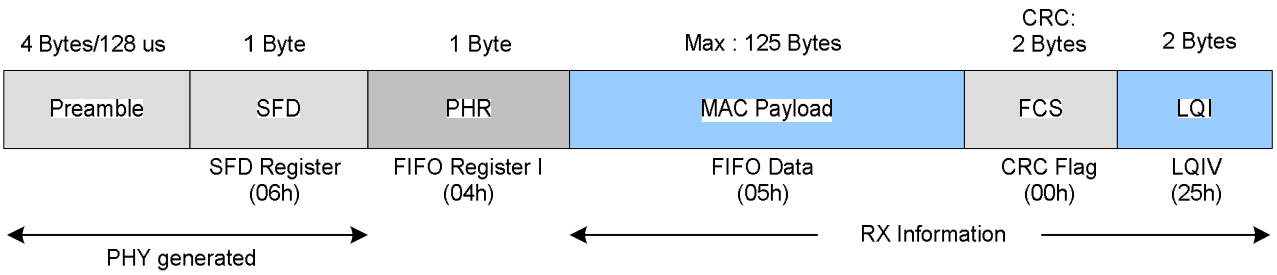
21.4 A8125 Frame Structure

A8125 contains a 256 byte TX FIFO and a 256 byte RX FIFO located from 0900h ~ 0AFFh.
The physical FIFO depth is 64 bytes. A8125 supports logical FIFO extension up to 256 bytes.
A8125 supports Serial Packet ID (SID:0857h~085Eh), the length is 4/8 bytes.
A8125 supports the dynamic length function for PHR frame.

TX Operation



RX Operation



21.5 Transceiver Frequency

A8125 is a half-duplex transceiver with embedded PA and LNA. For TX or RX frequency setting, user just needs to set up one register, CHN (0811h), for frequency agility.

A8125's main PLL features are:

- Frantional-N to generate RX/TX frequencies for all IEEE 802.15.4 - 2.4 GHz channels
- Autonomous calibration loops for stable operation within the operating range
- Fast PLL settling to support frequency hopping

During receive operation, the frequency synthesizer works as a local oscillator. During transmit operation, the voltage-controlled oscillator (VCO) is directly modulated to generate the RF transmit signal. The frequency synthesizer is implemented as a fractional-N PLL.

The PLL is designed to support 16 channels in the 2.4 GHz ISM band with channel spacing of 5 MHz according to IEEE 802.15.4. An offset scheme is implemented to get the center frequency of these channels as follows:

F_{LO} = 2400 + (CHN x 0.5) in [MHz], where CHN is the channel number, addr 0811h.

A8125's LO frequency $F_{LO} = F_{LO\_BASE} + F_{OFFSET}$. Therefore, A8125 is very easy to implement frequency hopping by **ONE register setting, (CHN, 0811h).** In general, user can plan the wanted channels by a CHN Look-Up-Table between master and slaves for two-way frequency hopping. Below is the LO frequency block diagram.

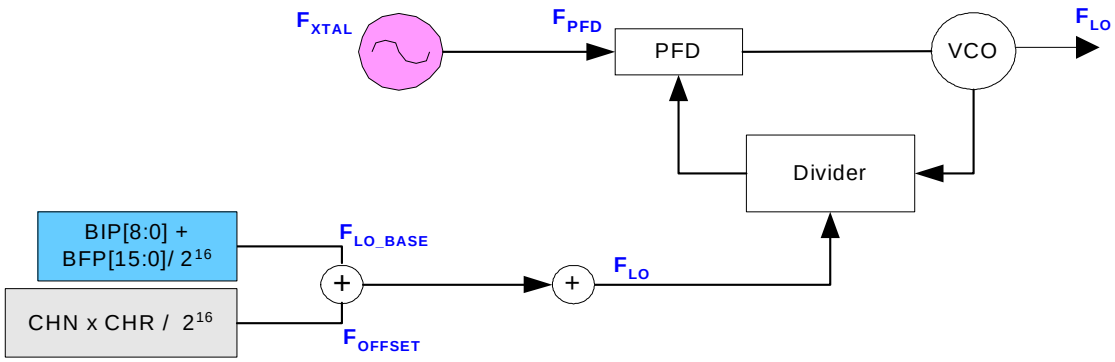


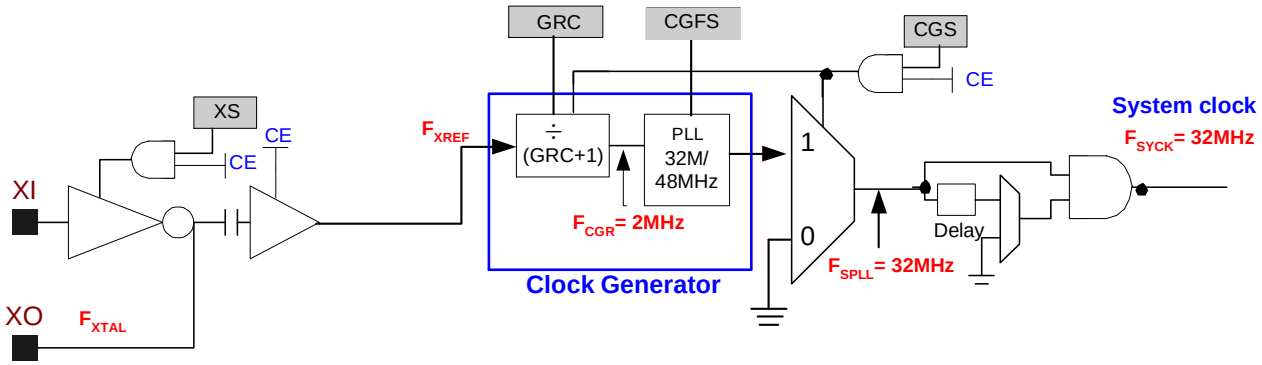
Figure 21.4 Block Diagram of Local Oscillator

21.5.1 RF Clock

The RF clock of A8125 (F_{SYCK}= 32 MHz) is generated by the PLL clock generator which reference frequency (F_{CGR}= 2MHz) is derived from frequency divider of crystal oscillator.

$F_{CGR} = \frac{F_{XREF}}{(GRC[3:0]+1)}$, where GRC [3:0] (0Eh) is the divide number to get F_{CGR} (2 MHz) from crystal oscillator.

Below is block diagram of system clock where F_{XTAL} is the crystal frequency. User can set XS, GRC, CGS to get F_{SYCK} = 32MHz. F_{XREF} is a reference clock to generate F_{CGR} = 2MHz and F_{SPLL} = 32MHz. After delay circuitry, F_{SYCK} (32MHz) is derived.



F_{XTAL}	F_{XREF}	F_{CGR}	GRC [3:0]	XS	CGS
16 MHz	16 MHz	Must be 2 MHz	[0111]	1	1

Figure 21.5 System Clock Block Diagram

A8125 supports programmable data rate by MDR [1:0] (0810h). Additional feature such as turbo mode (2Mbps @ MSK modulation) is implemented in this device. See below table for details.

F_{SYCK} (system clock)	MDR [1:0] (0810h)	CGFS[1:0] (0810h)	Turbo Mode
Reserved	[00]	[00]	Reserved
32 MHz	[01]	[01]	1 Mbps
32 MHz	[10]	[01]	2 Mbps
Reserved	[11]	[10]	Reserved

Table 12.1 Data Rate Configuration

21.5.2 LO Frequency Setting

To set up 2.4GHz LO Frequency (F_{LO}), user can refer to below 4 steps.

1. Set the base frequency (**F_{LO_BASE}**) by PLL Register II (0812h) and III (0813h).
   Recommend to set **F_{LO_BASE} ~ 2400.001MHz**.

2. Set channel step F_{CHSP} = 500KHz by PLL Register IV (0814h).

3. Set CHN [7:0] to get offset frequency by PLL Register I (0811h).
   F_{OFFSET} = CHN [7:0] * F_{CHSP}

4. LO frequency is equal to base frequency plus offset frequency.
   F_{LO} = F_{LO_BASE} + F_{OFFSET}

21.5.2.1 How to set F_{LO_BASE}

Regarding to LO frequency setting, Table 12.2 shows 2400.001 MHz base frequency by 16MHz Xtal.

STEP	ITEMS	VALUE	NOTE
1	F_{XTAL}	16 MHz	Crystal Frequency
2	BIP[7:0]	0x96	To get F_{LO_BASE} =2400 MHz
3	BFP[15:0]	0x0004	To get F_{LO_BASE} ~ 2400.001 MHz
4	F_{LO_BASE}	~2400.001 MHz	LO Base frequency

Table 12.2 How to configure F_{LO_BASE}

21.5.2.2 How to set $F_{LO} = F_{LO\_BASE} + F_{OFFSET}$

Regarding to frequency offset scheme, Table 12.3 shows IEEE 802.15.4 Channel 11 (2405.001 MHz) by 16MHz Xtal.

STEP	ITEMS	VALUE	NOTE
1	F_{LO_BASE}	~2400.001 MHz	After cofigure BIP and BFP
2	CHR[14:0]	0x0800	To get F_{CHSP}= 500 KHz
3	CHN[7:0]	0x0A	To set channel number = 10
4	F_{OFFSET}	5 MHz	To get F_{OFFSET}= 500 KHz * (CHN) = 5MHz
5	F_{LO}	~2405.001 MHz	To get F_{LO}= F_{LO_BASE} + F_{OFFSET}

Table 12.3 How to configure F_{LO}

21.5.3 Frequency Agility

A8125 supports frequency agility with a channel spacing of 5 MHz according to IEEE 802.15.4 and RF4CE specification. The center frequency of these channels is defined as follows:

CHN [7:0] PLL I (0811h)	Channel Number (IEEE 802.15.4)	Center Frequency (MHz)	Note
0x0A	11	2405	
0x14	12	2410	
0x1E	13	2415	
0x28	14	2420	
0x32	15	2425	RF4CE
0x3C	16	2430	
0x46	17	2435	
0x50	18	2440	
0x5A	19	2445	
0x64	20	2450	RF4CE
0x6E	21	2455	
0x78	22	2460	
0x82	23	2465	
0x8C	24	2470	
0x96	25	2475	RF4CE
0xA0	26	2480	

Table 12.4 Channel Assignment for IEEE 802.15.4 - 2.4 GHz Band

When the PLL is enabled during state transition from Standby to TX Ready, the settling time is typically 70 µs, including settling of PLL and Power Amplify. Switching from Standby to RX Ready is typically done 70 µs. This makes the radio transceiver highly suitable for frequency hopping applications.

IEEE 802.15.4	PDL	TDL [2:0]	Note

Operation Mode	(0835h)	(0835h)	
Slot	PDL = [10], 32 us	TDL = [100], 64 us	
Unslot	PDL = [10], 32 us	TDL = [100], 64 us	

Table 17 Settling time configuraiton for IEEE 802.15.4 operation modes.

21.6 Frame Filtering

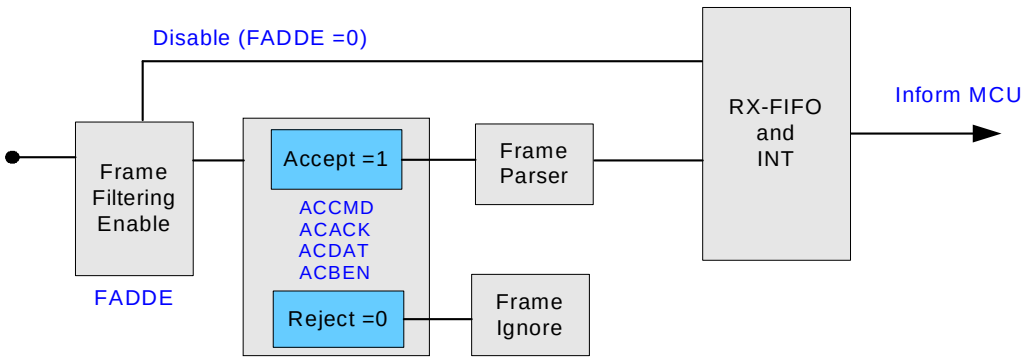
A8125 supports frame filtering to accept or to ignore coming packets regarding to frame type by setting (083Dh ~ 083Eh). User just needs to set PCORR (083Dh, 1 for coordinator and 0 for end device) and enable FADDE (083Dh). With different frame type filtering (Beacon or Command or Data or ACK) and consigned PAD_ID, Short Address and Long Address of specific IEEE 802.15.4 network into ADF Frame Registers (083Fh ~ 084Ah), The frame filtering function rejects non-intended frames, third filtering level, automatically identify valid packets to inform MCU to simplify IEEE 802.15.4 network complexity and MCU loading.

ADF control Register (Address: 083Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
083Dh	W	**FADDE**	**ACBEN**	**ACDAT**	**ACACK**	**ACCMD**	**ACRES**	**PCORR**	**MAXVER1**
Reset		1	1	1	1	1	1	0	0
083Eh	W	**MAXVER0**	**RESMUX2**	**RESMUX1**	**RESMUX0**	**--**	**--**	**--**	**--**
Reset		1	0	0	0	--	--	--	--

FADDE: MAC Address Filtering.
[0]: Disable. **[1]:** Enable.

PCORR: PAN Corrdinator.
[0]: End device. **[1]:** Corrdinator.



ADF Frame Register (Address: 083Fh ~ 084Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
083Fh	**W**	**PID15**	**PID14**	**PID13**	**PID12**	**PID11**	**PID10**	**PID9**	**PID8**
Reset		1	1	1	1	1	1	1	1
0840h	**W**	**PID7**	**PID6**	**PID5**	**PID4**	**PID3**	**PID2**	**PID1**	**PID0**
Reset		1	1	1	1	1	1	1	1
0841h	**W**	**SADD15**	**SADD14**	**SADD13**	**SADD12**	**SADD11**	**SADD10**	**SADD9**	**SADD8**
Reset		1	1	1	1	1	1	1	1
0842h	**W**	**SADD7**	**SADD6**	**SADD5**	**SADD4**	**SADD3**	**SADD2**	**SADD1**	**SADD0**
Reset		1	1	1	1	1	1	1	1
0843h	**W**	**LADD63**	**LADD62**	**LADD61**	**LADD60**	**LADD59**	**LADD58**	**LADD57**	**LADD56**
Reset		1	1	1	1	1	1	1	1
0844h	**W**	**LADD55**	**LADD54**	**LADD53**	**LADD52**	**LADD51**	**LADD50**	**LADD49**	**LADD48**

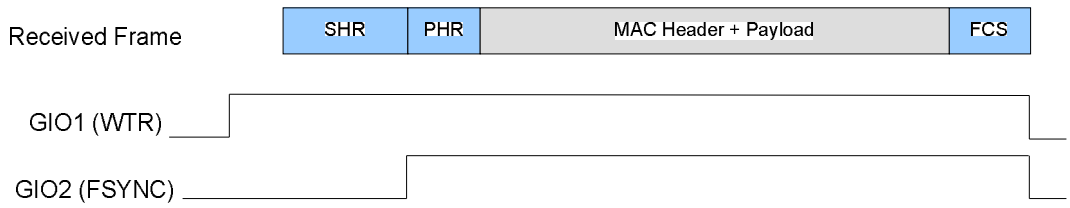
Reset		1	1	1	1	1	1	1	1
0845h	**W**	**LADD47**	**LADD46**	**LADD45**	**LADD44**	**LADD43**	**LADD42**	**LADD41**	**LADD40**
Reset		1	1	1	1	1	1	1	1
0846h	**W**	**LADD39**	**LADD38**	**LADD37**	**LADD36**	**LADD35**	**LADD34**	**LADD33**	**LADD32**
Reset		1	1	1	1	1	1	1	1
0847h	**W**	**LADD31**	**LADD30**	**LADD29**	**LADD28**	**LADD27**	**LADD26**	**LADD25**	**LADD24**
Reset		1	1	1	1	1	1	1	1
0844h	**W**	**LADD23**	**LADD22**	**LADD21**	**LADD20**	**LADD19**	**LADD18**	**LADD17**	**LADD16**
Reset		1	1	1	1	1	1	1	1
0849h	**W**	**LADD15**	**LADD14**	**LADD13**	**LADD12**	**LADD11**	**LADD10**	**LADD8**	**LADD8**
Reset		1	1	1	1	1	1	1	1
084Ah	**W**	**LADD7**	**LADD6**	**LADD5**	**LADD4**	**LADD3**	**LADD2**	**LADD1**	**LADD0**
Reset		1	1	1	1	1	1	1	1

PID[15:0]: PAN ID Storage.

SADD[15:0]: Short Address Storage.

LADD[63:0]: Long Address Storage.

Frame reception starts with detection of a start-of-frame delimiter (SFD), followed by the length byte. When the reception is completed, The FSYNC (Frame Sync, 080Dh or 080Eh), which can be output on GIO1 or GIO2, can be connected to a timer input on a MCU to capture the start of received frames.



Filtering Algorithm Map

Conditions								
FADDE = 1								
MAXVER [1:0]<= [01]								
RESMUX [9:7] = [000]								
Source and Destination address modes != [01]								
Beacon Frames Filtering	Data Frames Filtering			ACK Frames Filtering	MAC Command Frames Filtering			Reserved Frame Filtering
ACBEN = 1	ACDAT = 1			ACACK = 1	ACCMD = 1			ACRES = 1
Length byte >= 9	Length byte >= 9			Length byte = 5	Length byte >= 9			
Dest addr mode = 0	Dest addr mode = 0	Dest addr mode = 2	Dest addr mode = 3		Dest addr mode = 0	Dest addr mode = 2	Dest addr mode = 3	

source addr mode = 2 or 3	PAN COR = 1	Dest PAN ID = PID[15:0] or 0xFFFF	Dest PAN ID = PID[15:0] or 0xFFFF		PAN COR = 1	Dest PAN ID = PID[15:0 or 0xFFFF	Dest PAN ID = PID[15:0] or 0xFFFF	
source PAN ID = PID[15:0] or 0xFFFF	Source PAN ID = PID[15:0]	Dest addr = SADD[15:0] or 0xFFFF	Dest addr = LADD[63:0]		Source PAN ID = PID[15:0]	Dest addr = SADD[15:0] or 0xFFFF	Dest addr = LADD[63:0]	

FADDE (083Dh) bit controls whether frame filtering is applied or not. When disabled, A8125 will accept all received frames. When enabled (which is the default setting), A8125 will only accept frames that fulfill all of the following requirements:

-- The length byte must be equal to or higher than the “minimum frame length”, which is derived from the source and destination address mode and PAN ID compression subfields of the FCF.

-- The value of the frame version subfield of the FCF cannot be higher than MAXVER[1:0] (083Eh).

-- The source and destination address modes cannot be reserved values (1).

-- Destination address:
(1) If a destination PAN ID is included in the frame, it must match PANID[15:0] (083Fh ~ 0840h) or must be the broadcast PAN identifier (0xFFFF).

(2) If a short destination address is included in the frame, it must match either SADD[15:0] (0841h ~ 0842h) or the broadcast address (0xFFFF).

(3) If an extended destination address is included in the frame, it must match LADD[63:0] (0843h ~ 084Ah).

-- Frame type:
(1) Beacon frames (0) are only accepted when:
- ACBEN = 1 (083Dh)
- Length byte >= 9
- The destination address mode is 0 (no destination address)
- The source address mode is 2 or 3 (i.e. a source address is included)
- The source PAN ID matches PANID [15:0] (083Fh ~ 0840h), or PANID equals 0xFFFF

(2) Data (1) frames are only accepted when:
- ACDAT = 1 (083Dh)
- Length byte >= 9
- A destination address and/or source address is included in the frame. If no destination address is included in the frame, the PCORR = 1(31h) and the source PAN ID must equal PANID [15:0] (083Fh ~ 0840h).

-- Acknowledgment (2) frames are only accepted when:
- ACACK = 1 (083Dh)
- Length byte = 5

-- MAC command (3) frames are only accepted when:
- ACCMD = 1 (083Dh)
- Length byte >= 9
- A destination address and/or source address is included in the frame. If no destination address is included in the frame, PCORR = 1 (083Dh) and the source PAN ID must equal PANID [15:0] (083Fh ~ 0840h) for the frame to be accepted.

-- Reserved frame types (4, 5, 6 and 7) are only accepted when:
- ACRES = 1 (default is 0)
- Length byte >= 9

If a frame is rejected, A8125 will start searching a new frame once current frame is rejected.

The FSYNC (0Bh or 0Ch) will go high when start of frame delimiter is completely received and remains high until either the last byte in MPDU is received or the received frame has failed to pass address recognition and been rejected.

FSYNC can preferably be connected to a timer capture pin on MCU to extract timing information of transmitted and received data frames.

Tips and Tricks

The following register settings must be configured correctly:

• PCORR (083Dh) must be set if the device is a PAN coordinator, and cleared if not.
• RESMUX [9:7] must be [000].
• MAXVER[1:0] (083Dh) must correspond to the supported version(s) of the IEEE 802.15.4 standard.
• The local address information (PANID [15:0], SADD [15:0, LADD [63:0]) must be loaded into ADF Frame Register (083Fh ~ 084Ah).

During operation in a busy IEEE 802.15.4 environment, A8125 will receive large numbers of non-intended ACK frame. To effectively block reception of these frames, use ACK Frame Filtering (ACACK=0 (083Dh)).

Set ACACK = 1 after successfully starting a transmission with acknowledgment request, and clear the bit again after the acknowledgment frame has been received, or the timeout has been reached.

It is not necessary to turn off the receiver while changing the values of (083D ~ 083Eh) registers and (083Fh ~ 084Ah) register. However, **if the changes take place between reception of the SFD byte and the source PAN ID, the modified values will impact Frame Parser to induce errors.**

21.7 TX power setting

Please see reference code for more detail.

21.8 State machine

In chapter 9.2 and chapter 21.1, user can learn both accessing A8125's control registers as well as issuing Strobe commands.

21.8.1 Key states

A8125 supports 6 key operation states. Those are,
(1) Standby mode
(2) Sleep mode
(3) Idle mode
(4) PLL mode
(5) TX mode
(6) RX mode

After power on reset or software reset or deep sleep mode, user has to do calibration process because all control registers are in initial values. The calibration process of A8125 is very easy, user only needs to issue Strobe commands and enable calibration registers. After calibration, A8125 is ready to do TX and RX operation. User can start wireless transmission.

Strobe Command								Description
b7	b6	b5	b4	b3	b2	b1	b0	
1	0	0	0	x	x	x	x	Sleep mode
1	0	0	1	x	x	x	x	Idle mode
1	0	1	0	x	x	x	x	Standby mode

1	0	1	1	x	x	x	x	PLL mode
1	1	0	0	x	x	x	x	RX mode
1	1	0	1	x	x	x	x	TX mode

Mode	RF Register retention	RF Regulator	Xtal Osc.	VCO	PLL	RX	TX	Strobe Command
Sleep	Yes	ON	OFF	OFF	OFF	OFF	OFF	(1000-xxxx)b
Idle	Yes	ON	OFF	OFF	OFF	OFF	OFF	(1001-xxxx)b
Standby	Yes	ON	ON	OFF	OFF	OFF	OFF	(1010-xxxx)b
PLL	Yes	ON	ON	ON	ON	OFF	OFF	(1011-xxxx)b
TX	Yes	ON	ON	ON	ON	OFF	ON	(1101-xxxx)b
RX	Yes	ON	ON	ON	ON	ON	OFF	(1100-xxxx)b

Remark: x means “don’t care”

Table 15.1. Operation mode and strobe command

21.8.2 FIFO mode

This mode is suitable for the requirements of general purpose applications and can be chosen by setting FMS = 1. After calibration, user can issue Strobe command to enter standby mode where write TX FIFO or read RX FIFO. From standby mode to packet data transmission, only one Strobe command is needed. Once transmission is done, A8125 is auto back to standby mode. Figure 21.6and Figure 21.7are TX and RX timing diagram respectively. Figure 21.8 illustrates state diagram of FIFO mode.

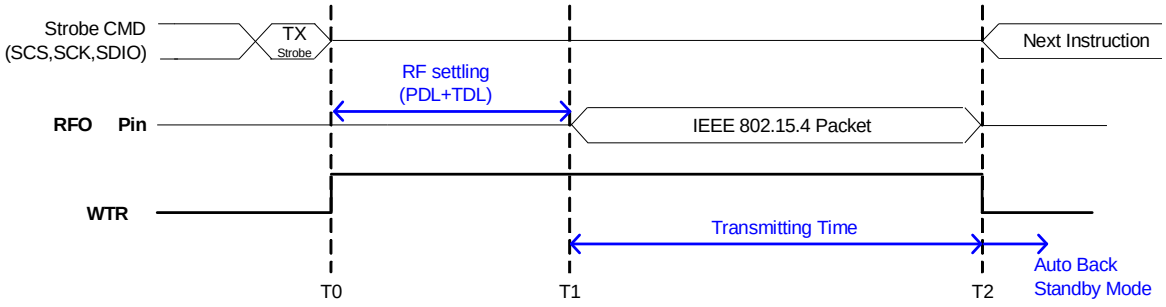


Figure 21.6TX timing of FIFO Mode

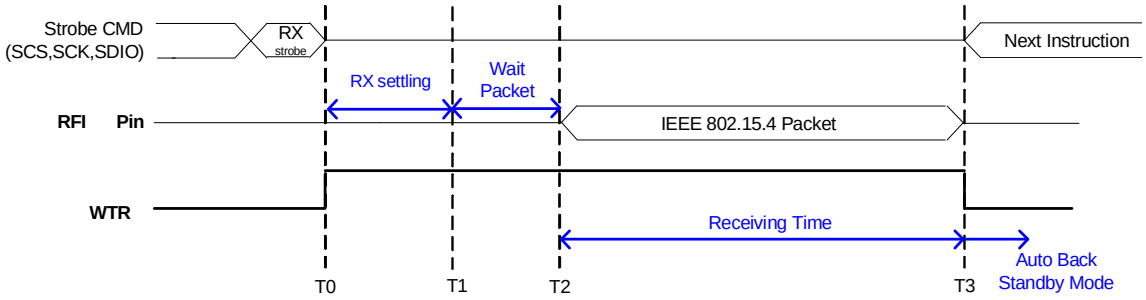


Figure 21.7 RX timing of FIFO Mode

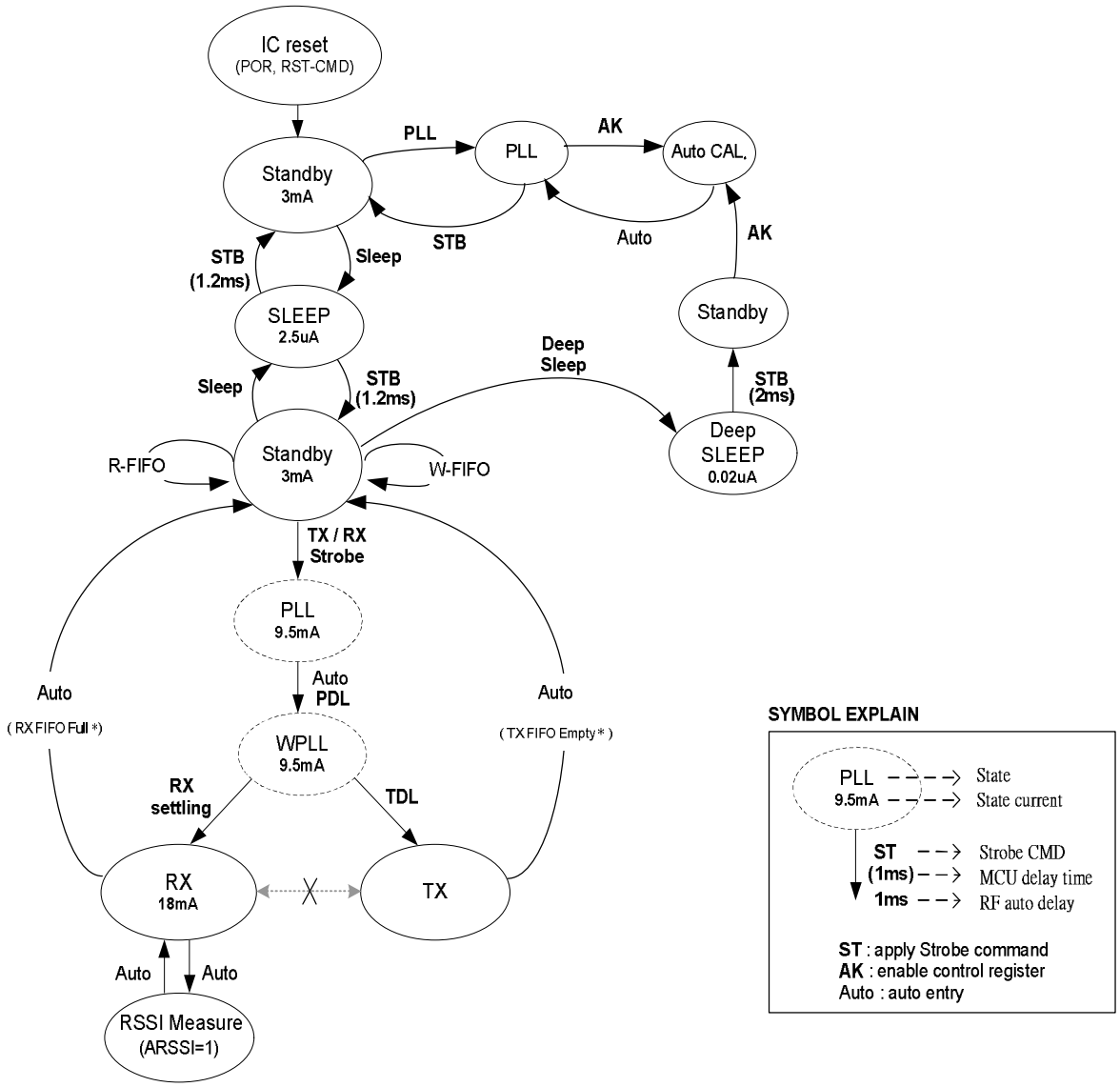


Figure 21.8 State diagram of FIFO Mode

21.10 Pseudo Random Number Generator

A8125 supports hardware 16-bits pseudo random number generator for several purposes like

1. be used to generate random keys used for security.
2. be used to generate PAN_ID or short address.
3. be used to generate the seed of Random MAC Back-off timer.

Mode Select Register (Address: 0803h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	DLS	PNS	PNIVS	ACKS	ARTS	CSMAS	SLOT

Reset		--	0	0	0	1	0	1	0

PNIVS: PN initial seed select. Recommend PNIVS = [0].
[0]: Use RF calibration value. [1]: Manual setting by PNIV (35h).

PNG Register I、II(Address: 084Dh~084Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
084Dh	R	PNO15	PNO14	PNO13	PNO12	PNO11	PNO10	PNO9	PNO8
	W	PNIV15	PNIV14	PNIV13	PNIV12	PNIV11	PNIV10	PNIV9	PNIV8
Reset		0	1	1	1	0	0	0	1
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
084Eh	R	PNO7	PNO6	PNO5	PNO4	PNO3	PNO2	PNO1	PNO0
Reset	W	PNIV7	PNIV6	PNIV5	PNIV4	PNIV3	PNIV2	PNIV1	PNIV0
Reset		0	1	0	1	0	0	1	1

PNO [15:0]: 16-bits Random number generator output.

PNIV [15:0]: Initial value of 16-bits Random number generator.

How to get a 16-bits pseudo random number

Step1:Initial RF.
Step2:choose a source to be the seed of PN generator by PNIVS (00803h).
Step3:write a 16-bits seed (non-zero) into PNG Register (084Dh ~ 084Eh).
Step4:Read a 16-bits random number from PNG Register (084Dh ~ 084Eh).

Remark:
1. A8125 will always read the same 16-bits random number if it is in RX mode.

21.11 RF Interrupt

A8125 integrates the many RF events to interrupt MCU in RFINT. User can save MCU computing power by RF interrupt. As shown as the figure 20.11, RFINT event are including TWOR, WOR, ADCM, EDS, CCAS, ARTE, WTR and CSMAS signals. RF INT vector is located in 0x53 and user can put an interrupt service routine in 0x53. Except WOR and TWOR signal, other signals can be output to GIO1 or GIO2 by GIO1S (080Dh) or GIO2S (080Eh) setting. Please refer Figure 21.11,

When RF interrupt occurs, user can check IST[3:0] (083Ch) to know which one source trigger RF interrupt and check INTF to know the status of respective function. For example, IST[3:0]= 0001b,it is trigger by WTR signal. If RF is in RX mode, the status of INTF equals CRCF status. It is convenient for user and read the Interrupt Status Register (083Ch) once to know the interrupt source and the relative status.

Interrupt State Register (Address: 083Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	**ISTRN**	**--**	**CCAM1**	**CCAM0**	**ERX**	**EDS**	**CCAS**	**--**
	R	**INT**	**IST3**	**IST2**	**IST1**	**IST0**	**EDS**	**CCAS**	**INTF**
Reset		0	--	0	1	0	0	0	--

ISTRN: Interrupt state reset. (write only). Recommend ISTRN = [0].
[1]: Reset interrupts sources. Auto clear when done.

INT: Interrupt source state.
[0]: None. **[1]:** Busy.

IST[3:0]: Interrupt source select.

INTF: Interrupt flag.
INTF status is shown as the respective function as the below table.

IST[3:0]	Interrupt source	INTF (Bit 0)	Note
0000	none	none	

0001	WTR	CRCF	
0010	CSMA_CA	CSMAF	
0011	CCA	CCAF	
0100	ART	Reserved	
0101	EDM	None	
0110	FPF	FPF	
0111	ADCM	None	
1000	WOR	CRCF	
1001	TWOR	None	

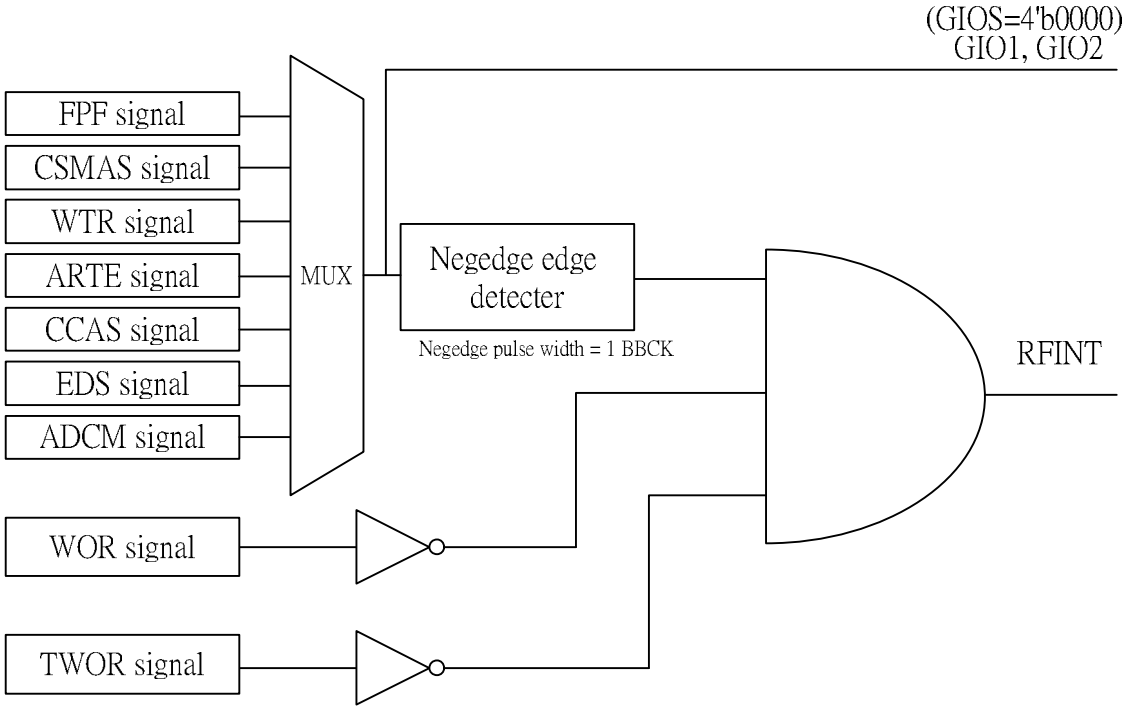


Figure 21.11 RF interrupt source

22. Flash memory controller

SFR RELATED REGISTERS

FLASH memory is controlled using PCON(0x87)'s PWE bit, FLASHCTRL(0x9A) and FLASHTMR (0x9B). An SFR register named FLASHCTRL (0x9A) is used to control communication between MCU and flash. FLSHCTRL(0x9A) is consisted of 6bits used to control all FLASH related operations. Lower five bits of FLSHTMR (0x9B) named FREQ[4:0] determine real CLK frequency with 1MHz step resolution. FREQ[4:0] after reset is set to 20MHz by default, provides optimal timing for flash macro. Please contact AMICCOM FAE for more details flash operation reference code.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9Ah FLSHCTRL	R/W	CTRL.7	CTRL.6	CTRL.5	CTRL.4	CTRL.3	CTRL.2	CTRL.1	CTRL.0
Reset		0	0	0	0	0	0	0	0

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9Bh FLSHTMR	R/W				Fewq.4	Fewq.3	Fewq.2	Fewq.1	Fewq.0
Reset		0	0	0	0	0	0	0	0

FREQ[4:0]	Frequency MHz
0x00	-
0x01	1
0x02	2
...	...
0x14	20

Table 3. FREQ intervals

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9Ch FLSHTPG	R/W								
Reset		0	0	1	0	0	1	1	1

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9Dh FLSHTER	R/W								
Reset		1	1	1	1	1	0	0	1

Setting higher clock frequency is not supported since given Flash macro has limited its clock frequency up to 20MHz by Tkp read cycle time. FLASHCTRL register is write protected by TA enable procedure listed below:

```
CLR  EA ;disable interrupt system
MOV TA, #0xAA
MOV TA, #0x55
MOV FLASHCTRL,#<value> ; Any direct addressing instruction writing FLASHCTRL register.
  SETB  EA  ;Enable interrupt system
```

The Program Write Enable (PWE) bit, located in PCON register, is used to enable/ disable PRGROMWR and PRGRRAMWR pin active during MOVX instructions.

PCON (087h) Power control

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
87h PCON	R/W	SMOD	-	-	PWE	-	SWB	STOP	CKSE
Reset		0	0	0	0	0	0	0	0

When PWE bit is set to logic 1, the MOVX @DPTR,A instruction writes data located in accumulator register in to Program Memory addressed by DPTR register (active: DPH:DPL). The MOVX @ Rx,A instruction writes data located in accumulator register into program memory addressed by P2 register (bit 15:8) and Rx register (bit 7:0). Program Memory can be read by MOVC only regardless of PWE bit.

CHIP ERASE OPERATION

Chip erase operation is enabled by setting CTRL[5:0]=0x04 of FLSHCTRL register according to MCU TA enable procedure. PCON.PWE bit must be also set, then first MOVX instruction writing to program memory space at address belong to certain FLASH macro begins sector erase operation. During erase operation MCU is halted by asserting FLASHBUSY pin. When FLASH macro is blank and ready for new programming. To erase another FLASH macro, the whole procedure needs to be repeated with change MOVX address pointing to certain FLASH macro. Preprogramming of whole FLASH macro is executed automatically without any interaction with user, before real chip erase. It extends lifecycle of FLASH macro.

SECTOR ERASE OPERATION

The 16KB Flash macro has 129 sectors (128Bytes each) which can be erased separately. Sector erase operation is enabled by setting CTRL[5:0] = 0x22 of FLSHCTRL register according to MCU TA enable procedure. PCON.PWE bit must be also set. The first MOVX instruction writing to program memory space at selected sector address begins sector erase operation. During sector erase operation, MCU is gated by asserting FLASHBUSY pin. When sector has been erased, FLASHBUSY pin is deactivated and FNOP is automatically written. MCU executes next instruction. Selected FLASH macro sector(s) is blank and ready for new programming. To erase another sectors whole procedure needs to be repeated. Programming of whole sector is executed automatically without any interaction with user, before real erase. It extends lifecycle of FLASH macro.

PROGRAM OPERATION

Word program operation is enabled by setting CTRL[5:0]=0x01 of FLSHCTRL register according to MCU TA enable procedure. PCONE.PWE bit must be set too, then each write to program memory space by MOVX instruction addressing odd bytes begins word program operation. During program operation MCU is halted by asserting FLASHBUSY pin. When word has been programmed FLASHBUSY pin is deactivated. MCU executes next instruction which can be (i) programming of next memory word (ii) CTRL[5:0] = 0x00 according to MCU TA enable procedure. Number of programmed by bytes must be always even number(2,4,6…) . For example to program byte at address 0x003, first must be written byte at address 0x002 then second MOVX instruction write at address 0x003 begins physical write to FLASH macro. When number of programmed bytes is not even then it must be filled with extra neutral byte. The neutral bytes does not program any bit in a FLASH macro.
Note: Flash memory can programmed once. Please erase sector firstly if change the content in the flash memory.

23. In Circuit Emulator (ICE)

A8125 support In Circuit Emulator on chip. It is a real-time hardware debugger as a non-intrusive system. It doesn't need to occupy any hardware resource such as the UART and Timer. User develops firmware complete producing code without any modification using ICE. It helps user to track down hidden bugs within the application running with microcontroller. The ICE with Hardware USB dongle provides a powerful SOC development tool with silicon using 2-wire protocol. The ICE fully supports Keil uVision2/3/4 interface to hardware debuggers. It allows Keil software user to work with uvision2/3/4. For more detail information, please reference Application note.

23.1 PIN define

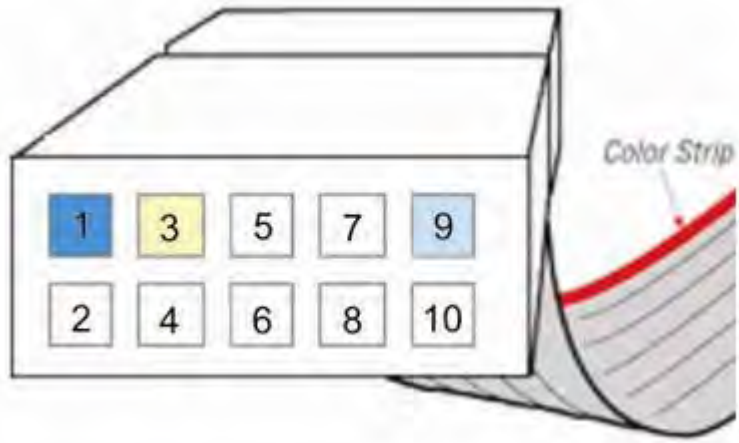


Fig 22.1 The USB connectors

Pin	Signal name	Description	Pin	Signal name	Description
1	ttck	Clock signal (in)	2	GND	Signal Ground
3	ttdio	Data (io)	4	VCCIO	Used to VCCIO detection
5	NU	Do not use	6	NU	Do not use or connect
7	NU	Do not use	8	NU	Do not use or connect
9	rsto	Reset output (od)	10	GND	Signal Ground

Fig22.2 The Pin define within USB connector

Note: RSTO pin is open drain (od) type active low. It forces logic zero to issue reset. When RSTO is inactive its output is floating, and should be connected to global system reset with pull-up resistor. This pin can be left unconnected.

There are 10 pin in the ICE connectors. 2-wire ICE only use 2 pins (PIN1 and PIN3). The PIN9 is optional and it can connect reset signal. PIN2 and PIN10 are GND pin. PIN4 is VCCIO pin. The recommended circuit shows as the below figure. (Fig21.3). There is a resister (100 ohm) between A8510 and pin connected the connector.

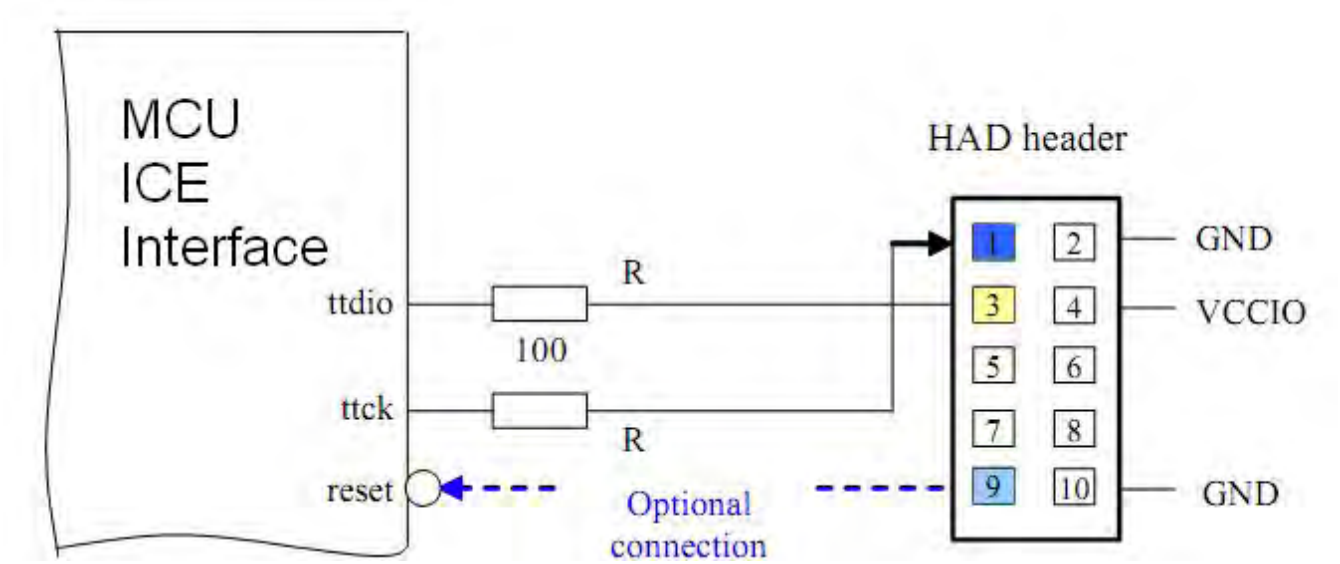


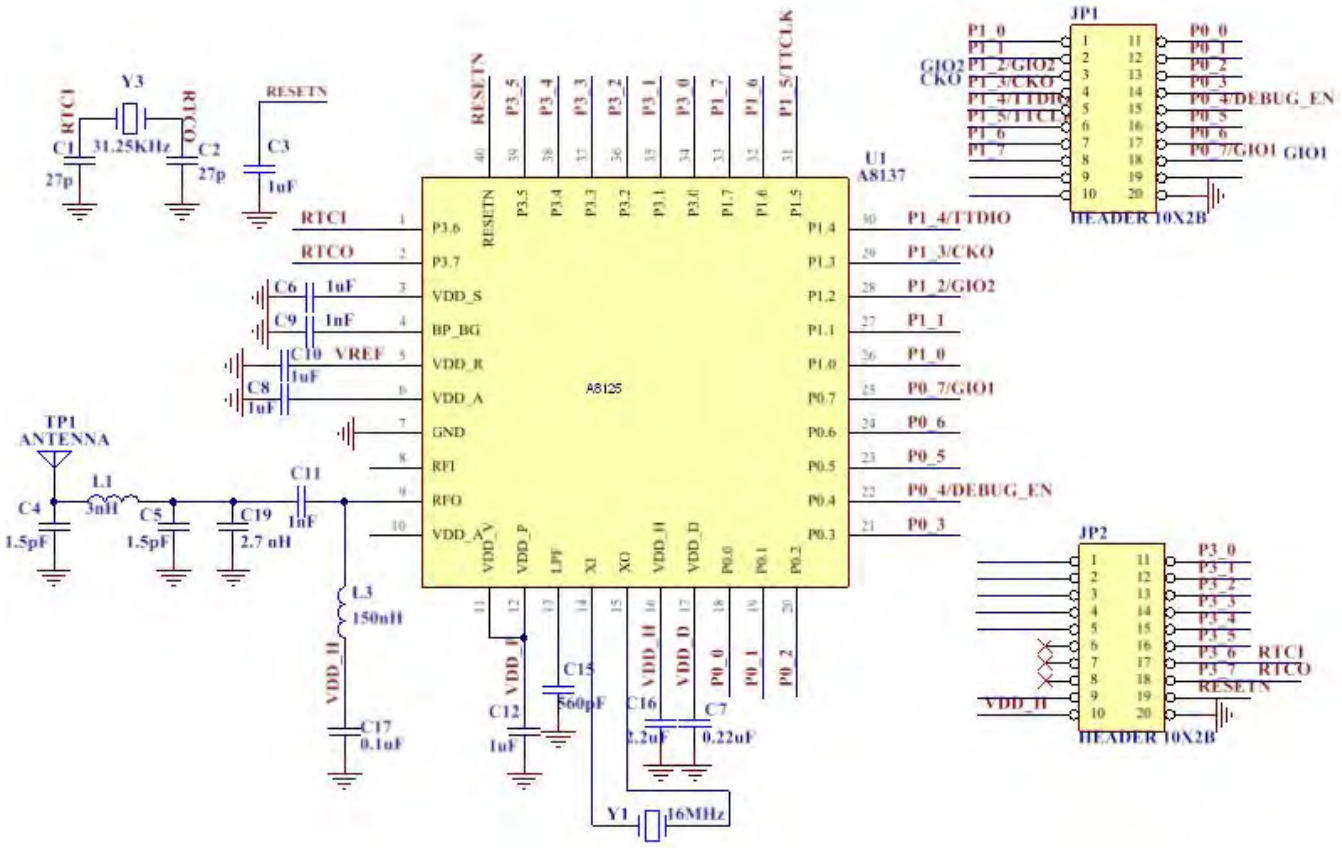
Fig 22.3 The connections between A8125 and USB connectors

23.2 ICE Key feature

The ICE supports source level debugging, 2 hardware breakpoint, auto refresh of all register and In system programming (ISP). User can use ICE to download firmware by Keil software or AMICCOM tool.

24. Application circuit

Below is AMICCOM's reference application circuit. Please refer A8125 module specification for more details.



25. Abbreviations

ADC	Analog to Digital Converter
AIF	Auto IF
FC	Frequency Compensation
AGC	Automatic Gain Control
BER	Bit Error Rate
BW	Bandwidth
CD	Carrier Detect
CHSP	Channel Step
CRC	Cyclic Redundancy Check
DC	Direct Current
FEC	Forward Error Correction
FIFO	First in First out
FSK	Frequency Shift Keying
ID	Identifier
ICE	In Circuit Emulator
I^2C	Inter-Integrated Circuit
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PFD	Phase Frequency Detector for PLL
PLL	Phase Lock Loop
POR	Power on Reset
PWM	Pulse width modulation
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXRF	Transmitter Radio Frequency
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

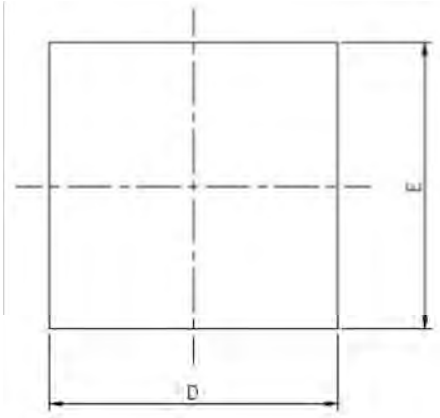
26. Ordering Information

Part No.	Package	Units Per Reel / Tray
A81X25F4000AQ5A/Q	QFN40L, Pb Free, Tape & Reel, -40℃～85℃	3K
A81X25F4005AQ58/Q	QFN32L, Pb Free, Tape & Reel, -40℃～85℃	3K
A81X25F4000AQ5A	QFN40L, Pb Free, Tray, -40℃～85℃	490EA
A81X25F4005AQ58	QFN32L, Pb Free, Tray, -40℃～85℃	490EA

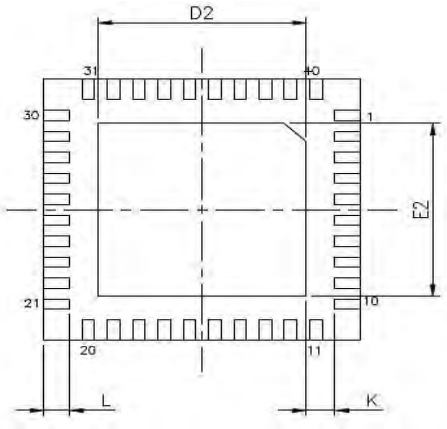
27. Package Information

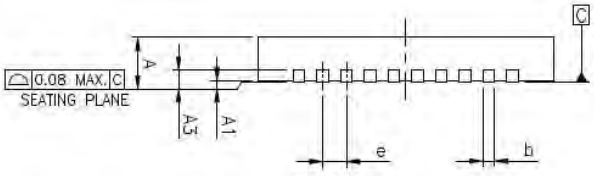
QFN 40L (5 X 5 X 0.8mm) Outline Dimensions

Top View



Bottom View



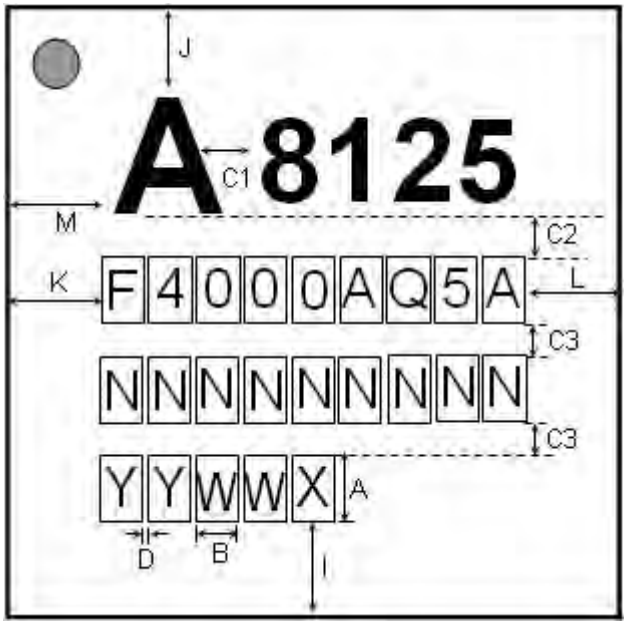


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.031	0.70	0.75	0.80
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3		0.008 REF			0.20 REF	
b	0.006	0.008	0.010	0.15	0.20	0.25
D	0.194	-	0.200	4.924	-	5.076
D_2	0.126	-	0.138	3.20	-	3.50
E	0.194		0.200	4.924		5.076
E_2	0.126	-	0.138	3.20	-	3.50
e		0.016			0.40	
L	0.013	0.016	0.019	0.324	0.40	0.476
k		0.008			0.2	

28. Top Marking Information

- Part No. : **A81X25F4000AQ5A**
- Pin Count : **40**
- Package Type : **QFN**
- Dimension : **5*5 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**

TOP MARKING LAYOUT:



❖ CHARACTER SIZE : (Unit in mm)

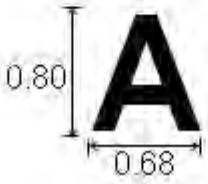
A : 0.55
B : 0.36
C1 : 0.25　C2 : 0.3　C3 : 0.2
D : 0.03
M : 1.5

YYWW : DATECODE

X : PKG HOUSE ID

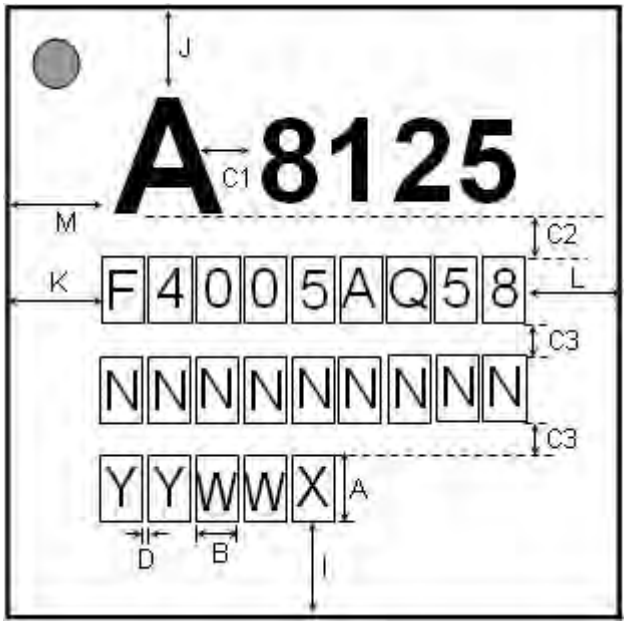
NNNNNNNNN : LOT NO.
(max. 9 characters)

I=J
K=L



- Part No. : **A81X25F4005AQ58**
- Pin Count : **32**
- Package Type : **QFN**
- Dimension : **5*5 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**

TOP MARKING LAYOUT:



❖ CHARACTER SIZE : (Unit in mm)

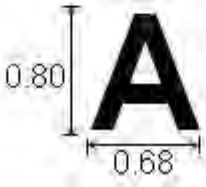
A : 0.55
B : 0.36
C1 : 0.25　C2 : 0.3　C3 : 0.2
D : 0.03
M : 1.5

YYWW : DATECODE

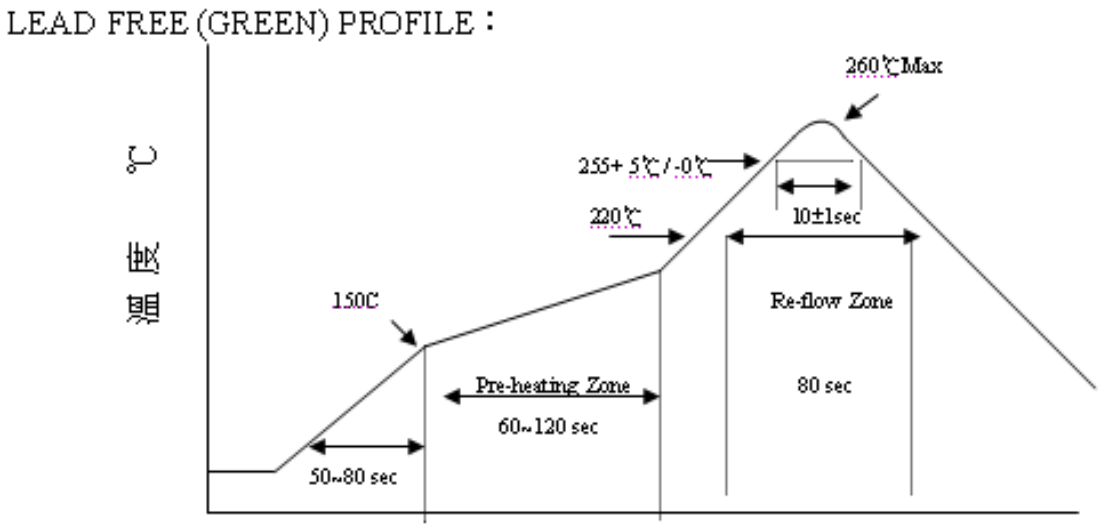
X : PKG HOUSE ID

NNNNNNNNN : LOT NO.
(max. 9 characters)

I=J
K=L



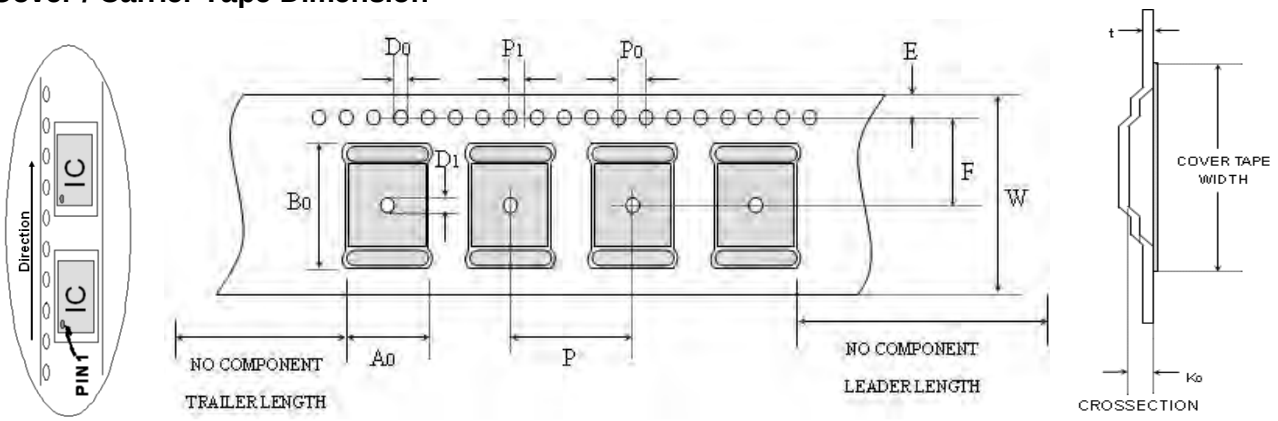
29. Reflow Profile



Actual Measurement Graph

30. Tape Reel Information

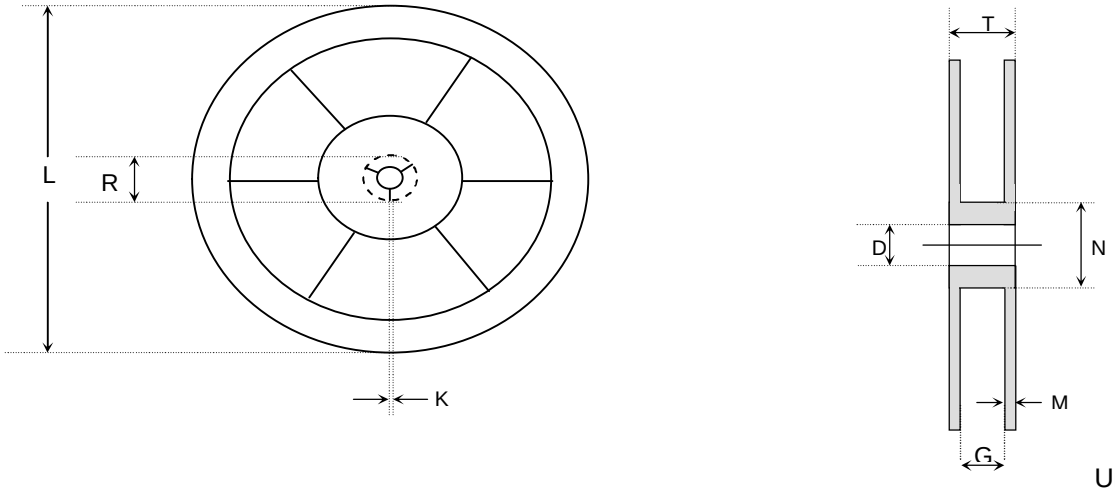
Cover / Carrier Tape Dimension



Unit: mm

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W	K0	t	Cover tape width
QFN3*3	8±0.1	3.25±0.1	3.25±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75±0.1	5.5±0.05	12±0.3	1.25±0.1	0.3±0.05	9.3±0.1
QFN 4*4	8±0.1	4.35±0.1	4.35±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75±0.1	5.5±0.05	12±0.3	1.25±0.1	0.3±0.05	9.3±0.1
QFN 5*5	8±0.1	5.25±0.1	5.25±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75±0.1	5.5±0.05	12±0.3	1.25±0.1	0.3±0.05	9.3±0.1
SSOP	12±0.1	8.2±1	8.8±1.5	4.0±0.1	2.0±0.1	1.5±0.1	1.5±0.1	1.75±0.1	7.5±0.1	16±0.1	2.1±0.4	0.3±0.05	13.3±0.1

REEL DIMENSIONS



Unit: mm

TYPE	G	N	M	D	K	L	R
QFN	12.9±0.5	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9
SSOP	16.3±1	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9

31. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.