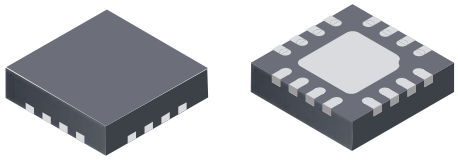
High Current Photoflash Capacitor Charger with IGBT Driver for Two Li+ Batteries

Features and Benefits

- Wide battery voltage range: 1.5 to 11 V
- Integrated 55 V DMOS switch in very thin profile 3 mm × 3 mm, 0.75 mm nominal height package
- Peak current limit continuously adjustable from 1.0 to 3.2 A
- Output voltage sensing on primary side: no resistor divider required
- >75% efficiency
- Fast charge time
- Charge Complete indication
- Flexible, high current IGBT drive
- Independent IGBT driver supply
- Separate sink and source pins with 6 Ω pull-up and 20 Ω pull-down
- Interlocked trigger pin improves noise immunity
- No primary-side Schottky diode needed

Package: 16-contact TQFN (suffix ES)



Approximate Scale 1:1

Description

The A8425 charges photoflash capacitors for digital cameras, camcorders, and DSC combos. An integrated 55 V DMOS switch drives the transformer in a flyback topology optimized for 2-cell Li+ battery input. An integrated IGBT driver with separate source and sink pins allows high performance red-eye reduction implementation.

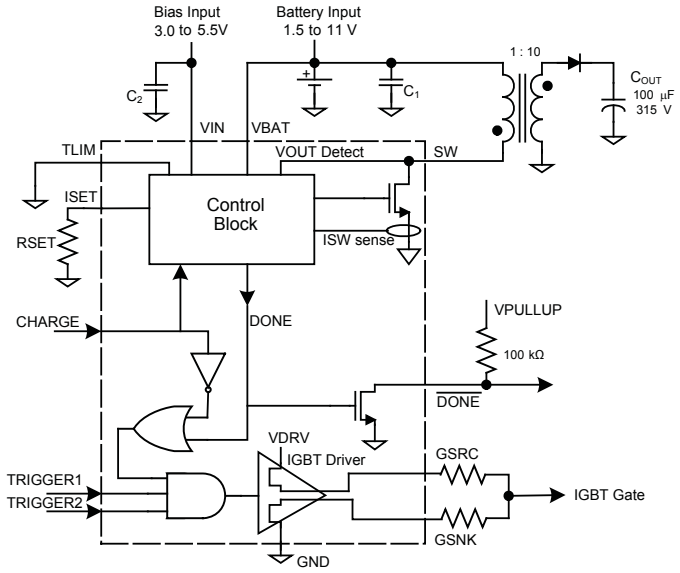
The A8425 offers programmable peak switch current limit from 1.0 to 3.2 A, continuously adjustable using a resistor to ground. A proprietary control scheme optimizes the capacitor charging time. Low quiescent current and low shutdown current further improve system efficiency and extend battery life.

The A8425 is available in 16-contact 3 mm × 3 mm TQFN packages. This small, very thin profile (0.75 mm nominal overall height) package is ideal for space-constrained applications. It is lead (Pb) free, with 100% matte-tin leadframe plating.

Applications include:

- SLR camera flash
- Digital camcorder/DSC combo flash
- 2 Li+ input strobe

Typical Application



Selection Guide

Part Number	Packing*
A8425EESTR-T	Tape and reel, 1500 pieces/reel

*Contact Allegro for additional packing options.

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Units
SW Pin	V_{SW}		–0.3 to 55	V
VBAT Pin	V_{BAT}		–0.3 to 12	V
VIN Pin	V_{IN}		–0.3 to 7	V
Remaining Pins			–0.3 to V_{IN} + 0.3 V	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

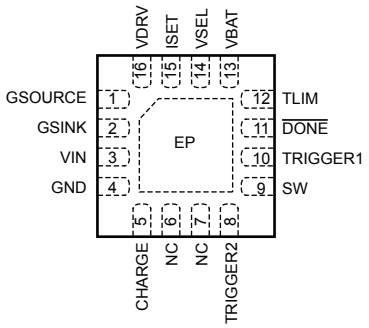
*With respect to GND.

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	47	ºC/W

*Additional thermal information available on Allegro website.

Pin-out Diagram

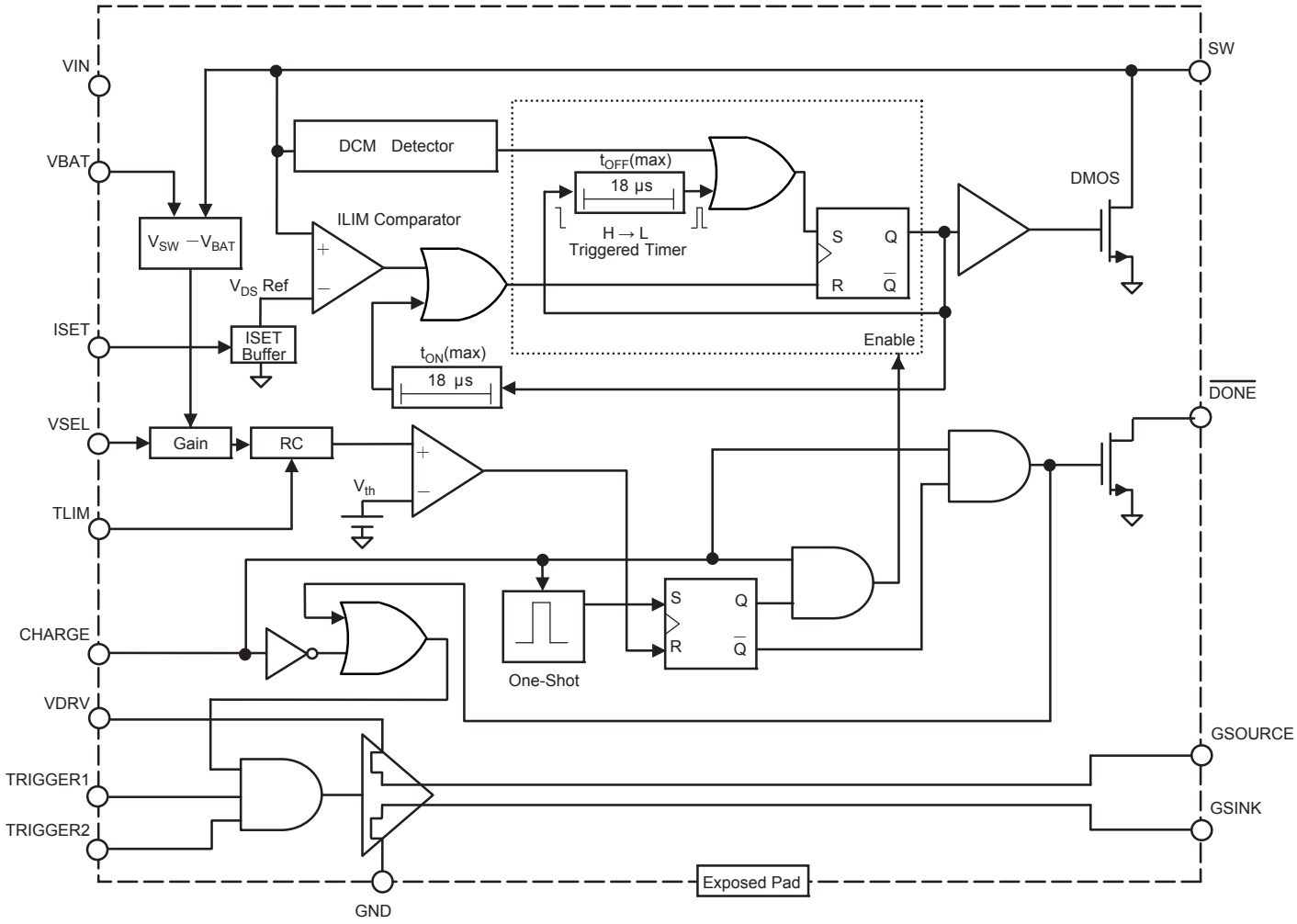


(Top View)

Terminal List Table

Number	Name	Function
1	GSOURCE	IGBT gate drive – source connection
2	GSINK	IGBT gate drive – sink connection
3	VIN	Input voltage; connect to a 3.0 to 5.5 V voltage source
4	GND	Ground connection
5	CHARGE	Pull high to initiate charging; pull low to enter low-power standby mode
6, 7	NC	No connection
8	TRIGGER2	IGBT input trigger 2; internally ANDed with TRIGGER1 pin
9	SW	Drain connection of internal power MOSFET switch; connect to the other terminal of the transformer primary winding
10	TRIGGER1	IGBT input trigger 1; internally ANDed with TRIGGER2 pin
11	$\overline{\text{DONE}}$	Pulls low when output reaches target value and CHARGE pin is high; remains low until CHARGE pin is cycled
12	TLIM	Sets time limit for minimum pulse width (secondary-side conduction time); apply logic high for shorter pulses or logic low for longer pulses; see Selection of Transformer section for details
13	VBAT	Battery voltage; connect to the same power supply as is used for the transformer primary winding
14	VSEL	Output voltage selection; use in conjunction with transformers of differing turns ratios (N = 8, 9, or 10) to achieve target output voltage and optimal efficiency (this feature is not yet finalized)
15	ISET	Sets the maximum switch current; connect an external resistor (value of 25 to 80 kΩ) between this pin and GND to set the target peak current (between 1.0 and 3.2 A)
16	VDRV	Supply for IGBT gate driver
–	EP	Exposed pad for enhanced thermal dissipation (not connected electrically)

Functional Block Diagram



ELECTRICAL CHARACTERISTICS typical values valid at V_{IN} = V_{BAT} = 3.6 V, R_{SET} = 40 kΩ, I_{SWlim} = 2.0 A, and T_A = 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBAT Pin Voltage Range[1]	V_{BAT}		1.5	–	11	V
VIN Pin Voltage Range[1]	V_{IN}		3.0	–	5.5	V
UVLO Enable Threshold	V_{INUV}	V_{IN} rising	2.55	2.65	2.75	V
UVLO Hysteresis	$V_{INUVhys}$		–	150	–	mV
Switch Current Limit[2]	$I_{SWlimMAX}$	Maximum, I_{SET} = 55 µA	2.9	3.2	3.5	A
	$I_{SWlimMIN}$	Minimum, I_{SET} = 17 µA	–	1.0	–	A
SW Current Limit to ISET Current Ratio	I_{SWlim}/I_{SET}	I_{SET} = 55 µA, CHARGE = high	–	58.5	–	kA/A
ISET Pin Voltage While Charging	V_{SET}	I_{SET} = 55 µA, CHARGE = high, I_{SW} = 0 A (VBAT disconnected)	–	1.182	–	V
		I_{SET} = 55 µA, CHARGE = high, I_{SW} = 3.2 A	–	1.268	–	V
ISET Pin Internal Resistance	$R_{SET(INT)}$		–	330	–	Ω
GND Pin Internal Resistance	$R_{GND(INT)}$		–	27	–	mΩ
Switch On-Resistance	$R_{SWDS(on)}$	V_{IN} = 3.6 V, I_D = 800 mA, T_A = 25°C	–	0.2	–	Ω
Switch Leakage Current[1]	I_{SWlk}	V_{SW} = V_{BAT} = 11 V, in shutdown	–	–	1	µA
VIN Pin Supply Current	I_{IN}	Shutdown (CHARGE = 0 V, TRIGGER = 0 V	–	0.01	1	µA
		Charging done	–	25	50	µA
		Charging (CHARGE = V_{IN}, TRIGGER = 0 V)	–	2	–	mA
VBAT Pin Supply Current	I_{BAT}	Shutdown (CHARGE = 0 V, TRIGGER = 0 V)	–	0.01	1	µA
		Charging done	–	–	1	µA
		Charging (CHARGE = V_{IN}, TRIGGER = 0 V)	–	25	50	uA
CHARGE Pin Input Current	I_{CHARGE}	V_{CHARGE} = V_{IN}	–	36	–	µA
CHARGE Pin Input Voltage High[1]	$I_{CHARGE(H)}$	Over input supply range, V_{IN}	1.4	–	–	V
CHARGE Pin Input Voltage Low[1]	$I_{CHARGE(L)}$	Over input supply range, V_{IN}	–	–	0.4	V
CHARGE Pin Pull-down Resistor	R_{CHARGE}		–	100	–	kΩ
Maximum Switch-off Timeout	t_{offMAX}		–	18	–	µs
Maximum Switch-on Timeout	t_{onMAX}		–	18	–	µs
$\overline{\text{DONE}}$ Pin Output Leakage Current[1]	I_{DONElk}		–	–	1	µA
$\overline{\text{DONE}}$ Pin Output Low Voltage[1]	V_{DONEL}	32 µA into $\overline{\text{DONE}}$ pin	–	–	100	mV
Output Comparator Trip Voltage (measured as V_{SW} – V_{BAT}; see [1] for VSEL= GND)	$V_{OUTTRIP}$	VSEL = GND	31	31.5	32	V
		VSEL = open	–	35	–	V
		VSEL = VIN	–	39.4	–	V
Output Comparator Overdrive	V_{OUTOV}	200 ns pulse width (90% to 90%)	–	200	400	mV
Minimum dV/dt for ZVS Comparator	dV/dt	Measured at SW pin	–	20	–	V/µs

Continued on the next page …

ELECTRICAL CHARACTERISTICS (continued) typical values valid at V_{IN} = V_{BAT} = 3.6 V, R_{SET} = 40 kΩ, I_{SWlim} = 2.0 A, and T_A=25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
IGBT Driver						
VDRV Pin IGBT Driver Supply Voltage	V_{DRV}		3	–	5.5	V
TRIGGERx Pins Input Current	I_{TRIG}	$V_{TRIGGER}$ = V_{IN}	–	36	–	µA
TRIGGERx Pins High Input Voltage[1]	$V_{TRIG(H)}$	Over input supply range, V_{IN}	1.4	–	–	V
TRIGGERx Pins Low Input Voltage[1]	$V_{TRIG(L)}$	Over input supply range, V_{IN}	–	–	0.4	V
TRIGGERx Pins Pull-down Resistor	R_{TRIGPD}		–	100	–	kΩ
GSOURCE On-Resistance to VDRV	$R_{SrcDS(on)}$	V_{DRV} = 3.6 V, $V_{GSOURCE}$= 1.8 V	–	6	–	Ω
GSINK On-Resistance to GND	$R_{SnkDS(on)}$	V_{DRV} = 3.6 V, V_{GSINK}= 1.8 V	–	20	34	Ω
Propagation Delay (Rising)	t_{dr}	Connect GSOURCE to GSINK, R_{GATE} = 12 Ω, C_{LOAD} = 6500 pF, V_{DRV} = 3.6 V	–	30	–	ns
Propagation Delay (Falling)	t_{df}		–	140	–	ns
Output Rise Time	t_r		–	80	–	ns
Output Fall Time	t_f		–	320	–	ns

[1]Specifications over the range T_A= –40°C to 85°C; guaranteed by design and characterization.
[2]Current limit guaranteed by design and correlation to static test. Refer to Application Information section for peak current in actual circuits.

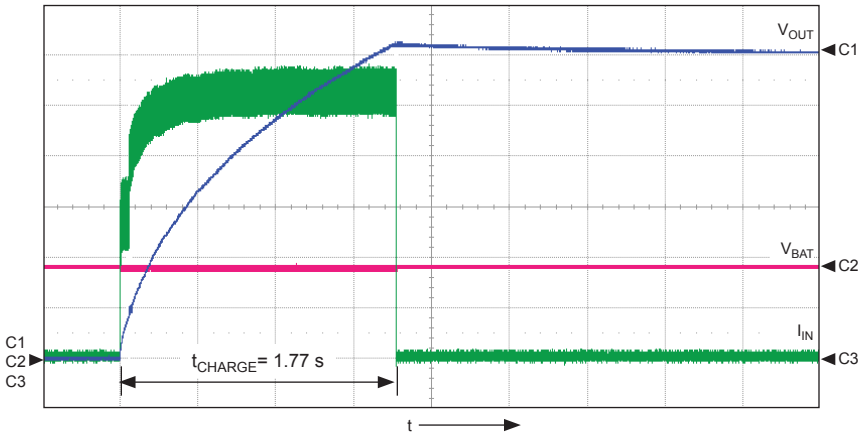
Performance Characteristics

Charging Time at Various Peak Current Levels

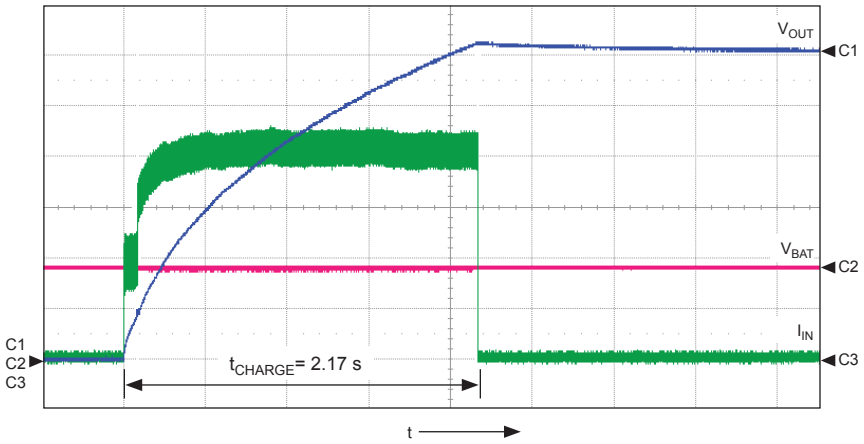
Common Parameters		
Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	V_{BAT}	2 V
C3	I_{IN}	250 mA
t	time	500 ms
Conditions	**Parameter**	**Value**
	V_{IN}	3.6 V
	V_{BAT}	3.6 V
	C_{OUT}	100 µF/330 V

Transformer = DCT9.5/5ER, L_P = 7 µH, N = 10

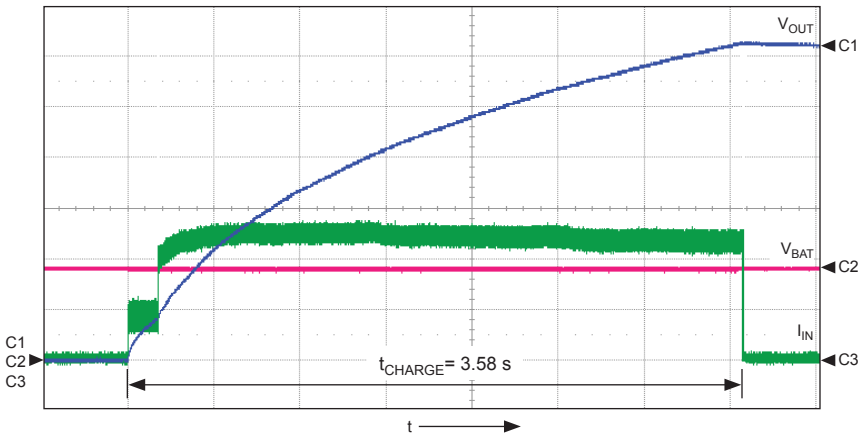
Conditions	Parameter	Value
	R_{SET}	25 kΩ
	I_P	≈3.15 A



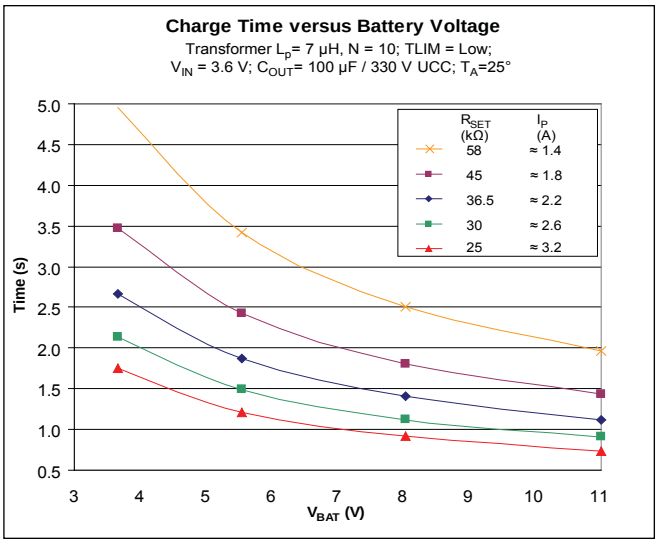
Conditions	Parameter	Value
	R_{SET}	30 kΩ
	I_P	≈2.6 A



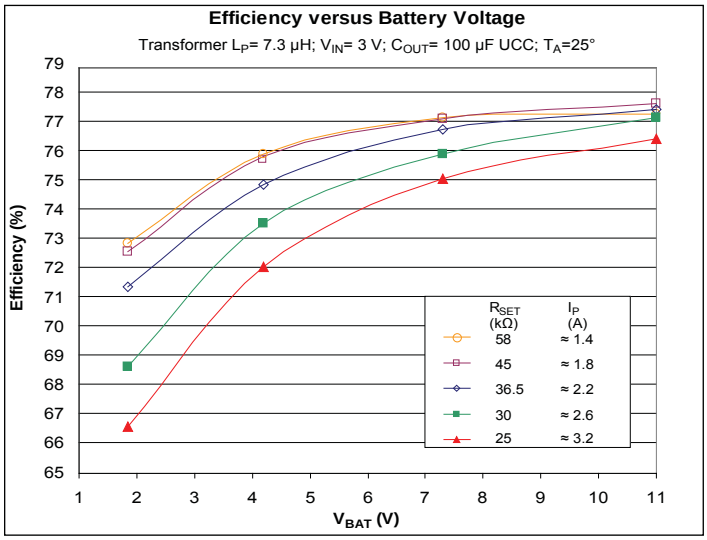
Conditions	Parameter	Value
	R_{SET}	45 kΩ
	I_P	≈1.8 A



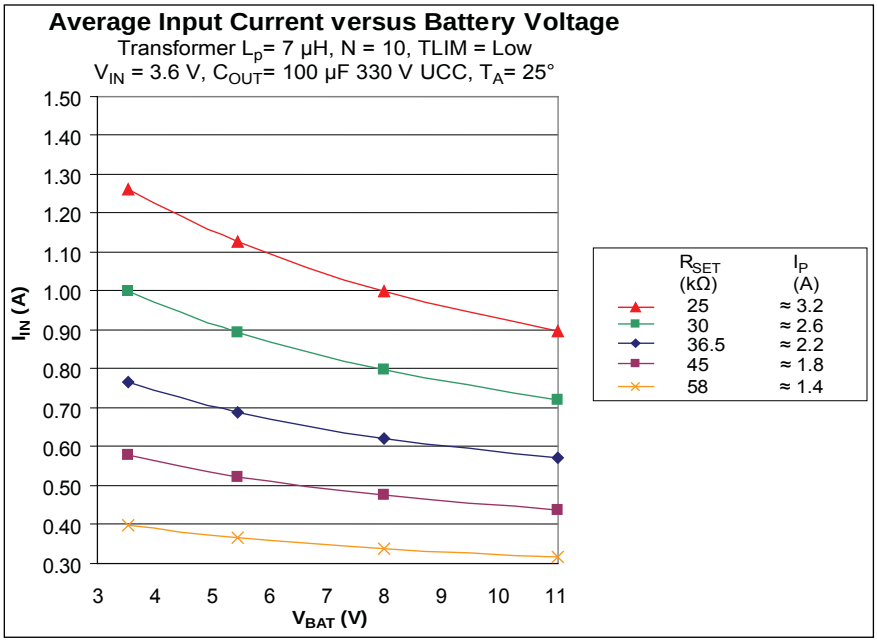
Performance Characteristics



C_{OUT}= 100 µF. For larger or smaller capacitances, charging time scales proportionally.



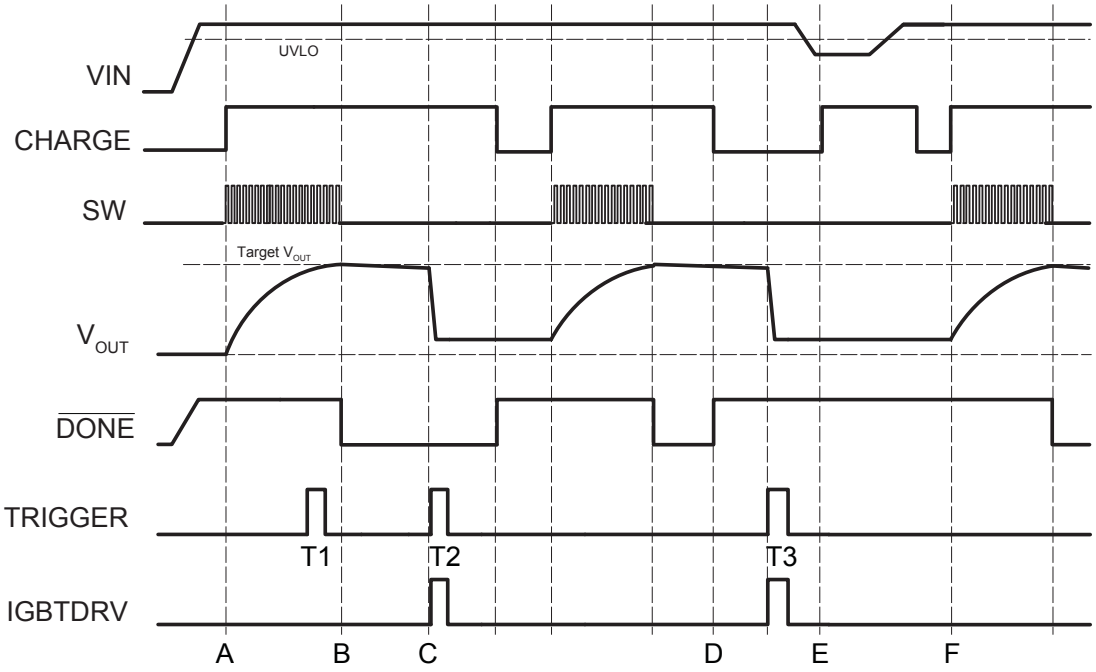
This data was obtained using a TDK DCT9.5/5ERUxxS003 transformer (L_P = 7.6 µH, 3.2 A, N = 10). Highest efficiency is achieved at high battery voltage and large peak current (1.4 to 1.8 A). At a maximum peak current of 3.2 A, conduction losses from the MOSFET and from the transformer windings dominate, so efficiency suffers.



The average input current decreases with higher V_{BAT}. .

Timing and IGBT Interlock Function

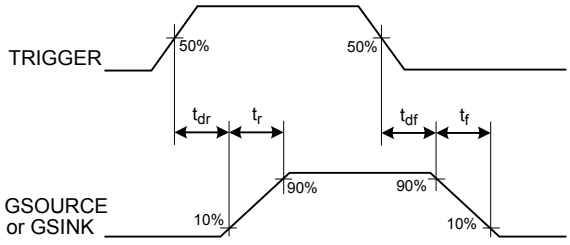
The two TRIGGER signals are internally ANDed together. As shown in the timing diagram, below, triggering is enabled when the CHARGE pin is low. This feature improves noise immunity.



Explanation of Events

A	Start charging process by pulling CHARGE pin high, provided that V_{IN} is above the UVLO level. Triggering (T1) is locked during the charging process (CHARGE and $\overline{DONE}$ pins are both high).
B	Charging stops when V_{OUT} reaches the target voltage level. Triggering (T2) is enabled after completion of charging (CHARGE pin is high and $\overline{DONE}$ pin is low).
C	Start a new charging process with a low-to-high transition at the CHARGE pin.
D	Pull the CHARGE pin low to put the controller into the low-power standby mode. Triggering (T3) is always enabled when CHARGE is low.
E	Charging does not start, because V_{IN} is below the UVLO level when the CHARGE pin goes high.
F	After V_{IN} goes above the UVLO level, another low-to-high transition at the CHARGE pin is required to start the charging process.

IGBT Drive Timing Definition



Application Information

Circuit Description

The A8425 is a photoflash capacitor charger control IC with a high current limit (up to 3.2 A) and low $R_{DS(on)}$ (0.23 Ω maximum). The IC also integrates an IGBT driver for strobe operation of the flash, dramatically saving board space in comparison with discrete solutions for strobe flash operation.

The IC is turned on by a low-to-high signal on the CHARGE pin. When the charging cycle is initiated, the primary current ramps up linearly at a rate determined by the battery voltage and the primary side inductance. When the primary current reaches the set limit, the internal MOSFET is turned off immediately to allow the energy to be dumped into the photoflash capacitor through the secondary winding. The secondary current drops linearly as the output capacitor is charged. The charging cycle starts again when the transformer flux is reset or after a predetermined time period (18 µs maximum off-time) has passed, whichever occurs first.

Timer Mode and Fast Charging Mode

The A8425 achieves fast charging times and high efficiency by operating in discontinuous conduction mode (DCM) through most of the charging process. The relationship of Timer Mode and Fast Charging Mode is shown in figure 1.

The IC operates in Timer Mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 40 V (actual value depends on input voltage and transformer inductance). Timer Mode is a fixed period, 18 µs, off-time control. One advantage of having Timer Mode is that it limits the initial battery current surge and thus acts as a "soft-start." A time expanded view of a Timer Mode interval is shown in figure 2.

As soon as a sufficient voltage has built up at the output capacitor, the IC enters Fast-Charging Mode. In this mode, the next switching cycle starts after the secondary side current has stopped flowing, and the switch voltage has dropped to a minimum value. A proprietary circuit is used to allow minimum-voltage switching, even if the SW pin voltage does not drop to 0 V. This enables Fast-Charging Mode to start earlier than previously possible, thereby reducing the overall

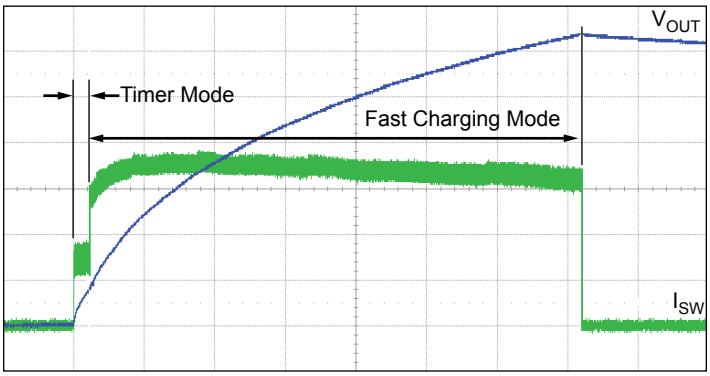
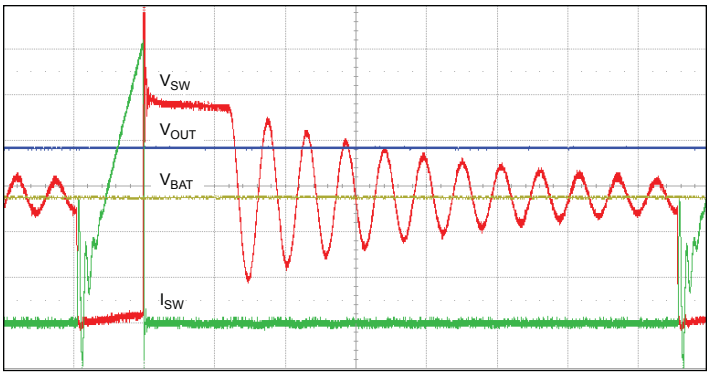


Figure 1. Relationship of Timer mode and Fast Charging mode

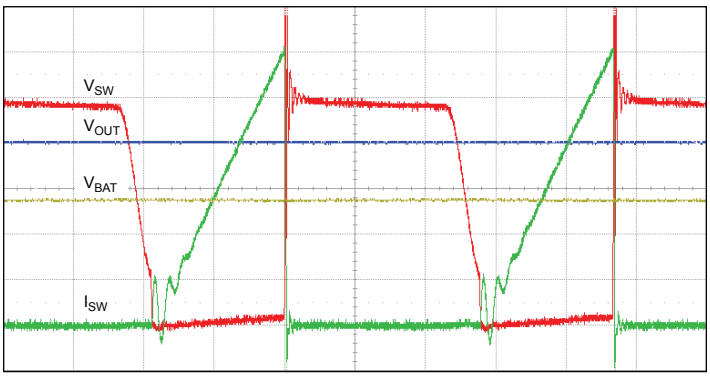


t = 2 µs/div; V_{OUT} =10 V/div; V_{BAT} =2 V/div.; V_{SW} =2 V/div; I_{SW} =200 mA/div. V_{IN} = 3.6 V; V_{BAT} =5.5 V; R_{SET} = 66.5 kΩ; Transformer L_P= 7.5 µH, N = 10

Figure 2. Timer Mode

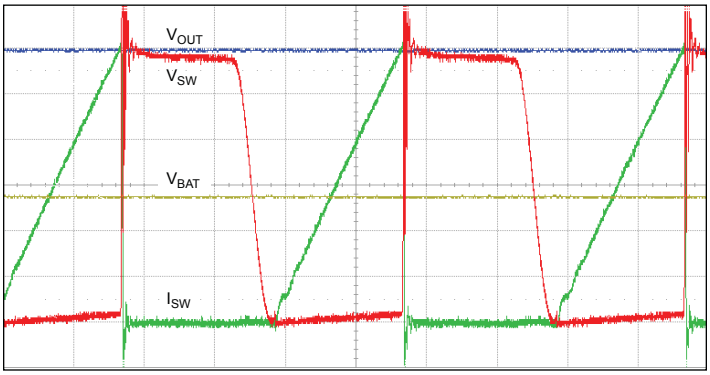
charging time. Minimum-voltage switching is shown in figure 3.

During Fast-Charging Mode, when V_{OUT} is high enough such that the reflected voltage (V_{OUT} / N) is greater than V_{BAT}, true zero-voltage switching (ZVS) is achieved. This further improves efficiency as well as reduces switching noise. A ZVS interval is shown in figure 4.



t = 1 µs/div; V_{OUT} =10 V/div; V_{BAT} =2 V/div.; V_{SW} =2 V/div; I_{SW} =200 mA/div. V_{IN} = 3.6 V; V_{BAT} =5.5 V; R_{SET} = 66.5 kΩ; Transformer L_P= 7.5 µH, N = 10

Figure 3. Fast Charging Mode, minimum voltage



t = 1 µs/div; V_{OUT} =10 V/div; V_{BAT} =2 V/div.; V_{SW} =2 V/div; I_{SW} =200 mA/div. V_{IN} = 3.6 V; V_{BAT} =5.5 V; R_{SET} = 66.5 kΩ; Transformer L_P= 7.5 µH, N = 10

Figure 4. Zero-voltage switching

Selection of Switching Current Limit

The A8425 features continuously adjustable peak switching current between 1.0 and 3.2 A. This is done by selecting the value of the external resistor RSET (connected between the ISET pin and GND), which determines the ISET bias current, and therefore the switching current limit, I_{SWlim}.

To the first order approximation, I_{SWlim} is related to I_{SET} and R_{SET} by the following equation:

$$I_{SWlim} = I_{SET} \times K$$

$$= (V_{SET} \times R_{SET}) \times K\,, \qquad (6)$$

where V_{SET} = 1.2 V, K = 59000 when the IC bias voltage, V_{IN}, is 3.6 V.

In real applications, the switching current limit is affected by bias voltage, battery voltage, and the transformer primary inductance, L_P. If necessary, the following expressions can be used to determine I_{SWlim} more accurately:

$$I_{SET} = V_{SET} / (R_{SET} + R_{SET(INT)} - K \times R_{G(INT)})\,, \qquad (7)$$

where $R_{SET(INT)}$ is the internal resistance of the ISET pin (330 Ω typical), $R_{G(INT)}$ is the internal resistance of the bonding wire for the GND pin (27 mΩ typical), and:

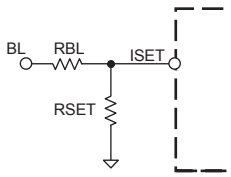
$$I_{SWlim} = I_{SET} \times (K' + V_{IN} \times K'') + (V_{BAT} / L_P) \times t_d\,, \qquad (8)$$

where K' = 47500, K" ≈ 3500 at T_A= 25°C, and t_d is the delay in SW turn-off (0.1 µs typical).

Figure 5 can be used to determine the relationship between R_{SET} and I_{SWlim} at various bias voltages.

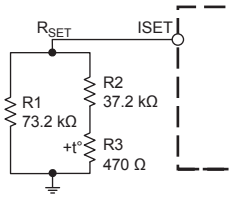
Smart Current Limit (Optional)

With the help of some simple external logic, the user can change the charging current according to the battery voltage. As an example (refer to the circuit diagram below), assume that the ISET current level is normally 50 µA (for I_{SWlim} = 3.0 A). Further, when



the battery voltage drops below 2.5 V, an external BL (battery-low) signal comes high. A resistor, RBL, connected from the BL node to the ISET pin, then injects 20 µA into RSET. This effectively reduces ISET current to 30 µA (for I_{SWlim} = 1.8 A). If necessary, BL can also be connected to the TLIM pin to reduce the minimum pulse width. The disadvantage of this method is that the 20 µA current is always flowing whenever the BL signal goes high.

In another example of a possible application, we can make use of a PTC thermistor to decrease the switch current limit when the board temperature exceeds 65°C. Referring to the following figure, R3 is a PTC type thermistor such as the Murata PRF18BG471QB1RB.



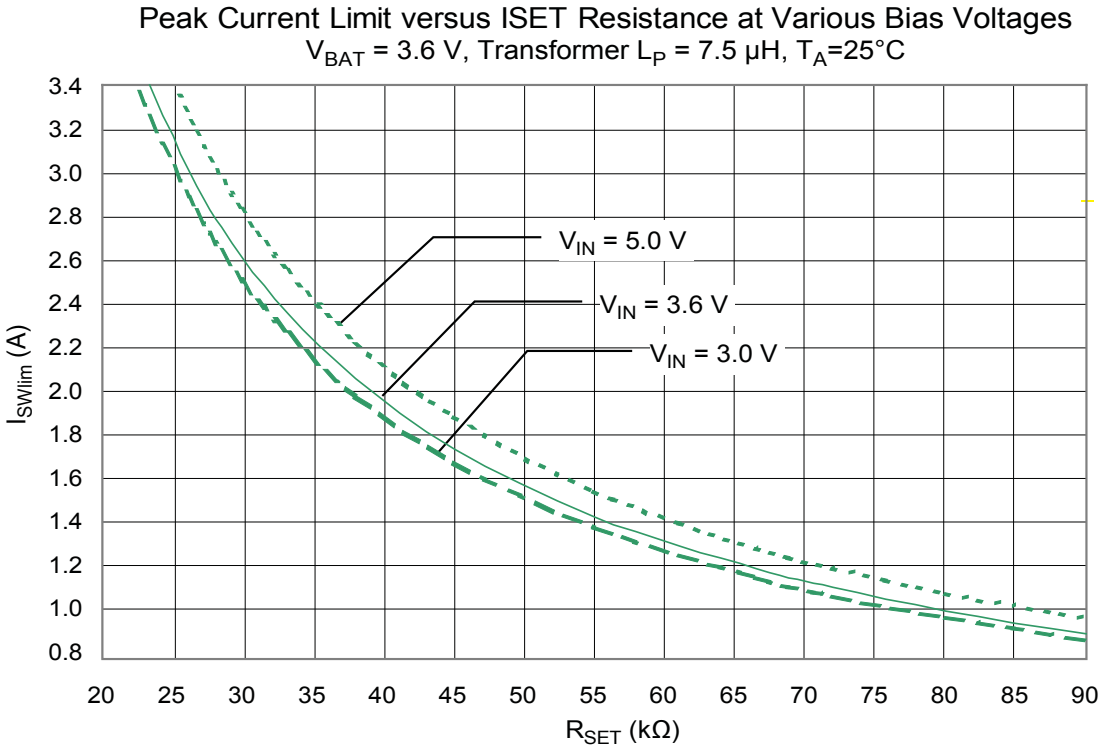


Figure 5. Chart of current versus limit settings

In this configuration, the peak currents at various PCB temperatures are as follows:

T_{PCB} (°C)	R_3 (kΩ)	R_{SET} (kΩ)	I_{peak} (A)
25	0.470	25.0	3.2
65	4.7	26.6	3.0
80	47.0	39.2	2.0

IGBT Gate Driver Application

The integrated IGBT driver is used to drive an external flash trigger IGBT. Separate GSOURCE and GSINK pins allow the user to adjust IGBT turn-on and turn-off rise times. For the Electrical Characteristics table in this document, IGBT drive timing is defined with the GSOURCE and GSINK pins connected together, and supplying a load comprising a 12 Ω resistor and a 6500 pF capacitor.

IGBT Gate Driver Interlock

The TRIGGERx pins are ANDed together to control the IGBT gate driver. If only one trigger pin is used, the other pin must be connected to VIN to ensure it is at logic high. However, triggering is disabled (locked) during charging. This is to prevent switching noises from interfering with the IGBT driver. After the CHARGE pin goes high (at the start of a charging cycle), the IC must wait for completion of the charging cycle ($\overline{\text{DONE}}$ goes low) before triggering can be enabled, according to the following chart:

Conditions		Resulting State
CHARGE	$\overline{\text{DONE}}$	IGBT Gate Driver
Low	Don't Care	Enabled
High	High	Disabled
High	Low	Enabled

Red Eye Reduction

The IGBT gate driver is always enabled when the CHARGE pin is low. If the CHARGE pin is disabled before sufficient voltage has built up on the output capacitor, the flash may not fire. In the case of red-eye reduction flashes, it is recommended to keep the CHARGE pin low until completion of triggering pulses. This ensures that the IGBT gate driver will remain enabled regardless of the $\overline{\text{DONE}}$ pin state.

Selection of Transformer

1. The transformer turns ratio ($N = N_S/N_P$) determines the output voltage:

$$V_{OUT} = K \times N - V_d \ , \qquad (6)$$

where K is 31.5 typical and V_d is the forward drop of the output diode (approximately 2 V).

2. The primary inductance L_P determines the on-time of the switch:

$$t_{on} = -L_P / R \times \ln\left(1 - I_{SWlim} \times R / V_{BAT}\right) , \qquad (7)$$

where R is the total resistance in the primary current path (including the $R_{DS(on)}$ of SW and the DC resistance of the transformer).

If V_{BAT} is much larger than $I_{SWlim} \times R$, then t_{on} can be approximated by:

$$t_{on} = I_{SWlim} \times L_P / V_{BAT} . \qquad (8)$$

3. The secondary inductance, L_S , determines the off-time of the switch:

$$t_{off} = (I_{SWlim} / N) \times L_S / V_{OUT} . \qquad (9)$$

Because $L_S / L_P = N \times N$:

$$t_{off} = (I_{SWlim} \times L_P \times N) / V_{OUT} . \qquad (10)$$

The minimum pulse width for t_{off} determines what is the minimum primary inductance required for the transformer. For example, if I_{SWlim} = 0.7 A, N = 10, and V_{OUT} = 315 V, then L_P must be at least 9 µH in order to keep t_{off} at 200 ns or longer.

In general, choosing a transformer with a larger L_P results in higher efficiency (because a larger L_P means lower switch frequency and hence lower switching loss). But a transformer with a larger L_P also requires more windings and a larger magnetic core. Therefore a trade-off must be made between transformer size and efficiency. The TLIM pin can be used to select between two minimum pulse width settings (200 ns and 400 ns), in order to provide greater design flexibility.

An additional feature allows wider choices of transformers. The VSEL pin selects the value of K, among 31.5, 35, and 39.4. These values correspond to transformers with an N of 10, 9, and 8 respectively for the same target output voltage of approximately 315 V. By using transformers with lower turns ratios, an efficiency gain of 1% to 2% can be typically expected.

Component Selection

Selection of the flyback transformer should be based on the peak current, according to the following table. Note: The maximum peak current must be derated at higher temperatures.

I_{Peak} Range (A)	Supplier	Part Number	L_P (µH)	N
1.0 to 2.0	TDK	LDT565630T-001	6	10.4
1.0 to 2.0	TDK	DCT5EPL-UxxS002	8	10
1.0 to 3.2	TDK	DCT9.5/5ER-UxxS003	7.6	10
1.4 to 3.2	TCE	T-17-160 (TTRN-060)	5.6	10.2

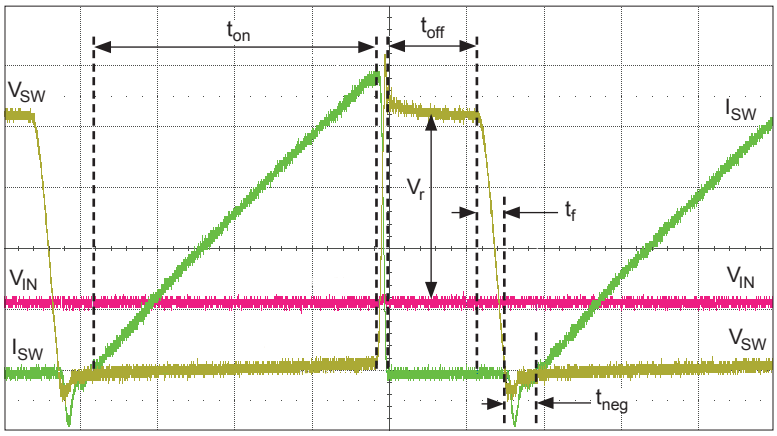
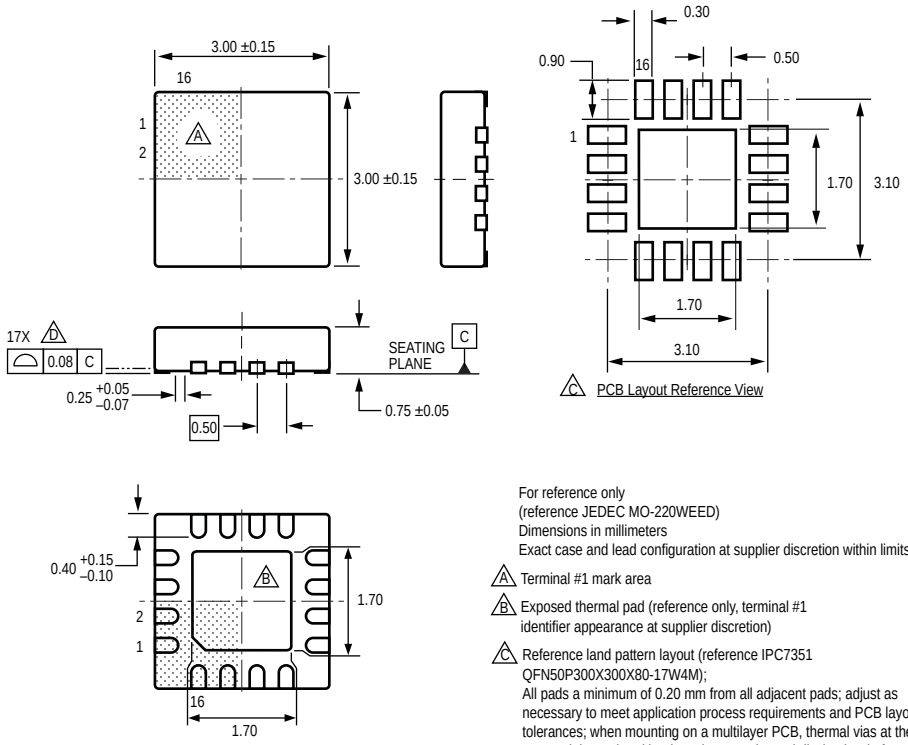


Figure 6. Relationship of t_{off} and switch output.

Package ES, 3 mm x 3 mm 16-Contact TQFN
with Exposed Thermal Pad



For reference only
(reference JEDEC MO-220WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Revision History

Revision	Revision Date	Description of Revision
Rev. 1	April 19, 2012	Update Selection Guide, miscellaneous format changes

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