A8503

High Efficiency 6-Channel, 2 MHz, WLED/RGB Driver for Medium Displays, with Integrated 55 V Power Switch

Features and Benefits

- Active current sharing between LED strings for ±0.6% accuracy and matching
- Drives up to 12 series × 6 parallel = 72 LEDs (V_f = 3.2 V, I_f = 20 mA) at 5 V
  - Each individual current sink is capable of 35 mA
- Adjustable overvoltage protection (OVP)
- 600 kHz to 2 MHz adjustable switching frequency
- Open or shorted LED string protection
- Open Schottky diode protection
- Overtemperature, cycle-by-cycle current limit, undervoltage, and soft start time-out protections
- Selectable latched/auto-restart protection modes
- No audible MLCC noise during PWM dimming
- No pull-up resistors required for LED modules that use ESD capacitors

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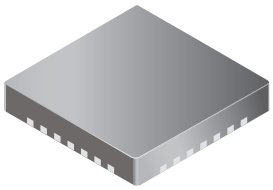
Package: 26 contact MLP/QFN (suffix EC)



Not to scale

Description

The A8503 is a multi-output WLED/RGB LED driver for medium-size LCD backlighting. It integrates a current-mode boost converter with internal power switch and six current sinks. The boost converter can provide output voltages up to 47 V. The boost converter can drive up to 72 LEDs at 20 mA per LED with a battery voltage down to 5 V. The LED sinks are capable of sinking up to 35 mA each, and can also be paralleled together to achieve even higher LED currents. The A8503 provides protection against overvoltage, open diode, open or shorted LED string, and overtemperature. A dual level cycle-by-cycle current limit function provides soft start and protects against overloads. A soft start timeout monitor is provided to enhance protection when starting up into a fault condition.

When the MODE pin is set low, the A8503 latches on a fault, and can be re-enabled only by cycling the input voltage, V_{IN}, or by toggling the EN pin. Connecting the MODE pin high provides auto-restart after fault events. The A8503 features

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Applications

- Notebook and sub-notebook displays
- LCD monitors
- LCD panels

Typical Application

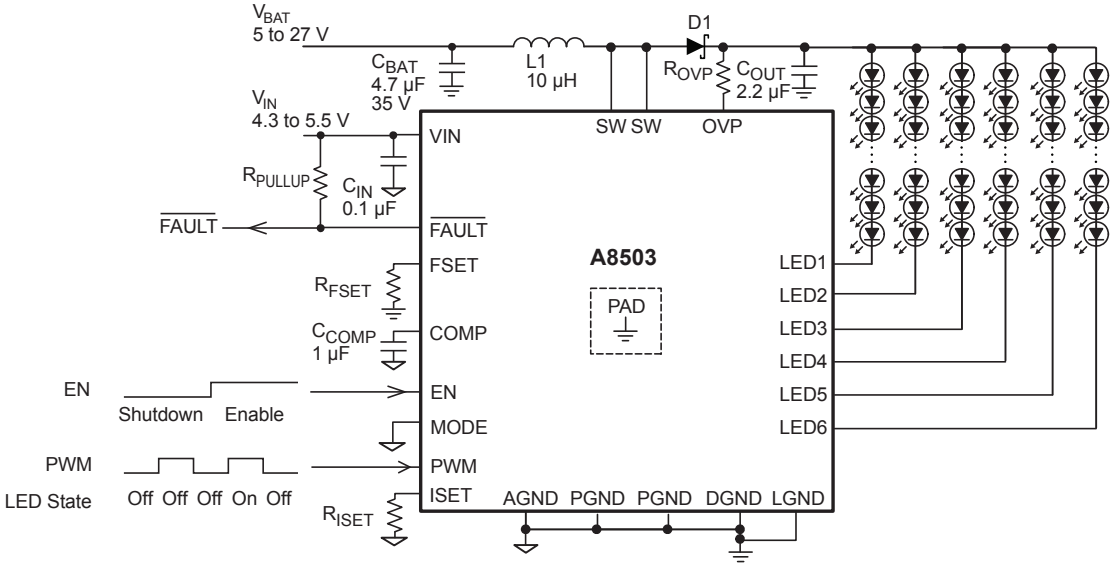

Figure 1. Typical application circuit

Features and Benefits (continued)

- Extends battery life
  - Efficiency optimized for 3-cell notebooks
  - 0.1 µA shutdown current
  - Unique architecture eliminates external voltage divider and associated battery drain
- Rugged and small footprint solution
- 55 V, 2 A DMOS switch in 4 mm × 4 mm package—allows IPC-2221/2 / IPC-D-275 compliant PCB layout

Description (continued)

EN (enable) and PWM (dimming) pins to comply with popular notebook backlight control interfaces.

The device is offered in a 26-contact, 4 mm × 4 mm, 0.75 mm nominal overall height QFN, with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

Selection Guide

Part Number	Packing	Package
A8503GECTR-T	1500 pieces per 7-in. reel	26-contact QFN/MLP with exposed thermal pad

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
SW Pins	V_{SW}		–0.3 to 57	V
LED1 through LED6 Pins	V_{LEDx}		–0.3 to 34	V
OVP Pin	V_{OVP}		–0.3 to 47	V
Remaining Pins			–0.3 to 7	V
Operating Ambient Temperature	T_A	Range G	–40 to 105	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	EC package, on 4-layer PCB based on JEDEC standard	35	ºC/W

*Additional thermal information available on the Allegro website

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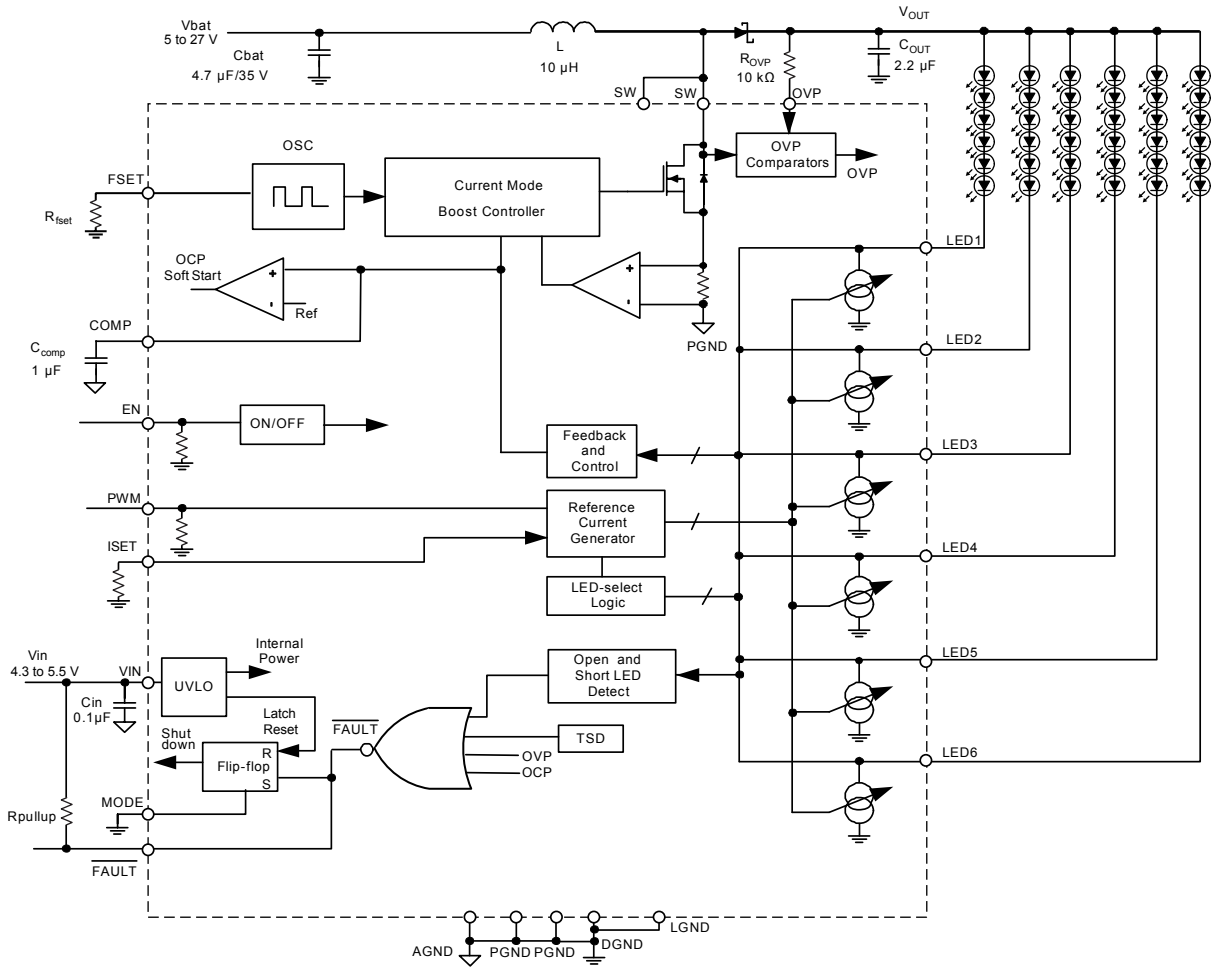
Functional Block Diagram



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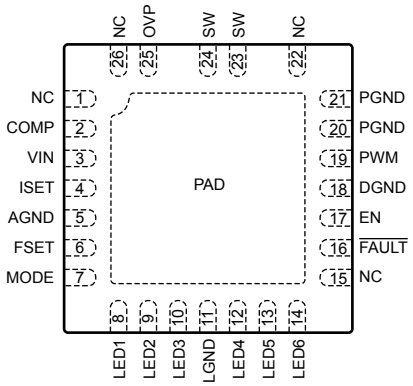
Pin-out Diagram



(Top View)

Terminal List Table

Name	Number	Function
AGND	5	Connect to common star ground
COMP	2	Compensation pin; connect 1 µF capacitor to AGND or common star ground
DGND	18	Digital ground; connect to common star ground
EN	17	Device enable
$\overline{\text{FAULT}}$	16	During normal operation, this pin is high (high impedance); at a fault event, this pin pulls low
FSET	6	Set switching frequency; connect R_{FSET} from FSET to AGND
ISET	4	Sets 100% current through LED string; connect R_{ISET} from ISET to AGND
LEDx	8,9,10,11, 12,13,14	LED current sinks; connect unused LEDx pins to ground
LGND	11	Power ground pin for LEDx current sinks; connect to common star ground
MODE	7	Apply V_{IL} for latching faults, apply V_{IH} for auto-restart; see Fault Mode table
NC	1, 15, 22, 26	Not connected internally
OVP	25	Connect this pin to output capacitor +ve node through R_{OVP} to enable overvoltage protection; select R_{OVP} > 10 kΩ (V_{OVP} is 44 V typical)
PAD	–	Exposed thermal pad, common star ground for PGND, DGND, LGND, and AGND; connect to copper plane of the application PCB for heat transfer
PGND	20, 21	Power ground; connect both pins to common star ground
PWM	19	PWM LED-current control; apply logic level PWM for dimming
SW	23, 24	DMOS switch drain node; tie SW pins together on the PCB
VIN	3	Input supply for the IC; decouple with a 0.1 µF ceramic capacitor

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ELECTRICAL CHARACTERISTICS[1] Valid using circuit shown in figure 1, $T_A = T_J = 25°C$ except • indicates specifications guaranteed from −40°C to 105°C, $V_{IN} = 5.0$ V, EN = PWM = V_{IH}, $R_{ISET} = 12.4$ kΩ, $R_{FSET} = 34$ kΩ, MODE = AGND, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.[2]	Max.	Unit
Input Voltage Range	V_{IN}		•	4.2	–	5.5	V
Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling	•	–	–	4.0	V
Undervoltage Lockout Hysteresis Window	$V_{UVLOHYS}$			–	0.1	–	V
Supply Current	I_{VIN}	Switching, at no load		–	7	–	mA
		Shutdown, EN= V_{IL}, $T_A = 25°C$		–	0.1	1	µA
		Standby, EN = V_{IH}, PWM = V_{IL}	•	–	1	2	mA
Boost Controller							
Switching Frequency	f_{SW}		•	1.2	1.5	1.9	MHz
Minimum Switch Off-Time	$t_{off(min)}$			–	72	–	ns
Minimum Switch On-Time	$t_{on(min)}$			–	72	–	ns
Logic Input Levels (EN and PWM pins)							
Input Voltage Level Low	V_{IL}		•	–	–	0.4	V
Input Voltage Level High	V_{IH}		•	1.5	–	–	V
Input Leakage Current	I_{ILKG}	EN = PWM = 5 V		–	100	–	µA
Overvoltage Protection							
Output Overvoltage Threshold	V_{OVP}			–	44	–	V
Overvoltage Protection Leakage Current	I_{OVPLKG}	$V_{OVP} = 22$ V, $R_{OVP} = 0$ Ω, EN = V_{IL}		–	0.1	–	µA
Overvoltage Protection Sense Current	I_{OVPH}			–	240	–	µA
Boost Switch							
Switch On-Resistance	$R_{DS(on)}$	$I_{SW} = 1$ A		–	250	–	mΩ
Switch Leakage Current	$I_{SWLKG(B)}$	$V_{SW} = 22$ V		–	0.1	–	µA
Switch Current Limit	I_{SWLIM}			–	2.7	–	A
LED Current Sinks							
LEDx Pin Regulation Voltage	V_{LEDx}			–	600	–	mV
I_{SET} to I_{LEDx} Current Gain	A_{ISET}	$I_{SET} = 100$ µA		–	320	–	A/A
ISET Pin Voltage	V_{ISET}			–	1.235	–	V
ISET Allowable Current Range	I_{SET}		•	33	–	110	µA
LEDx Current Accuracy[3]	Err_{ILEDX}	LED1 through LED6 = 0.6 V, at 100% Current	•	–3	±0.6	3	%
LEDx Current Matching[4]	ΔI_{LEDX}	$I_{SET} = 100$ µA, LED1 though LED6 = 0.6 V, at 100% Current	•	–3	±0.6	3	%
Switch Leakage Current (LEDx)	$I_{SWLKG(L)}$	$V_{LEDx} = 12$ V, EN = 0		–	0.1	–	µA
LED Short-Detect Voltage	V_{SC}	LEDx pin voltage level that forces latched shutdown, MODE = low		–	18.7	–	V

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ELECTRICAL CHARACTERISTICS[1] (continued) Valid using circuit shown in figure 1, $T_A = T_J = 25°C$ except • indicates specifications guaranteed from −40°C to 105°C, $V_{IN} = 5.0$ V, EN = PWM = V_{IH}, $R_{ISET} = 12.4$ kΩ, $R_{FSET} = 34$ kΩ, MODE = AGND, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.[2]	Max.	Unit
Soft Start							
Soft Start Boost Current Limit	$I_{SW(SS)}$	Initial soft start current for boost switch		–	0.4	–	A
Soft Start LEDx Current Limit	$I_{LED(SS)}$	Current through enabled LEDx pins during soft start		–	2.6	–	mA
Soft Start Timeout	$t_{TO(SS)}$	The longest duration the boost is allowed to operate during soft start		–	131,072	–	Clock Cycles
Thermal Shutdown Threshold	T_{SHDN}	T_J rising		–	165	–	°C
Thermal Shutdown Hysteresis	$T_{SHDN(hys)}$			–	45	–	°C
$\overline{\text{FAULT}}$ Pin							
$\overline{\text{FAULT}}$ Pull-Down Voltage	V_{FAULT}	Voltage on $\overline{\text{FAULT}}$ pin with fault enabled, 10 kΩ pull-up resistor, to 3.3 V	•	–	–	0.4	V
$\overline{\text{FAULT}}$ Pull-Down Resistance	R_{FAULT}	Resistance between $\overline{\text{FAULT}}$ pin and ground with fault enabled, $I_{FAULT} = 100$ µA		–	77	–	Ω

[1]Specifications over the range T_A = -40°C to 105°C; guaranteed by design and characterization.
[2]Typical values are at $T_A = 25°C$.
[3]LED accuracy is defined as $100 \times (I_{SET} \times 320 – I_{LED(av)}) / (I_{SET} \times 320)$, $I_{LED(av)}$ measured as the average of I_{LED1} through I_{LED6}.
[4]LED current matching is defined as $(I_{LEDx} – I_{LED(av)}) / I_{LED(av)}$, with $I_{LED(av)}$ as defined in footnote 3.

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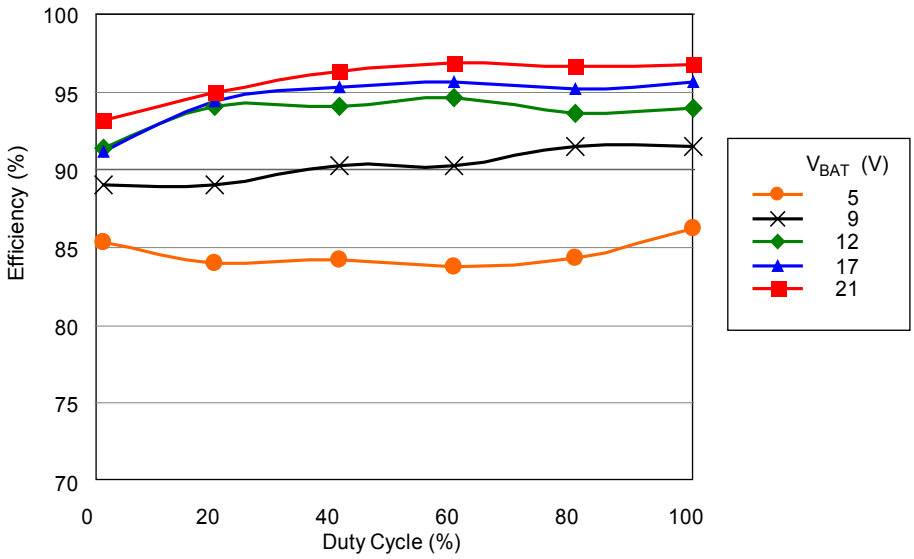
Characteristic Performance

High Efficiency Boost Converter

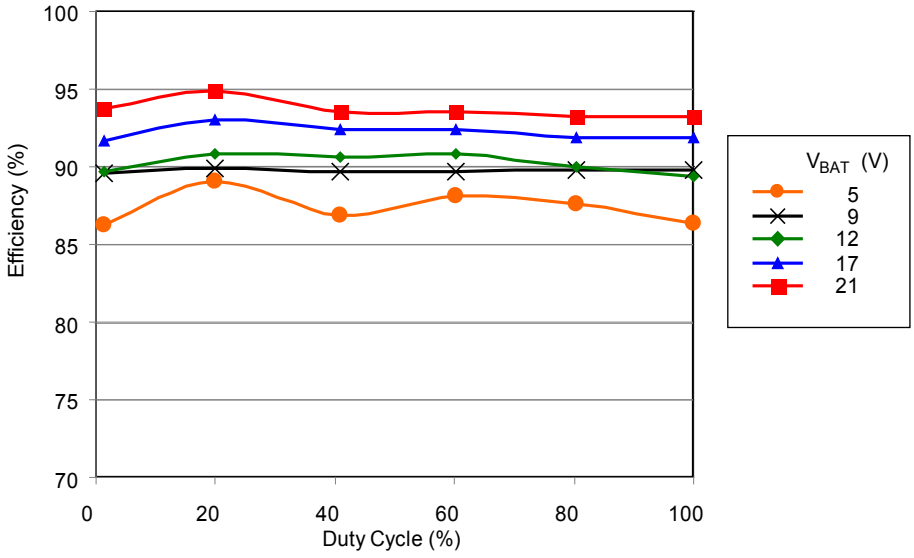
PWM Efficiency

at Various Input Voltage Levels (V_{BAT})
V_{IN} = 5 V, six channels with 9 series LEDs each,
20 mA per channel, PWM = 200 Hz, f_{SW} = 1.5 MHz



PWM Efficiency

at Various Input Voltage Levels (V_{BAT})
V_{IN} = 5 V, six channels with 9 series LEDs each,
20 mA per channel, PWM = 200 Hz, f_{SW} = 980 kHz



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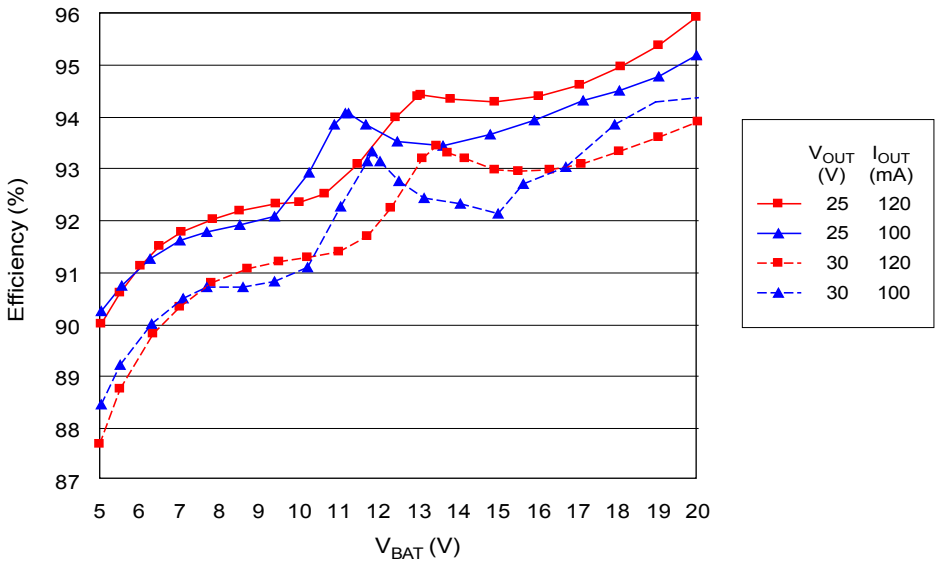
Characteristic Performance

High Efficiency Boost Converter

Efficiency (P_{OUT}/P_{BAT}) versus Battery Supply Voltage

for Various Output Power Levels

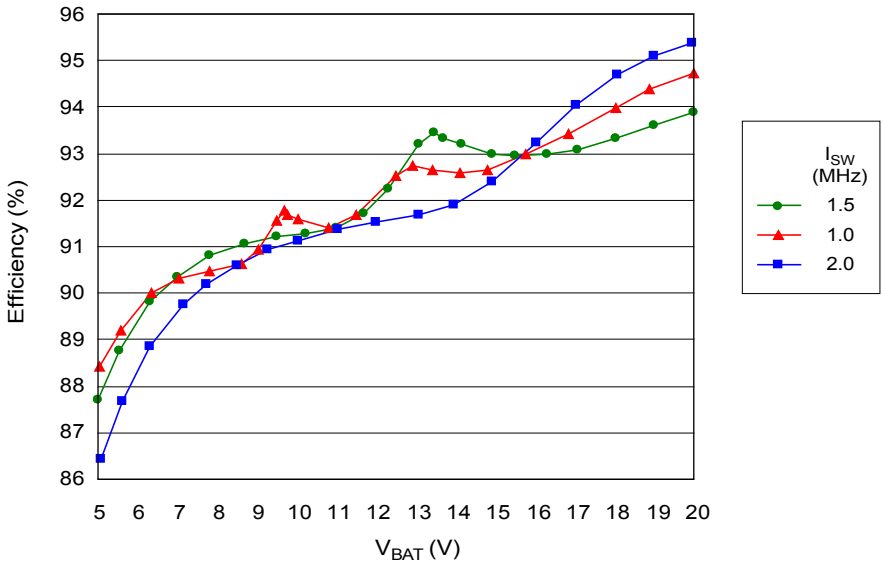
L1 = 6.8 µH, f_{SW} = 1.5 MHz, V_{IN} = 5.0 V



Efficiency (P_{OUT}/P_{BAT}) versus Battery Supply Voltage

for Various Switching Frequencies

V_{IN} = 5.0 V, V_{OUT} = 30 V I_{OUT} = 120 mA



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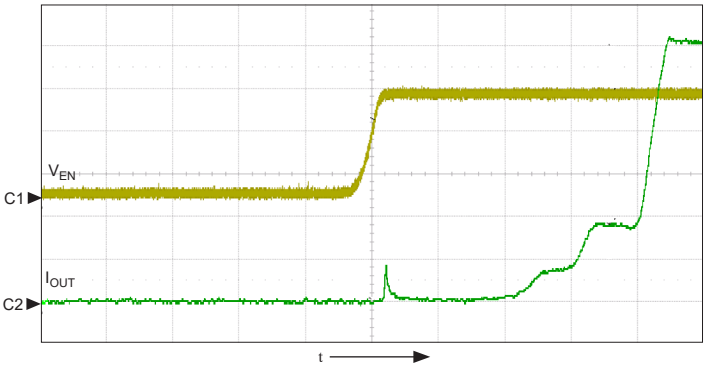
Characteristic Performance

Turn-on and Shutdown

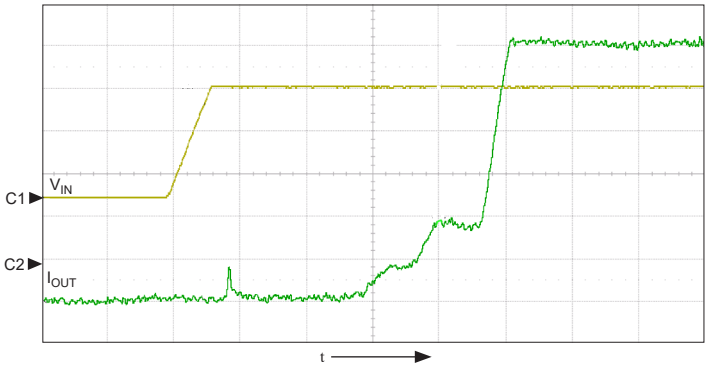
V_{IN} = 5 V, V_{BAT} = 7 V, I_{LEDx} = 20 mA, six LED channels with 10 series LEDs each

(A) Turn-on using the EN pin, with V_{IN} = 5 V



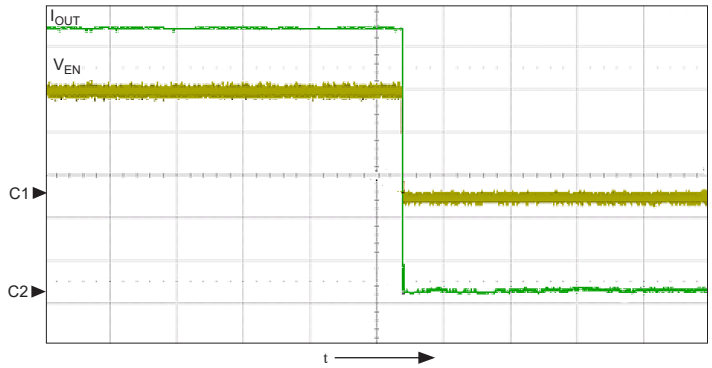
Symbol	Parameter	Units/Division
C1	V_{EN}	2 V
C2	I_{OUT}	20 mA
t	time	2 ms

(B) Turn-on using the VIN pin, with EN high



Symbol	Parameter	Units/Division
C1	V_{IN}	2 V
C2	I_{OUT}	20 mA
t	time	2 ms

(C) Shutdown using the EN pin



Symbol	Parameter	Units/Division
C1	V_{EN}	2 V
C2	I_{OUT}	20 mA
t	time	200 µs

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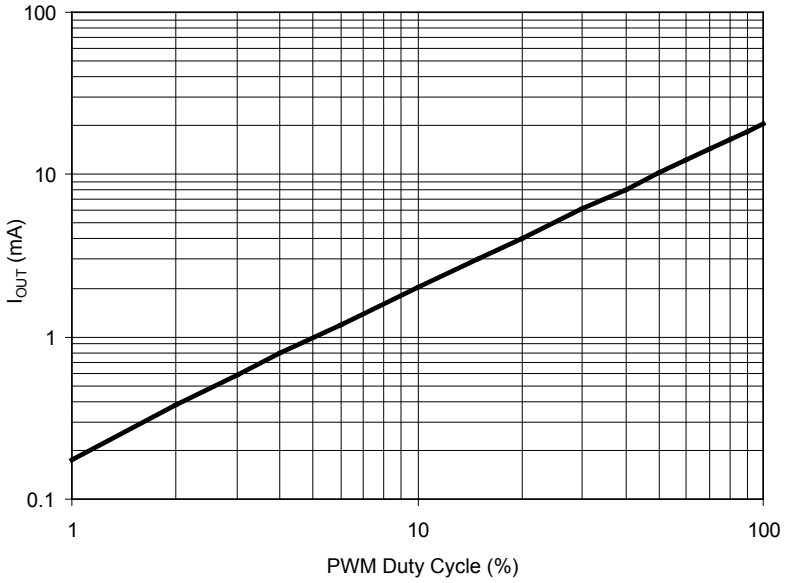
Characteristic Performance

Average LED Current a Various PWM Duty Cycles

V_{IN} = 5.0 V, V_{BAT} = 12 V, PWM = 200 Hz, Output = six LED channels with 10 series LEDs each



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Functional Description

The A8503 is a multi-output WLED/RGB LED driver for backlighting medium-size displays. It has an integrated boost converter to increase input supply voltage, allowing it to drive up to 12 LEDs per channel on 6 channels with a V_f(max) of 3.2 V at 20 mA per LED, at 5 V supply. The boost converter is a fixed frequency current-mode converter. The switching frequency can be set in a range from 600 kHz to 2 MHz, by an external resistor, R_{FSET}, connected between FSET and ground. The integrated boost DMOS switch is rated for 55 V, 2 A. This switch is protected against overvoltage, and has pulse-by-pulse current limiting. The current limiting is independent of duty cycle.

The A8503 has six well-matched current sinks that provide regulated current through the LEDs, for uniform display brightness. The boost converter is controlled by monitoring all LEDx pins simultaneously and continuously. All LED sinks are rated for 34 V to allow PWM dimming control.

LED Current Setting

The maximum LED current can be set, to 32 mA/channel, through the ISET pin. Connect a resistor, R_{ISET}, between this pin and ground to set the reference current level, I_{SET}. The value of I_{SET} (mA) is determined by:

$$I_{SET} = 1.235 / R_{ISET}\ (k\Omega) \quad .$$

The resulting current is multiplied internally by a gain of 320, then is mirrored to all enabled LEDx pins. This sets the maximum current through LEDx, referred as the *100% Current*, as shown in figure 2A. The LEDx current can be reduced from the 100% Current value by applying an external PWM signal on the PWM pin (see figure 2B).

Boost Switching Frequency Setting

Connect an external resistor between the FSET pin and AGND, to set boost switching frequency, f_{SW}. The value of the boost switching frequency, f_{SW} (MHz), is determined by:

$$f_{SW} = 52 / R_{FSET}\ (k\Omega) \quad .$$

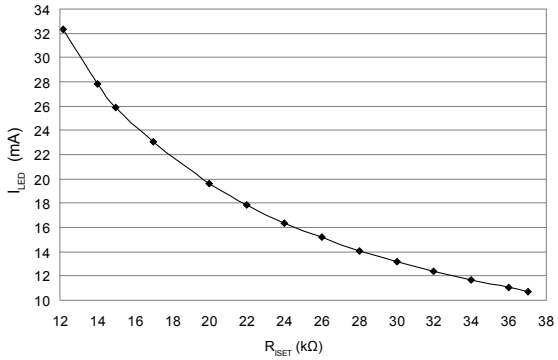
The typical R_{FSET} versus frequency curve is shown in figure 3.

Enable

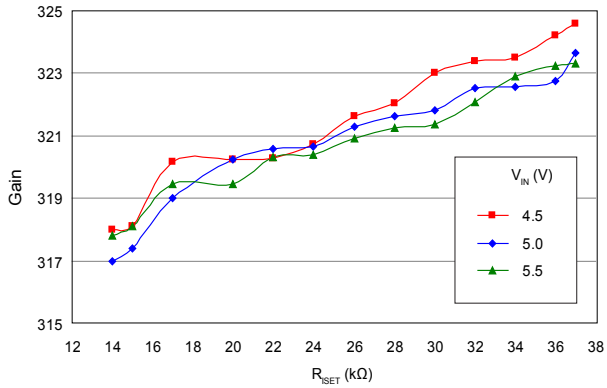
The IC turns on when a high signal is applied on the EN pin and turns off when this pin is pulled low.

PWM Dimming

The A8503 has a very wide range of PWM signal input. It can accept a PWM signal from 100 Hz to 5 kHz. When a PWM high signal is applied, the LEDx pins sink 100% Current. When the



(A)



(B)

Figure 2. Effect of value of R_{ISET} on current through an LED string. Panel A shows level of 100% current, and panel B shows LEDx gain.

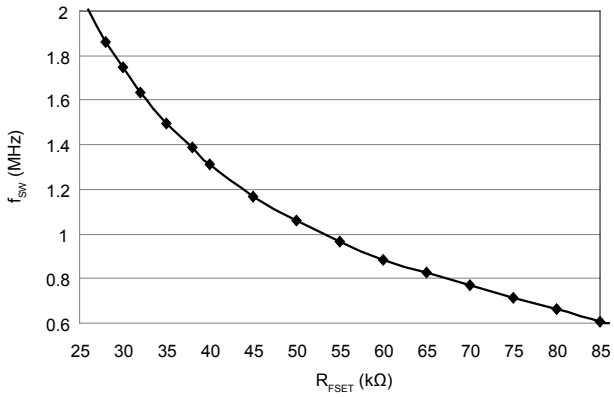


Figure 3. Switching frequency setting versus R_{FSET} (V_{IN} = 5 V, V_{BAT} = 12 V).

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PWM signal is low, the LED sinks turn off. Referring to figure 5, there is a 4 µs ramp-up delay between when the PWM signal is applied and when the current reaches the 90% level. Increase the applied PWM pulse-width by 3 µs to compensate for this delay.

Startup Sequence

When EN is pulled high, the IC enters soft start. The IC first tries to determine which LEDx pins are being used, by raising the LEDx pin voltage with a small current. After a duration of 512 switching cycles, the LEDx pin voltage is checked. Any LEDx channel with a drain voltage smaller then 100 mV is removed from the control loop.

After the first PWM positive trigger, the boost current is limited to 0.4 A and all active LEDx pins sink $^1/_{12}$ of the set current until output voltage reaches sufficient regulation level. When the device comes out of soft start, boost current and the LEDx pin currents are set to normal operating level. Within a few cycles, the output capacitor charges to the voltage required to supply full LEDx current. After V_{OUT} reaches the required level, LEDx current toggles between 0% and 100% with each PWM command signal.

In case of a heavy overload on output voltage at startup, the device may stay in soft start mode indefinitely, if the output voltage cannot rise to the LED regulation level and the MODE pin is tied high. To avoid this scenario, A8503 has a soft start timeout when the MODE pin is tied low. With the MODE pin low, if the device does not finish soft start during 131,072 switching cycles, it is shut down.

LED Open and Short Detect

All unused LED pins should be connected to ground to prevent any undesired faults from triggering. For LED short detect, any enabled LEDx pins that have a voltage exceeding the short circuit detect voltage, V_{SC}, causes the device to shut down irrespective of what mode the A8503 is in. The open LED fault will be triggered as soon as an enabled LEDx pin does not have sufficient current flowing through it to stay in regulation. This will result in increased output voltage until the LED is back in regulation or overvoltage protection (OVP) is tripped. If OVP is tripped, depending on the mode of operation, the A8503 will either shut down (MODE = low) or will remove the LED string from operation and continue to operate normally (MODE = high). Please refer to the Fault Mode table for latched and non-latched fault conditions.

Overvoltage Protection

The A8503 has two independent overvoltage protection features to protect the device against output overvoltage. The overvoltage level can be set, from 44 to 50 V typical, with an external resistor, ROVP. When the current though the OVP pin exceeds 240 µA, the OVP comparator goes high and the device shuts down in an OVP fault state when the MODE pin is low. If the MODE pin is high, the OVP fault disables all LEDx strings that are below regulation, thus preventing them from controlling the boost output voltage.

The device also offers open Schottky diode protection. If for any reason the voltage on the SW pins exceeds more than 57 V, the IC shuts down and remains latched irrespective of the MODE pin level. The overvoltage protection circuit is shown in figure 6.

Calculate the value for R_{OVP} as follows:

$$R_{OVP} = (V_{OVP} - 44) / 240\ \mu A\ ,$$

where V_{OVP} is the desired typical OVP level in V, and R_{OVP} is in Ω.

Overcurrent Protection

The IC provides pulse-by-pulse current limiting at 2.7 A for the boost MOSFET. If the overcurrent fault state persists, the boost control loop will force the compensating capacitor to rise in voltage until it reaches the overcurrent fault level. This fault shuts down the IC and is latched when MODE pin is low (MODE = AGND). If MODE pin is high, the overcurrent fault forces the device into soft start.

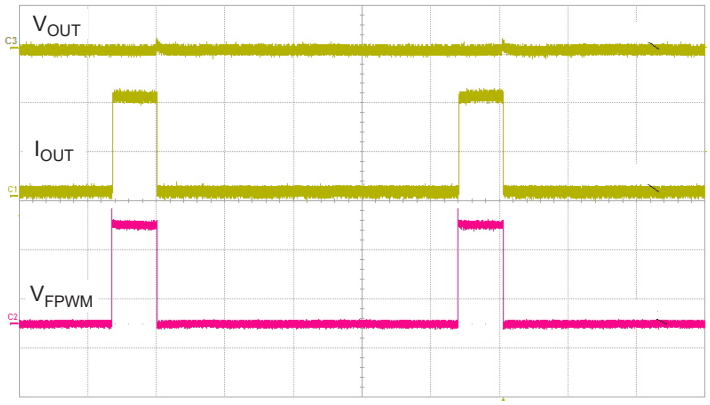

Figure 4. PWM Pin Dimming, f_{PWM} = 200 Hz, duty cycle = 10%. C1, I_{OUT} 50 mA / div; ; C2, V_{FPWM} (signal on PWM pin) 2 V / div; C3, V_{OUT} 5 V / div, AC coupled.

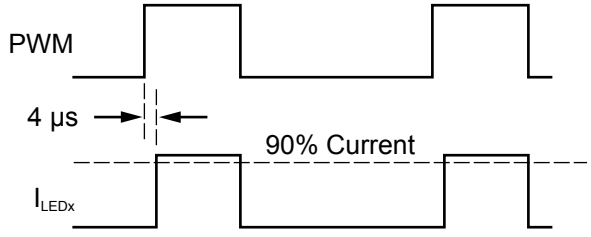

Figure 5. I_{LEDx} versus PWM input

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Input UVLO

The device is shut down when input voltage, V_{IN}, falls below V_{UVLO}.

Thermal Shutdown Protection (TSD)

The device shuts down when junction temperature exceeds 165°C. If the MODE pin is low, the thermal shutdown will latch the device off until EN is pulled low or UVLO is triggered. The A8503 will recover automatically when the MODE pin is high and the junction temperature falls below 120°C.

Fault Mode

The MODE pin controls the latching of faults as shown in the Fault Mode table. Latched faults are reset when EN is pulsed low or V_{IN} falls below UVLO level.

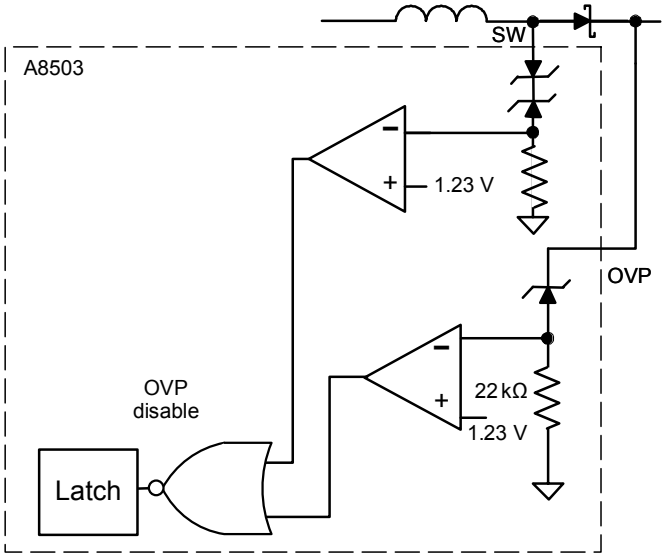

Figure 6. Overvoltage protection circuitry

Fault Mode Table

Protection	MODE = AGND	MODE = V_{IN}	Description
Overvoltage Protection	Latched	Auto-restart	Fault occurs when OVP pin exceeds V_{OVP} threshold. Used to protect the output voltage from damaging the part.
Open Diode Protection	Latched	Latched	Fault occurs when SW node exceeds the safe operating voltage of the boost DMOS switch. Typical value is 57 V.
Pulse-by-Pulse Current Limiting	Auto-restart	Auto-restart	Fault occurs when the current through the DMOS switch exceeds I_{SWLIM}, 2.7 A typical. The DMOS switch is turned off on a cycle-by-cycle basis.
Overcurrent Protection	Latched	Auto-restart	Fault occurs when the COMP pin exceeds the overcurrent detect threshold. Multiple pulse-by-pulse current limits will cause the COMP pin voltage to rise. After a time period determined by the COMP current and the compensation capacitor, the COMP voltage will exceed the overcurrent detect threshold and force a fault.
Overtemperature Protection	Latched	Auto-restart	Fault occurs when the die temperature exceeds the overtemperature threshold, 165°C typical.
Shorted LED Protection	Latched	Latched	Fault occurs when the LEDx pin voltage exceeds V_{SC}, 18.7 V typical.
V_{IN} UVLO	No	No	Fault occurs when V_{IN} drops below V_{UVLO}, 4.0 V typical. This fault resets all latched faults.
Soft Start Timeout	Latched	Auto-restart	Fault occurs if the IC is unable to finish soft start within approximately 131,000 clock cycles (approximately 74 ms at 1.73 MHz) after EN is set high.

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Application Information

A typical application circuit for dimming an LCD monitor backlight with 72 LEDs is shown in figure 1. Figure 7 shows two dimming methods: digital PWM control (PWM signal on the PWM pin) and analog PWM control, with the analog signal, V_A, applied to the ISET pin through a resistor, R_A.

The current flowing through R_A can be calculated as:

$$I_A = (V_A - V_{SET}) / R_A .$$

This current changes the reference current, I_{SET}, as follows:

$$I_{SET} = V_{SET} / R_{SET} - (V_A - V_{SET}) / R_A .$$

LED current can be changed by changing V_A. ISET can be changed in the range from 33 to 100 µA.

Application Circuit for 1000:1 Dimming Level

A wider dimming range can be achieved by changing the reference current, I_{SET}, while using PWM dimming. For higher output, current levels turn on Q1 (see figure 8). R_{ISET} and R_{ISETP} set the 100% current level. This current level can be set up to 32 mA, and then it can be dimmed by applying 100% to 0.33% duty cycle on the PWM pin. The reference current can be reduced by turning off Q1. LED current can be dimmed to 10 mA by reducing reference current through the ISET pin. This provides a 1000:1 combined dimming level range. Figure 9 shows the accuracy, Err_{LEDX}, that results using this circuit.

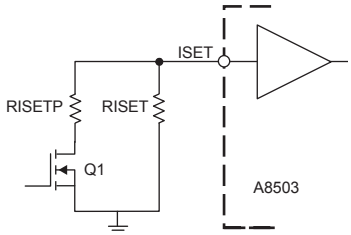

Figure 8. Configuration for 1000:1 dimming.

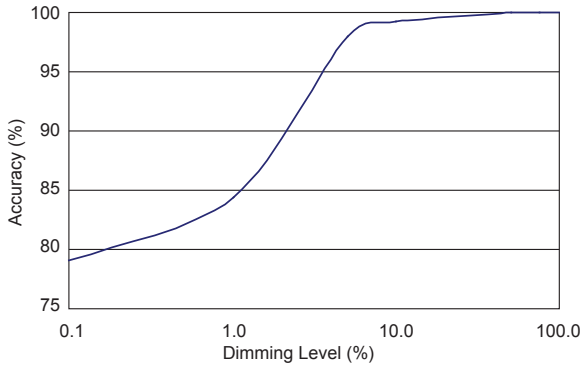

Figure 9. Typical accuracy, normalized to the 100% current level, versus dimming level, with F_{PWM} = 100 Hz.

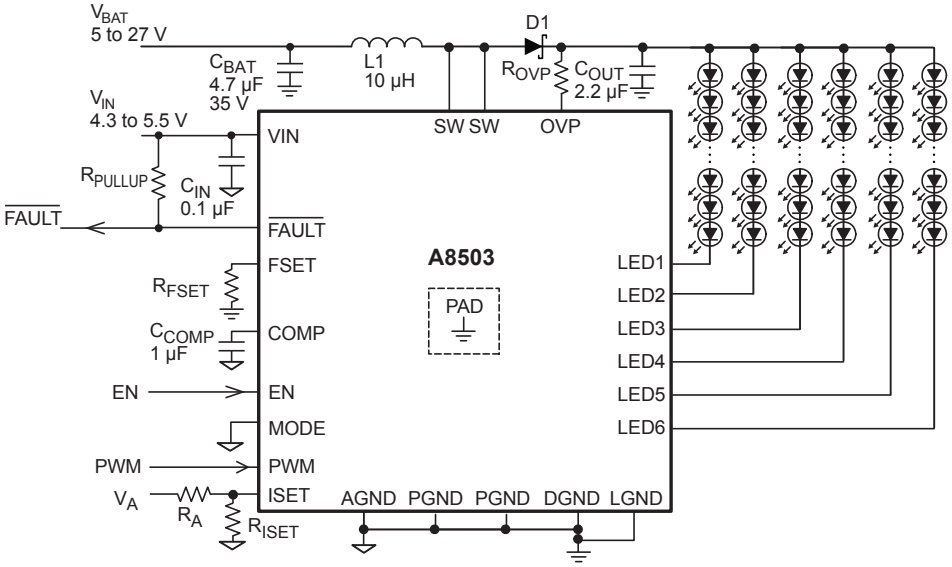

Figure 7. Typical application circuit for analog dimming with external DC voltage source V_A. This method of dimming can be combined with digital PWM dimming.

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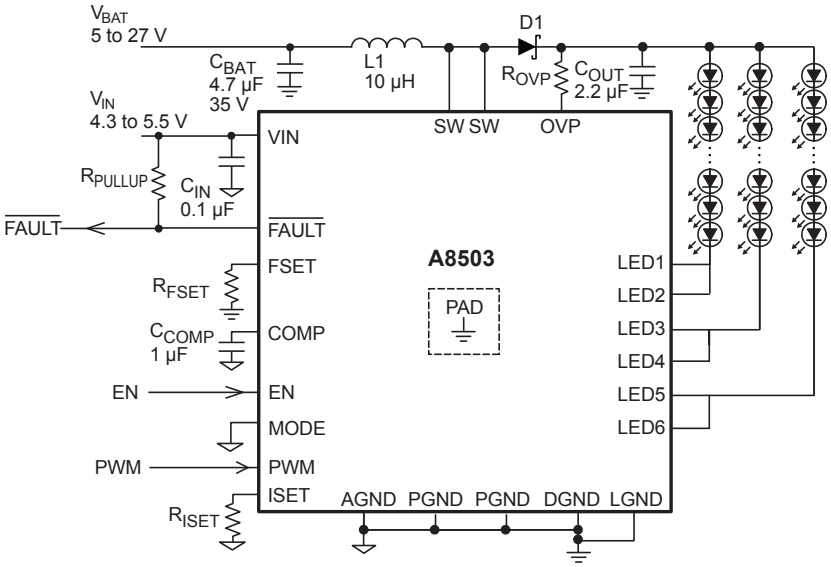

Figure 10. Typical application circuit with LED channels paralleled together to achieve higher LED current (up to 64 mA per string).

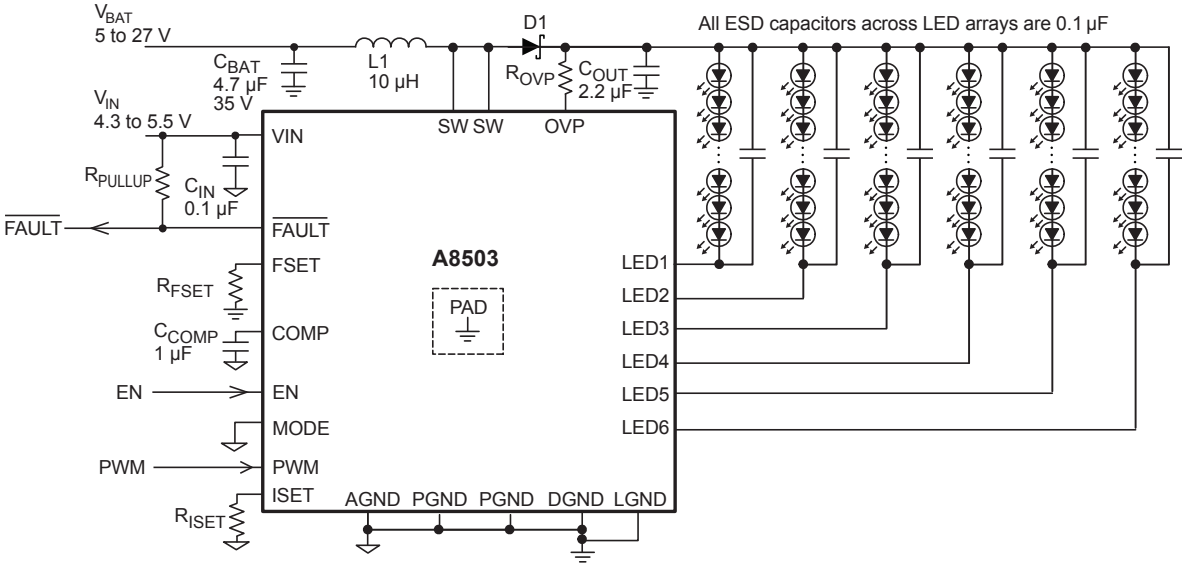

Figure 11. Typical application circuit for LED modules with ESD capacitors with values up to 10 nF.

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Recommended Components Table

Component	Rating	Part Number	Source
C_{BAT}	4.7 µF / 35 V, X5R ceramic capacitor	GMK316F475ZG-T	Taiyo Yuden
C_{COMP}	1 µF / 10 V		
C_{IN}	0.1 µF / 10 V		
C_{OUT}	2.2 µF / 50 V, X7R	GRM31CR71H225KA88L	Murata
D1	Schottky diode 60 V, 1.5 A	10MQ060NTRPBF	International Rectifier
R_{FSET}	34 kΩ, 1%		
R_{ISET}	19.6 kΩ, 1% (for 20 mA LED current)		
R_{OVP}	10 kΩ		
R_{PULLUP}	10 kΩ		
L1	10 µH, 1.3 A	SLF6028T-100M1R3-PF	TDK
Alternate inductors	6.8 µH, 1.3 A 4.7 µH, 1.6 A	D53LC A915AY-6R8M NP04SZB 4R7N	Toko Taiyo Yuden

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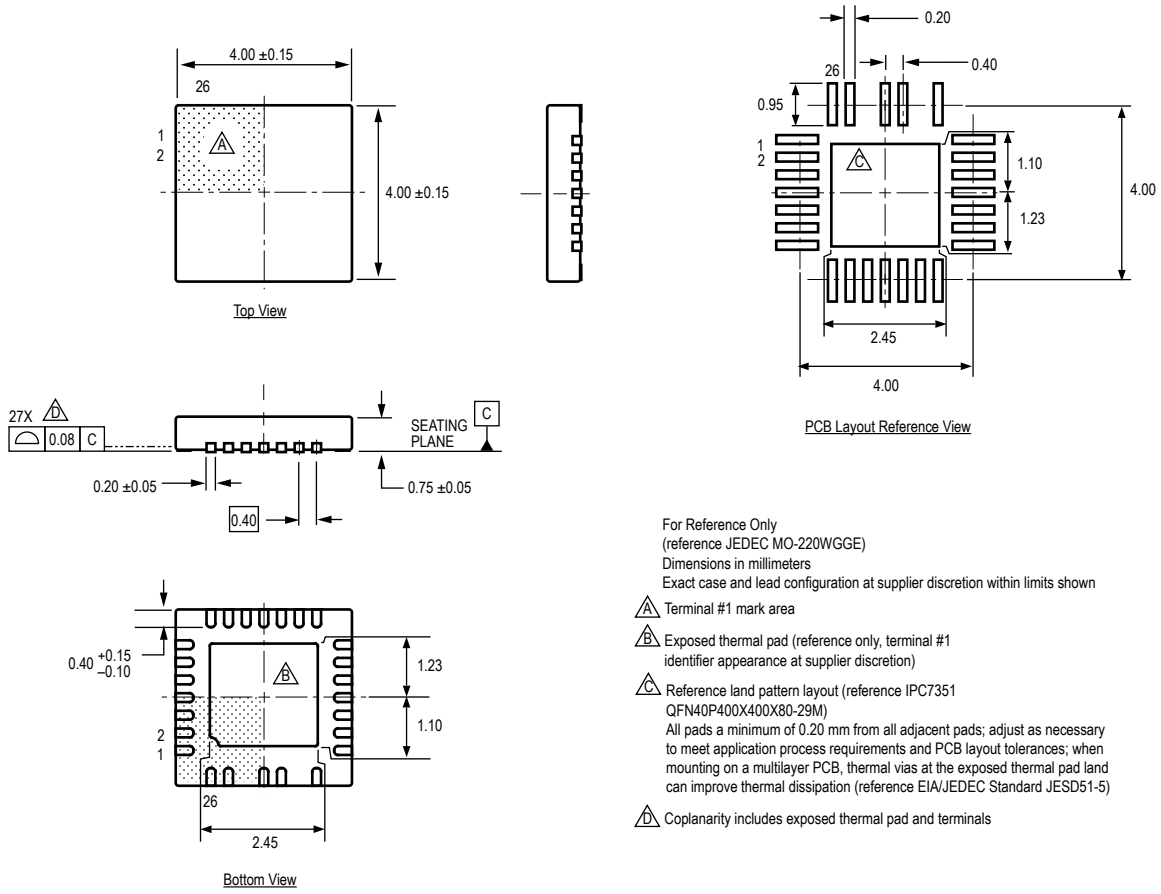
Package EC, 26-contact QFN



For Reference Only
(reference JEDEC MO-220WGGE)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN40P400X400X80-29M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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