DESCRIPTION

The A8600 is a high-efficiency driver for white light-emitting diodes (LED(s)). It is designed for large liquid-crystal displays (LCD(s)) that employ an array of LED(s) as the light source. A current-mode step-up controller drives up to six parallel strings of multiple series-connected LED(s). Each string is terminated with ballast that achieves ±1.5% current regulation accuracy, ensuring even bright-ness for all LED(s).

The A8600 has a wide input-voltage range from 4.5V to 26V, and provides a fixed 20mA or adjustable 15mA to 25mA full-scale LED current. The A8600 has two dimming control modes to enable a wide variety of applications. In direct DPWM mode, the LED current is directly turned on and off by a PWM signal. In analog dimming mode, an internal phase-locked loop (PLL) circuit translates the PWM signal into an analog signal and linearly controls the LED current down to 12.5%. Below 12.5%, digital dimming is added to allow lower average LED current down to 1%. Both control methods provide 100:1 dimming range. The A8600 has multiple features to protect the controller from fault conditions. Separate feedback loops limit the output voltage if one or more LED(s) fail open or short. The controller features cycle-by cycle current limit to provide consistent operation and soft-start capability. A thermal shutdown circuit provides another level of protection. The step-up controller uses an external MOSFET, which provides good efficiency and allows for scalable output power and maximum operating voltage. Low feedback voltage at each LED string (450mV) helps reduce power loss. The A8600 features selectable switching frequency (500kHz, 750kHz, or 1MHz), which allows trade-offs between external component size and operating efficiency.

The A8600 is available in QFN20 (4x4) Package.

ORDERING INFORMATION

Package Type	Part Number	
QFN20	Q20	A8600Q20R
		A8600Q20VR
Note	R: Tape & Reel V: Green Package	
AiT provides all Pb free products, suffix " V " means Green Package		

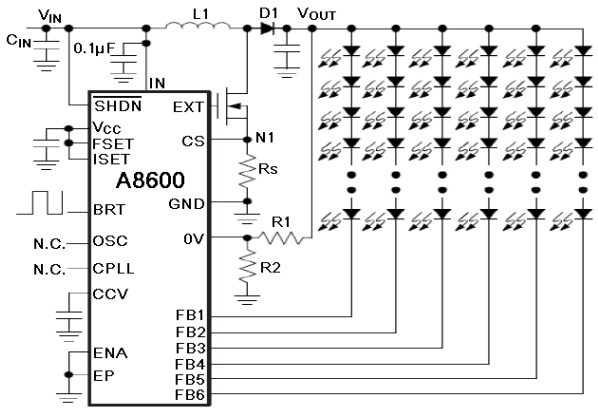
FEATURES

- Drives Six Parallel Strings with Multiple Series-connected LED(s) per String
- ±1.5% Current Regulation Accuracy Between Strings
- Low 450mV Feedback Voltage at Full Current Improves Efficiency
- Step-Up Controller Regulates the Output Just Above the Highest LED String Voltage
- Full-Scale LED Current Adjustable from 15mA to 25mA, or Preset 20mA
- Wide 100:1 Dimming Range
- Programmable Dimming Control: Direct DPWM or Analog Dimming
- Built-In PLL for Synchronized Dimming Control Open and Short LED Protections
- Output Over voltage Protection
- Wide Input Voltage Range from 4.5V to 26V
- External MOSFET Allows a Large Number of LED(s) per String
- 500kHz/750kHz/1MHz Switching Frequency
- Available in QFN20 (4x4) Package

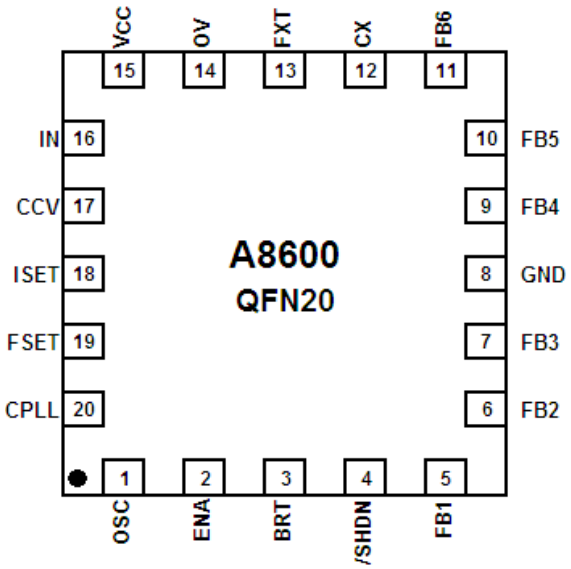
APPLICATIONS

- Notebook, Sub notebook, and Tablet Computer Displays
- Automotive Systems
- Handy terminals

TYPICAL APPLICATION



PIN DESCRIPTION



Top View

Pin #	Symbol	Function
1	OSC	Oscillator Frequency Selection Pin. Connect OSC to V_{CC} to set the step-up converter's oscillator frequency to 1MHz. Connect OSC to GND to set the frequency to 500kHz. Float OSC to set the frequency to 750kHz.
2	ENA	Analog Dimming Enable. ENA sets the PWM control mode. Set ENA low to enable direct DPWM dimming. Set ENA HIGH to enable analog dimming. In both modes, the duty cycle of the PWM signal at the BRT input controls the LED current characteristics. See the Dimming Control section for a complete description.
3	BRT	Brightness Control Input. The duty cycle of this digital input signal controls the LED current characteristics. The allowable frequency range is 100Hz to 500Hz in analog dimming mode. The duty cycle can be 100% to 1%. The BRT frequency can go above 500Hz in direct DPWM mode as long as the BRT pulse width is greater than 50µs minimum. See the Dimming Control section for a complete description.
4	/SHDN	Shutdown Control Input. The A8600 shuts down when /SHDN is less than 0.8V. Pulling /SHDN above 2.1V enables the A8600. /SHDN can be connected to the input voltage if desired.
5	FB1	LED String 1 Cathode Connection. FB1 is the open-drain output of an internal regulator, which controls current through FB1. FB1 can sink up to 27mA. If unused, connect FB1 to GND.
6	FB2	LED String 2 Cathode Connection. FB2 is the open-drain output of an internal regulator, which controls current through FB2. FB2 can sink up to 27mA. If unused, connect FB2 to GND.
7	FB3	LED String 3 Cathode Connection. FB3 is the open-drain output of an internal regulator, which controls current through FB3. FB3 can sink up to 27mA. If unused, connect FB3 to GND.

8	GND	Ground
9	FB4	LED String 4 Cathode Connection. FB4 is the open-drain output of an internal regulator, which controls current through FB4. FB4 can sink up to 27mA. If unused, connect FB4 to GND.
10	FB5	LED String 5 Cathode Connection. FB5 is the open-drain output of an internal regulator, which controls current through FB5. FB5 can sink up to 27mA. If unused, connect FB5 to GND.
11	FB6	LED String 6 Cathode Connection. FB6 is the open-drain output of an internal regulator, which controls current through FB6. FB6 can sink up to 27mA. If unused, connect FB6 to GND.
12	CS	Step-Up Controller Current-Sense Input. Connect the CS input to a ground referenced sense resistor to measure the current in the external MOSFET switch.
13	EXT	External MOSFET Gate-Drive Output
14	OV	Over voltage Sense. Connect OV to the center tap of a resistive detection threshold for voltage limiting at OV is 1.23V (typ).
15	V_{CC}	5V Linear Regulator Output. VCC provides power to the A8600 and is also used to bias the gate driver for the external MOSFET. Bypass VCC to GND with a ceramic capacitor of 1μF or greater. If VIN is less than or equal to 5.5V, connect VCC to IN to the disable the internal LDO and use the external 5V supply to V_{CC}. When /SHDN is low, the internal linear regulator is disabled.
16	IN	Supply Input. VIN biases the internal 5V linear regulator that powers the device. Bypass IN to GND directly at the pin with a 0.1μF or greater ceramic capacitor.
17	CCV	Step-Up Converter Compensation Pin. Connect a 0.1μF ceramic capacitor and 1.2kΩ resistor from CCV to GND. When the A8600 shuts down, CCV is discharged to 0V through an internal 20kΩ resistor.
18	ISET	Full-Scale LED Current Adjustment Pin. The resistance from ISET to GND controls the full-scale current in each LED string: I_{LEDmax} = 20mA x 100kΩ/R_{ISET} The acceptable resistance range is 74kΩ < R_{ISET} < 133kΩ, which corresponds to full-scale LED current of 27mA > I_{LEDmax} > 15mA. Connect ISET to V_{CC} for a default full-scale LED current of 20mA.
19	FSET	PLL Free-Running Frequency Control Pin. The resistance from FSET to GND controls the PLL oscillator's free-running frequency, f_{PLL}: f_{PLL} = 1 / (10 x R_{FSET} x 800pF) The capture range is 0.6 x f_{PLL} to f_{PLL}. The acceptable resistance range for FSET is 250kΩ < R_{FSET} <754kΩ, which corresponds to a frequency range of 500Hz > f_{PLL} > 166Hz. The resulting capture frequency range is 100Hz to 500Hz.
20	CPLL	Phase-Locked Loop-Compensation Capacitor Pin. The capacitance at CPLL compensates the PLL loop response. Connect a 0.1μF ceramic capacitor from CPLL to GND.
EP	EP	Exposed Backside Pad. Solder to the circuit board ground plane with sufficient copper connection to ensure low thermal resistance. See the PCB Layout Guidelines section.

ABSOLUTE MAXIMUM RATINGS

IN,/SHDN, to GND	-0.3V ~ 28V
FB_ to GND	-0.3V ~ 28V
V_{CC}, BRT, ENA, OSC, OV to GND	-0.3V ~ 6.0V
ISET, CCV, CS to GND	-0.3V to V_{CC} +0.3V
FSET, CPLL, EXT to GND	-0.3V to V_{CC} +0.3V
Continuous Power Dissipation (T_A=+70℃)	20-Pin
Thin QFN (derate 16.9mW/℃ above +70℃)	1349mW
Maximum Junction Temperature	150℃
Operating Temperature Range	-40℃ to 85℃
Storage Temperature Range	-65℃ to 125℃
Lead Temperature (Soldering, 10s)	300℃

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL INFORMATION

Thermal Resistance (θ_{JA})	37℃/W
(θ_{JC})	20℃/W

Thermal Resistance is specified with approximately 1 square inch of 1 oz. copper.

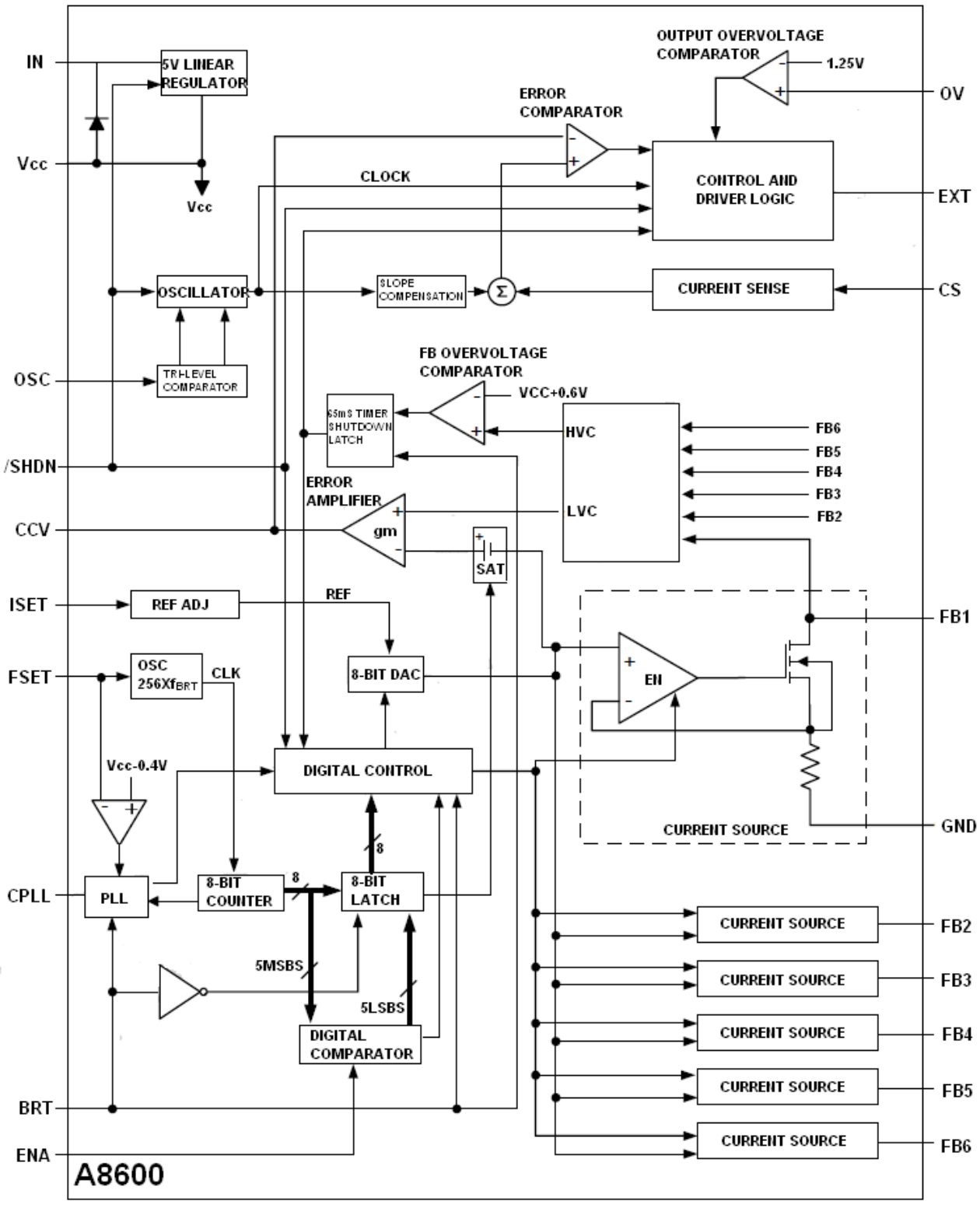
ELECTRICAL CHARACTERISTICS

(V_{IN}=12V, $V_{/SHDN}$=V_{IN}, CCV=0.1μF, T_A=0℃ to +85℃, unless otherwise specified. Typical values are at T_A=25℃.)

Parameter	Conditions		Min	Typ.	Max	Units
IN Input Voltage Range	V_{IN}=V_{CC}		4.5	-	5.5	V
	V_{CC}=bypassed to GND through 1uF capacitor		5.5	-	26.0	
IN Quiescent Current	$V_{/SHDN}$=high	V_{IN}=26V	-	1	2	mA
	BRT=GND	V_{IN}=V_{CC}=5V	-	1	2	
V_{CC} Output voltage	$V_{/SHDN}$=5V,6V < V_{IN} < 26V, 0 < I_{VCC} < 10mA		4.7	5	5.3	V
V_{CC} Short Circuit Current	-		15	56	130	mA
V_{CC} UVLO Threshold	Rising edge, hysteresis=20mV		4	4.25	4.45	V
EXT High Level	10mA from EXT to GND		V_{CC}-0.1	V_{CC}	-	V
EXT Low Level	-10mA from EXT to V_{CC}		-	0	0.1	V
EXT On-Resistance	EXT high or low		-	2	5	Ω
EXT Sink/Source Current	EXT forced to 2V		-	1	-	A
OSC High-Level Threshold	-		V_{CC}-0.4	-	-	V
OSC Midlevel Threshold	-		1.5	-	V_{CC}-2.0	V
OSC Low-Level Threshold	-		-	-	0.4	V
Operating Frequency	V_{OSC}=V_{CC}		0.9	1	1.1	MHz
	V_{OSC}=open		675	750	825	kHz
	V_{OSC}=GND		450	500	550	
Minimum Duty Cycle	PWM mode		-	10	-	%
	Pulse skipping, no load		-	0	-	
Maximum Duty Cycle	-		94	95	-	%
CS Trip Voltage	Duty cycle=75%		85	100	115	mV
/SHDN Logic-Input High Level	-		2.1	-	-	V
/SHDN Logic-Input Low Level	-		-	-	0.8	V
BRT, ENA Logic-Input High Level	-		2.1	-	-	V
BRT, ENA Logic-Input Low Level	-		-	-	0.8	V
/SHDN Leakage Current	/SHDN=26V		-	-	+42	μA
CS Leakage Current	V_{CS}=GND		-	+40	+50	μA
OSC Leakage Current	-		-3	-	+3	μA
BRT,ENA Leakage Current	-		-1	-	+1	μA
FSET,ISET Leakage Current	FSET=ISET=V_{CC}		-1	-	+1	μA
OV Leakage Current	-		-0.1	-	+0.1	μA
ISET Voltage	-		1.12	1.19	1.26	V
ISET High-Level Threshold	Default setting for 20mA full-scale LED current		V_{CC}-0.4	-	-	V

Parameter	Conditions	Min	Typ.	Max	Units
Full-Scale FB-Output Current	SET=V_{CC}, BRT=100%	19.4	20	20.6	mA
	R_{ISET}=80kΩ to GND, BRT=100%	24.25	25	25.75	
	R_{ISET}=133kΩ to GND, BRT=100%	14.4	15	15.6	
20% Output Current	ISET=V_{CC},BRT=20%	3.84	4	4.16	mA
Current Regulation Between Strings	ISET=V_{CC},BRT=100%	-1.5	-	+1.5	%
	ISET=V_{CC},BRT=20%	-2.0	-	+2.0	
Minimum FB-Regulation Voltage	R_{ISET}=80kΩ to GND, BRT=100%	300	500	800	mV
	ISET=V_{CC},BRT=100%	270	450	720	
	ISET=V_{CC},BRT=12.5%	150	275	500	
Maximum FB_Ripple	ISET=V_{CC},C_{OUT}=1μF, OSC=V_{CC}	-	120	200	mV_{P-P}
FB-On-Resistance	V_{FB-} =50mV	-	13	20	Ω
FB-Leakage Current	/SHDN=GND,V_{FB}-=26V	-	-	1	μA
	/SHDN=V_{IN},BRT=GND, V_{FB-}=15V	-	10	28	
BRT Input Frequency	-	100	-	500	Hz
Minimum BRT Duty Cycle	PLL active	-	12.5	-	%
OV Threshold Voltage	-	1.16	1.23	1.30	-
FB_ Over voltage Threshold	-	V_{CC}+0.2	V_{CC}+0.6	V_{CC}+1.45	V
FAULT Shutdown Timer	V_{FB-}>5.6V(typ)	50	65	80	ms
Thermal-Shutdown Threshold	-	-	170	-	℃
FSET High-Level Threshold	PLL disabled	V_{CC}-0.4	-	-	V
BRT Frequency Capture Range	R_{FSET}=500kΩ	150	200	250	Hz
	R_{FSET}=250kΩ	300	400	500	

BLOCK DIAGRAM



DETAILED INFORMATION

Operation

The A8600 is a high-efficiency driver for arrays of white LED(s). It contains a fixed frequency, current mode, PWM step-up controller, 5V linear regulator, dimming control circuit, and six regulated current sources (see Figure 2). When enabled, the step-up controller boosts the output voltage to provide sufficient headroom for the current sources to regulate their respective string currents. The A8600 features selectable switching frequency (500kHz, 750kHz, or 1MHz), which allows trade-offs between external component size and operating efficiency. The control architecture automatically skips pulses at light loads to improve efficiency and prevents overcharging the output capacitor.

A PWM logic input signal, BRT, controls the LED brightness. The A8600 supports both analog and digital control of the LED current, and achieves 100:1 dimming range. The A8600's dimming control circuit consists of a PLL, a digital comparator, and a DAC. In direct DPWM mode, the step-up controller and current source are directly turned on and off by the PWM signal. In analog dimming mode, an internal PLL, digital comparator, and DAC circuit translate the PWM signal into an analog signal that linearly controls the LED current, down to a PWM duty factor of 12.5%.

The A8600 has multiple features to protect the controller from fault conditions. Separate feedback loops limit the output voltage if one or more LED(s) fail open or short. During operation, if one or more strings fails, the corresponding current sources are disabled after an internal timer expires. The remaining LED Strings still operate normally. If all strings fails, the controllers shuts down and latches off. The controller features cycle-by-cycle current limit to provide consistent operation and soft-start capability. A thermal-shutdown circuit pro-vides another level of protection.

The A8600 includes a 5V linear regulator that provides the internal bias and gate drive for the step-up controller. When an external 5V is available, the internal LDO can be overdriven to decrease power dissipation. Otherwise, connect the IN pin to an input greater than 5.5V. The internal LDO is disabled when /SHDN is low.

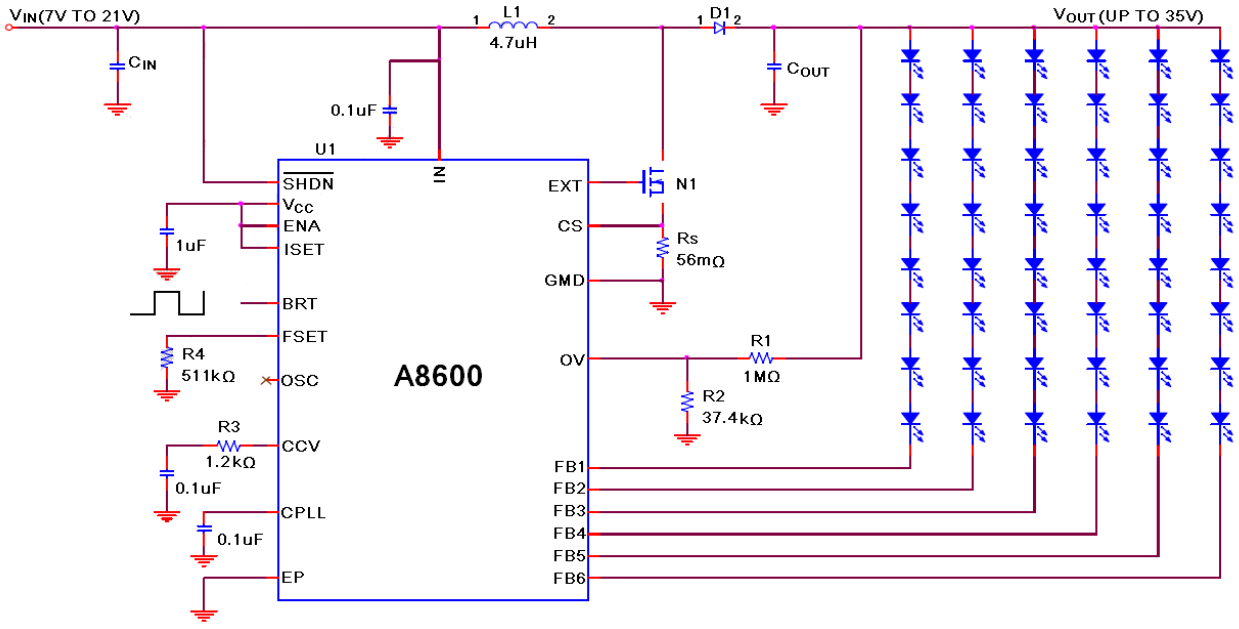


Figure 1.Typical Operating Circuit

Fixed Frequency Step-up Controller

The A8600's fixed-frequency, current mode, step up controller automatically chooses the lowest active FB_ voltage to regulate the feedback voltage. Specifically, the difference between the lowest FB_ voltage and the current source-control signal plus an offset (V_{SAT}) is integrated at the CCV output. The resulting error signal is compared to the external switch current plus slope compensation to terminate the switch on time. As the load changes, the error amplifier sources or sinks current to the CCV output to adjust the required peak inductor current. The slope-compensation signal is added to the current-sense signal to improve stability at high duty cycles.

At light loads, the A8600 automatically skips pulses to improve efficiency and prevent overcharging the output capacitor. In SKIP mode, the inductor current ramps up for a minimum on-time of approximately 150ns, then discharges the stored energy to the output. The switch remains off until another pulse is needed to boost the output voltage.

Internal 5V Linear Regulator V_{CC} and UVLO

The A8600 includes an internal low dropout linear regulator (V_{CC}). When VIN is higher than 5.5V and /SHDN is high, this linear regulator generates a 5V supply to power an internal PWM controller, control logic, and MOSFET driver. This linear regulator can deliver at least 10mA of total additional load current. If V_{IN} is less than or equal to 5.5V, V_{CC} and IN can be connected together and powered from an external 5V supply. There is an internal diode from V_{CC} to IN, so V_{IN} must be greater than V_{CC} (see Figure 2).

The A8600 includes UVLO protection. The controller is disabled until V_{CC} exceeds the UVLO threshold of 4.25V (typ). Hysteresis on UVLO is approximately 20mV. The V_{CC} pin should be bypassed to GND with a 1µF or greater ceramic capacitor.

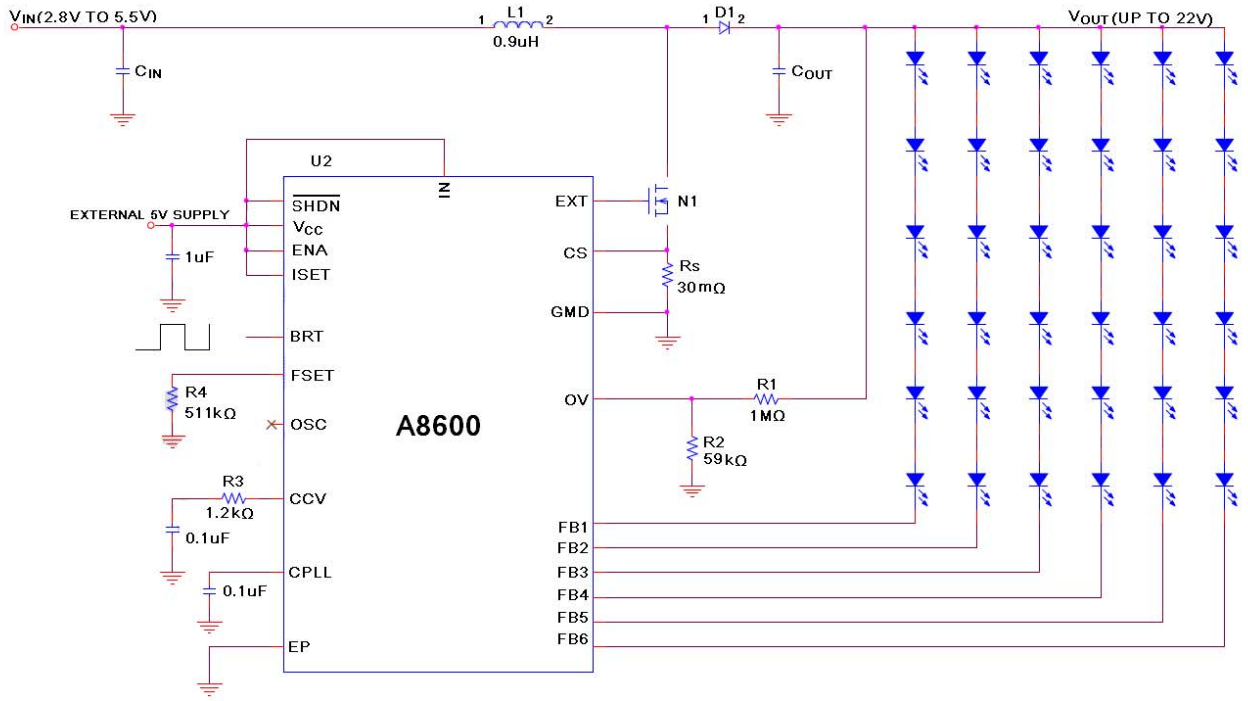


Figure 2 Low-Input-Voltage Application Circuit

Startup

At startup, the A8600 checks each FB_ pin to determine if the respective current string is enabled. Each FB_ pin is internally pulled up with a 180µA current source. If an FB_ pin is connected to GND, the corresponding string current source is disabled. This feedback scan takes approximately 4.2ms, after which the step-up converter begins switching.

Shutdown

When the /SHDN pin is less than 0.8V, the A8600 shuts down the internal LDO, the reference, current sources, and all control circuitry. The resulting supply current is less than 10µA. While the n-channel MOSFET is turned off, the step-up regulator's output is connected to IN through the external inductor and rectifier diode.

Frequency Selection

A tri-level OSC input sets the internal oscillator frequency for the step-up converter, as shown in Table 1. High frequency (1MHz) operation optimizes the regulator for the smallest component size, at the expense of efficiency due to increased switching losses. Low-frequency (500kHz) operation offers the best overall efficiency, but requires larger components and PCB area.

Table 1 Frequency Selection

OSC	SWITCH FREQUENCY(kHz)
GND	500
Open	750
V_{CC}	1000

Over voltage Protection

To protect the step-up converter when the load is open, or the output voltage becomes excessive for any reason, the A8600 features a dedicated over voltage feedback input (OV). The OV pin is connected to the center tap of a resistive voltage-divider from the high voltage output (see Figure 1). When the A8600 is powered up, if none of the LED strings on FB1–FB6 are connected to the step-up converter output, the step-up converter regulates the output voltage to V_{OUT} =1.23V(1 + R1 / R2). When V_{OV} exceeds 1.23V, a comparator turns off N1. The step-up converter switch is reenabled after the output voltage drops below the protection threshold.

LED Current Sources

Maintaining uniform LED brightness and dimming capability are critical for LCD backlight applications. The A8600 is equipped with a bank of six matched current sources. These specialized current sources are accurate to within ±1.5% and can be switched on and off within 10µs, enabling PWM frequencies of up to 2kHz. All LED full-scale currents are identical and are set through the ISET pin (15mA < ILED < 27mA).

The minimum voltage drop across each current source is approximately 450mV at 20mA. The low voltage drop helps reduce dissipation while maintaining sufficient compliance to control the LED current within the required tolerances.

The LED current sources can be disabled by grounding the respective FB_ pin at startup. When the IC is powered up, the controller scans settings for all FB_ pins. If an FB_ pin is not grounded, an internal circuit pulls this pin high, and the controller enables the corresponding current source to regulate the string current. If the FB_ pin is grounded, the controller disables the corresponding current regulator. The current regulator

cannot be disabled by grounding any of the FB_ pins after the IC is powered up.
All FB_ pins in use are measured and the highest signal (HVC) and the lowest signal (LVC) are extracted for two feedback loops. HVC is used to identify excessive dissipation across the current-source inputs. When HVC is greater than V_{CC} + 0.6V (typ) for greater than 65ms (see the Current-Source Fault Protection section), a fault latch is set and the A8600 is shut down. The LDO output is not affected by the fault latch. LVC is fed into the step-up converter's error amplifier to regulate the step-up converter's output voltage.

Current-Source Fault Protection

The LED current sources are protected against string open, short, and gross mismatch faults, using over voltage detection circuitry on each FB_ pin. If any of these three fault conditions persists for a preset duration, the fault strings are disabled. The duration of the fault time depends on the dimming mode and the duty cycle of the BRT input (DBRT). In the DPWM mode, the timeout interval is:

$$t_{TIMEOUT\_DPWM} = 65ms/D_{BRT}$$

In analog dimming mode, the fault time is fixed at 65ms for D_{BRT} greater than 12.5%. When D_{BRT} is less than 12.5%, the timeout interval is:

$$t_{TIMEOUT\_ANALOG} = 8.125ms/D_{BRT}$$

The fault latch can be cleared by cycling the power or toggling the shutdown pin/SHDN.

Open-Current Source Protection

The A8600 step-up converter output voltage is regulated according to the minimum value of the enable FB_ voltages. If an individual LED string is open, the respective FB_ is pulled down to near ground. In this situation, the step-up converter output voltage increases but is clamped to a level set with the OV feedback input. When this elevated output voltage is applied to the undamaged strings, excessive voltage drop develops across the FB_ pins. If the resulting HVC signal exceeds V_{CC} + 0.6V for greater than 65ms, the fault strings are disabled to protect the circuit.

LED-Short and String Mismatch Protection

Normally, white LED(s) have variations in forward-voltage drop of 3.1V to 3.6V. The A8600 can tolerate slight mismatches between LED strings. When the sum of the LED forward voltages creates a mismatch in the strings so the HVC signal exceeds V_{CC} + 0.6V for greater than 65ms, the fault condition circuit is triggered in much the same way as the circuit responds to open string faults. Similar protection is activated when an LED is shorted. The larger the number of series-connected LED(s) (N), the smaller the tolerable mismatch between LED(s):

$$\sum_{N} Error < V_{CC} + 0.6V - V_{SAT}$$

$$V_{SAT} \approx 450mV \text{ and } V_{CC} = 5V$$

$$\sum_{N} Error < 5.150V$$

$$\text{Average Error Per LED} = \frac{5.150V}{N}$$

For N = 8, the average error per LED = 644mV.
For N = 10, the average error per LED = 510mV.
The larger the total mismatch, the larger the voltage drop required across each current source to correct for the error, and therefore the larger the dissipation within the A8600.

Dimming Control

The A8600 features both analog and digital dimming control. Analog dimming can provide potentially higher converter efficiency because of low voltage drop across each WLED when the current is low. Digital dimming (DPWM) provides less WLED color distortion since the WLED current is held at full scale when the WLED is on. The A8600's dimming control circuit consists of a PLL, a digital comparator, and a DAC. The controller provides 100:1 dimming range through either analog or digital control methods. Both methods translate the duty cycle of the BRT input into a control signal for the LED current sources. In analog dimming mode, the current-source outputs are DC and the BRT duty cycle (12.5% < D_{BRT} < 100%) modulates the amplitude of the currents. For D_{BRT} < 12.5%, the LED current is digitally modulated to reduce the average LED current down to 1% of full scale. The PLL detects the BRT frequency and phase, and adjusts the current-source amplitude and duty cycle synchronously (see Figure4).
In digital dimming mode, the step-up controller and current source are directly turned on and off by the PWM signal. The current pulse magnitude, or full-scale current, is set by ISET and is independent of PWM duty factor. The current-source outputs are PWM signals synchronized to the BRT input signal (see Figure 5).
The full-scale current in both methods is specified by resistance from the ISET pin to ground:

$$I_{LED\,\max} = \frac{20mA \times 100k\Omega}{R_{ISET}}$$

The acceptable resistance range is 74kΩ < R_{ISET} <133kΩ, which corresponds to full-scale LED current of 27mA > I_{LEDmax} > 15mA. Connect ISET to V_{CC} for a default full-scale LED current of 20mA. When ENA is high, the analog dimming is enabled, when ENA is low, digital dimming is enabled.
When the current-source output is pulse width modulated, current-source turn-on is synchronized with the BRT signal. Synchronization and low jitter in the PWM signals help reduce flicker noise in the display. The current through each FB_ pin is controlled only during the step-up converter's on-time. During the converter's off-time, the current sources are turned off. The output voltage does not discharge and stays high. Each FB_ pin can withstand 28V, which is the pin's maximum rated voltage.
Table 2 summarizes the characteristics of both analog and digital dimming methods. A PLL translates the duty cycle of the BRT input into a reference for the A8600's current sources. A resistor from the FSET pin to ground controls the PLL's free running frequency:

$$f_{PLL} = \frac{1}{10 \times R_{FSET} \times 800pF}$$

The PLL's loop filter bandwidth is set with a capacitor from the CPLL pin to ground. This filter integrates the phase difference between the BRT input signal and the PLL oscillator. The filter bandwidth determines the PLL's dynamic response to frequency changes in the BRT signal. For most applications, a 0.1µF capacitor is adequate for oscillator frequencies in the 166Hz < f_{PLL}< 500Hz range. The PLL frequency capture window is 0.6 x f_{PLL} to f_{PLL}.

The PLL is disabled in DPWM mode; consequently, the BRT frequency is not limited by f_{PLL}. The maximum BRT frequency is determined by the minimum BRT on-time of 50μs and the minimum acceptable dimming factor. If a 1% dimming factor is needed, the maximum BRT frequency is 200Hz. If a 10% dimming factor is acceptable, the maximum BRT frequency is 2kHz.

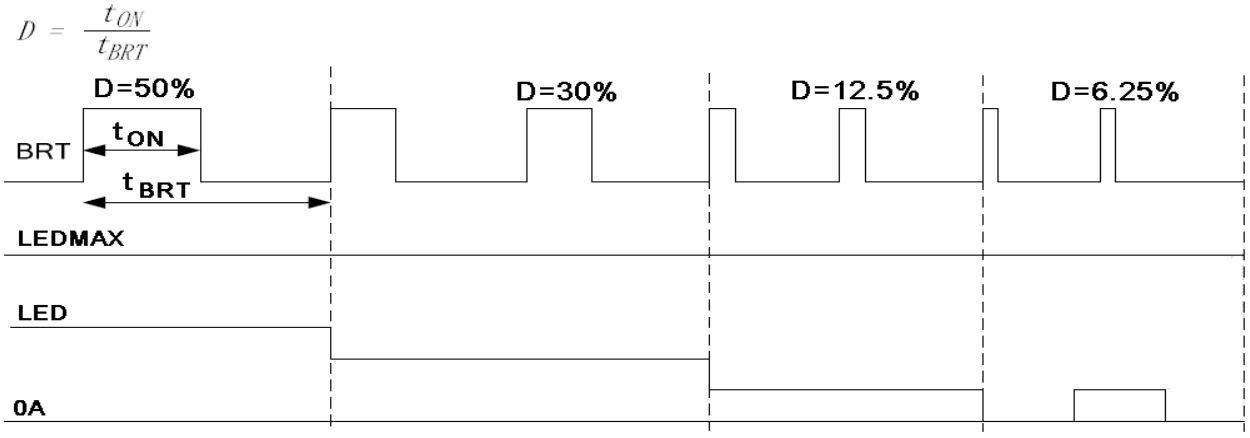


Figure 3.LED Current Control Using Analog Dimming Mode

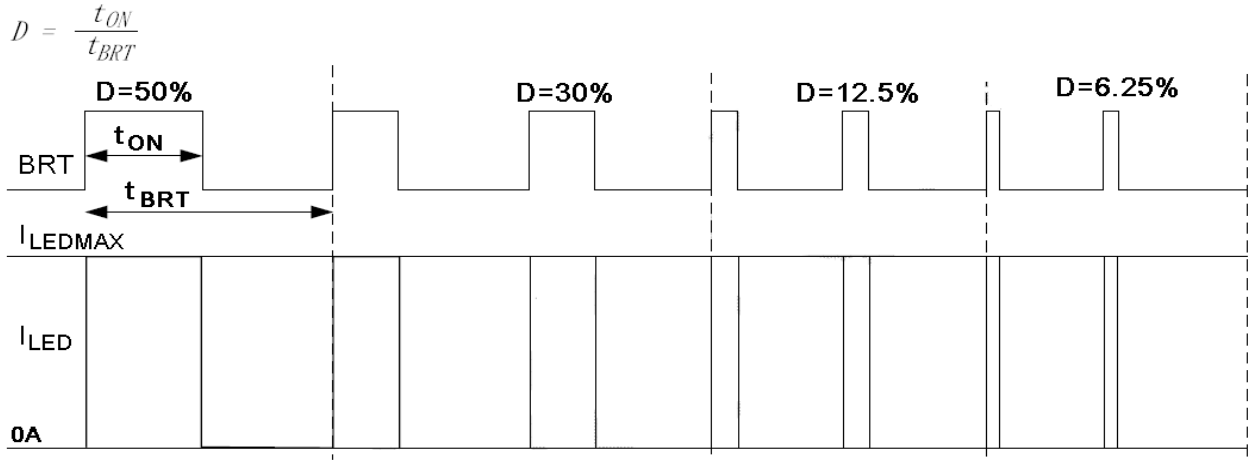


Figure 4.LED Current Control Using DPWM Dimming Mode

Table 2.Dimming Mode

MODE	ENA	PLL FREQUENCY	CPLL	DESCRIPTION
Analog+DPWM	>2.1V	250 kΩ<RFSET<754 kΩ	0.1uF	Analog dimming from 100% to 12.5% brightness. From 12.5% to 1% brightness, DPWM dimming is employed. BRT frequency is 100Hz to 500Hz.
Direct DPWM	<0.8V	V_{FSET}>V_{CC}-0.4V, disable PLL	OPEN	Direct dimming by BRT signal. BRT frequency can be 100Hz to 2kHz; 50us minimum BRT on-time limits the minimum brightness.

In analog dimming mode, load-current transients can occur when the BRT frequency abruptly changes on the fly. Large regulation transients induce a flash on the LED load that is observable with the naked eye and should therefore be avoided. Such annoying flashes can be eliminated by dynamically changing the ENA pin setting. When a capacitor is connected to the CPLL pin and the ENA pin is grounded, the PLL continues to run but does not affect the dimming. When fast PLL lockup transitions are required, the ENA pin can be momentarily pulled to ground; after the PLL is locked up, ENA can be pulled high to reenable PLL in dimming control.

Table 3.Component List

CIRCUIT	FIGURE 1	FIGURE 1	FIGURE 1	FIGURE 2
Switching Frequency	1MHz	750kHz	500kHz	750kHz
White LED	3.2V(typ), 3.5V (max) at 20mA Nichia NSSW008C	3.2V(typ), 3.5V (max) at 20mA Nichia NSSW008C	3.2V(typ), 3.5V (max) at 20mA Nichia NSSW008C	3.2V(typ), 3.5V (max) at 20mA Nichia NSSW008C
Number of White LEDs	6 series x 6 parallel, 20mA (max)	8series x 6 parallel, 20mA (max)	10series x 6parallel, 25mA (max)	6series x 6parallel, 20mA (max)
Input Voltage	4.5V to 5.5V, V_{CC} = IN	7V to 21V	7V to 21V	2.8V to 5.5V, V_{CC} = 5V
Inductor L1	2.2μH , 2.5A power inductor Sumida CDRH5D16-2R2	4.7μH , 2.05A power inductor Sumida CDRH5D16-4R7	4.7μH , 3.6A power inductor Sumida CDRH8D28-4R7	0.9μH, 4.7A power inductor Sumida CDRH5D16-0R9
Input Capacitor	10μF ±10%, 10V X5R ceramic capacitor (1206) Murata GRM31MR61A106K	10μF ±10%, 25V X5R ceramic capacitor (1206) Murata GRM 31CR61E106KA	10μF ±10%, 25V X5R ceramic capacitor (1206) Murata GRM31CR61E106KA	10μF ±10%, 10V X5R ceramic capacitor (1206) Murata GRM31MR61A106K
COUT Output Capacitors	2.2μF ±10%, 50V X7R ceramic capacitor (1x) Murata GRM31CR71H225K	2.2μF ±10%, 50V X7R ceramic capacitor (1206)(1x) Murata GRM31CR71H225K	4.7μF ±10%, 50V X7R ceramic capacitor (1210) (1x) Murata GRM32ER71H475K	2.2μF ±10%, 50V X7R ceramic capacitor (1x) Murata GRM31CR71H225K
MOSFET N1	30V, 3A n-channel MOSFET(6-pin SC70) Vishay Si1402DH	60V, 2.8A n-channel MOSFET(6-pin TSOP) Fairchild semiconductor FDC5612 Sanyo Semiconductor CPH6424	60V , 6A n- channel MOSFET (Power PAK 1212- 8) Vishay Si7308DN	30V, 4.9A n-channel MOSFET (6-pin TSOP) Vishay Si3456BDV
Diode Rectifier D1	2A, 30V Schottky diode Nihon EC21QS03L	2A, 40V Schottky diode Toshiba CMS11 Nihon EC21QS04	3A, 60V Schottky diode Nihon EC31QS06	3A, 30V Schottky diode Nihon EC31QS03L
Sense Resistor	50mP ±1%, 1/2W IRC LRC-LRF-1206LF-01-R050-F	56mP ±1%, 1/2W IRC LRC-LRF-1206LF-01-R056-F	40mP ±1%, 1/2W IRC LRC-LRF-1206LF-01-R040-F	30mP ±1%, 1/2W IRC LRC-LRF-1206LF-01-R030-F

Thermal Shutdown

The A8600 includes a thermal-protection circuit. When the local IC temperature exceeds +170℃(typ), the controller and current sources shut down and do not restart until the die temperature drops by 15℃.

Application Information

All A8600 designs should be prototyped and tested prior to production. Table 3 provides a list of power components for the typical applications circuit. External component value choice is primarily dictated by the output voltage and the maximum load current, as well as maximum and minimum input voltages. Begin by selecting an inductor value. Once L is known, choose the diode and capacitors.

Inductor Selection

The inductance, peak current rating, series resistance, and physical size should all be considered when selecting an inductor. These factors affect the converter's operating mode, efficiency, maximum output load capability, transient response time, output voltage ripple, and cost. The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance minimizes the current ripple, and therefore reduces the peak current, which decreases core losses in the inductor and I2R losses in the entire power path.

However, large inductor values also require more energy storage and more turns of wire, which increases physical size and I2R copper losses in the inductor. Low inductor values decrease the physical size, but increase the current ripple and peak current. Finding the best inductor involves the compromises among circuit efficiency, inductor size, and cost. When choosing an inductor, the first step is to determine the operating mode: continuous conduction mode (CCM) or discontinuous conduction mode (DCM).

The A8600 has a fixed internal slope compensation, which requires a minimum inductor value. When CCM mode is chosen, the ripple current and the peak current of the inductor can be minimized. If a small-size inductor is required, DCM mode can be chosen. In DCM mode, the inductor value and size can be minimized but the inductor ripple current and peak current are higher than those in CCM. The controller can be stable, independent of the internal slope compensation mode, but there is a maximum inductor value requirement to ensure the DCM operating mode. The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full-load current.

The controller operates in DCM mode when LIR is higher than 2.0, and it switches to CCM mode when LIR is lower than 2.0. The best tradeoff between inductor size and converter efficiency for step-up regulators generally has an LIR between 0.3 and 0.5.

However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of required turns and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can reduce losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, LIR higher than 2.0 can be chosen for DCM operating mode. Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

The detail design procedure can be described as follows: Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{OUT(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the Typical Operating Characteristics, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN\_MIN}}{V_{OUT}}\right)^2 \left(\frac{V_{OUT} - V_{IN\_MIN}}{I_{OUT(MAX)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

The A8600 has a minimum inductor value limitation for stable operation in CCM mode at low input voltage because of the internal fixed slope compensation. The minimum inductor value for stability is calculated by the following equation:

$$L_{CCM(MIN)} = \frac{(V_{OUT(MAX)} + V_{DIODE} - 2 \times V_{IN(MIN)}) \times R_S}{51mV \times f_{OSC(MIN)}}$$

where 51mV is a scale factor based on slope compensation, and R_S is the current sense resistor. To determine the minimum inductor value, the R_S can be temporarily calculated using the following equation:

$$R_{S-TMP} = \frac{100mV}{1.2 \times I_{IN(DCMAX)}}$$

where 100mV is the current-limit sense voltage. The minimum inductor value should be recalculated after the RS is determined (see the Sense-Resistor Selection section).
Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$, using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the Typical Operating Characteristics:

$$I_{IN(DCMAX)} = \frac{I_{OUT(MAX)} \times V_{OUT}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times (V_{OUT(MAX)} - V_{IN(MIN)})}{L \times V_{OUT(MAX)} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

When DCM operating mode is chosen to minimize the inductor value, the calculations are different from that in the above CCM mode. The maximum inductor value for DCM mode is calculated by the following equation:

$$L_{DCM(MAX)} = \left(1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)} + V_{DIODE}}\right) \times \frac{V_{IN(MIN)}^2 \times \eta}{2 \times f_{OSC(MAX)} \times V_{OUT(MAX)} \times I_{OUT(MAX)}}$$

The peak inductor current in DCM mode is calculated using the following equation:

$$I_{PEAK} = \sqrt{\frac{I_{OUT(MAX)} \times 2 \times V_{OUT(MAX)} \times (V_{OUT(MAX)} + V_{DIODE} - V_{IN(MIN)})}{L \times f_{OSC(MIN)} \times \eta \times (V_{OUT(MAX)} + V_{DIODE})}}$$

The inductor's saturation current rating should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.
Considering the typical operating circuit, the maximum load current ($I_{OUT(MAX)}$) is 120mA with a 28.72V output and a minimal input voltage of 7V. Choosing a DCM operating mode and estimating efficiency of 90% at this operating point:

$$L_{DCM(MAX)} = \left(1 - \frac{7V}{28.72V + 0.4V}\right) \times \frac{(7V)^2 \times 0.9}{2 \times 0.825MHz \times 28.72V \times 120mA} = 5.8\mu H$$

An inductance less than $L_{DCM(MAX)}$ is required, so a 4.7μH inductor is chosen. The peak inductor current at minimum input voltage is calculated as follows:

$$I_{PEAK} = \sqrt{\frac{120mA \times 2 \times 28.72 \times (28.72V + 0.4V - 7V)}{4.7\mu H \times 0.675MHz \times 0.9 \times (28.72V + 0.4V)}} = 1.35A$$

Sense-Resistor Selection

The detected signal is fed into the step-up converter control compensation loop through the CS pin. The A8600's current mode step-up converter senses the switch current from CS to GND with an external resistor, R_S. The current-limit sense voltage is a fixed 100mV. The required resistance is calculated based upon the peak inductor current at the end of the switch on-time:

$$R_S < \frac{V_{CS\_EC} + 25.6mV \times (0.75 - D_{MAX})}{I_{PEAK}}$$

where 25.6mV is a scale factor from slope compensation, V_{CS_EC} is the current-sense voltage listed in the Electrical Characteristics table (85mV),and the D_{MAX} is the maximum duty cycle at minimum input voltage and maximum output voltage. In DCM operating mode, it is calculated by the following equation:

$$D_{MAX} = \frac{L \times I_{LIM} \times f_{OSC}}{V_{IN(MIN)}}$$

For the typical operating circuit as Figure 1:

$$D_{MAX} = \frac{4.7\mu H \times 1.35A \times 0.75MHz}{7V} = 0.68$$

$$R_S < \frac{85mV + 25.6mV \times (0.75 - 0.68)}{1.35A} = 64m\Omega$$

Again, R_S is calculated as a maximum, so a 56mP current-sense resistor is chosen. The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging on the output capacitor, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{OUT(MAX)}}{C_{OUT}} \left(\frac{V_{OUT(MAX)} - V_{IN(MIN)}}{V_{OUT(MAX)} f_{OSC}} \right)$$

And:

$$V_{RIPPLE(ESR)} = I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the Inductor Selection section).
The output voltage-ripple voltage should be low enough for the FB_ current-source regulation. The ripple voltage should be less than $200mV_{P-P}$. For ceramic capacitors, the output-voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

External MOSFET Selection

The A8600's step-up converter uses an external MOSFET to enable applications with scalable output voltage and output power. The boost switching architecture is simple and ensures that the controller is never exposed to high voltage. Only the external MOSFET, diode, and inductor are exposed to the output voltage plus one Scotty diode forward voltage:

$$V_{BV} = N \times V_{F\_LED} + V_{F\_SCHOTTKY} + V_{FB\_}$$

The MOSFET's breakdown ratings should be higher than V_{BV} with sufficient margin to ensure long-term reliability.

A conservative rule of thumb, a minimum 30% margin would be recommended for MOSFET breakdown voltage. The external MOSFET should have a current rating of no less than the I_{PEAK} derived from the Inductor Selection section. To improve efficiency, choose a MOSFET with low $R_{DS(ON)}$. The A8600's gate-drive linear regulator can provide 10mA. Select the external MOSFET with a total gate charge so the average current to drive the MOSFET at maximum switching frequency is less than 10mA:

$$Q_{g(MAX)} \times f_{OSC} < 10mA$$

For example, the Si3458DV is specified with 16nC of max total gate charge at Vg = 10V. For 5V of gate drive, the required gate charge is 8nC, which equates to 8mA at 1MHz The MOSFET conduction loss or resistive loss is caused by the MOSFET's on-resistance ($R_{DS(ON)}$). This power loss can be estimated as:

$$PD_{RES(MAX)} = \frac{R_{DS(ON)} \times L \times f_{OSC} \times I_{PEAK}^{3}}{3 \times V_{IN(MIN)}}$$

For the above Si3458DV, the estimated conduction loss is:

$$PD_{RES(MAX)} = \frac{0.1\Omega \times 4.7\mu H \times 750kHz \times 1.35A^{3}}{3 \times 7V} = 0.04W$$

The approximate maximum switching loss can be Calculated as:

$$PD_{SW(MAX)} = \frac{t_{turn-off} \times I_{PEAK} \times V_{OUT} \times f_{OSC}}{2}$$

For the above Si3458DV, the approximate switching loss is:

$$PD_{SW(MAX)} = \frac{10ns \times 1.35A \times 28.72V \times 750kHz}{2} = 0.145W$$

Rectifier Diode Selection

The A8600's high switching frequency demands a high-speed rectifier. Scotty diodes are recommended for most applications because of their fast recovery time and low forward voltage. The diode should be rated to handle the output voltage and the peak switch current. Make sure that the diode's peak current rating is at least I_{PEAK} calculated in the Inductor Selection section and that its breakdown voltage exceeds the output voltage.

Setting the Over voltage Protection Limit

The OV protection circuit should ensure the circuit safe operation; therefore, the controller should limit the output voltage within the ratings of all MOSFET, diode, and output capacitor components, while providing sufficient output voltage for LED current regulation. The OV pin is connected to the center tap of a resistive voltage divider (R1 and R2 in Figure 1) from the high-voltage output. When the controller detects the OV pin

voltage reaching the threshold V_{OV_TH}, typically 1.23V, OV protection is activated. Hence, the step-up converter output over voltage protection point is:

$$V_{OUT(OVP)} = V_{OV\_TH} \times (1 + \frac{R1}{R2})$$

In Figure 1, the output OVP voltage is set to:

$$V_{OUT(OVP)} = 1.23V \times (1 + \frac{1M\Omega}{37.4k\Omega}) = 34.1V$$

Input Capacitor Selection

The input capacitor (C_{IN}) filters the current peaks drawn from the input supply and reduces noise injection into the IC. A 10μF ceramic capacitor is used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. In some applications, C_{IN} can be reduced below the values used in the typical operating circuit. Ensure a low noise supply at IN by using adequate C_{IN}. Alternatively, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC low pass filter.

Select C_{IN}'s RMS ripple current rating to ensure that its thermal rise is less than approximately 10°C:

$$I_{RMS} = \frac{dI_L}{2 \times \sqrt{3}}$$

LED Selection and Bias

The series/parallel configuration of the LED load and the full-scale bias current have a significant effect on regulator performance. LED characteristics vary significantly from manufacturer to manufacturer. Consult the respective LED data sheets to determine the range of output voltages for a given brightness and LED current. In general, brightness increases as a function of bias current. This suggests that the number of LED(s) could be decreased if higher bias current is chosen; however, high current increases LED temperature and reduces operating life. Improvements in LED technology are resulting in devices with lower forward voltage while increasing the bias current and light output. LED manufacturers specify LED color at a given LED current. With lower LED current, the color of the emitted light tends to shift toward the blue range of the spectrum.

A blue bias is often acceptable for business applications but not for high image-quality applications such as DVD players. Direct DPWM dimming is a viable solution for reducing power dissipation while maintaining LED color integrity. Careful attention should be paid to switching noise to avoid other display quality problems. Using fewer LED(s) in a string improves step-up converter efficiency, and lowers breakdown voltage requirements of the external MOSFET and diode. The minimum number of LED(s) in series should always be greater than the maximum input voltage. If the diode voltage drop is lower than the maximum input voltage, the voltage drop across the current-sense inputs (FB_) increases and causes excess heating in the IC. Between 8 and 12 LED(s) in series is ideal for input voltages up to 20V.

LED VFB_ Variation

The A8600 has accurate (±1.5%) matching for each current source. However, the forward voltage of each white LED can vary up to ±5% from part to part. The accumulated voltage difference in each string equates to additional power loss within the IC. For the best efficiency, the voltage difference between strings should be minimized. The difference between lowest voltage string and highest voltage string should be less than 4.5V. Otherwise, the internal LED short-circuit protection shuts the part off.

Choosing the Appropriate Dimming Mode

Analog dimming mode allows lower peak LED current and results in higher converter efficiency and lower noise compared to direct DPWM mode. Unfortunately, the LED color spectrum can shift as a function of DC current so DPWM mode is often used to achieve more consistent display characteristics. (See the LED manufacturer's data sheet to determine the extent of the color shift.) When the A8600 is configured with an FSET resistor and CPLL capacitor, the ENA signal can toggle between modes on the fly. Care should be exercised when switching between modes to prevent the current from becoming unstable during the PLL lock-in time. To avoid such problems, force the controller into DPWM mode between transitions.

LCD Panel Capacitance

Some LCD panels include a capacitor in parallel with LED string to improve ESD immunity. The A8600 can start up without a problem for string capacitance up to 0.27μF.

PCB Layout Guidelines

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Minimize the area of the high current switching loop of the rectifier diode, external MOSFET, sense resistor, and output capacitor to avoid excessive switching noise. Use wide and short traces for the gate-drive loop from the EXT pin, to the MOSFET gate, and through the current-sense resistor, then returning to the IC GND pin.

2) Connect high-current input and output components with short and wide connections. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the external MOSFET, then to the current-sense resistor, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the rectifier diode, to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Avoid using vias in the high-current paths. If vias are unavoidable, use multiple vias in parallel to reduce resistance and inductance.

3) Create a ground island (PGND) consisting of the input and output capacitor ground and negative terminal of the current-sense resistor. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog ground island (AGND) consisting of the over voltage detection-divider ground connection, the ISET and FSET resistor connections, CCV and CPLL capacitor connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the GND pins directly to the exposed backside pad. Make no other connections between these separate ground planes.

4) Place the over voltage detection-divider resistors as close to the OV pin as possible. The divider's center trace should be kept short. Placing the resistors far away causes the sensing trace to become antennas that can pick up switching noise. Avoid running the sensing traces near LX.

5) Place the IN pin bypass capacitor as close to the device as possible. The ground connection of the IN bypass capacitor should be connected directly to GND pins with a wide trace.

6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and ground. If possible, avoid running the LX node from one side of the PCB to the other. Use DC traces as shields, if necessary.
7) Refer to the A8600 evaluation kit for an example of proper board layout.

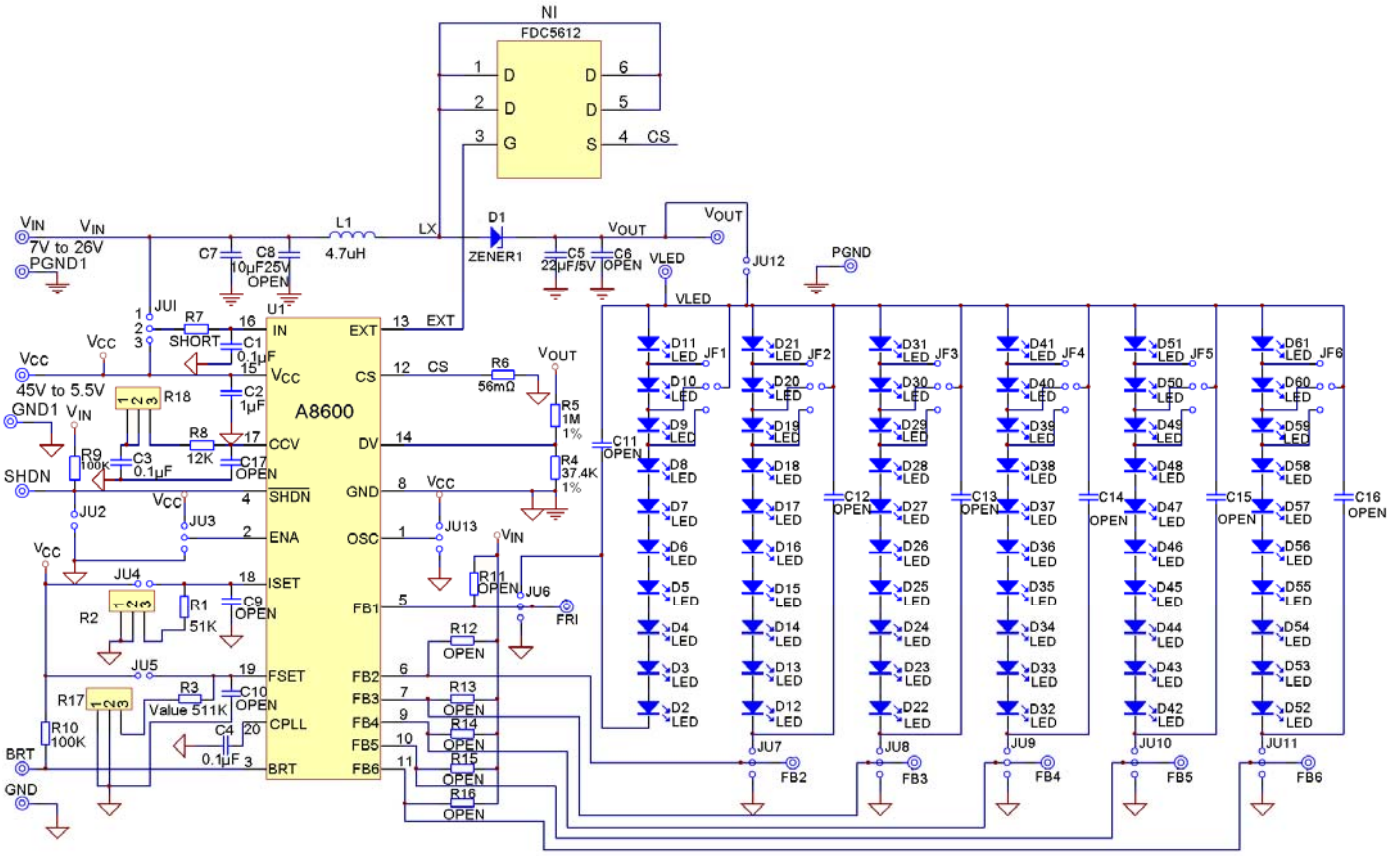


Figure 5:A8600 Layout Circuit

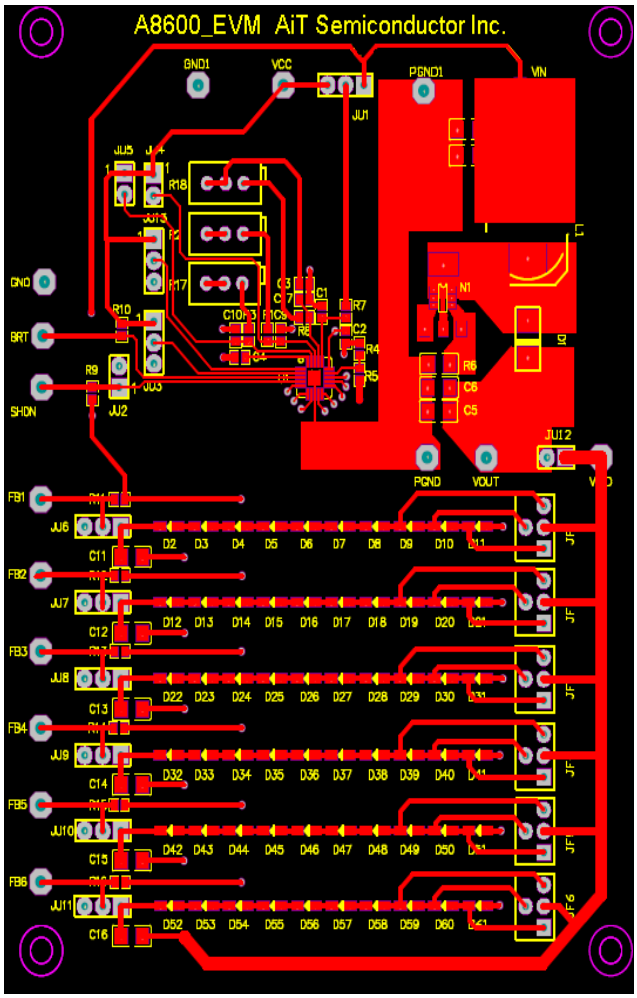


Figure 6:TOP Layer Layout

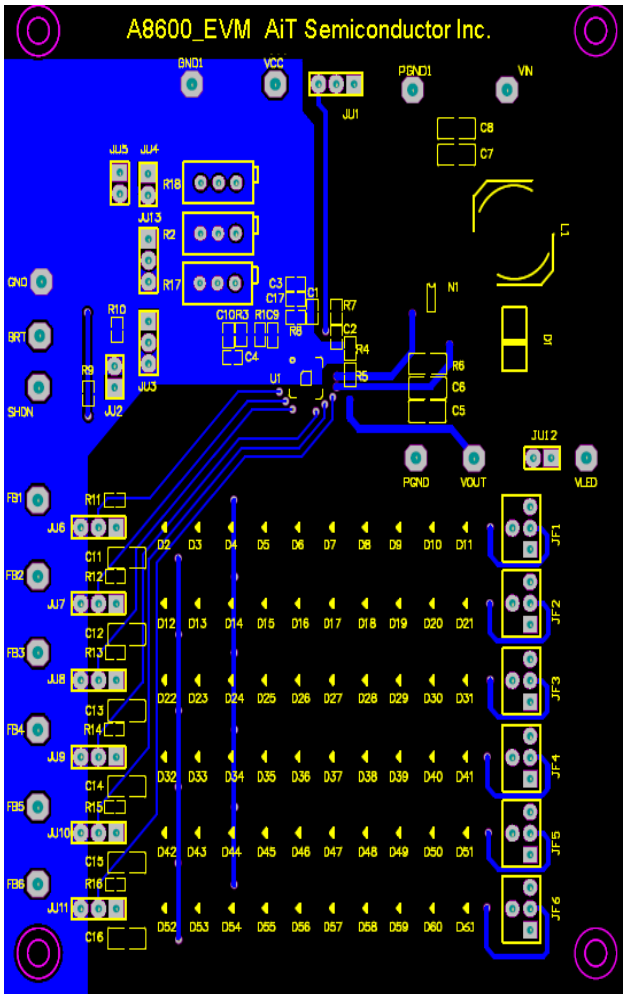
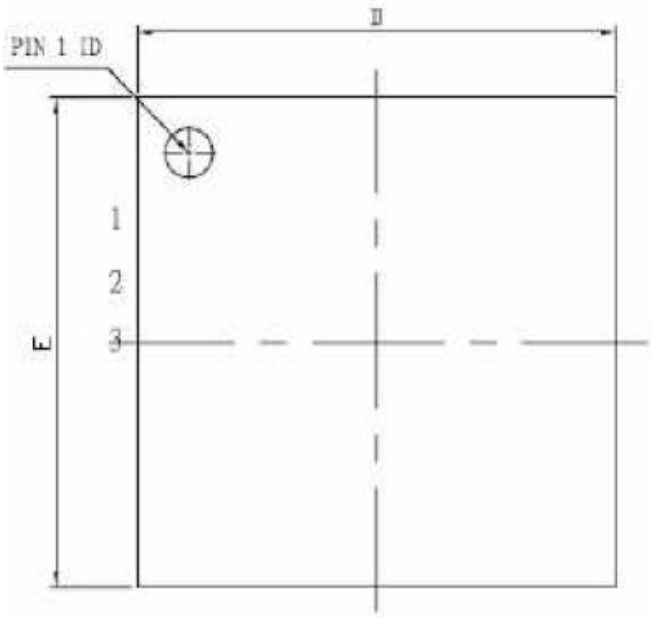


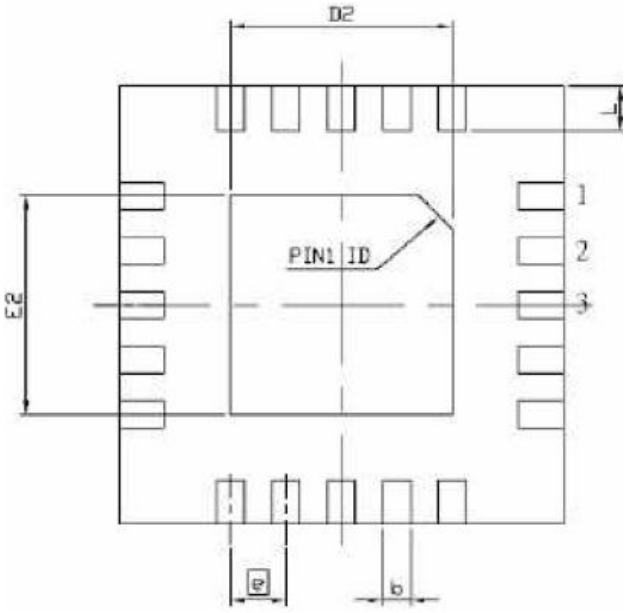
Figure 7:BOTTOM Layer Layout

PACKAGE INFORMATION

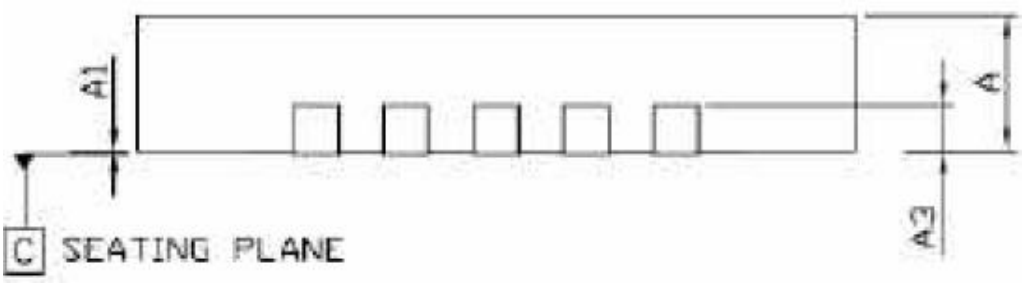
Dimension in QFN20 (4x4) Package (Unit: mm)



TOP VIEW



BOTTOM VIEW



Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	1.90	2.00	2.10
E	3.90	4.00	4.10
E2	1.90	2.00	2.10
e		0.50 BSC	
L	0.30	0.40	0.50

NOTES:1.All dimensions are in millimeter.

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