Agamem Mircoelectronics Inc. **AA88368AP**

PRELIMINARY **10-BIT DAC**

■ FEATURES

- 14 bits serial data input (3 wire serial data transfer method, DI, CLK, LD)
- R-2R resistor ladder used for D/A conversion
- 10 channels with 10 bits resolution monotonic D/A converter
- 10channel buffer operational amplifiers operating in the full voltage range from VCC to GND
- Max. +/- 3.5 LSBs Integral Non-Linearity
- Max +/- 1 LSB Differential Non-Linearity
- Max. 10 MHz Serial data input
- Serial I/O for cascade application
- Max. 2.0 mA analog output drive/sink current
- Two separate power supply/ground lines for system and analog power supply
- Single +5 V system power supply
- Silicon-gate CMOS process

■ DESCRIPTION

The AA88368AP is an 10-bit resolution digital to analog converter (DAC), designed for interface with 10 bits micro-controller. The AA88368AP has 10 channels with operational amplifier output buffers. Digital data are input serially in max. 10MHz by individual channel units. The latched digital data are converted into analog DC voltages by the D/A converter in 20μs settling time. AA88368AP is a single 5V power DAC. Output could be full swing as the analog power is equal to the system power.

The AA88368AP has 10 operational amplifier output buffers for each one of 10 channels. These operational amplifier output buffers are used to provide high current drive/sink capability. The AA88368AP is suitable for electronic volumes and replacement for potentiometers for adjustment, in addition to normal D/A converter applications.

AA88368AP is a 20 pins SSOP package. Its operation temperature range is specified over -10℃ to 75℃. Figure 2 shows its pin assignment.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	-0.3 ~ +6.0	V
Upper reference voltage of D/A converter	V_{DD}	-0.3 ~ +6.0	V
Input voltage	V_{IN}	-0.3 ~ +6.0	V
Output voltage	V_{OUT}	-0.3 ~ +6.0	V
Power dissipation	P_D	400	mW
Operating temperature	T_{OPR}	-25 ~ +85	℃
Storage temperature	T_{STG}	-55 ~ +125	℃

■ RECOMMENDED OPERATING CONSITIONS (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	-	5.5	V

Figure 1. Logic symbol

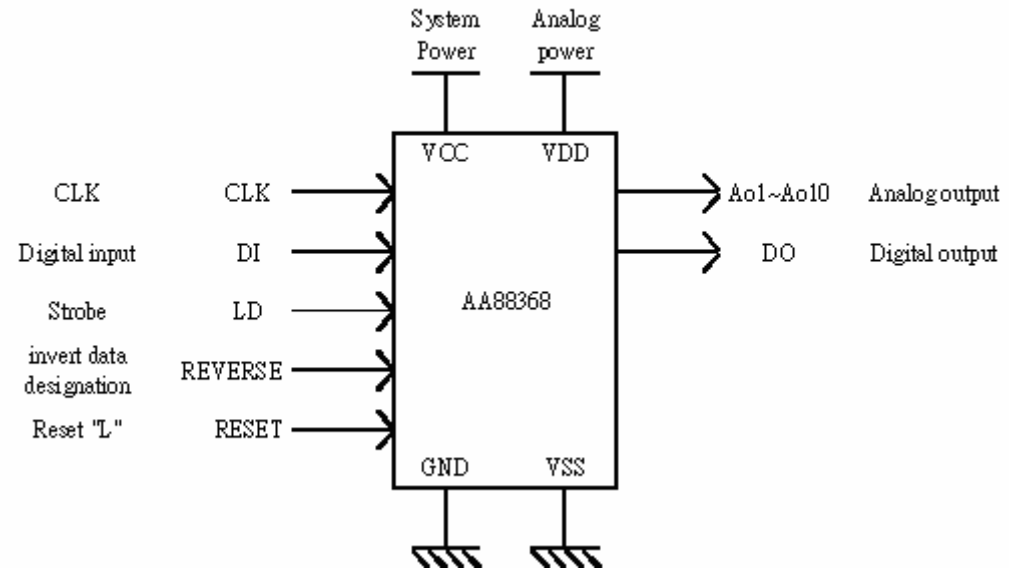
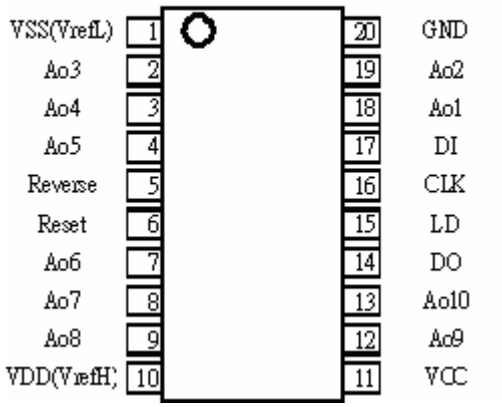


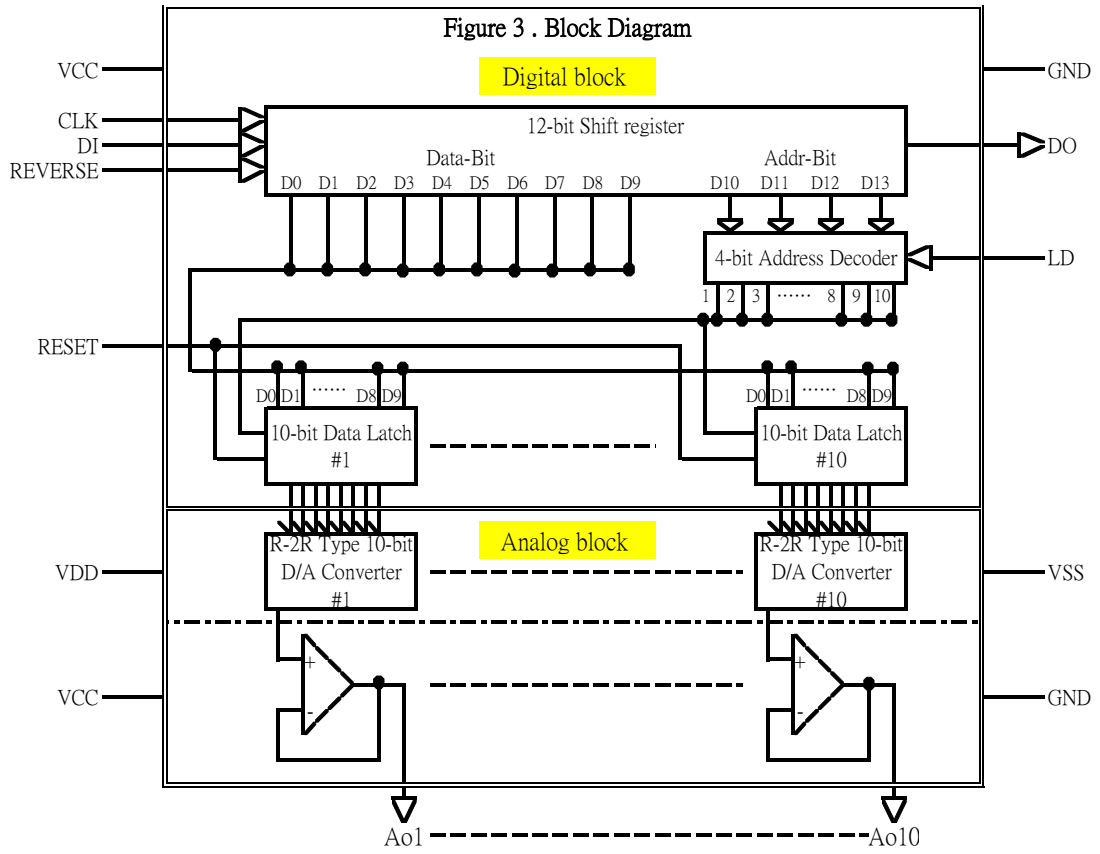
Figure 2. Pin Assignment—Top



■ PIN DESCRIPTION

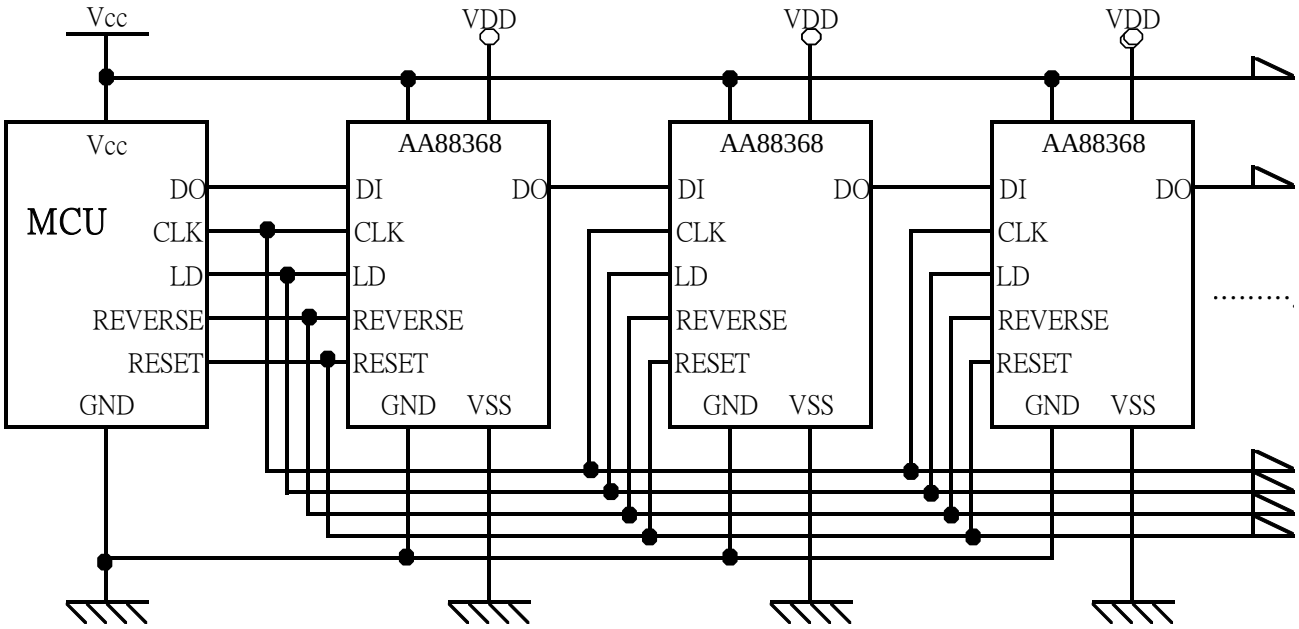
Pin No.	Pin name	Analog / Digital	I / O	Function
1	V_{SS}	Analog	-	D/A converter lower reference voltage input terminal
2	Ao3	Analog	O	10bit D/A converter output terminal (CH3)
3	Ao4	Analog	O	10bit D/A converter output terminal (CH4)
4	Ao5	Analog	O	10bit D/A converter output terminal (CH5)
5	Reverse	Digital	I	It is inverted about the data designation 10bit LSB and MSB.
6	Reset	Digital	I	The analog output of all channels is fixed for “L”.
7	Ao6	Analog	O	10bit D/A converter output terminal (CH6)
8	Ao7	Analog	O	10bit D/A converter output terminal (CH7)
9	Ao8	Analog	O	10bit D/A converter output terminal (CH8)
10	VDD	Analog	-	D/A converter upper reference voltage input terminal
11	VCC	-	-	Power supply terminal
12	Ao9	Analog	O	10bit D/A converter output terminal (CH9)
13	Ao10	Analog	O	10bit D/A converter output terminal (CH10)
14	D_0	Digital	O	Terminal to output LSB data of 14-bit shift register
15	LD	Digital	I	When H-level signal is input to this terminal, the value stored in 14-bit shift register is loaded in decoder and D/A converter output register.
16	CLK	Digital	I	Shift clock input terminal. Input signal at DI pin is input to 14-bit shift register of shift clock pulse.
17	DI	Digital	I	Serial data input terminal to 14-bit long serial data
18	Ao1	Analog	O	10bit D/A converter output terminal (CH1)
19	Ao2	Analog	O	10bit D/A converter output terminal (CH2)
20	GND	-	-	GND terminal

Figure 3 . Block Diagram



* : VDD、VSS used for the analog block except operational amplifier block

Figure 4. Cascade Connection Example



*：Analog power (VDD, VSS) can be different each other depend on application consideration

■ FUNCTIONAL DESCRIPTION

DEVICE CONFIGURATION

As illustrated in Figure 3 Block Diagram, AA88368AP is composed by digital block and analog block. The digital block consists of a Shift Register, a Address decoder and 8 Data Latches. The analog block consists of 10 R-2R D/A converters and 10 Operational Amplifier Buffers. For stability consideration, the power supply and ground lines are separate between the digital block and the operational amplifier buffers, and R-2R D/A converters.

LOCK DESCRIPTIONB

SHIEFT RGISTER

The AA88368AP has a 14 bits shift register to store 14 bits anytime. At the rising edge of CLK signal, the external digital data will be shifted into the LSB of the Shift-Register. And the original contents in the Shift Register will also shift right. The 14th bit(MSB) will also output to DO for cascade application for this device. Figure 4 shows the configuration.

ADRESS DECODER and DATA LATCH

When the LD pin is on high then the 14 bits stored in the shift register will be latched. The 4 upper bits (addr-bit) will send to address decoder to select one of the ten Data Latches. The 10 lower bits(data-bit) will be written into the indicated Data-Latch as the internal digital data.

R-2R D/A CONVERTER

The internal digital data from the Data Latch will be transferred into a analog DC voltage with 8-bit resolution by R-2R D/A converter in a max.20us settling time.

OPERATIONAL AMPLIFIER BUFFER

Each channel has a corresponding operational amplifier output buffer. It's used to get a complete monotonic analog DC output and provide a high current drive /sink capability up to 2mA. It could operate in the full range from VCC to GND as the analog power is equal to the system power.

DEVICE OPERATION

Figure 5 shows the input/output timing. A 14-bit address/data is serially input into the shift register through the DI pin synchronously at the rising edge of the CLK signal. The format of the shift register is shown in the Figure 6.The lower 10 bits (D0 ~ D9) are data bits to be converted, and the upper 4 bits(D10 ~ D13) are address bits to select a channel to be written. As the LD pin is on high, the address decoder load the upper 4 bits to select a Data-Latch, and write the 10 data bits into it. Figure 7 shows the Data-Latch address map, and Table2 shows the address decoding. 8 data bits written into individual Data-Latch are converted into analog DC voltage through R-2R resistor ladder, dividing the supply voltage |VDD-VSS| in 10-bit resolution. Output buffers at individual D/A converter outputs can rise up

the drive/sink ability to 2mA. Figure 8 shows a configuration of the R-2R resistor ladder D/A converter following with an operational amplifier. Table 3 is the mapping table of internal digital data and the corresponding output analog DC voltage.

Figure 5. Timing Chart

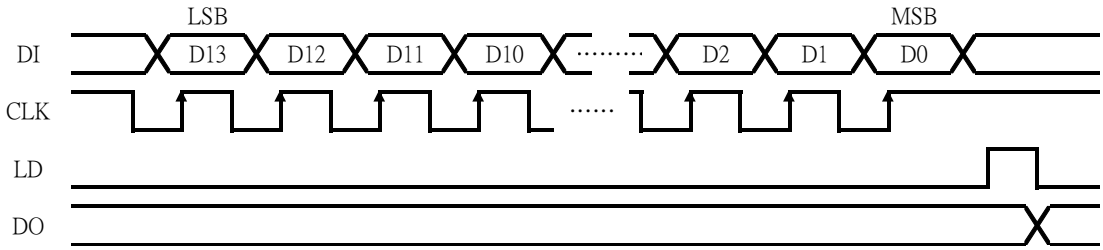


Figure 6. Shift Register Format

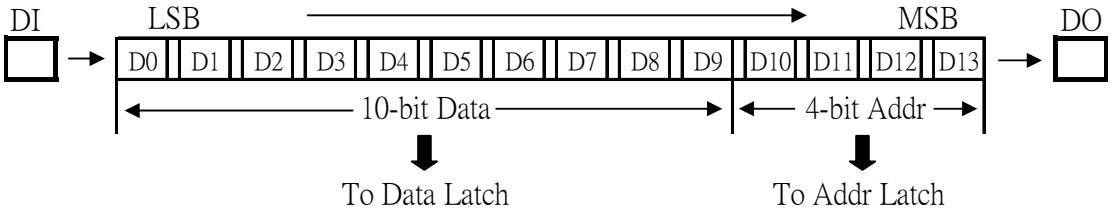
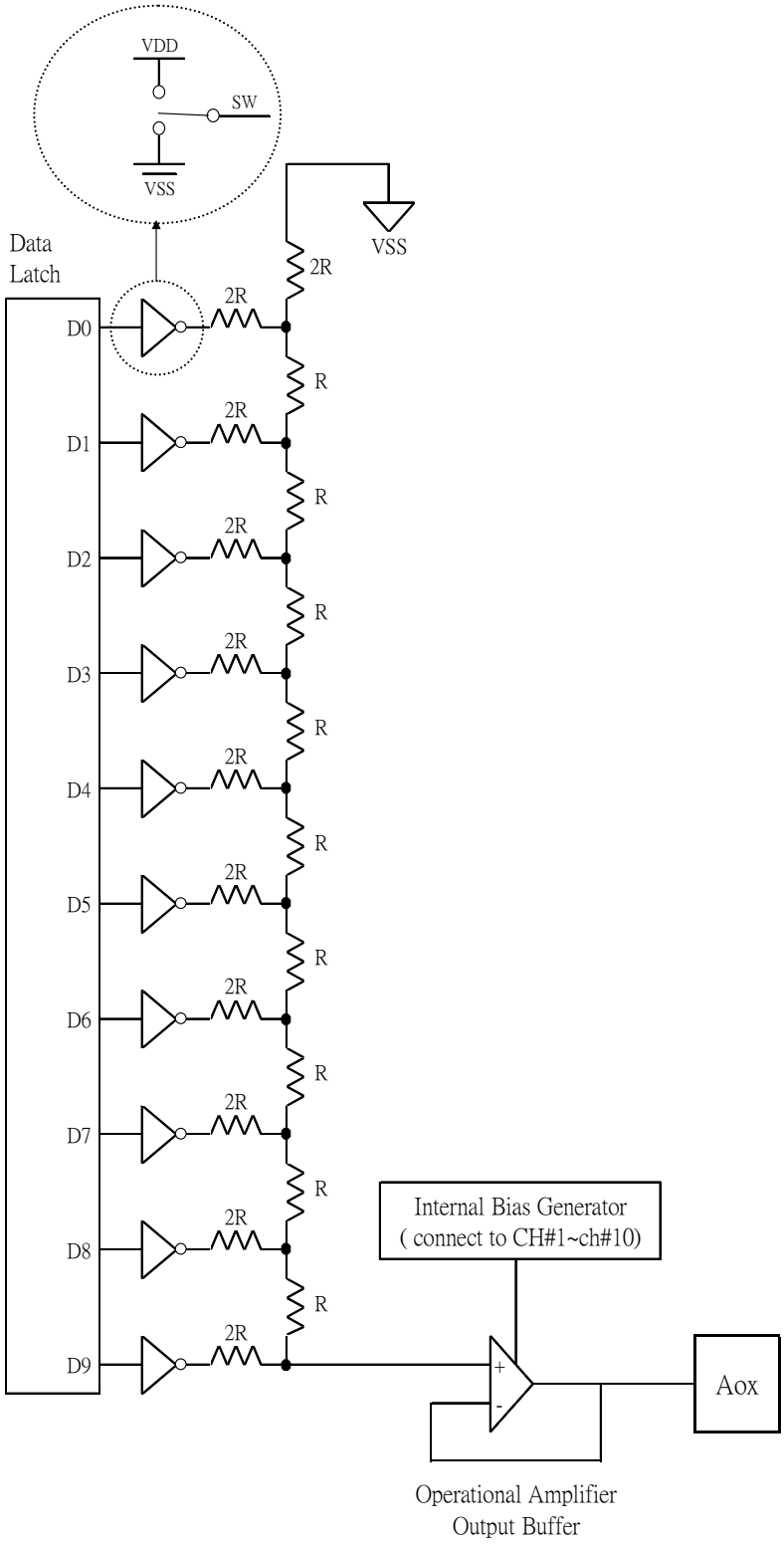


Figure 7. Data Latch Address Map.

ADDR	Data Latch	R-2R	OP	AO
1H	1H	1H	1H	AO1
2H	2H	2H	2H	AO2
3H	3H	3H	3H	AO3
4H	4H	4H	4H	AO4
5H	5H	5H	5H	AO5
6H	6H	6H	6H	AO6
7H	7H	7H	7H	AO7
8H	8H	8H	8H	AO8
9H	9H	9H	9H	AO9
10H	10H	10H	10H	AO10

Figure 8 Configuration of R-2R Resistor Ladder D/A Converter with Operational Amplifier Output Buffer



■ CIRCUIT OPERATIONS

D10	D11	D12	D13	DAC selection
O	O	O	O	Don't care
O	O	O	I	AO1 selection
O	O	I	O	AO2 selection
O	O	I	I	AO3 selection
O	I	O	O	AO4 selection
O	I	O	I	AO5 selection
O	I	I	O	AO6 selection
O	I	I	I	AO7 selection
I	O	O	O	AO8 selection
I	O	O	I	AO9 selection
I	O	I	O	AO10 selection
I	O	I	I	Don't care
I	I	O	O	Don't care
I	I	O	I	Don't care
I	I	I	O	Don't care
I	I	I	I	Command for test

Reverse = open or VCC short setting (data：MSB first)										
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D/A output
0	0	0	0	0	0	0	0	0	0	VrefL
0	0	0	0	0	0	0	0	0	1	(VrefH-VrefL) / 1024*1+VrefL
0	0	0	0	0	0	0	0	1	0	(VrefH-VrefL) / 1024*2+VrefL
0	0	0	0	0	0	0	0	1	1	(VrefH-VrefL) / 1024*3+VrefL
⋮										⋮
1	1	1	1	1	1	1	1	1	0	(VrefH-VrefL) / 1024*1022+VrefL
1	1	1	1	1	1	1	1	1	1	(VrefH-VrefL) / 1024*1023+VrefL

Reverse = L setting (data：LSB first)										
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D/A output
0	0	0	0	0	0	0	0	0	0	VrefL
1	0	0	0	0	0	0	0	0	0	(VrefH-VrefL) / 1024*1+VrefL
0	1	0	0	0	0	0	0	0	0	(VrefH-VrefL) / 1024*2+VrefL
1	1	0	0	0	0	0	0	0	0	(VrefH-VrefL) / 1024*3+VrefL
⋮										⋮
0	1	1	1	1	1	1	1	1	0	(VrefH-VrefL) / 1024*1022+VrefL
1	1	1	1	1	1	1	1	1	1	(VrefH-VrefL) / 1024*1023+VrefL

■ ELECTRICAL CHARACTERISTICS

Digital characteristics (unless otherwise noted, VCC=5V, VrefH=5V, VrefL=0V, Ta=25℃)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Power supply current	I_{CC}	-	0.85	2.8	ma	CLK=10MHz operated, VCC=5V, IAO=0us
Input leak current	I_{ILK}	-5	-	5	ua	Vin=0~V_{CC}
Input voltage ”L”	V_{IL}	-	-	0.8	V	
Input voltage ”H”	V_{IH}	2	-	-	V	
Output voltage ”L”	V_{OL}	0	-	0.4	V	I_{OL}=2.5ma
Output voltage ”H”	V_{OH}	4.6	-	5	V	I_{OH}=2.5ma

■ ANALOG CHARACTERISTICS

(unless otherwise noted, VCC=5V, VrefH=5V, VrefL=0V, Ta=25℃)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Consumption current		IrefH	-	4.5	7.5	mA	VrefH=5V, VrefL=0V Data condition：maximun current
D/A converter Upper reference voltage		VrefH	3	-	5	V	Reference voltage can not always be set to any value in this range, because it is restricted the buffer amplifier output voltage range
D/A converter Lower reference voltage		VrefL	0	-	1.5	V	
Buffer amplifier Output voltage range		Vo	0.1	-	4.9	V	Io = + / - 100uA
			0.2	-	4.75	V	Io = +/- 1ma
Buffer amplifier Output drive range		Io	-2	-	2	mA	Upper satuation voltage = 0.35V Lower satuation voltage = 0.23V
Accuracy	Differential non-linearity error	S_{DL}	-1	-	1	LSB	VrefH=4.796V, VerfL=0.7V, Vcc=5.5V (2mV/LSB) Without load (Io=0mA)
	Non-linearity error	S_L	-3.5	-	3.5		
	Zero code error	S_{ZERO}	-25	-	25	mV	
	Full scale error	S_{FULL}	-25	-	25		
Buffer amplifier Output impedance		RO	-	5	15	Ohm	
Pull-up I/O internal R value		RUP	12.5	25	37.5	Kohm	Vin: 0V（resistance value alters by the applied voltage）

NOTES:

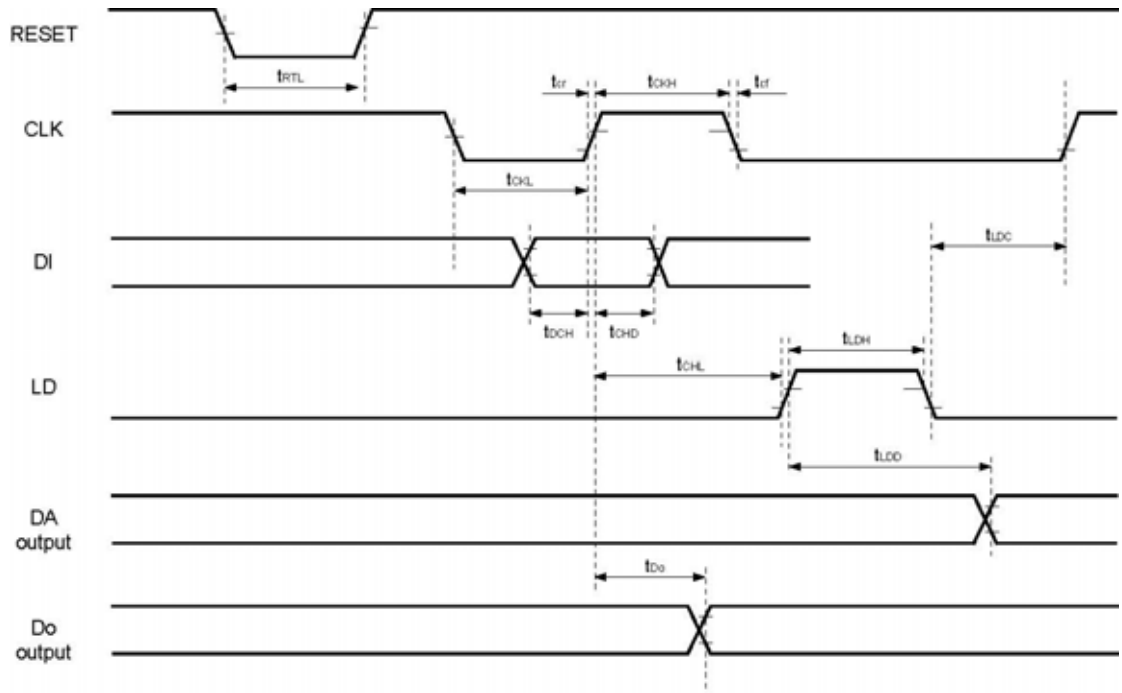
Integral Non-Linearity : The difference between the digital data converted output values and a reference straight line drawn through the first and the last output values

Differential Non-Linearity : The difference from the ideal increment value when the digital data is increased by 1 bit.

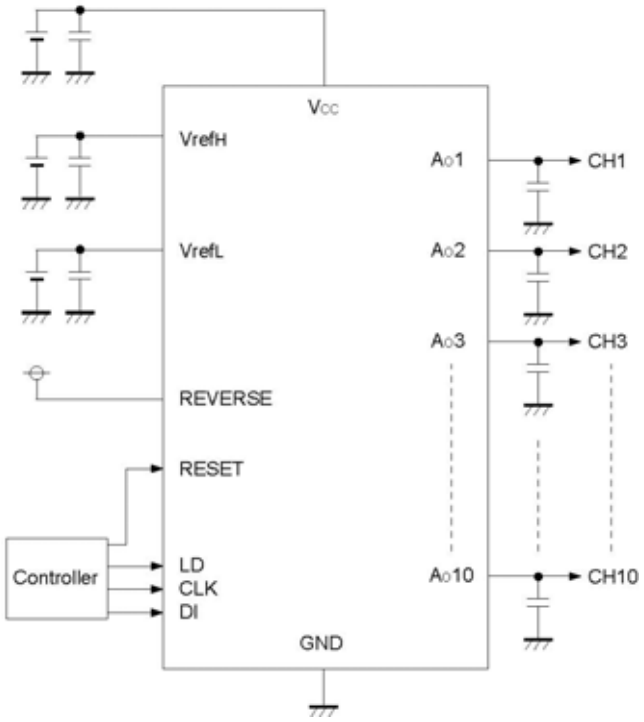
■ AC CHARACTERISTICS

(unless otherwise noted, VCC=5V, VrefH=5V, VrefL=0V, Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Reset “L” pulse width	TRTL	50	-	-	ns	
Clock “L” pulse width	TCKL	50	-	-		
Clock “H” pulse width	TCKH	50	-	-		
Clock rise time	TCR	-	-	50		
Clock fall time	TCF	-	-	50		
Data setup time	TDCH	20	-	-		
Data hold time	TCHD	40	-	-		
LD setup time	TCHL	50	-	-		
LD hold time	TLDC	50	-	-		
LD “H” pulse duration	TLDH	50	-	-		
Data output delay time	TDO	-	-	200		CL=100pf
D/A output settling time	TLDO	-	7	20	us	CL<1000pf, VO: 0.5V~4.5V, the time until the becomes the final value of 1/2LSB



●Application circuit



■ OPERATION NOTES

• There are 3 different type of power supply terminal and 1 type of GND terminal in this IC. Each of these terminals requires the constant power supply for operating.

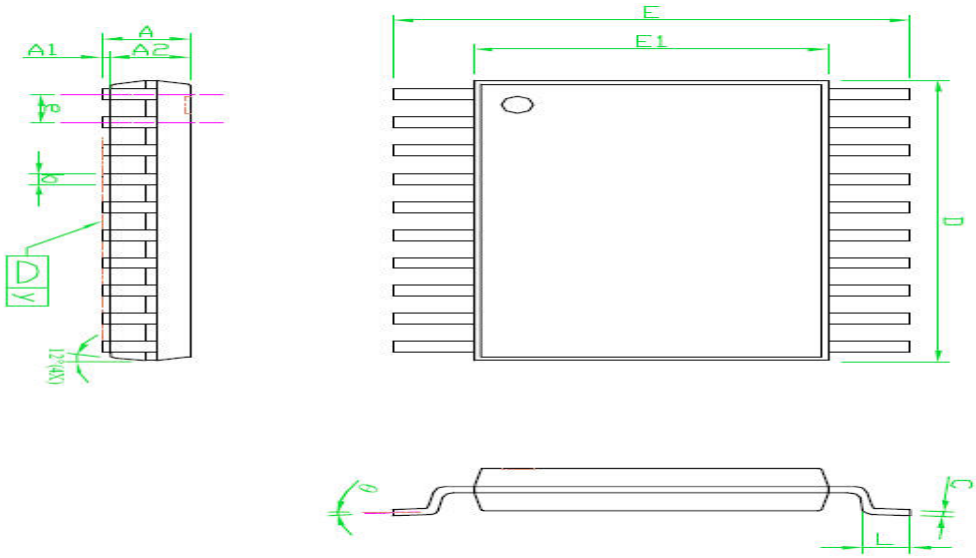
• Pile up ripple and noise to these power supply terminals, it can‘t keep the accuracy of the D/A converter. Therefore external bypass capacitor recommend to set as close as possible to the terminals between VDD and GND in order to stabilizes the D/A converter.

• The capacitor between output and GND recommend to set under 100pF including parasitic capacitor in order to reduces jitter from layout of the output line and noise.

• LSB-first or MSB-first decoding are selected by REVERSE terminal. Therefore, REVERSE terminal should be set as —open“ or —VDD short“ at LSB-first mode, —GND short“ at MSB-first mode.

• RESET terminal uses the I/O-cell of the internal pull-up resistance, adding a capacitor between this terminal and GND, this IC will have equivalent function as power-on-reset, by making a time-delay. When a reset signal is inputted from the controller, it is possible that the output of all channels are fixed on Low-level in the —L“ section on the pulse.

■ TSSOP 20L PACKAGE DIMENSION



NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
2. TOLERANCE +-0.1mm UNLESS OTHERWISE SPECIFIED
3. COPLANARITY: 0.1mm
4. CONTROLLOMG DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. FOLLOWED FROM JEDEC MO-153

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.20	-	-	0.048
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-	0.30	0.007	-	0.012
C	0.09	-	0.20	0.004	-	0.008
D	6.40	6.50	6.60	0.252	0.256	0.260
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-	0.65	-	-	0.026	-
L	0.45	0.60	0.75	0.018	0.024	0.030
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	-	8°