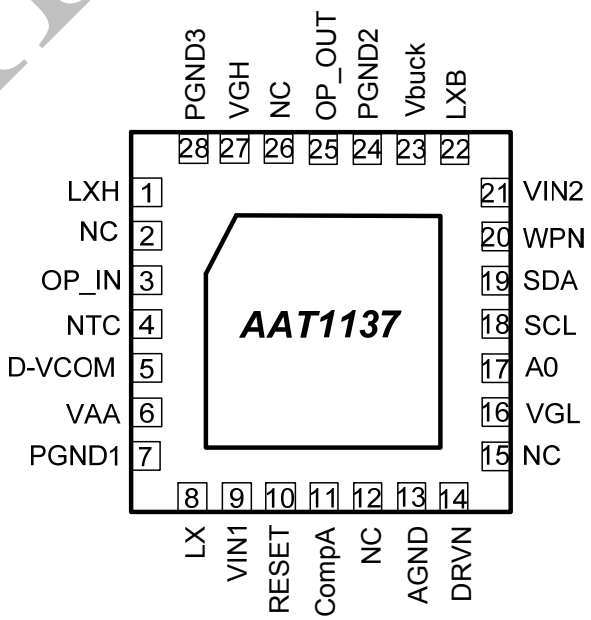
MULTI-CHANNEL POWER SUPPLY FOR TFT LCD PANELS

FULLY I2C INTERFACE CONTROL – TWO BOOST, BUCK, CHARGE PUMP, TWO OPERATIONAL AMPLIFIER, RESET

FEATURES

- 2.5V to 5.5V Input Supply Voltage Range
- Fully I^2C Interface Control
- Current Mode Sync Boost Regulator for VAA
  - Built-in 16V, 2.5A, 0.2Ω N-MOSFET
  - Setting via I^2C Interface
    Output Voltage, Switching Frequency,
    Soft Start Time, Delay Time and OCP
- Current Mode Sync Buck Regulator for V_{BUCK}
  - Built-in 5V, 1.2A, 0.28Ω P-MOSFET
  - Setting via I^2C Interface
    Output Voltage, Switching Frequency,
    and Delay Time
- Current Mode Boost Regulator for VGH
  - Built-in 40V, 1.2A, 0.2Ω N-MOSFET
  - Temperature Compensation (T/C)
  - Setting via I^2C Interface
    Output Voltage, Switching Frequency,
    Delay Time, and VGHT Voltage
- Negative Charge Pump Regulator for VGL
  - Setting via I^2C Interface
    Output Voltage, Switching Frequency,
    and Delay Time
- Operational Amplifier for VCOM
  - ±150mA Short-Circuit Current
  - 25V/μs Slew Rate
  - Setting via I^2C Interface
    Output Voltage
- Operational Amplifier for Line-Repaired
  - ±150mA Short-Circuit Current
  - 25V/μs Slew Rate
- RESET Output (XAO)
  - Open Drain Output
  - Setting via I^2C Interface
    Detect Voltage, and Delay Time
- Protection
  - Input Under-Voltage Lockout (UVLO)
  - Over Voltage Protection (OVP)
    For VAA, V_{BUCK}, and VGH
  - Under Voltage Protection (UVP)
    For VAA, V_{BUCK}, VGH, and VGL
  - Short Circuit Protection (SCP) For VAA
  - Over Temperature Protection (OTP)
- WQFN 28-4X4X0.75mm Package Available

PIN CONFIGURATION



APPLICATIONS

- Tablet Panel
- Notebook Panel

GENERAL DESCRIPTION

The AAT1137 is a highly integrated power management IC for TFT LCD panels. The device consists of two current mode boost regulators, a current mode buck regulator, a negative charge pump regulator, a reset function, and two operational amplifiers. The AAT1137 also includes I^2C interface for setting various parameters such as each regulator's output voltage, switching frequency, soft start time, delay times, buffer output voltage, etc.

The AAT1137 includes a current mode synchronous boost regulator that provides a fast transient response supply voltage for the source driver. The source driver boost is capable of generating up to 13.3V. A second current mode non-synchronous boost supplies the gate-on (VGH) voltage, and is capable of an output voltage of up to 35V. The VGH non-synchronous boost includes a temperature compensation function. Both boost regulators integrate a low R_{DSON} N-MOSFET, and operates at a programmable switching frequency between 600kHz and 1.2MHz.

The synchronous current mode buck regulator operates at a programmable switching frequency between 1.2MHz and 2.1MHz, and typically supplies system logic power (TCON). It provides fast load transient response to pulsed loads while producing efficiencies over 90%. This buck regulator integrates a 5V, 1.2A, 0.28Ω, power MOSFET that allows the use of ultra-small inductors and ceramic capacitors.

The AAT1137 negative charge pump regulator generates VGL supply voltage for the gate-off voltage. This negative output voltage is set by the I^2C interface.

The programmable operational amplifier drives the LCD backplane (VCOM). This unity-gain buffer is capable of rail-to-rail input and output, ±150mA output short-circuit current, and a 25V/μs slew rate. Output voltage can be programmed by I^2C interface using 7-bits or 128 steps, eliminating mechanical potentiometers to reduce labor cost.

A second operational amplifier is included for the Panel repair-line. This buffer is not controlled by I^2C interface and its output is set using an external signal.

The reset functions (XAO) is used to monitor the device supply voltage. The reset signal is issued via an open drain NMOS when the supply is below a programmable thresholds voltage. The thresholds and the delay time are programmable via I^2C interface.

The AAT1137 device includes various protection features such as input under-voltage lockout (UVLO) and over temperature shutdown (OTP). Regulator outputs include under voltage protection (UVP), overload voltage protection (OVP), and short circuit protection (SCP).

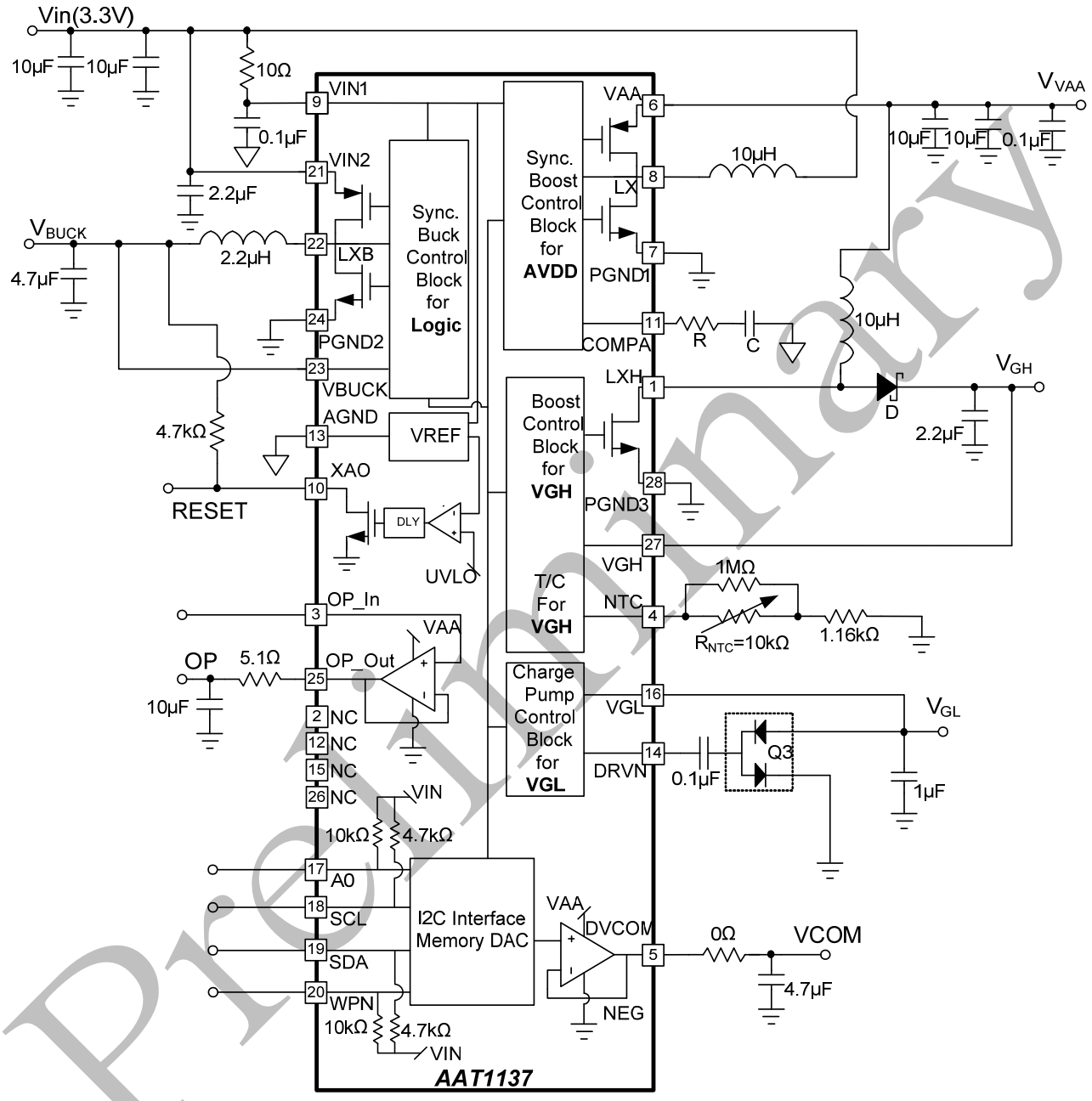
The AAT1137 is available in a small WQFN 28 pin 4X4X0.75mm with a bottom side exposed thermal pad to provide optimal heat dissipation. The device is rated to operate from –40 to +85℃ temperature range.

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1137	AAT1137 -Q44-T	Q44: WQFN28-4X4	T: Tape and Reel	–40°C to +85°C	1137 XXXXXX XXXX	Device Type Lot no. (6~9 Digits) Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VIN1, VIN2 to GND	V_{IN}	–0.3 to +6.5	V
PGND1, PGND2, PGND3 to AGND		–0.3 to +0.3	
LX to PGND1	V_{H1}	–0.3 to +16	V
LXB to PGND2	V_{H2}	–0.3 to +6.5	V
LXH to PGND3	V_{H3}	–0.3 to +45	V
Input Voltage 1 (A0, SCL, SDA, WPN, VBUCK)	V_{I1}	–0.3 to V_{IN} +0.3	V
Input Voltage 2 (OP_In)	V_{I2}	–0.3 to V_{H1} +0.3	V
Input Voltage 3 (VGH)	V_{I3}	–0.3 to V_{H2} +0.3	V
Input Voltage 4 (VGL)	V_{I4}	–16 to +0.3	V
Output Voltage 1 (COMPA, XAO, NTC)	V_{O1}	–0.3 to V_{IN} +0.3	V
Output Voltage 2 (VAA, OP_Out, DVCOM, DRVN)	V_{O2}	–0.3 to V_{H1} +0.3	V
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Resistance	θ_{JA}	36	°C /W
Power Dissipation, @ T_A = +25°C , T_J = +125°C	P_d	2.778	W
ESD Susceptibility Human Body Mode	HBM	2k	V
ESD Susceptibility Machine Mode	MM	200	V

Note:
1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.
2. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, VIN1 = VIN2 = 3.3V, V_{VAA} = 10V, V_{GH}= 25V, V_{GL}= –6V, VCOM = 4V)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN1 Input Voltage Range	V_{IN}		2.5	-	5.5	V
VIN2 Input Voltage Range	V_{IN}		2.5	-	5.5	V
VIN1 Under Voltage Lockout	V_{UVLO}	Rising	2.0	2.2	2.3	V
		Falling	1.85	2.05	2.15	
VIN1 Operating Current	I_{IN1}	Not Switching	-	3	-	mA
		Switching	-	6	-	mA
VIN2 Operating Current	I_{IN2}	Not Switching	-	3	-	mA
		Switching	-	6	-	mA
VAA Operating Current	I_{VAA}	DVCOM = 5V	-	5	-	mA
Thermal Shutdown	T_{SH}	2 Bits, Step = 25°C	125	-	200	°C
Thermal Shutdown Hysteresis	T_{Hys}		-	20	-	°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, VIN1 = VIN2 = 3.3V, V_{VAA} = 10V, V_{GH}= 25V, V_{GL}= –6V, VCOM = 4V)

Synchronous Current Mode Boost Regulator (for VAA)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VAA Output Voltage Range	V_{VAA}	6 Bits, Step = 0.1V	7	-	13.3	V
LX Oscillation Frequency	f_{OSC1}	2 Bits, Step = 200kHz	600	-	1200	kHz
LX Current Limit	I_{LIM1_LX}	2 Bits, Step = 0.5A	2	-	3	A
LX NMOS ON-Resistance	R_{ON1_NMOS}		-	0.2	-	Ω
LX NMOS Leakage Current	I_{Leak1_NMOS}		-	1	20	μA
LX PMOS ON-Resistance	R_{ON1_PMOS}		-	0.8	-	Ω
LX PMOS Leakage Current	I_{Leak1_PMOS}		-	1	20	μA
LX Maximum Duty Cycle	D_{MAX1}		86	90	-	%
Line Regulation		2.2V < VIN < 5.5V, I_{VAA} = 200mA	-	0.08	0.15	%/V
Load Regulation		0< I_{VAA} < Full	-	1	-	%
Transconductance	g_{m1}	ΔI = 5μA	-	85	-	μS
Voltage Gain	A_{V1}		-	700	-	V/V
Soft Start Time T1	t_3	4 Bits, Step = 1ms	1	-	12	ms
Soft Start Time T2	t_4	3 Bits, Step = 1ms	3	-	10	ms
Over Voltage Protect Voltage	V_{OVP_VAA}	Hys.= 5%	-	120	-	%
Under Voltage Protect Voltage	V_{UVP_VAA}		75	80	85	%
Duration to UVP Trigger Time	t_{UVP_VAA}		-	50	-	ms
Short Circuit Protect Voltage	V_{SCP_VAA}		35	40	45	%
VAA Output Voltage Accuracy			–1	-	+1	%

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, VIN1 = VIN2 = 3.3V, V_{VAA} = 10V, V_{GH}= 25V, V_{GL}= –6V, VCOM = 4V)

Synchronous Current Mode Buck Regulator (for V_{LOGIC})

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
BUCK Output Voltage Range	V_{BUCK}	5 Bits, Step = 0.1V	0.8	-	3.3	V
LXB Oscillation Frequency	f_{OSC2}	2 Bits, Step = 300kHz	1200	-	2100	kHz
LXB NMOS On-Resistance	R_{ON2_NMOS}	I_{SWB} = 100mA	-	0.25	-	Ω
LXB NMOS Leakage Current	I_{LEAK2_NMOS}	V_{IN2} = 0.6V	-	1	20	µA
LXB PMOS On-Resistance	R_{ON2_PMOS}	I_{SWB} = 100mA	-	0.28	-	Ω
LXB PMOS Leakage Current	I_{LEAK2_PMOS}	V_{IN2} = 0.6V	-	1	20	µA
LXB Current Limit	I_{CLIM2}		-	1.2	-	A
LXB Maximum Duty Cycle	D_{MAX2}		-	100	-	%
Line Regulation	-	V_{IN2} = 2.2V to 5.5V	-	0.1	-	%/V
Load Regulation	-	0 < I_{LOAD} < 1A	-	0.5	-	%/A
Soft Start Time	t_{13}		0.5	-	2.5	ms
Delay Time	t_8	2 Bits, Step = 1000µs	0.5	-	3.5	ms
Over Voltage Protect Voltage	V_{OVP_BUCK}		-	120	-	%
Under Voltage Protect Voltage	V_{UVP_BUCK}		-	80	-	%
Duration to UVP Trigger Time	t_{UVP_BUCK}		-	50	-	ms
Output Voltage Accuracy			–1.5	-	+1.5	%

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, VIN1 = VIN2 = 3.3V, V_{VAA} = 10V, V_{GH}= 25V, V_{GL}= –6V, VCOM = 4V)

Non-synchronous Current Mode Boost Regulator (for VGH)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage Range	V_{GH}	5 Bits, Step = 1V	15	-	35	V
LXH Oscillation Frequency	f_{OSC3}	2 Bits, Step = 200kHz	600	-	1,200	kHz
LXH Current Limit	I_{LIM3}		-	1.2	-	A
LXH NMOS ON-Resistance	R_{ON3}	I_{SW} = 0.1A	-	0.2	-	Ω
LXH NMOS Leakage Current	I_{Leak3}		-	1	20	μA
LXH Maximum Duty Cycle	D_{MAX3}		-	88	-	%
Line Regulation		2.2V < VIN < 5.5V, I_{OUT} = 100mA	-	0.08	-	%/V
Load Regulation		0< I_{GH} < Full	-	1	-	%
Transconductance	g_{m3}	ΔI = 5μA	-	85	-	μS
Voltage Gain	A_{V3}		-	700	-	V/V
Soft Start Time	t_{12}		4	-	10	ms
Delay Time	t_5	4 Bits, Step = 1ms	3	-	18	ms
Over Voltage Protect Voltage	V_{OVP_VGH}	Hys.= 0.15V	-	105	-	%
Under Voltage Protect Voltage	V_{UVP_VGH}		75	80	85	%
Duration to UVP Trigger Time	t_{UVP_VGH}		-	50	-	ms
VGH Output Voltage Accuracy			–3	-	+3	%
VGHT Voltage Range	V_{GHT}	4 Bits, Step = 1V	25	-	39	V
NTC Source Current	I_{NTC}		-	20	-	μA

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, VIN1 = VIN2 = 3.3V, V_{VAA} = 10V, V_{GH}= 25V, V_{GL}= –6V, VCOM = 4V)

Negative Charge Pump Regulator (for VGL)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage Range	V_{GL}	4 Bits, Step = –1V	–14	-	–5	V
DRVN source current	I_{DRVN}		20	-	-	mA
Charge Pump Frequency	f_{OSC4}	2 Bits, Step = 1/4*f_{OSC1}	1/4*f_{OSC1}	-	f_{OSC1}	kHz
Soft Start (VGL)	t_{14}		2	-	3.5	ms
Delay Time (VGL)	t_{11}	4 Bits, Step=1ms	0	-	15	ms
Under Voltage Protect Voltage	V_{UVP_VGL}		75	80	85	%
Duration to UVP Trigger Time	t_{UVP_BUCK}		-	50	-	ms
VGL Output Voltage Accuracy			–3	-	+3	%

Unit-Gain Operational Amplifier (for VCOM Buffer & Line Repaired)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{OP}		7.0	-	13.3	V
Input Supply Current	I_{OP}		-	3	-	mA
Input Bias Current	I_{B_OPIN}	V_{OP_IN} = 5V	–40	-	+40	nA
Input Offset Voltage	V_{OS}	V_{OP_IN} = 5V	–17	-	+17	mV
Output Swing	V_{OP_SH}	I_{OP_OUT} = –5mA, V_{OP_IN} = 0V	-	0.08	0.15	V
		I_{OP_OUT} = –50mA, V_{OP_IN} = 5V	-	5.03	5.06	
	V_{OP_SL}	I_{OP_OUT} = 50mA, V_{OP_IN} = 5V	4.94	4.97	-	
		I_{OP_OUT} = 5mA, V_{OP_IN} = 10V	9.85	9.92	-	
Short Circuit Current	I_{SHORT}	Measure I_{OP_OUT}	-	±150	-	mA
Slew Rate	SR	V_{OP_IN} = 2V to 8V, V_{OP_IN} = 8V to 2V, 20% to 80%	-	25	-	V/µs
Settling Time	t_S	V_{OP_IN} = 4.5V to 5.5V, 90%	-	5	-	µs
Power Supply Rejection Ratio	PSRR		-	85	-	dB
Bandwidth	BW	–3dB	-	10	-	MHz

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, VIN1 = VIN2 = 3.3V, V_{VAA} = 10V, V_{GH}= 25V, V_{GL}= –6V, VCOM = 4V)

DVCOM Buffer

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
DVCOM Output Voltage Range	V_{VCOM}	7Bits, Step = 0.01V	2.646	-	4.17	V
DVCOM Output Voltage Accuracy			–1	-	+1	%

RESET (XAO)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
XAO Output Voltage	V_{RST}	I_{RST} = 1.2mA	-	-	0.2	V
XAO Detect Voltage	V_{DET}	5Bits, Step = 0.1V	1.6	-	3.6	V
XAO Delay Time	t_2	3 Bits, Step = 1ms	1	-	8	ms

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, VIN1 = VIN2 = 3.3V, V_{VAA} = 10V, V_{GH}= 25V, V_{GL}= –6V, VCOM = 4V)

I²C Interface

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input High Voltage	V_{IH2}		1.5	-	-	V
SCL, SDA Input Low Voltage	V_{IL2}		-	-	0.6	V
SCL, SDA Input Capacitance	C_{SI}		-	5p	-	F
SDA Output Low Voltage	V_{OL}	I_{SINK} = 3mA	-	-	0.4	V
SCL Clock Frequency	f_{OSCI2C}		-	-	400k	Hz
SCL Clock High Period	t_{IH3}		0.6	-	-	µs
SCL Clock Low Period	t_{IL3}		1.3	-	-	µs
SCL, SDA Receiving Rise Time	t_{R1}		-	20+0.1 *C_B	300	ns
SCL, SDA Receiving Fall Time	t_{F1}		-	20+0.1 *C_B	300	ns
I²C Data Setup Time	t_{S1}		100	-	-	ns
I²C Data Hold Time	t_{H1}		0	-	900	ns
I²C Setup Time for START Condition	t_{S2}		0.6	-	-	µs
I²C Hold Time for START Condition	t_{H2}		0.6	-	-	µs
I²C Bus Free Time Between STOP and START Conditions	t_{BUS}		4.7	-	-	µs
I²C Pulse Width of Suppressed Spike	t_{PS}		0	-	50	ns
I²C Bus Capacitance	C_B		-	-	400	pF
SDA, SCL Pull Up resistor	R_{PU}		4.7	10.0	-	kΩ

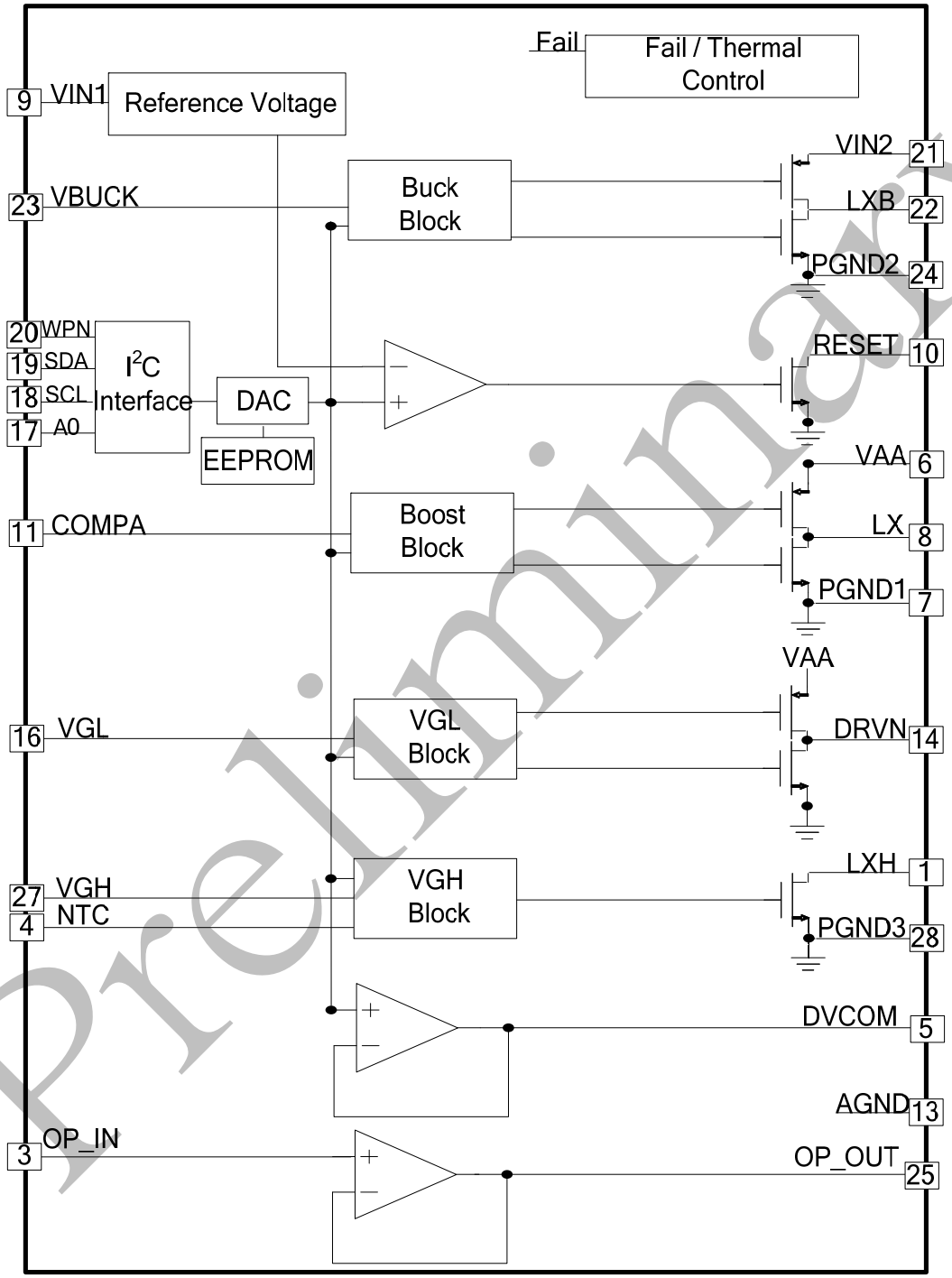
NVM

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Byte Write Time	t_{BYTE}		-	-	10	ms
Byte Read Access Time	B_{RT}		-	200	-	ns
NVM Programmable Times	N_{NVM}		-	1,000		Cycle

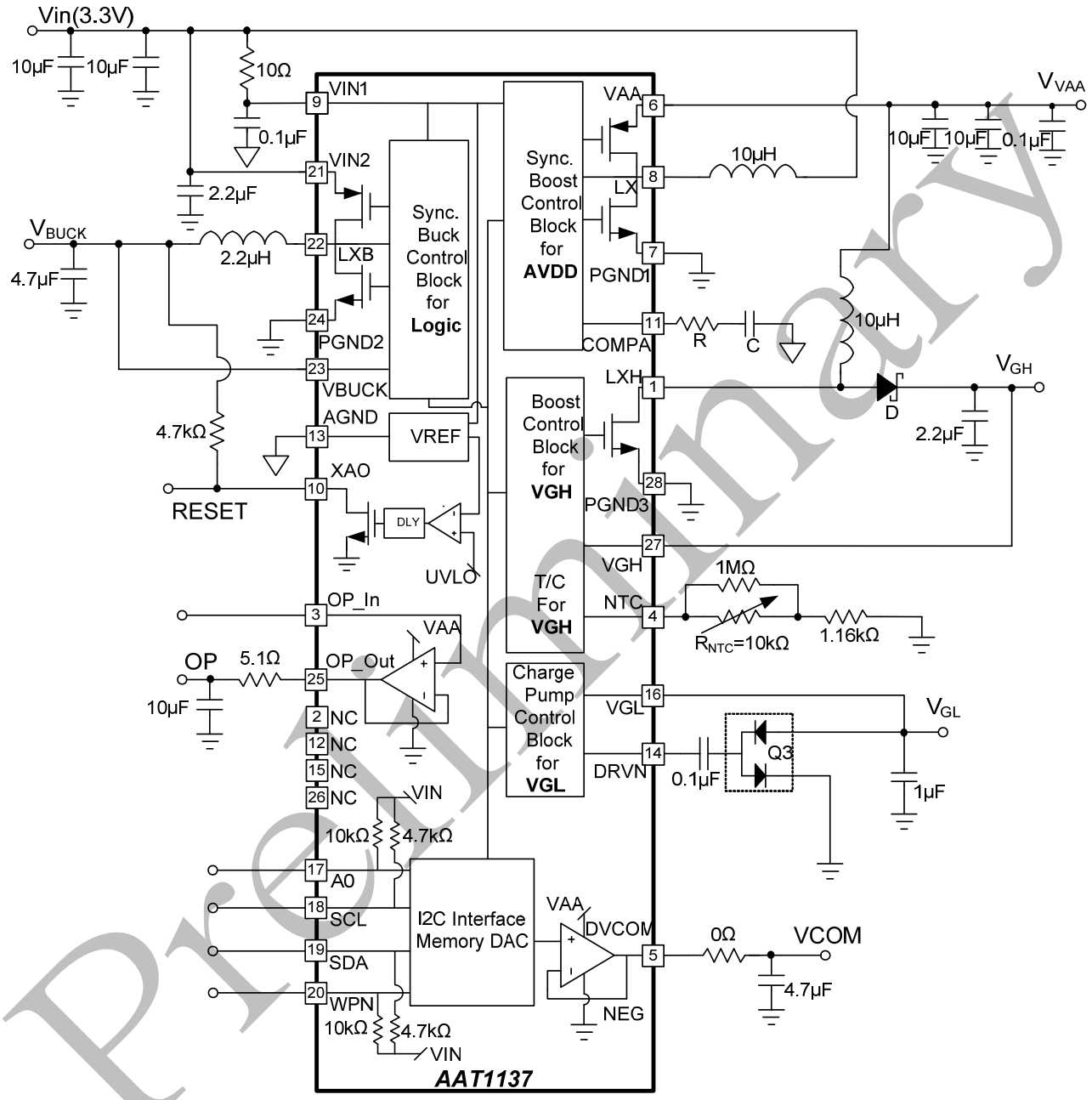
PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	LXH	-	Switch Node of Boost Converter for VGH
2	NC	-	Not Connected
3	OP_OUT	O	Operational Amplifier Output
4	NTC	O	Negative Temperature Compensation Pin for VGH
5	DVCOM	O	VCOM Buffer Output
6	VAA	OI	VAA Boost Converter Output
7	PGND1	-	Power Ground (LX Power Return)
8	LX	-	Switch Node of Boost Converter for VAA
9	VIN1	I	Power Supply Pin for Boost Converter
10	XAO	O	Voltage Detector Output for Reset
11	COMPA	O	Compensation Pin for VAA Boost Converter
12	NC	-	Not Connected
13	AGND	-	Analog Ground
14	DRVN	O	Voltage Driver Output of VGL Regulator
15	NC	-	Not Connected
16	VGL	I	Negative Charge Pump (VGL) Voltage Sense Pin
17	A0	I	I^2C Compatible Device Address Bit 0
18	SCL	I	I^2C Compatible Serial Clock Input
19	SDA	I	I^2C Compatible Serial Data Input/Output
20	WPN	I	Write Protection
21	VIN2	I	Power Supply Pin for Buck Converter
22	LXB	-	Switch Node of Buck Converter
23	VBUCK	I	Output Sensing Pin for Buck Converter
24	PGND2	-	Power Ground (LXB Power Return)
25	OP_In	I	Operational Amplifier Input
26	NC	-	Not Connected
27	VGH	I	VGH Voltage Sensing Pin
28	PGND3	-	Power Ground (LXH Power Return)

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



THEORY OF OPERATION

The AAT1137 offers a complete solution for powering TFT LCD panels. The device integrates two current mode boost regulators, one synchronous boost regulator for the source driver supply, and the second non-synchronous boost regulator with temperature compensation to generate a gate-on voltage for VGH. The AAT1137 also includes a negative charge pump regulator for the gate-off voltage, a synchronous buck regulator for system logic power, a XON reset function for input supply monitor, and two unity-gain operational amplifiers (Buffers) in the device. One unity-gain operational amplifier (Buffer) is for supplying the LCD backplane VCOM, and a second for panel line-repair. The AAT1137 includes various system protection schemes such as soft start, power up sequencing, fault protection, thermal shutdown and supervisory reset. The AAT1137 also includes I^2C interface for various device settings such as output voltages, switching frequency, soft start time, delay time, etc.

Under Voltage Lockout (UVLO)

For systematic startup, AAT1137 employs a UVLO rising threshold of 2.2V typical. Thus, the input supply must exceed the UVLO threshold for the regulators to begin switching. Likewise, the device shuts down all functions when the input voltage is lower than UVLO falling threshold of 2.05V. A 150mV hysteresis is added to prevent device chattering when the input supply is noisy or unstable during power up or power down.

Boost Regulator for VAA

The synchronous VAA boost converter integrates a low R_{DSON} (typical 0.2Ω) NMOS for the low side switch, and a PMOS as the output rectifier. The boost output voltage, over current protection (OCP) threshold, soft start time, delay time and switching frequency are programmed via I^2C interface. The output voltage can be set from 7V to13.3V with a step resolution of 0.1V. Over current protection (OCP) threshold ranges from 2A to 3A with 0.5A steps, soft start time can be set from 3ms to 10ms with 1ms steps, and the delay time can be set from 1ms to 12ms with 1ms steps. The LX switching frequency can be programmed for either 600kHz, 800kHz, 1000kHz, or 1.2MHz. The boost regulator operates from a minimum input voltage of 2.5V, and delivers an output voltage that reaches the maximum capable duty cycle. The duty cycle (D) is calculated by

$$D = \frac{V_O - V_I}{V_O} \text{ or } \frac{V_O}{V_I} = \frac{1}{1-D}$$

where V_O (V_{VAA}) is the output of the boost regulator. Typical maximum duty cycle is approximately 90%.

At the heart of the current mode topology are two feedback loops. See the AAT1137 Boost Regulator (VAA) Functional Block Diagram Figure 1.

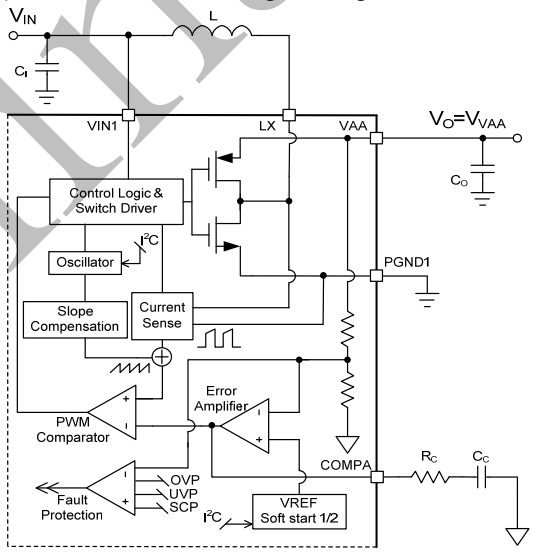


Figure 1. Boost Regulator (VAA) Functional Block Diagram

One feedback loop generates a ramp voltage as the inductor current flows through the on resistance of the internal low side power switch. The second loop monitors the boost output via an internal feedback. This feedback voltage is compared to an internal reference voltage using a transconductance error amp. Note that the internal reference voltage is adjusted via I^2C control to set the output voltage.

Regulation is achieved by modulating the internal low side power switch (NMOS) ON time. During the ON

time, the low side NMOS is turned ON to energize the inductor while the high side power switch (PMOS) rectifier is turned OFF. When the NMOS turns off, the PMOS rectifier will turn ON, releasing the inductor energy to regulate the output. The modulating duty cycle is determined by comparing the error amplifier output to the voltage ramp at the non-inverting input of the PWM comparator. Note that this voltage ramp is the sum of the signals generated by the inductor current sense circuitry and the slope compensation circuitry. Slope compensation is added to prevent sub-harmonic oscillations for duty cycles above 50%. During each rising edge of the internal clock pulse, the low side power switch is turned on. The switch is turned off when the voltage ramp generated at the non-inverting input of the PWM comparator exceeds the output voltage of the error amplifier or the voltage at the inverting input of the PWM comparator.

Over Voltage Protection (OVP) for VAA

When the VAA boost output exceeds its Over Voltage Protection threshold (120% of programmable output voltage), the AAT1137 disables the gate driver of this boost regulator and prevents the internal NMOS from switching. Once VAA voltage falls below the OVP threshold, with a hysteresis of approximately 5%, the boost will resume switching.

Under Voltage Protection (UVP) for VAA

When VAA output voltage drops below its under voltage protection threshold (80% of programmable output voltage) due to overload conditions, an internal fault timer of 50ms is activated. Once activated, if the fault condition surpasses the 50ms, the device will be shutdown. To restart the device, the V_{IN} power must be recycled below the UVLO falling threshold.

Short Circuit Protection (SCP) for VAA

When VAA output voltage drops below its short circuit protection threshold (40% of programmable output voltage) due to short circuit conditions, the device will immediately shutdown. This latched condition is reset by toggling V_{IN} power.

Buck Regulator for VBUCK

The buck regulator includes a high-side PMOS and a low-side NMOS which eliminate the need for an external Schottky diode. Low on-resistance for both the switches maximizes efficiency. Moreover, the buck is compensated internally so that no external compensation network is required.

The buck output voltage is programmed via I^2C interface, and can be set from 0.8V to 3.3V with 0.1V step resolution. The switching frequency of the buck can be set from 1200kHzs to 2.1MHz with 300kHz steps. The delay time before the buck begins its soft start can be programmed from 500µs to 3500µs using 1,000µs steps.

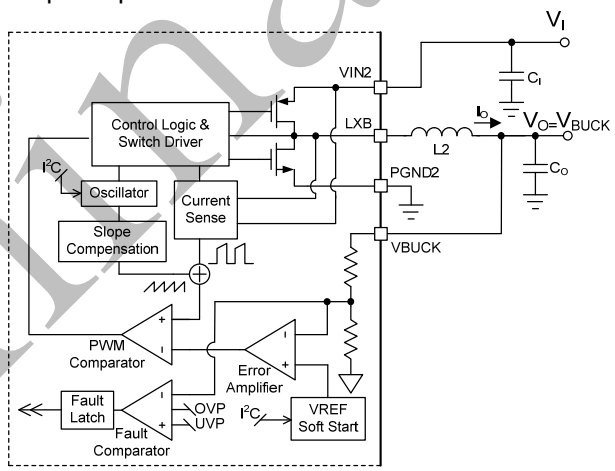


Figure 2. Buck Regulator Functional Block Diagram

The buck regulator also uses the peak current mode PWM control scheme for fast transient response and cycle-by-cycle current limiting. The PWM maintains a constant frequency and varies the duty ratio according to the output voltage and load current. This modulation scheme provides high efficiency at medium to heavy load conditions, and reduces the output ripple at light load conditions. It regulates output voltage from V_{IN} down to an output voltage as low as 0.8V. The duty cycle D is calculated by

$$D = \frac{V_O}{V_I} \quad (V_O = V_{BUCK})$$

where V_O (V_{BUCK}) is the output voltage of the buck regulator.

Buck Current Limit

The buck regulator includes cycle by cycle current limiting, with a threshold of typically 1.2A. When the current limit threshold is reached, the high side PMOS switch is turned off, releasing the inductive energy.

OVP & UVP for VBUCK

The Buck regulator also includes protection mechanisms such as OVP, UVP. When the buck output exceeds its Over Voltage Protection threshold (120% of programmable output voltage), the device will prevent the internal high side MOS from switching. Once the voltage falls below the OVP threshold, with a hysteresis of 5%, the buck will resume switching.

When the buck output drops below the Under Voltage Protection threshold (80% of programmable output voltage), an internal fault timer counter is activated. Once the fault condition surpasses 50ms, the buck and other regulators will be shutdown. To restart the device, the V_{IN} power must be recycled below the UVLO falling threshold.

Boost Regulator for VGH

The non-synchronous boost regulator that supplies the VGH voltage to the TFT-LCD gate-on voltage also uses a current mode control scheme. Similarly, the output voltage is programmed via I^2C interface, and can be set from 15V to 35V with 1V step resolution. The switching frequency of the VGH boost can be set from 600kHzs to 1.2MHz with 200kHz steps. The delay time before VGH powers up can be programmed from 3ms to 18ms using 1ms steps.

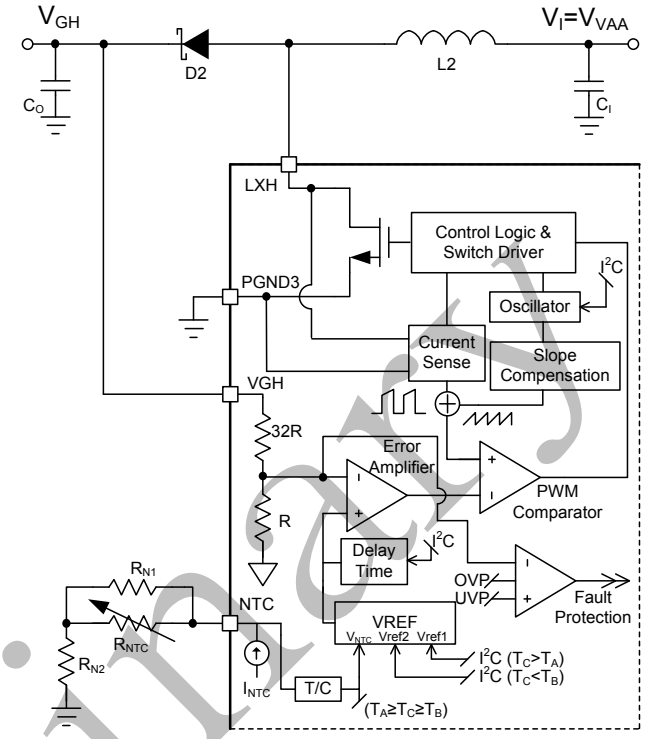


Figure 3. Boost Regulator for VGH Functional Block Diagram

OVP & UVP for VGH

The VGH boost regulator also includes OVP and UVP. Both protection mechanisms are the same as for VAA boost regulator, specifically 80% of VGH for UVP and 105% of VGH for OVP. UVP has a 50ms delay time to ensure a true UVP condition and a triggered condition latches the device, which can only be reset by recycling V_{IN} power.

VGH Temperature Compensation

The voltage (V_{NTC}) at NTC Pin will adjust the reference voltage at the non-inverting input of the error amplifier. This reference voltage will also adjust the VGH regulation voltage, and therefore tune the output voltage (V_{GH}). The output voltage (V_{GH}) is compensated accordingly. For conditions where the temperature is $T_B \leqq T_A \leqq T_C$, as show in the temperature compensation for VGH Figure 4, the reference or voltage at NTC is dependent on the voltage (V_{NTC}) at the NTC Pin via the following equation:

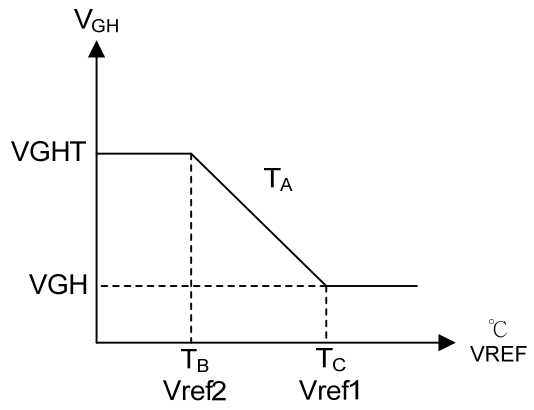


Figure 4. Temperature Compensation for VGH

$$V_{NTC} = I_{NTC} \times \left(R_{N2} + \frac{R_{N1} + R_{NTC}}{R_{N1} \times R_{NTC}} \right)$$

Thus, the output voltage V_{GH} will be

$$V_{GH} = k \times V_{NTC}$$

where k =33 is the internal resistive voltage divider ratio at the non-inverting input of the error amplifier,

If the ambient temperature T_A is below T_B, the V_{GH} voltage will be VGHT, which is set via I^2C and can be set from 25V to 39V with a 1V resolution. Likewise, if T_A is above T_C, the reference generated will be Vref1, and the V_{GH} voltage will be again dependent on the I^2C setting for a range of 15V to 35V. The conditions and equations that determine the V_{GH} voltage are summarized in Table 1.

Table 1.

°C / V	$T_A < T_B$	$T_B \leqq T_A \leqq T_C$	$T_A > T_C$
VREF	Vref2	V_{NTC}	Vref1
VGH	VGHT, I^2C Setting	Dependent on external RNTC network	VGH, I^2C Setting

Example

When $T_B \leqq T_A \leqq T_C$, it can follow below method to estimate the resistance of R_{N1} & R_{N2}, suppose a circuit with the following characteristics is required :

T_C=0°C ; VGH=18V

T_B=－10°C ; VGHT=27V

(1) The first step is to calculate the resistance of R_{NTC} and the 10kΩ NTC thermistor is used.

At Temperature T_C (0°C), R_{NTC_TC}=27680Ω

At Temperature T_B (-10 °C), R_{NTC_TB}=43499Ω

(2) The next step is to calculate the reference voltage of V_{NTC} :

$$V_{NTC(T_C)} = \frac{18V}{33} = 0.545V$$

$$V_{NTC(T_B)} = \frac{27V}{33} = 0.818V$$

(3) Now calculate the resistance of R_{N1}、R_{N2} that use below equation :

$$0.545 = I_{NTC\_TC} \cdot \left(R_{N2} + \frac{R_{NTC\_TC} \cdot R_{N1}}{R_{NTC\_TC} + R_{N1}}\right) \quad (A)$$

$$0.818 = I_{NTC\_TB} \cdot \left(R_{N2} + \frac{R_{NTC\_TB} \cdot R_{N1}}{R_{NTC\_TB} + R_{N1}}\right) \quad (B)$$

Here I_{NTC} at room temperature is 20μA, at T_C is about 19.43μA and 19.11μA at T_B.

(4) Using equation (B) subtract (A), it can obtain the standard quadratic equation :

$$R_{N1} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

Wrere

$$a = \frac{V_{NTC(T_B)}}{I_{NTC\_TB}} - \frac{V_{NTC(T_C)}}{I_{NTC\_TC}} + R_{NTC\_TA} - R_{NTC\_TB}$$

$$a = \frac{0.818}{19.11\mu} - \frac{0.545}{19.43\mu} + 27680 - 43499 \cong -1063.6$$

$$b = \left[\left(\frac{V_{NTC(T_B)}}{I_{NTC\_TB}}\right) - \left(\frac{V_{NTC(T_C)}}{I_{NTC\_TC}}\right)\right] \cdot (R_{NTC\_TC} + R_{NTC\_TB})$$

$$b = \left[\left(\frac{0.818}{19.11\mu}\right) - \left(\frac{0.545}{19.43\mu}\right)\right] \cdot (27680 + 43499) \cong 1.05 \times 10^9$$

$$c = \left[\left(\frac{V_{NTC(T_B)}}{I_{NTC\_TB}}\right) - \left(\frac{V_{NTC(T_C)}}{I_{NTC\_TC}}\right)\right] \cdot R_{NTC\_TC} \cdot R_{NTC\_TB}$$

$$c = \left[\left(\frac{0.818}{19.11\mu}\right) - \left(\frac{0.545}{19.43\mu}\right)\right] \cdot 27680 \cdot 43499 \cong 1.78 \times 10^{13}$$

Using the coefficients a, b and c we can solve the R_{N1}

$$R_{N1} = \frac{-1.05 \times 10^9 + \sqrt{(1.05 \cdot 10^9)^2 - 4 \cdot (-1063.6) \cdot 1.78 \cdot 10^{13}}}{2 \cdot (-1063.6)}$$

R_{N1}=1001457Ω

(5) The final step is to calculate R_{N2} :

$$R_{N2} = \frac{V_{NTC(TB)}}{I_{NTC\_TB}} - \frac{R_{N1} \cdot R_{NTC\_TB}}{R_{N1} + R_{NTC\_TB}}$$

$$R_{N2} = \frac{0.818}{19.11\mu} - \frac{1001457 \cdot 43499}{1001457 + 43499}$$

R_{N2}=1167Ω

Charge Pump Regulator for VGL

The negative charge pump controller is to provide the TFT-LCD gate-off voltage. This charge pump provides a negative voltage ranging from -5V maximum to -14V minimum, programmable with -1V step resolution using I^2C. The charge pump frequency can be programmed for either 0.25*f_{OSC1}, 0.5*f_{OSC1}, 0.75*f_{OSC1}, or 1*f_{OSC1}. The VGL delay time can be set from 0ms to 15ms with a 1ms step resolution. Note that the DRVN output pin can source at least 20mA

The negative charge pump regulator also includes Under Voltage Protection (UVP) mechanisms. When the output drops blow the Under Voltage Protection threshold (80% of programmable output voltage), an internal fault timer counter is activated. Once the fault condition surpasses 50ms, the device will shutdown all regulators. To restart the device, the V_{IN} power must be recycled below the UVLO falling threshold.

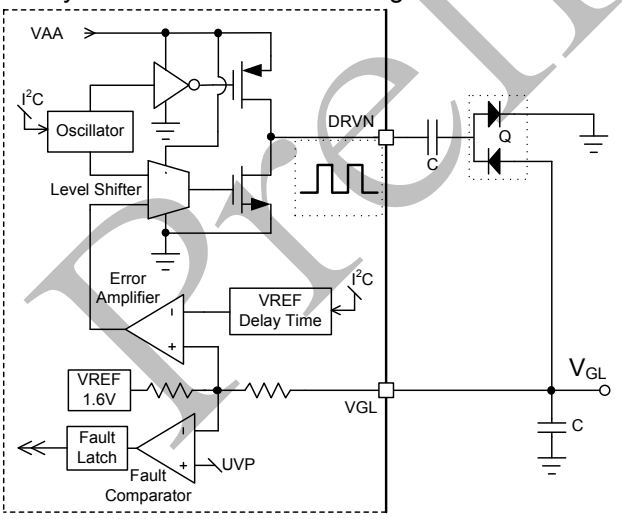


Figure 5. Negative Charge Pump Regulator Functional Block Diagram

Unity-Gain Operational Amplifier

There are two unity-gain operational amplifiers (buffer) in the device. Both buffers are capable of rail-to-rail input and output, ±150mA output short-circuit current, and a 25V/μs slew rate.

In the unity-gain configuration, the capacitive load adds a pole to the loop gain that impacts the stability of the system and leads to output peaking, ringing and oscillation. A higher pole frequency results in greater stability. In fact, if the pole frequency is lower than or close to the unity gain frequency, the pole can have a significant negative impact on phase and gain margins. Therefore, the stability decreases when the capacitive load increases.

One method of improving capacitive load drive is to insert a 2Ω to 20Ω resistor (R_{O1}) in series with the output, as shown in Figure 6. This reduces ringing with large capacitive loads while maintaining DC accuracy.

Another method for improving transient response is to add a snubber circuit at the output. A snubber circuit consists of a resistor (R_{O2}) in series with a capacitor (C_{O2}), which improves output settling time and reduces peaking. The advantage of this topology is that it draws no DC current nor does it reduce the gain.

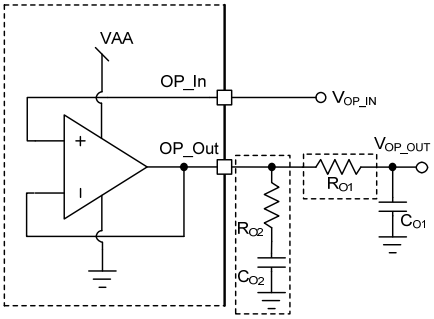


Figure 6. Unity-Gain Operational Amplifier Functional Block Diagram

VCOM Buffer

The programmable VCOM unity-gain operation amplifier can be used to digitally adjust a panel's VCOM voltage to remove flicker by controlling its output sink current. This buffer's output voltage is programmed via I^2C interface, and can be set from 3V to 4.27V with 0.01V step resolution.

Panel Repair-Line Buffer

A second unity-gain operational amplifier (buffer) is for the panel repair-line. Note that this second unity-gain operational amplifier is not controlled by I^2C, and its output voltage is set via the OP_In pin.

RESET (XAO)

This device has an internal reset circuit to monitor the voltage at V_{IN}. When V_{IN} is lower than the detect threshold V_{DET}, XAO output will be pulled low. XAO is an open-drain output that needs a pull-up resistor (R_X = 10kΩ) to a system supply. The V_{DET} is set via I^2C from 1.6V to 3V with 0.1V step resolution. In typical application, see Figure 7 for RESET Functional Block Diagram.

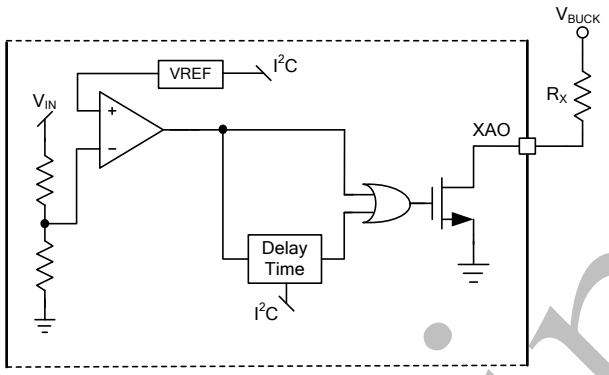


Figure 7. RESET Functional Block Diagram

When V_{IN} rises above its UVLO threshold (2.2V typ.), the output will be pulled High after t_2 delay time has completed. The t_2 delay time ranges from 1ms to 8ms with 1ms steps resolution and also can be set via I^2C. See Figure 8 for RESET Operation Timing Chart

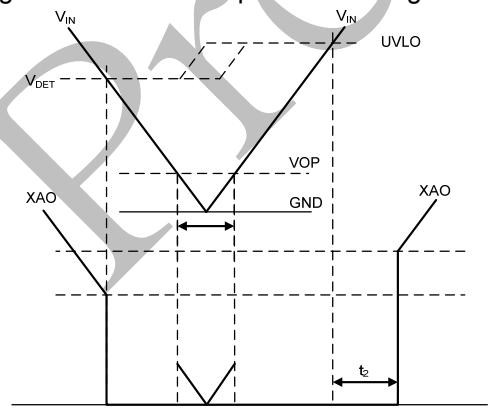


Figure 8. RESET Operation Timing Chart

Thermal Shutdown

The AAT1137 device enters into fault protection shutdown when the junction temperature reaches approximately the thermal shutdown threshold. The thermal shutdown threshold can be set via I^2C at either 125°C, 150°C, 175°C, or 200°C. To restart the device, the junction temperature must fall below the thermal shutdown threshold by the hysteresis value. The hysteresis is set at 20°C.

Power On/Off Sequence

The AAT1137 Power On/Off Sequence is as shown in Figure 9.

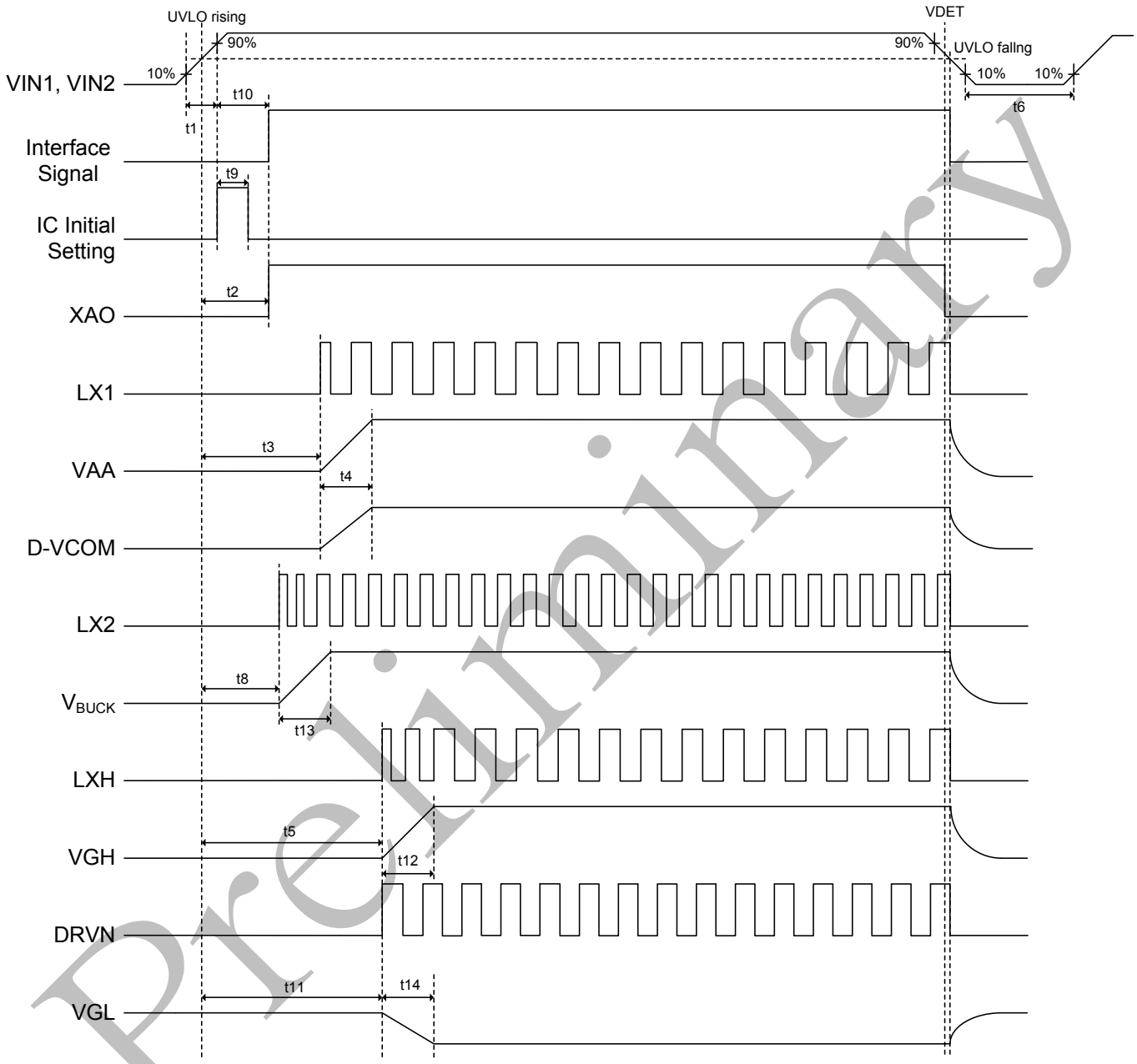


Figure 9. Power On/Off Sequence Timing Diagram

I²C Serial Interface

The AAT1137 features an I²C-compatible, 2-wire serial interface consisting of a SDA and a SCL. SDA and SCL are an I/O with an open-drain output that requires a pull up resistor to realize high-logic levels. The pull up resistors of the AAT1137 has built-in 4.7kΩ. Each slave on the I²C bus responds to a slave address byte sent immediately following a Start Condition. Below diagram shows the definition of timing on I²C bus:

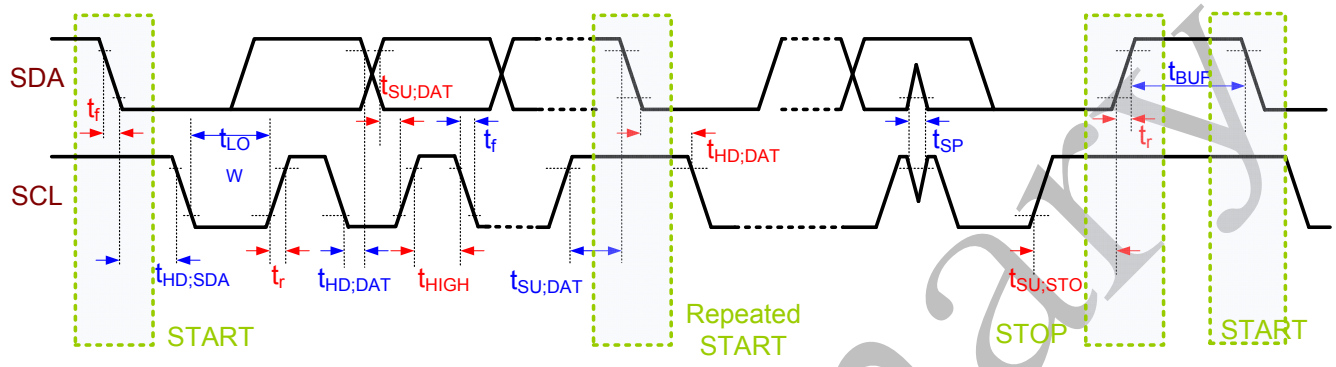


Figure 10. Definition of timing on I²C bus

The slave address byte contains the slave address in the most significant 7 bits and the R/W bit in the least significant bit. The slave address byte of the AAT1137 is shown as following:

1	0	0	1	1	1	A0	R/$\overline{W}$
MSB							LSB

Table 2 AAT1137 slave address byte

The bit 1 can be selected depending on the address pin configuration of A0 when the slave address conflict on the I²C bus.

I²C Protocol

When the R/W bit and A0 are 0 (such as in 9Ch), the master is indicating it will write data to the slave. If R/W = 1 and A0 is 0 (9Dh in this case), the master is indicating it wants to read from the slave. During an I²C write operation, the master must transmit a register address to identify the memory location where the slave is to store the data. The register address is always the second byte transmitted during a write operation following the slave address byte. The AAT1137 register map refers to the Table 3.

During power-up, the values stored in the EE (EEPROM, nonvolatile memory) are recalled into the DR (DAC Register, volatile memory).

Name	Symbol	Address	Default Value	Bit Count	Min	Max	Resolution
Channel Setting	-	00h	00h	7	-	-	-
VAA	V_{VAA}	01h	0Fh (8.5V)	6	7.0V	13.3V	0.1V
VAA LX Frequency	f_{OSC1}	02h	03h (1200kHz)	2	600kHz	1200kHz	200kHz
Soft-start Time1	t_3	03h	02h (3ms)	4	1ms	12ms	1ms
Soft-start Time2	t_4	04h	01h (4ms)	3	3ms	10ms	1ms
XAO Voltage	V_{DET}	05h	06h (2.2V)	5	1.6V	3.6V	0.1V
XAO Delay time	t_2	06h	00h (1ms)	3	1ms	8ms	1ms
Buck	V_{BUCK}	07h	04h (1.2V)	5	0.8V	3.3V	0.1V
Buck SW Frequency	f_{OSC2}	08h	00h (1200kHz)	2	1200kHz	2100kHz	300kHz
Buck Delay time	t_8	09h	00h (500µs)	2	500µs	3500µs	1000µs
VGH	V_{GH}	0Ah	03h (18V)	5	15V	35V	1V
VGH shaping Voltage	V9	0Bh	05h (11V)	4	1V	29V	2V
VGH Delay time	t_5	0Ch	02h (5ms)	4	3ms	18ms	1ms
VGH LX Frequency	f_{OSC3}	0Dh	03h (1200kHz)	2	600kHz	1200kHz	200kHz
D-Vcom	V_{VCOM}	0Eh	14h (3.2V)	7	3.0V	4.27V	0.01V
VAA OCP Setting	V_{OCP}	0Fh	02h (2.5A)	2	2A	3A	0.5A
OTP Setting	T_{SH}	10h	02h (175°C)	2	125°C	200°C	25°C
VAA Comp Setting	V_{COMP}	11h	02h	2	-	-	-
VGL	V_{GL}	12h	01h (-6V)	4	-5V	-14V	-1V
VGL DRVN Frequency	f_{OSC4}	13h	01h (0.5* f_{OSC1})	2	0.25* f_{OSC1}	f_{OSC1}	0.25
VGL Delay time	t_{11}	14h	00h (0ms)	4	0ms	15ms	1ms
VGHT	V_{GHT}	15h	06h (31V)	4	25V	39V	1V
Control Register	-	FFh	00h	8	-	-	-

Channel setting register 00h – Default 00h

MSB	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	LSB
Reserved	D-Vcom Enable=0 Disable=1	Vbuck Enable=0 Disable=1	VAA Enable=0 Disable=1	VGH Enable=0 Disable=1	VGL Enable=0 Disable=1	GPM Enable=0 Disable=1	NTC Enable=0 Disable=1

VAA Comp setting register 11h – Default 02h

MSB	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0

00h: External compensation

01h: Internal compensation, P<=0.4W

02h: Internal compensation, 0.4W<P<=0.8W (default)

03h: Internal compensation, 0.8W<P<=1.3W

Control register (FFH)

MSB	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	LSB
WEE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EE/$\overline{DR}$

*WEE =1: Write data to EEPROM.

EE/$\overline{DR}$=1: Read data from EEPROM.

EE/$\overline{DR}$=0: Read data from DAC register.

Table 3. Register Map

WRITE OPERATION

Write single byte to the DR (DAC Register):

Step 1: Master sends Start Condition.

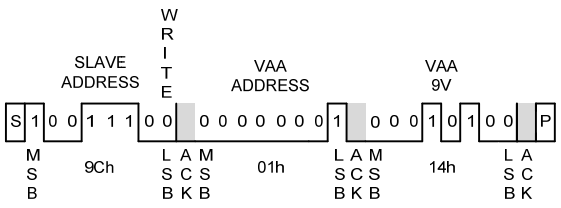
Step 2: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)
AAT1137 will acknowledge a bit for this byte.

Step 3: Send DR address (ex.01h, address of VAA)
AAT1137 will acknowledge a bit for this byte

Step 4: Send the data to be written to the DR (ex.14h, VAA = 9V)
AAT1137 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Example: Writing 14h (9V) to the DR address 01h (VAA)



Write multiple bytes to the DR (DAC register):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)

AAT1137 will acknowledge a bit for this byte.

Step 3: Send DR address (ex.01h, address of VAA)

AAT1137 will acknowledge a bit for this byte

Step 4: Send the data to be written to the DR (ex.14h, VAA = 9V)

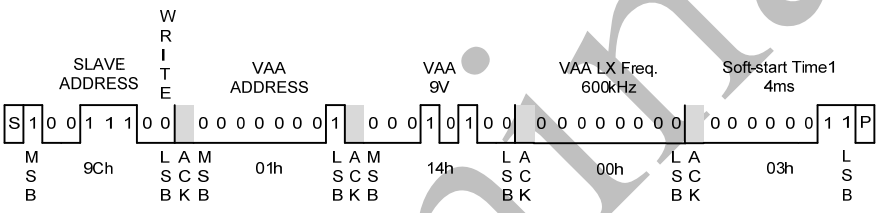
AAT1137will acknowledge a bit for this byte

Step 5: Master continues sending the other bytes to be written to the DRs.

AAT1137 will acknowledge a bit for each byte and DR address will automatically increase

Step 6: Master sends Stop Condition.

Example: Writing 14h(9V), 00h(600kHz), 03h(4ms) to the DR address 01h, 02h, 03h (VAA, VAA LX Frequency, Soft-start Time1)



Write all DR (DAC Register) data to EE (EEPROM):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)

AAT1137 will acknowledge a bit for this byte.

Step 3: Send CR (Control Register) address (FFh)

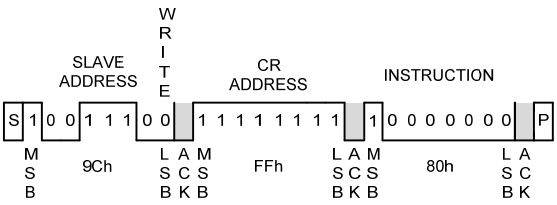
AAT1137 will acknowledge a bit for this byte

Step 4: Send the instruction 1XXXXXXXb (X: Don't care, ex. 80h) to make duplicate dates from DR to EE

AAT1137 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Example: Writing all DR data to EE



READ OPERATION

Read single data from DAC register (DR):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)
AAT1137 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1137 will acknowledge a bit for this byte

Step 4: Send the instruction 0XXXXXX0b (X: Don't care, ex. 00h) to specify that the data is read from the DR
AAT1137 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)
AAT1137 will acknowledge a bit for this byte.

Step 8: Send specified DR address to be read (ex.01h, address of VAA)
AAT1137 will acknowledge a bit for this byte

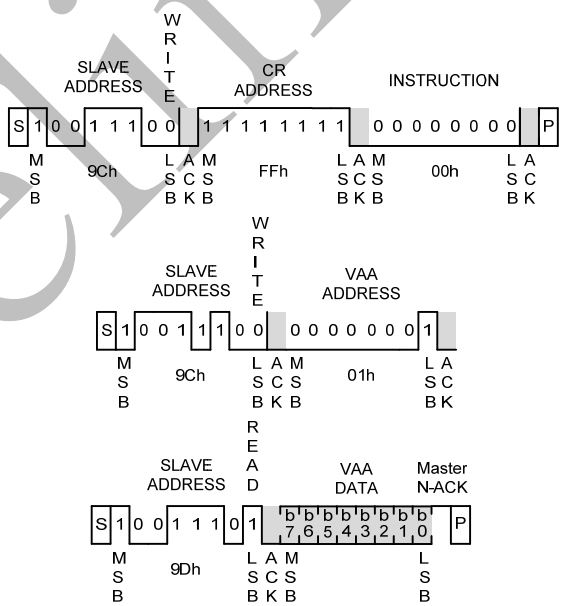
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value 9Dh. (the AAT1137 address 1001110b and R/W bit = High)
AAT1137 will acknowledge a bit for this byte.

Step 11: Master read the data from DR and not-acknowledges for this byte.

Step 12: Master sends Stop Condition.

Example: Reading data from the DR addresses 01h (VAA)



Read multiple data from DAC register (DR):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)
AAT1137 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1137 will acknowledge a bit for this byte

Step 4: Send the instruction 0XXXXXX0b (X: Don't care, ex. 00h) to specify that the data is read from the DR
AAT1137 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)
AAT1137 will acknowledge a bit for this byte.

Step 8: Send specified DR address to be read (ex.01h, address of VAA)
AAT1137 will acknowledge a bit for this byte

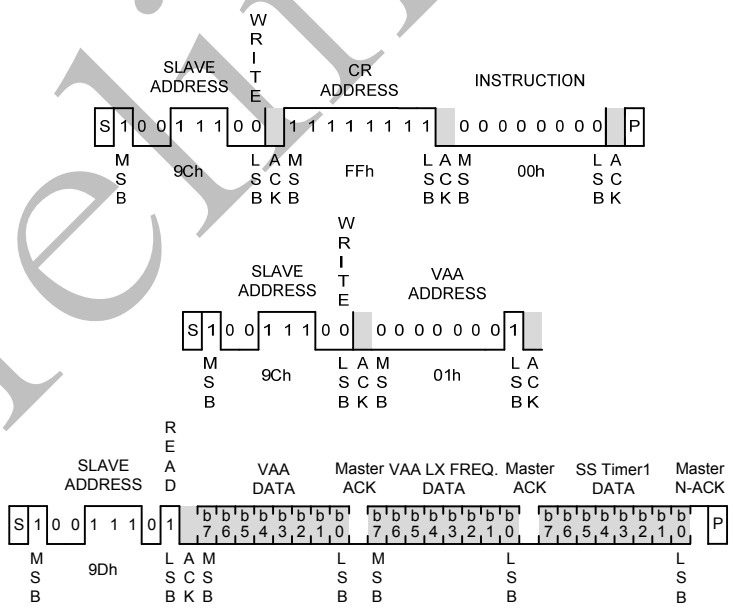
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value 9Dh. (the AAT1137 address 1001110b and R/W bit = High)
AAT1137 will acknowledge a bit for this byte.

Step 11: Master continues read the data from DR and acknowledges a bit for each byte. But, master not-acknowledges after received the last reading data. The DR address will automatically increase

Step 12: Master sends Stop Condition.

Example: Reading data from the DR addresses 01h, 02h, 03h (VAA, VAA LX Frequency, Soft-start Timer1)



Read single data from EEPROM (EE):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)
AAT1137 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1137 will acknowledge a bit for this byte

Step 4: Send the instruction 0XXXXXX1b (X: Don't care, ex. 01h) to specify that the data is read from the EE
AAT1137 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)
AAT1137 will acknowledge a bit for this byte.

Step 8: Send specified EE address to be read (ex.01h, address of VAA)
AAT1137 will acknowledge a bit for this byte

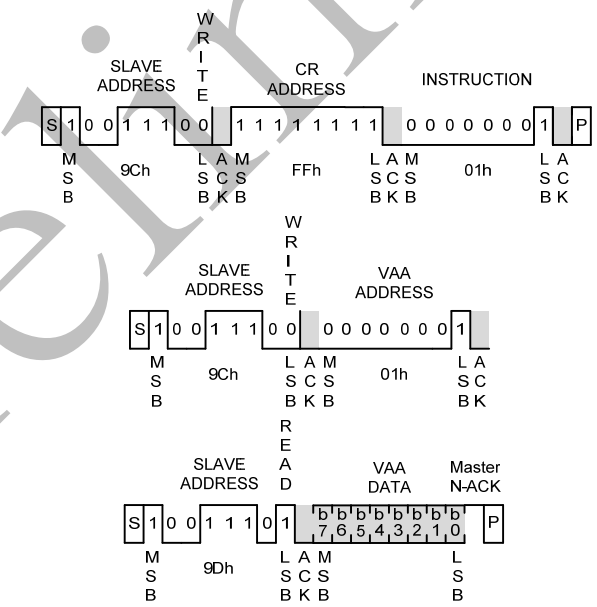
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value 9Dh. (the AAT1137 PMIC address 1001110b and R/W bit = High)
AAT1137 will acknowledge a bit for this byte.

Step 11: Master read the data from EE and not-acknowledges for this byte.

Step 12: Master sends Stop Condition.

Example: Reading data from the EE addresses 01h (VAA)



Read multiple data from EEPROM (EE):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)
AAT1137 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
AAT1137 will acknowledge a bit for this byte

Step 4: Send the instruction 0XXXXXX1b (X: Don't care, ex. 01h) to specify that the data is read from the EE
AAT1137 will acknowledge a bit for this byte

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value 9Ch. (the AAT1137 address 1001110b and R/W bit = Low)
AAT1137 will acknowledge a bit for this byte.

Step 8: Send specified EE address to be read (ex.01h, address of VAA)
AAT1137 will acknowledge a bit for this byte

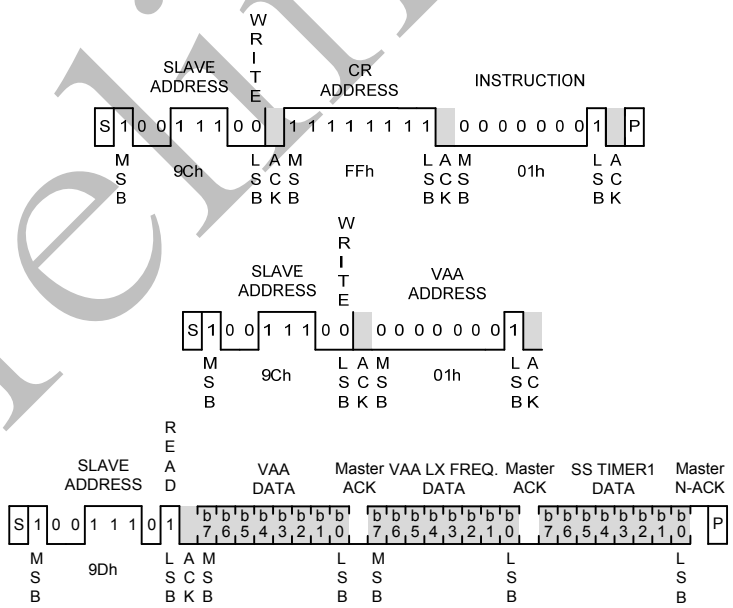
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value 9Dh. (the AAT1137 PMIC address 1001110b and R/W bit = High)
AAT1137 will acknowledge a bit for this byte.

Step 11: Master continues read the data from EE and acknowledges a bit for each byte. But, master not-acknowledges after received the last reading data. The EE address will automatically increase

Step 12: Master sends Stop Condition.

Example: Reading data from the EE addresses 01h, 02h, 03h (VAA, VAA LX Frequency, Soft-start Timer1)



S: Start Condition, P: Stop Condition, X : Don't Care, : Master to Slave, :Slave to Master

LAYOUT CONSIDERATION

System performance such as stability, transient response, and EMI is greatly affected by the PCB layout. Below are some general layout guidelines to follow when designing in the AAT1137.

Inductor

Always try to use shielded low EMI inductor with a ferrite core.

Bypass Capacitors

Place the low ESR ceramics bypass capacitors as close as possible to the VIN (VIN1 & VIN2) pin. This will help eliminate trace inductance effects and will minimize noise present on the internal supply rail. The ground connection of the VIN bypass capacitor should referenced to analog ground (AGND).

Output Capacitors

Minimize the trace length and maximize the trace width to minimize the parasitic inductance between the output capacitors of each regulator and its load for best transient response.

High Current Loop

The boost and buck regulator contain the high current loop. High current flows from the positive terminal of the input bulk capacitor, through the inductor, the catch diode, the output capacitor, to the negative terminal of the output capacitor, and back to the negative terminal of the input bulk capacitor. This high current path should be minimized in length and its trace width maximized. The inductor, catch diode, output capacitor should be placed as close as possible to the switch node LX (LX, LXB, LXH). The input bulk capacitance should also be placed close to these power path components to shorten the power ground length between the input and output.

Feedback and Compensation Components

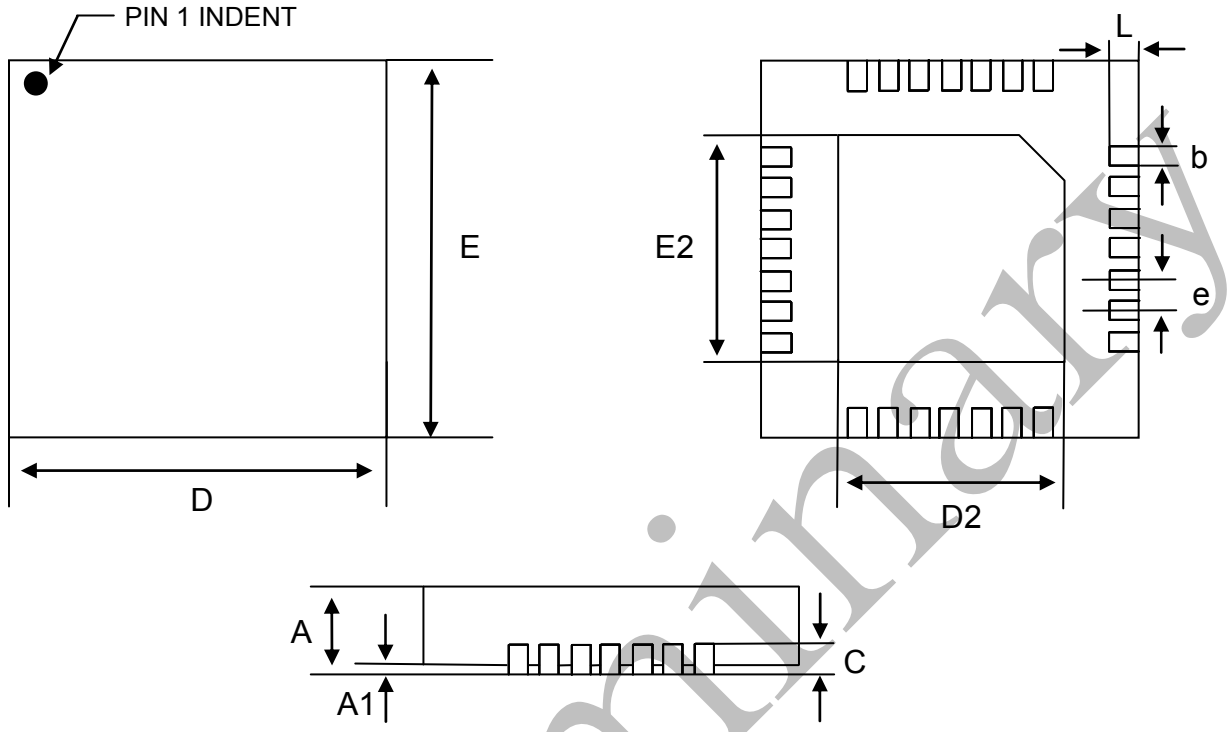
Any components for feedback should be placed as close as possible to its respective feedback pin. Minimize any feedback trace length to avoid noise pickup. Likewise, compensation components should be place as close as possible to the pin or device.

Ground Plane

Use a power ground plane for the boost and buck output capacitor ground, for the boost and buck input bulk capacitor ground, charge pump output capacitor grounds, and PGND pins PGND1, PGND2, PGND3). All power ground nodes should be connected using short trace length but wide trace width, which helps lower IR drops and minimize noise. Create an analog ground plane (AGND) for VIN bypass capacitor grounds, compensation component ground, feedback resistive network grounds, and also the AGND pins. Note that the IC's bottom side expose pad should also be connected to the analog ground plane. Analog ground (AGND) and power ground ((PGND1, PGND2, PGND3) should be connected only at one signal point, near the expose pad by shorting the AGND pin to the expose pad.

PACKAGE DIMENSION

WQFN28-4X4



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
C	---	0.20	---
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e	-----	0.40	-----
L	0.35	0.40	0.45