

DATA SHEET

AB1100

Bluetooth 3.0 Single Chip for HID Applications

Preliminary Specification

VERSION 0.30 15-Mar-2010

AIROHA
Airoha Technology Corp.

This document is commercially confidential and must NOT be disclosed to third parties without prior consent. The information provided herein is believed to be reliable. But production testing may not include testing of all parameters. AIROHA Technology Corp. reserves the right to change information at any time without notification. ([HTTP://WWW.AIROHA.COM.TW](http://WWW.AIROHA.COM.TW) TEL:+886-3-6128800 FAX:+886-3-6128833 sales@airoha.com.tw)

This document is commercially confidential and must **NOT** be disclosed to third parties without prior consent.

The information provided herein is believed to be reliable. But production testing may not include testing of all parameters. AIROHA Technology Corp. reserves the right to change information at any time without notification.

Revision History

Version	Change Summary	Date	Author
0.10	Created	26-Sept-08	KH Chen
0.20	Update for AB1100D	25-Aug-09	Purple Liu
0.30	Update for AB1100E	15-Mar-10	Purple Liu

INDEX

REVISION HISTORY	2
REVISION HISTORY	3
1 FEATURES	6
2 DESCRIPTION.....	7
2.1 RADIO TRANSCEIVER	7
2.2 BASEBAND PROCESSOR	8
2.3 SERIAL COMMUNICATION INTERFACE	8
2.4 PERIPHERALS	8
3 PIN DEFINITION	10
4 PIN DESCRIPTION.....	11
5 RADIO TRANSCEIVER	13
5.1 RF FRONT-END.....	13
5.2 RECEIVER	13
5.3 TRANSMITTER	14
5.4 SYNTHESIZER	14
6 BASEBAND PROCESSING UNIT	15
6.1 BLUETOOTH FRAME DATA PROCESSOR	15
6.2 MODULATOR AND DEMODULATOR	16
6.3 BLUETOOTH TIMING PROCESSING UNIT	16
7 MCU AND MEMORY	17
8 PERIPHERAL CONTROL AND SERIAL COMMUNICATION INTERFACES .	18
9 POWER MANAGEMENT / REGULATION.....	19
9.1 POWER REGULATION	19
9.2 POWER MANAGEMENT UNIT (PMU).....	19
10 SOFTWARE STACK	20

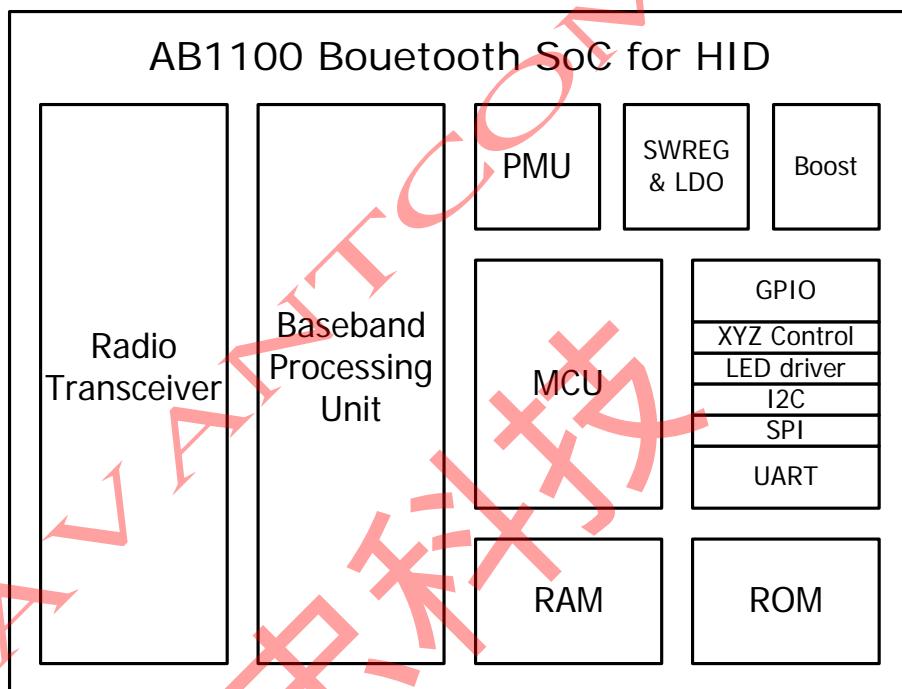
10.1 KEY FEATURES OF HID DEVICE STACK.....	.20
10.2 DEVELOPMENT ENVIRONMENTS AND TOOLS21
10.2.1 Software Development Environments	21
10.2.2 Test and Configuration Tools	21
11 ELECTRICAL CHARACTERISTICS	22
11.1 ABSOLUTE MAXIMUM RATINGS.....	.22
11.2 RECOMMENDED OPERATING CONDITIONS22
11.3 DIGITAL TERMINALS.....	.23
11.4 REFERENCE CLOCK23
11.5 SWITCHING REGULATOR CHARACTERISTICS24
11.5.1 BUCK REGULATOR24
11.5.2 BOOST REGULATOR24
11.6 TYPICAL CURRENT CONSUMPTION.....	.25
11.7 RADIO CHARACTERISTICS26
11.7.1 TRANSMITTER (BASIC DATA RATE).....	.26
11.7.2 RECEIVER (BASIC DATA RATE)27
11.7.3 TRANSMITTER (ENHANCED DATA RATE).....	.28
11.7.4 RECEIVER (ENHANCED DATA RATE)29
12 PACKAGE INFORMATION	30

1 Features

- Compliant with Bluetooth 3.0 specifications
- HID profile version 1.0 compliant
- Supports AFH
- Supports sniff sub-rating for longer battery life & faster re-connect
- Supports up to 19 buttons and 3 optical axis detection
- Supports SPI interface with 3/4-wire mode to sensor IC
- Supports I2C EEPROM interface
- Supports UART interface for firmware downloading and peripheral control
- Embedded 2 LED drivers with fader
- Low cost ROM based design with customer code support
- Embedded power management unit
- Integrated 1.8V Buck and 2.7~3.3V Boost switching regulator
- Single RF port for transmitter and receiver
- Receiver sensitivity of -88dBm at basic data rate
- Transmit power up to +6dBm with 20 dB gain tuning range
- QFN 7mmx7mm 56 pin package

2 Description

AB1100 is a single-chip IC for HID applications, which supports Bluetooth system version 3.0 features including AFH function. It supports sniff sub-rating for longer battery life & faster re-connect. Bluetooth 3.0 simple-pairing mechanism is also implemented. AB1100's scatternet can join up to 3 piconets. It complies with RF transceiver, baseband processor, PMU, switching regulator and Boost regulator. Several Serial Communication Interfaces including UART, I2C and SPI are supported.



2.1 Radio Transceiver

A common RF terminal is shared by the TX/RX paths of AB1100 with embedded TX/RX switch. Only an external balun and 3 matching components are required in the RF port.

A Low-IF architecture is implemented in the receiver part. The receiver sensitivity is -88dBm at basic data rate. The RSSI value which indicates the received signal power level is also measured and provided to the upper layers.

A direct-up conversion architecture is used in the transmitter part. The output power level at TX part is +6dBm for the basic data rate, with 20dB VGA gain tuning range.

A fractional-N synthesizer is implemented in AB1100 with internal loop filters such that no external components are required.

An internal crystal oscillator is integrated such that only an external 26MHz crystal is required. An internal 32.768KHz slow clock is also generated. External clock signal can also be fed into AB1100 instead of the 26MHz crystal clock signal.

2.2 Baseband Processor

The Baseband Processor of AB1100 supports Bluetooth 3.0 specifications including AFH. A digital data processing unit is in charge of the GFSK, DQPSK and D8PSK modulation/demodulation, channel filtering, error detection/correction, and burst framing.

A MCU-based Link Controller is implemented for the whole baseband control functions. A firmware is in charge of the Link Management Protocols, Profiles and MMI. Several hardware accelerators are implemented to support the baseband processing such as encryption, scatter-net operation, etc.

2.3 Serial Communication Interface

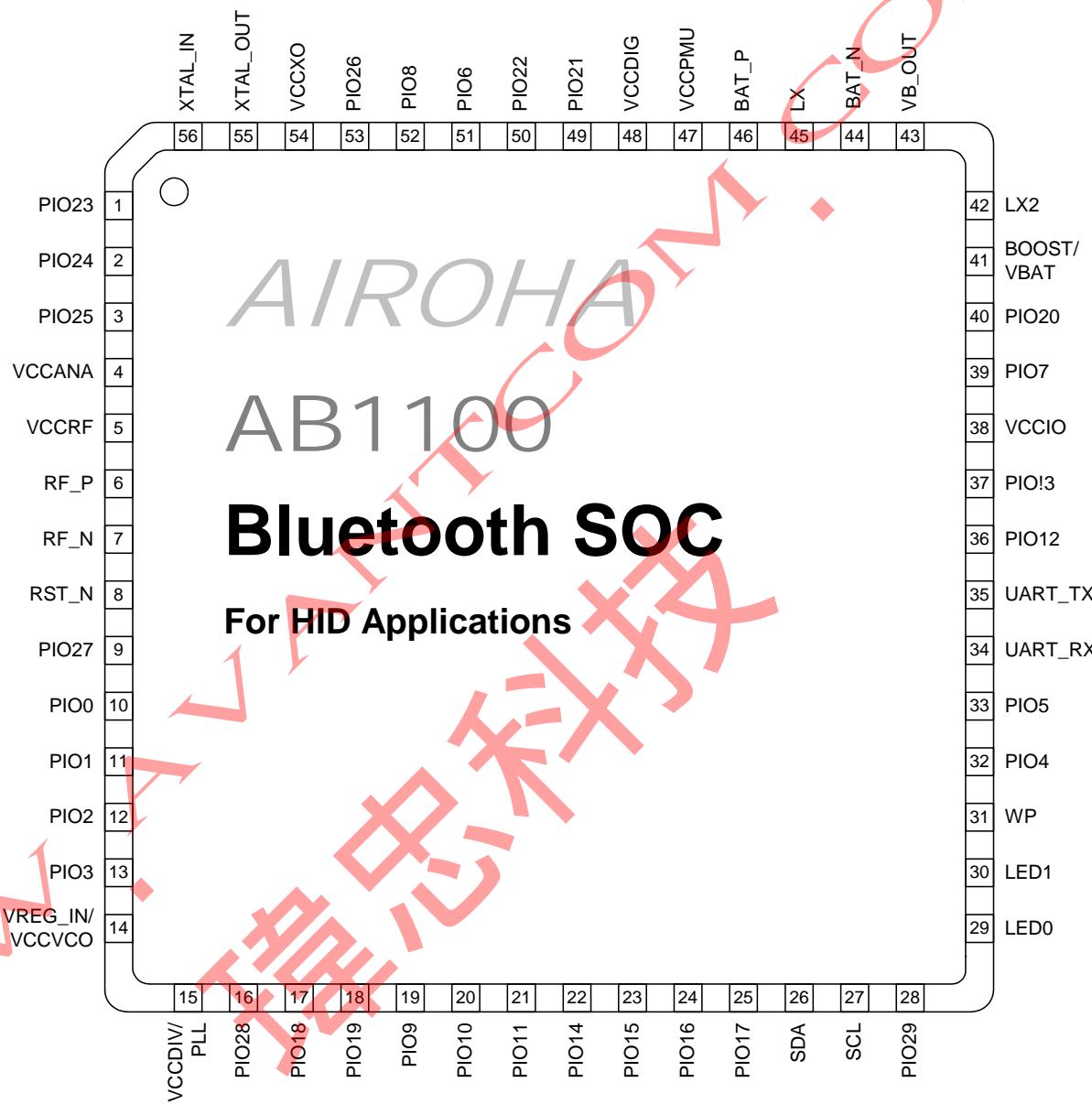
Several Serial Communication Interfaces including UART and SPI are supported in AB1100. A 1.8/3.3V I2C interface is implemented for EEPROM access. Up to 19 buttons and 3 optical axis detection are supported for external button control. Two LED drivers with faders for blue/red LEDs are also included.

2.4 Peripherals

An on-chip switching regulator or a linear regulator is used to provide 1.8V VCC to the whole chip from battery supply. A 2.7~3.3V (selectable) Boost switching regulator is also included for the power supply of PMU, LED and external sensor IC of the HID device. A PMU is embedded in AB1100 for the power management affairs.

ALLANTCOM.COM
捷聯公司

3 Pin Definition



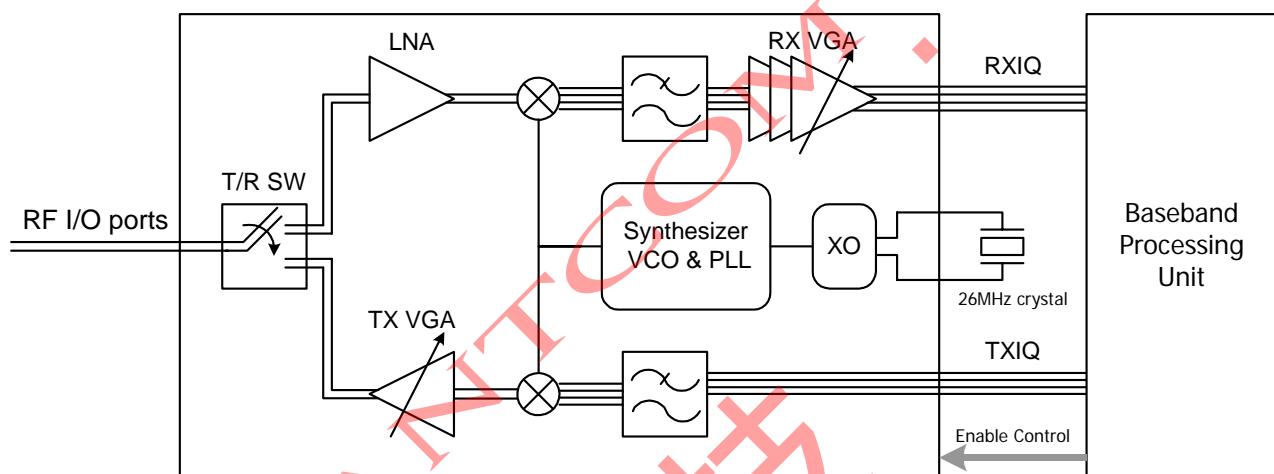
4 Pin Description

PIN	SIGNAL	TYPE	DESCRIPTION
1	PIO23	Input/Output, Digital	Programmable IO
2	PIO24	Input/Output, Digital	Programmable IO
3	PIO25	Input/Output, Digital	Programmable IO
4	VCCANA	Supply, 1.8V	VCC for IF/DA/AD
5	VCCRF	Supply, 1.8V	VCC for TX/RX front-end
6	RF_P	Input/Output, Differential RF	RF input/output P
7	RF_N	Input/Output, Differential RF	RF input/output N
8	RST_n	Input, Digital	Global reset
9	PIO27	Input/Output, Digital	Programmable IO
10	PIO0	Input/Output, Digital	Programmable IO
11	PIO1	Input/Output, Digital	Programmable IO
12	PIO2	Input/Output, Digital	Programmable IO
13	PIO3	Input/Output, Digital	Programmable IO
14	VREG_IN	Supply, 1.8V	VCO regulator input
15	VCCDIV	Supply, 1.8V	VCC for Divider bias
16	PIO28	Input/Output, Digital	Programmable IO
17	PIO18	Input/Output, Digital	Programmable IO
18	PIO19	Input/Output, Digital	Programmable IO
19	PIO9	Input/Output, Digital	Programmable IO
20	PIO10	Input/Output, Digital	Programmable IO
21	PIO11	Input/Output, Digital	Programmable IO
22	PIO14	Input/Output, Digital	Programmable IO
23	PIO15	Input/Output, Digital	Programmable IO
24	PIO16	Input/Output, Digital	Programmable IO
25	PIO17	Input/Output, Digital	Programmable IO
26	SDA	Input/Output, Digital	I2C data line, 1.8V
27	SCL	Input/Output, Digital	I2C clock line, 1.8V
28	PIO29	Input/Output, Digital	Programmable IO

29	LED0	Open Drain	LED 0 for Red Light
30	LED1	Open Drain	LED 1 for Blue Light
31	WP	Output, Digital	Write Protect Control for EEPROM
32	PIO4	Input/Output, Digital	Programmable IO
33	PIO5	Input/Output, Digital	Programmable IO
34	UART_RX	Input, Digital	UART RX
35	UART_TX	Output, Digital	UART TX
36	PIO12	Input/Output, Digital	Programmable IO
37	PIO13	Input/Output, Digital	Programmable IO
38	VCCIO	Supply, 1.8V~3.3V	VCC for IO
39	PIO7	Input/Output, Digital	Programmable IO
40	PIO20	Input/Output, Digital	Programmable IO
41	BOOST_VBAT	Input, Analog	Boost Enable Signal
42	LX2	Supply	Boost Regulator input
43	VB_OUT	Output, 2.7~3.3V	Boost Regulator output
44	BAT_N	GND	Battery input N, Connected to GND
45	LX	Analog	Switching Regulator output
46	BAT_P	Supply	Battery input P, as Switching/Linear regulator input
47	VCCPMU	Supply, 5V	VCC for PMU
48	VCCDIG	Supply, 1.8V	VCC for Digital circuits
49	PIO21	Input/Output, Digital	Programmable IO
50	PIO22	Input/Output, Digital	Programmable IO
51	PIO6	Input/Output, Digital	Programmable IO
52	PIO8	Input/Output, Digital	Programmable IO
53	PIO26	Input/Output, Digital	Programmable IO
54	VCC XO	Supply, 1.8V	VCC for XO
55	XTAL_OUT	Analog	Crystal output
56	XTAL_IN	Analog	Crystal input

5 Radio Transceiver

The AB1100 RF transceiver is a 2.4GHz-band transceiver for the Bluetooth applications. There are three main functions – transmitter, receiver, and synthesizer. The enable control signals of these functions are given by the Baseband Processing Unit.



5.1 RF Front-end

The RX input ports and TX output ports share the same RF terminals such that no external T/R switch is required. Only a balun and some matching components are placed outside the RF terminals.

5.2 Receiver

The AB1100 RF receiver implements a Low-IF architecture, which is composed with two parts: RF front-end and Low-IF part. The RF front-end part comprises a LNA and a quadrature mixer. The LIF part comprises a low-pass filter (LPF) for out-band filtering and a variable gain amplifier (VGA).

The LNA input shares the same RF ports with TX output. The RX front-end gain could be adjusted, and thus reduce the probability of bit errors caused by poor signal-to-noise ratio. After the LNA is followed by a quadrature mixer that down-converts the RF signal to Low-IF band.

At the LIF part, the down-converted signal is first low-pass filtered by the LPF, amplified by the VGA, and then sent to the ADC for demodulation. The 3dB bandwidth of the LPF could be adjusted through RF registers. The LNA and VGA provide more than 80dB gain control range.

5.3 Transmitter

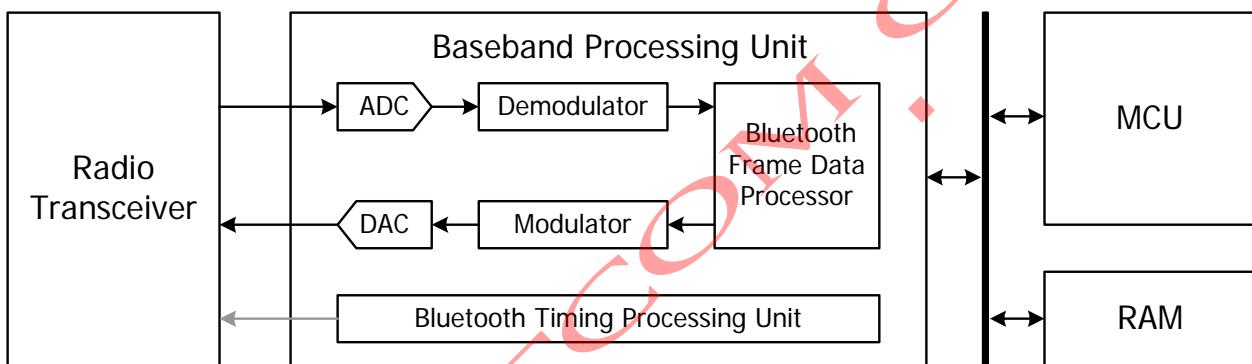
The AB1100 RF transmitter implements a direct-up-conversion architecture, which comprises a LPF, a modulator and a VGA stage. The TX baseband signals are fed from baseband DAC, generated by the baseband modulators. A LPF is implemented to attenuate the second sidelobe of signal spectrum and unwanted oversampling clock or spurious signals. The 3dB bandwidth of the LPF could be adjusted through RF registers. The VGA provides variable gain with more than 28dB dynamic range, and could be controlled through RF register interface.

5.4 Synthesizer

The AB1100 implements a fractional-N synthesizer with embedded VCO and loop filter without the need of external components. AB1100 also integrates an internal crystal oscillator that only an external 26MHz crystal is required. External clock signal can also be fed into AB1100 instead of the 26MHz crystal clock signal.

6 Baseband Processing Unit

The Baseband Processing Unit (BPU) comprises a Digital-to-Analog Convert (DAC), an Analog-to-Digital Converter (ADC), a digital modulator, a digital demodulator, a Bluetooth Frame Data Processor, and a Timing Processing Unit (TPU).



6.1 Bluetooth Frame Data Processor

AB1100 baseband processing unit supports all packet types of Bluetooth 1Mbps, 2Mbps and 3Mbps modes. On transmitter side, the frame data processor can construct Bluetooth data packet according to the packet type given by MCU. The constructed data packet then will be converted to analog modulated signal format by the modulator and DAC.

On the receiver side, the analog received signal will be first converted to digitized data format by the ADC and demodulator, and then the frame data processor will de-construct the received data to several parts and identify if the received signal is a valid Bluetooth packet and if the packet is for the device itself. The received header data and PSDU data will be stored into memory if it is a valid Bluetooth data packet and is for the device itself.

Access code check, Header Error Check (HEC) and PSDU CRC checking functions are performed by the frame data processor, too, to see if this received signal is valid and error free or not. A data whitening circuit and an encryption engine are also included in the frame data processor for both transmitter and receiver paths.

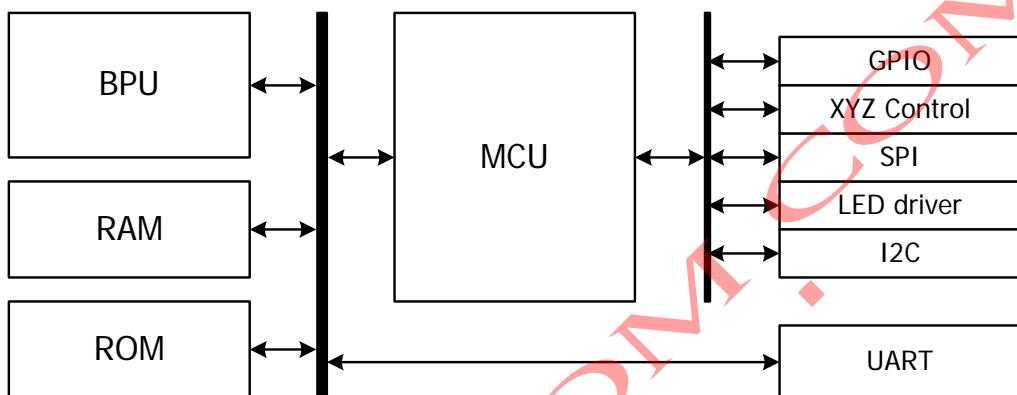
6.2 Modulator and Demodulator

The modulator can generate GFSK, DQPSK and D8PSK signals according to which data rate is adopted in the frame data. The demodulator can convert the received data signal to digitized data bit format according to the modulation type indicated in the header region.

6.3 Bluetooth Timing Processing Unit

A Bluetooth Timing Processing Unit (TPU) is embedded in the Baseband processing unit. TPU is in charge of generating RF timing control signals to the RF radio part, such as TX enabling signals and RX enabling signals.

7 MCU and memory



The micro-control unit (MCU) executes the Bluetooth protocol software stack, controls the Bluetooth baseband processing unit (BPU) and Serial Communication Interfaces. 2Mbits ROM is embedded in AB1100 to store the software stack, and 24Kbytes RAM is provided to support the MCU and baseband data processing.

Data are transferred between MCU, ROM, RAM and BPU with a shared memory bus. The UART interface is also connected to the memory bus for direct access. There is another peripheral bus that connects the peripherals with MCU.

8 Peripheral Control and Serial Communication Interfaces

There are 19 GPIOs for button control, 3 optical axis' detection IO ports, 2 LED drivers, one SPI interface, and one I2C interface connected to MCU with a peripheral bus. There is also a UART for firmware downloading and peripheral control.

The 19 GPIO ports and 3 axis detection IO ports can fully controlled by the MCU and thus can fulfill the HID MMI requirements in most applications.

The LED drivers integrate fader function and can drive red and blue LEDs for HID device indication purposes.

A SPI interface allows AB1100 to communicate with external HID device controller to exchange the MMI information such as button, axis control, etc. Both 3-wire and 4-wire mode SPI interfaces are supported in AB1100. When 3-wire mode is selected, pin 23 (SPI_MOSI) would be data I/O pin of the SPI interface. Only Master Mode is supported in AB1100.

The I2C interface is used to connect to a serial EEPROM, with 100KHz/400KHz/800KHz bus clock rate at 1.8/3.3V voltage level.

The UART interface supports up to 3M baud rate, and is directly connected to the memory interface.

9 Power Management / Regulation

AB1100 integrates a Power Management Unit (PMU), two internal switching regulators: one Bulk regulator from VBAT to 1.8V VCC, and one Boost regulator from VBAT to higher voltage (2.7~3.3V, selectable), and a 1.5V LDO regulator for VCO.

9.1 Power Regulation

A switching regulator is embedded to convert VBAT to 1.8V voltage supply for the core of AB1100. There is another Boost regulator to up convert the VBAT supply voltage to a higher level (2.7~3.3V, selectable) for the power supply of PMU, LED driver, and external sensor IC. All these regulators are integrated within AB1100.

9.2 Power Management Unit (PMU)

A PMU is designed in AB1100 for the power management affairs. During general operations, MCU may get into sleep mode for power saving. At this moment the PMU watches the keys and wake up MCU if one of the keys is pressed. PMU also monitors the battery voltage and report to MCU.

10 Software Stack

10.1 Key Features of HID Device Stack

The Airoha AB1100 HID software stack provides total solution of Bluetooth HID profile (device role), including all protocol stacks and profiles defined in HID v1.0. In addition, it has some extra features as shown below:

- Configurable MMI: Customers can modify user interface behavior by setting registers in EEPROM. In addition, AB1100 provides a set of function interface in ARIODA HID Customer Code Environment. Customers can re-write these functions to configure their own MMI.
- Support mainstream optical sensors by default, and can be chosen by EEPROM settings. Customers can re-write the MMI using ARIODA HID Customer Code Environment for other optical sensor.
- Good report rate for HID Mouse. (up to 125Hz)
- Supports up to 19 buttons and 3 optical axis' detection.
- Low-power operation based on various hardware-wakeup mechanisms.

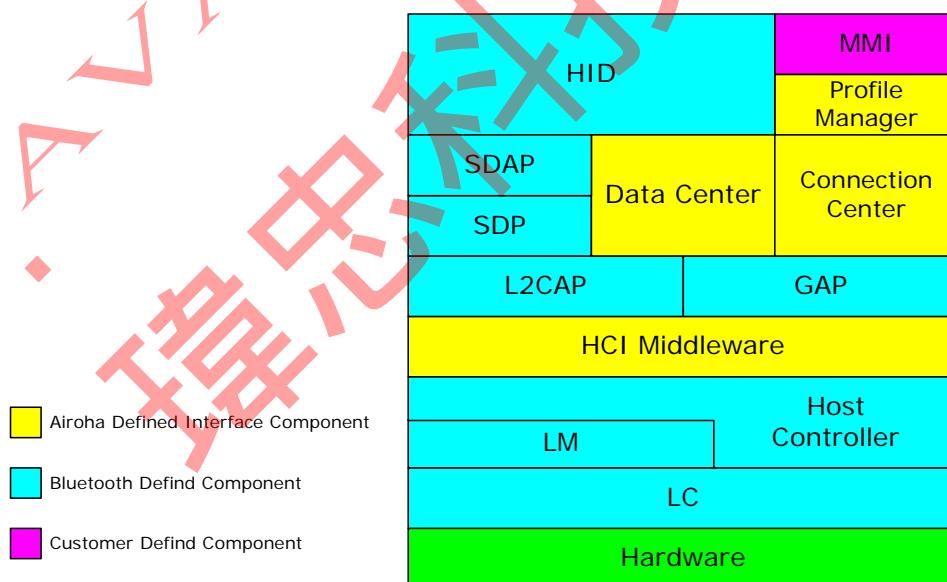


Figure 10.1: HID Software Stack

10.2 Development Environments and Tools

10.2.1 Software Development Environments

AB1100 provides a set of function interface in **ARIOHA HID Customer Code Environment**. Customers can rewrite these functions to control their hardware components, such as keypad, LED, SPI , optical sensor and etc..

10.2.2 Test and Configuration Tools

Various tools are provided for testing and configuration as shown below:

- AB1100 LabTest
 - AB1100 LabTest provides the capability for RF testing and can be used as HID module testing during mass-production.
- AB1100 HID Configuration tool
 - AB1100 HID Configuration tool provides to customers the capability to configure the various settings, such as Button I/O, LED behavior, Battery Parameters, and Sensor settings stored in EEPROM.

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

ITEM	MIN.	MAX.
I/O supply voltage (VCCIO)	-0.3V	5.5V
Boost supply voltage (VB_IN)	-0.3V	5.5V
Switching Regulator supply voltage (BAT_P)	-0.3V	5.5V
Operating temperature	-40°C	+85°C
Storage temperature	-65°C	+150°C
LNA input level	-	+10 dBm
PA output load mismatch	-	10:1

AB1100 could be damaged by any stress in excess of the absolute maximum ratings listed below.

Item	Min.	Typ.	Max.	Unit
Core supply voltage (VCCANA, VCCR _F , VCCD _I V, VREG_IN, VCCDIG, VCCXO)		1.8		V
I/O supply voltage (VCCIO)	1.8		3.6	V
Boost supply voltage (VB_IN)	1.6		3.3	V
Switching Regulator supply voltage (BAT_P)	2		4.2	V

11.2 Recommended Operating Conditions

11.3 Digital Terminals

Item	Min.	Typ.	Max.	Unit
Input Voltage Levels				
Input logic level low (V_{IL})	0		$0.3 \times VCCIO$	V
Input logic level high (V_{IH})	$0.7 \times VCCIO$		$VCCIO + 0.4$	V
Output Voltage Levels ($1.7V \leq VCCIO \leq 1.9V$)				
Output logic level low (V_{OL}), $I_o = 4.0mA$			0.4	V
Output logic level high (V_{OH}), $I_o = -4.0mA$	$VCCIO - 0.4$			V
Output Voltage Levels ($2.7V \leq VCCIO \leq 3.0V$)				
Output logic level low (V_{OL}), $I_o = 4.0mA$			0.2	V
Output logic level high (V_{OH}), $I_o = -4.0mA$	$VCCIO - 0.2$			V

11.4 Reference Clock

Item	Min.	Typ.	Max.	Unit
Crystal Requirement				
Nominal Frequency		26		MHz
Operating Temperature Range	-30	25	85	°C
Frequency Stability over Operating Temperature Range	-10		+10	ppm
Crystal Oscillator Characteristics				
Tunning Range (with 128 steps)		95		ppm
Negative resistance (@ $C_0 = 0.89\text{pF}$, $C_L = 10\text{pF}$)		140		Ω
External Reference Clock Requirement				
Input Frequency		26		MHz
Clock Input Level (AC-coupled, sinusoidal or square wave)	0.2		1.8	V pk-pk
XTAL_IN input impedance		10		KΩ
XTAL_IN input capacitance		10		pF

11.5 Switching Regulator

Buck Regulator

external inductor = 33uH, external capacitor = 4.7uF

Item	Min.	Typ.	Max.	Unit
Input Voltage	2		3.6	V
Output Voltage	BAT_P > 2.2V	1.7	1.8	V
Rated Output Current (Iout)	BAT_P > 3.6V		60	mA
Switching Frequency		1		MHz
Power Efficiency	@Iout max		80	%

Boost Regulator

external inductor = 4.7uH, external capacitor = 10uF

Item	Min.	Typ.	Max.	Unit
Input Voltage	1.6		3.6	V
Output Voltage at VB_OUT = 3V setting	2.7	3	3.3	V
Rated Output Current (Iout)	VB_IN = 2.4V, VB_OUT=3V		100	mA
Switching Frequency		566		KHz
Power Efficiency	@Iout max		80	%

11.6 Typical Current Consumption

Core Supply Voltage = 1.8V @ 25°C

Item	Min.	Typ.	Max.	Unit
Transmit (Peak Current)		53		mA
Receive (Peak Current)		48		mA
DM1(TX mode)		53		mA
DM1(RX mode)		48		mA
Sniff mode, 10ms		5.1		mA
Sniff mode, 100ms				mA
Sniff mode, 1.28s				mA
Deep sleep (disconnected, link loss state, wake on interrupt)		27		µA

The current consumption was measured directly on the bulk and boost output.

11.7 Radio Characteristics

Transmitter (Basic Data Rate)

Core Supply Voltage = 1.8V @ 25°C

Item	Min.	Typ.	Max.	Unit
Maximum RF transmit Power ^{*1}		1		dBm
RF power control range		20		dB
20dB bandwidth for modulated carrier		950		KHz
Adjacent channel transmit power	+2MHz	-21		dBm
	-2MHz	-34		dBm
	+3MHz	-47		dBm
	-3MHz	-43		dBm
Frequency deviation	Average deviation in payload	140		KHz
	Maximum deviation in payload	160		KHz
Initial carrier frequency tolerance		10		KHz
Drift	DH1 packet	15		KHz
	DH3 packet	15		KHz
	DH5 packet	15		KHz
Drift Rate		5		KHz/50us
2 nd Harmonic Content			-30	dBm
3 rd Harmonic Content			-30	dBm

*1 The maximum RF transmit power could reach to 6dBm with appropriate settings

Receiver (Basic Data Rate)

Core Supply Voltage = 1.8V @ 25°C

Item	Min.	Typ.	Max.	Unit
Sensitivity at 0.1% BER	2.402GHz	-88		dBm
	2.441GHz	-88		dBm
	2.480GHz	-88		dBm
Maximum input power at 0.1% BER	0			dBm
Co-Channel interference		7		dB
Adjacent channel selectivity C/I	$F = F_0 + 1\text{MHz}$	-5		dB
	$F = F_0 - 1\text{MHz}$	-5		dB
	$F = F_0 + 2\text{MHz}$	-35		dB
	$F = F_0 - 2\text{MHz}$	-28		dB
	$F = F_0 + 3\text{MHz}$	-43		dB
	$F = F_{\text{image}}$	-18		dB
Maximum level of intermodulation interference		-32		dBm
Blocking @Pin=-67dBm with 0.1%BER	30-2000 MHz	-3		dBm
	2000-2400 MHz	-10		dBm
	2500-3000 MHz	-10		dBm
	3000-12750 MHz	0		dBm

Transmitter (Enhanced Data Rate)

Core Supply Voltage = 1.8V @ 25°C

Item	Min.	Typ.	Max.	Unit
Relative transmit power		-3		dB
$\pi/4$ DQPSK max carrier frequency stability $ \omega_o $		1		KHz
$\pi/4$ DQPSK max carrier frequency stability $ \omega_i $		3		KHz
$\pi/4$ DQPSK max carrier frequency stability $ \omega_o + \omega_i $		4		KHz
8DPSK max carrier frequency stability $ \omega_o $		1		KHz
8DPSK max carrier frequency stability $ \omega_i $		3		KHz
8DPSK max carrier frequency stability $ \omega_o + \omega_i $		4		KHz
$\pi/4$ DQPSK Modulation Accuracy	RMS DEVM	7		%
	99% DEVM			%
	Peak DEVM	19		%
8DPSK Modulation Accuracy	RMS DEVM	7		%
	99% DEVM			%
	Peak DEVM	19		%
In-band spurious emissions	$F > F_0 + 3\text{MHz}$			dBm
	$F < F_0 - 3\text{MHz}$			dBm
	$F = F_0 + 3\text{MHz}$	-34		dBm
	$F = F_0 - 3\text{MHz}$	-40		dBm
	$F = F_0 + 2\text{MHz}$	-23		dBm
	$F = F_0 - 2\text{MHz}$	-33		dBm
	$F = F_0 + 1\text{MHz}$	-30		dBm
	$F = F_0 - 1\text{MHz}$	-30		dBm
EDR Differential Phase Encoding		0		%

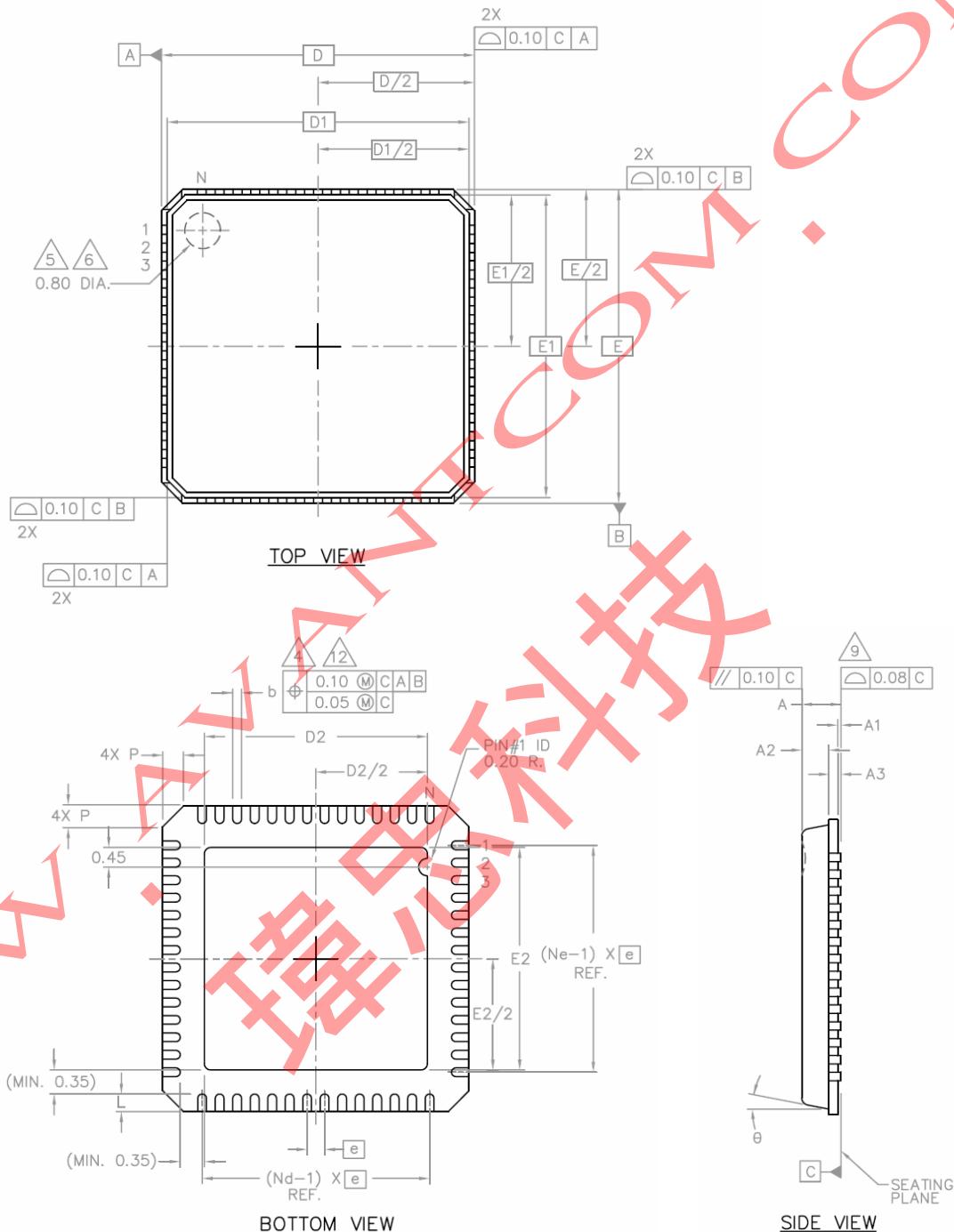
Receiver (Enhanced Data Rate)

Core Supply Voltage = 1.8V @ 25°C

Item		Min.	Typ.	Max.	Unit
Sensitivity at 0.01% EDR	$\pi/4$ DQPSK		-89		dBm
	8DPSK		-81		dBm
Maximum input power at 0.1% BER	$\pi/4$ DQPSK		0		dBm
	8DPSK		0		dBm
Co-Channel interference	$\pi/4$ DQPSK		10		dB
	8DPSK		17		dB
Adjacent channel selectivity C/I	$F = F_0 + 1\text{MHz}$	$\pi/4$ DQPSK		-11	dB
		8DPSK		-5	dB
	$F = F_0 - 1\text{MHz}$	$\pi/4$ DQPSK		-11	dB
		8DPSK		-5	dB
	$F = F_0 + 2\text{MHz}$	$\pi/4$ DQPSK		-34	dB
		8DPSK		-28	dB
	$F = F_0 - 2\text{MHz}$	$\pi/4$ DQPSK		-30	dB
		8DPSK		-23	dB
	$F = F_0 + 3\text{MHz}$	$\pi/4$ DQPSK		-41	dB
		8DPSK		-34	dB
	$F = F_{\text{image}}$	$\pi/4$ DQPSK		-15	dB
		8DPSK		-8	dB

12 Package Information

PUNCH QFN 56LD, 7x7x0.9 PKG 0.40 PITCH POD



SYMBOL	PITCH VARIATION			NOTE
	MIN.	NOM.	MAX.	
e	0.40 BSC			
N	56			3
Nd	14			3
Ne	14			3
L	0.30	0.40	0.50	
b	0.15	0.20	0.25	4
Q	—	—	—	
D2	4.75	4.90	5.05	
E2	4.75	4.90	5.05	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	—	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	—	0.65	0.70	
A3	0.20 REF.			
D	7.00 BSC			
D1	6.75 BSC			
E	7.00 BSC			
E1	6.75 BSC			
Θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	12

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED
BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE
PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.08mm.
10. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
11. APPLIED ONLY FOR TERMINALS.
12. Q AND R APPLIES ONLY FOR STRAIGHT TIEBAR SHAPES.
13. FOR 0.40 mm LEAD PITCH, THE LEAD POSITION TOLERANCE MUST BE 0.07mm
AT THE ACTUAL MEAN VALUE OF BODY SIZE.