DATASHEET

AB1112

Bluetooth 3.0 Single Chip with EDR Function
for Human Input Device Application

Preliminary Specification

VERSION 0.2 14-Mar-2013

Airoha Technology Corp.

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Revision History

Version	Change Summary	Date	Author
0.10	Created	Oct, 1st, 12	Max Lee
0.20	Add Pin information and performance data	Mar, 14th, 13	Max Lee

1 System Overview

1.1 General Description

AB1112 is an optimized single-chip solution which integrates baseband and radio for wireless human input device applications including game controller, wireless keyboard and remote control. It complies with Bluetooth system version 3.0 with the EDR function. AB1112 integrates the Li-ion battery charger circuit that provides 400mA charging current and reduces customer charging time.

1.2 Features

- Compliant with Bluetooth 3.0 specification
- Support EDR function
- HID profile version 1.1 compliant
- Device ID profile 1.3 compliant
- Support 3-axis detection
- Support hardware key-scan matrix
- Support SPI interface with 2/4-wire mode to mouse sensor IC
- Support I2C EEPROM interface
- Support UART interface for firmware downloading and peripheral control
- Embedded 4 LED drivers with fader
- Low cost ROM based design with customer code support
- Embedded power management unit
- Integrated 1.8V Buck and 1.8/2.7V LDO regulator
- Integrated Li-ion battery charger
- Single RF port for transmitter and receiver
- Receiver sensitivity of -89dBm at basic data rate
- Transmit power up to +4dBm with 25 dB gain tuning range
- QFN 7mm x 7mm 56 pin package

1.3 Applications

The typical application of AB1112 is wireless keyboard. The application block diagrams is illustrated as below

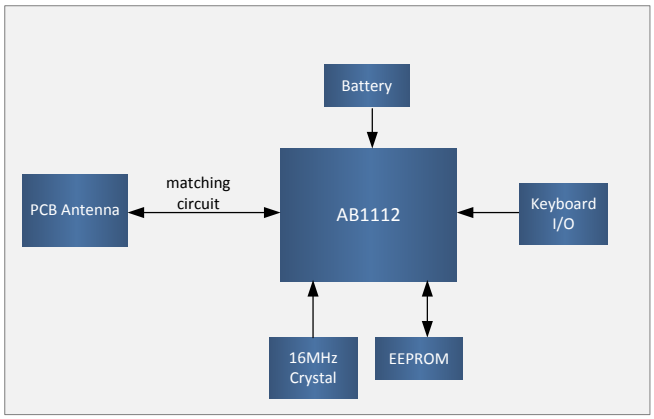


Figure 1-1 Wireless Keyboard Application Block Diagram

1.4 Block Diagram

AB1112 comprises three major parts, a 2.4G RF transceiver, a power manager unit, and a MCU platform. The heart of the MCU platform is an 8051 microcontroller with 288 Kbytes ROM for programs and 24 Kbytes SRAM for run-time data. Rich peripherals, such as UART, SPI and I2C, are supported. The power management unit integrates a high efficient DC-DC convert (BUCK) and a 400mA Charger.

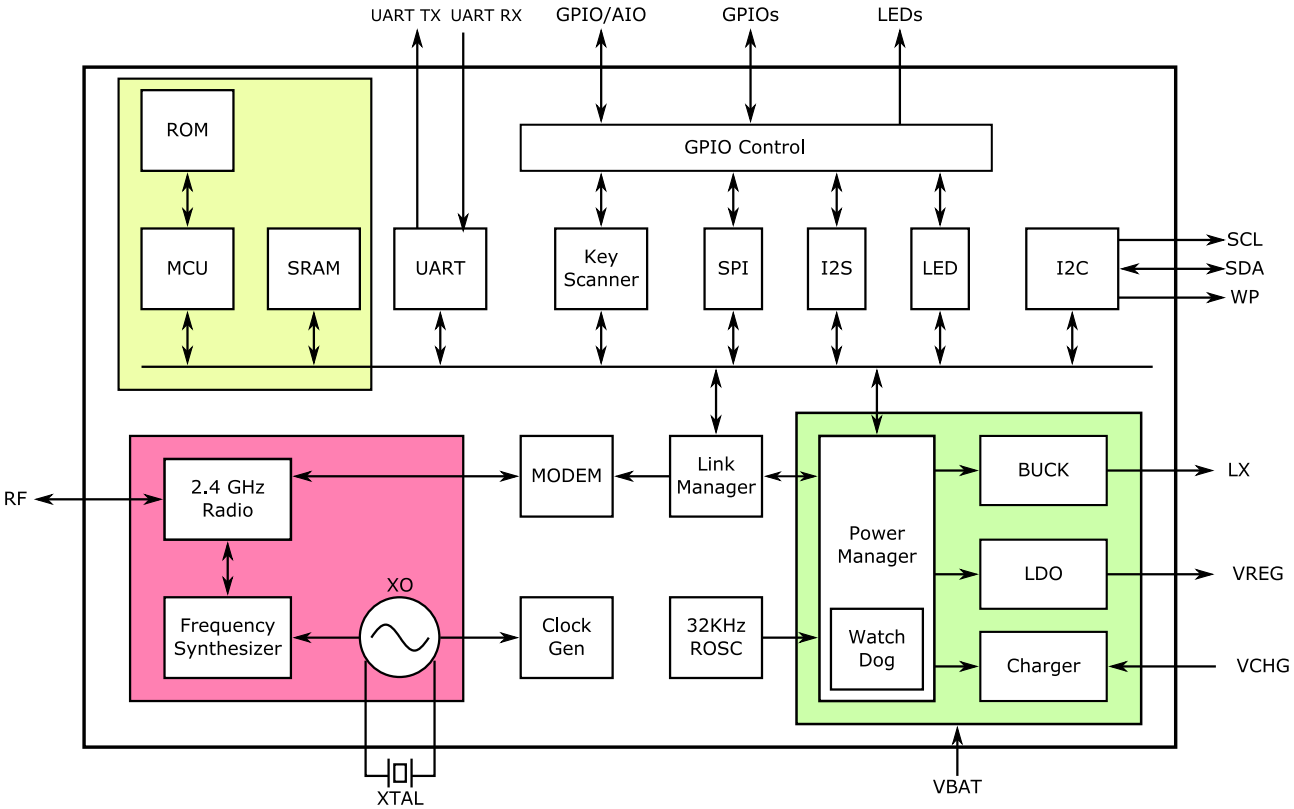


Figure 1-2 AB1112 Functional Block Diagram

2 Product Description

2.1 Pin Definition

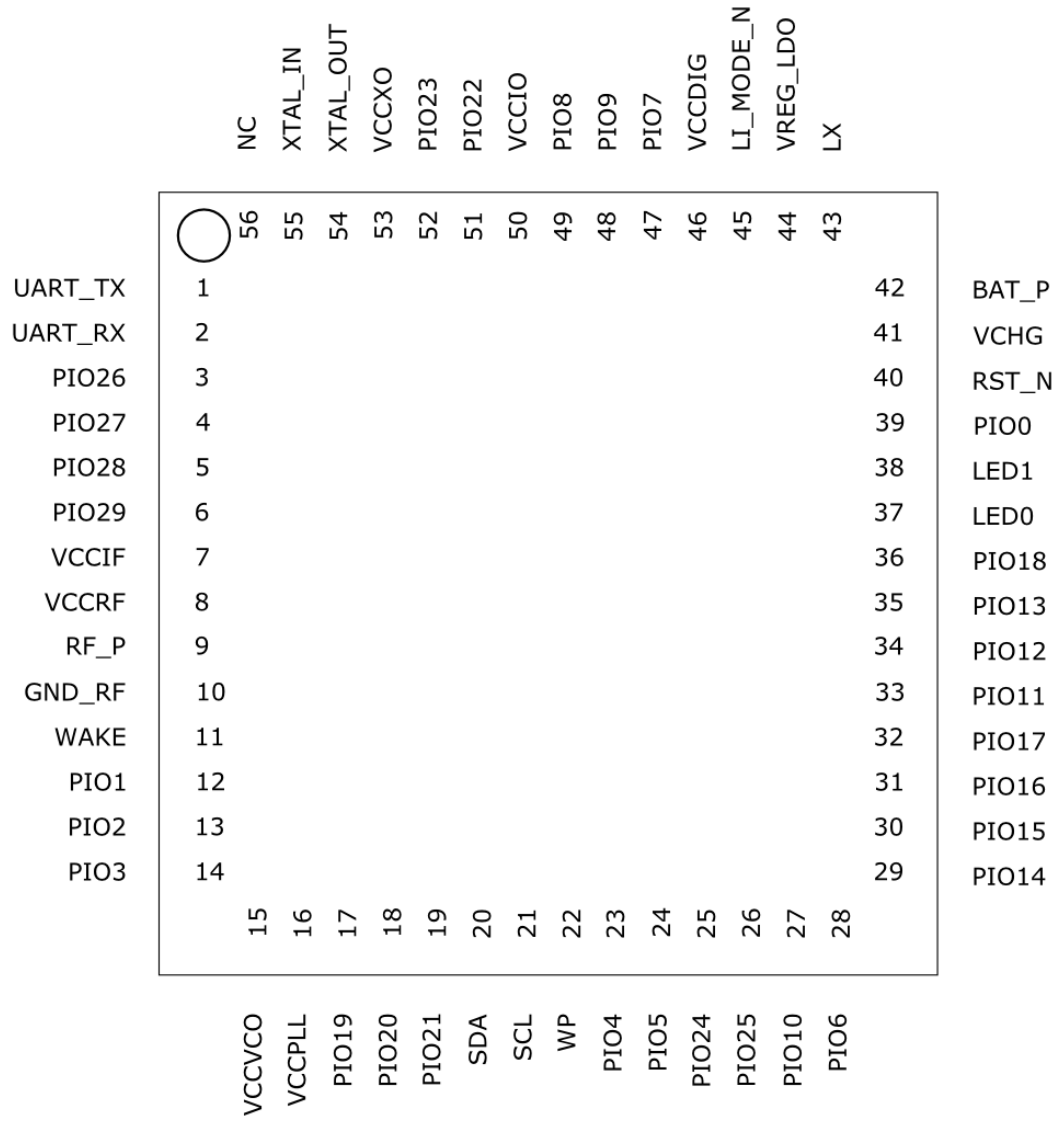


Figure 2-1 Pin Definition

2.2 Pin Description

PIN	SIGANL	TYPE	DESCRIPTION	ALTERNATIVE
1	UART_TX	Output, Digital	UART TX	
2	UART RX	Input, Digital	UART RX	
3	PIO26	Input/Output, Digital	Programmable IO	
4	PIO27	Input/Output, Digital	Programmable IO	
5	PIO28	Input/Output, Digital	Programmable IO	
6	PIO29	Input/Output, Digital	Programmable IO	
7	VCCIF	Supply, 1.8V	VCC for IF	
8	VCCRF	Supply, 1.8V	VCC for TX/RX front-end	
9	RF_P	Input/Output, single RF	RF input/output P	
10	GNDRF	Ground	Ground for RF	
11	WAKE	Input, Digital	Input Pin with 80K pull up	
12	PIO1	Input, Digital	Input Pin with 13k pull up	
13	PIO2	Input, Digital	Input Pin with 13k pull up	
14	PIO3	Input, Digital	Input Pin with 13k pull up	
15	VCCVCO	Supply, 1.8V	VCC for VCO	
16	VCCPLL	Supply, 1.8V	VCC for PLL	
17	PIO19	Input/Output, Digital	Programmable IO	
18	PIO20	Input/Output, Digital	Programmable IO	
19	PIO21	Input/Output, Digital	Programmable IO	
20	SDA	Input/Output, Digital	I2C data line	
21	SCL	Input/Output, Digital	I2C clock line	
22	WP	Output, Digital	Write Protect Control for EEPROM	
23	PIO4	Input/Output, Digital	Programmable IO	Uart_CTS, Z-axis_Z1, LED3
24	PIO5	Input/Output, Digital	Programmable IO	Uart_RTS, Z-asix_Z2, LED4

25	PIO24	Input/Output, Digital	Programmable IO	
26	PIO25	Input/Output, Digital	Programmable IO	
27	PIO10	Input/Output, Digital	Programmable IO	
28	PIO6	Input/Output, Digital	Programmable IO	
29	PIO14	Input/Output, Digital	Programmable IO	SPI_CSN, X-axis_X1, I2S_CLK
30	PIO15	Input/Output, Digital	Programmable IO	SPI_MOSI, X-axis_X2, I2S_DATA
31	PIO16	Input/Output, Digital	Programmable IO	SPI_MISO, Y-axis_Y1, I2S_WS
32	PIO17	Input/Output, Digital	Programmable IO	SPI_CLK, Y-axis_Y2,
33	PIO11	Input/Output, Digital	Programmable IO	
34	PIO12	Input/Output, Digital	Programmable IO	
35	PIO13	Input/Output, Digital	Programmable IO	
36	PIO18	Input/Output, Digital	Programmable IO	
37	LED0	Open Drain	LED 0 for Red Light	
38	LED1	Open Drain	LED 1 for Blue Light	
39	PIO0	Input/Output, Digital AIO,Analog	Programmable IO	AIO0
40	RST_N	Input, Digital	Global reset	
41	VCHG	Supply, 5V	VCC for PMU/Charger	
42	BAT_P	Supply	Battery input P, as Switching/Linear regulator input	
43	LX	Analog	Switching Regulator output	
44	VREG_LDO	Analog	Ldo output	
45	LI_MODE_N	Input, Digital	Charger function	
46	VCCDIG	Supply, 1.8V	VCC for Digital circuits	
47	PIO7	Input/Output, Digital	Programmable IO	
48	PIO9	Input/Output, Digital	Programmable IO	
49	PIO8	Input/Output, Digital AIO,Analog	Programmable IO	AIO1

50	VCCIO	Supply, 1.8V~3.3V	VCC for IO	
51	PIO22	Input/Output, Digital	Programmable IO	
52	PIO23	Input/Output, Digital	Programmable IO	
53	VCCXO	Supply, 1.8V	VCC for XO	
54	XTAL_OUT	Analog	Crystal output	
55	XTAL_IN	Analog	Crystal input	
56	NC			

Table 2-1 Pin Description

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

ITEM	MIN.	MAX.	UNIT
I/O supply voltage (VCCIO)	-0.3	5.5	V
Switching Regulator supply voltage (BAT_P)	-0.3	5.5	V
Charger supply voltage (VCHG)	-0.3	6.5	V
Operating temperature	-40	+85	°C
Storage temperature	-65	+150	°C
LNA input level	-	+10	dBm
PA output load mismatch	-	10:1	

Table 3-1 Absolute Maximum Ratings

AB1112 could be damaged by any stress in excess of the absolute maximum ratings listed above

3.2 Recommended Operating Conditions

Item	Min.	Typ.	Max.	Unit
Core supply voltage (VCCIF, VCCRF, VCCVCO, VCCPLL, VCCDIG, VCCXO)		1.8		V
I/O supply voltage (VCCIO)	1.8		3.6	V
Switching Regulator supply voltage (BAT_P)	2		4.2	V
Charger supply voltage (VCHG)	4.5	5	6.5	V

Table 3-2 Recommended Operating Conditions

3.3 Digital Terminals

Item	Min.	Typ.	Max.	Unit
Input Voltage Levels				
Input logic level low (V_{IL})	0		0.3*VCCIO	V

Input logic level high (V_{IH})	0.7*VCCIO		VCCIO+0.4	V
Output Voltage Levels (VCCIO=1.8V)				
Output logic level low (V_{OL}), I_O=4.0mA *			TBD	V
Output logic level high (V_{OH}), I_O=-4.0mA **	TBD			V
Output Voltage Levels (VCCIO=3.3V)				
Output logic level low (V_{OL}), I_O=4.0mA *			0.4	V
Output logic level high (V_{OH}), I_O=-4.0mA **	VCCIO-0.4			V

Table 3-3 Digital Terminals

3.4 Reference Clock

Item	Min.	Typ.	Max.	Unit
Crystal Requirement				
Nominal Frequency		16		MHz
Operating Temperature Range	-30	25	85	℃
Frequency Stability over Operating Temperature Range	-10		+10	ppm
Crystal Oscillator Characteristics				
Tuning Range		±30		ppm
Negative resistance		-150		Ω

Table 3-4 Reference Clock

3.5 Switching Regulator

External inductor = 10uH, External capacitor = 10uF

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		2		4.4	V
Output Voltage	BAT_P > 2.2V	1.7	1.8	1.9	V
Rated Output Current (Iout)			100		mA
Switching Frequency			1.3		MHz
Power Efficiency	@Iout=40mA		90		%

Table 3-5 Switching Regulator

3.6 High-Voltage LDO

External capacitor = 10uF

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		2.7		4.4	V
Output Voltage		2.5		3.2	V
Rated Output Current (Iout)			100		mA

Table 3-6 High-Voltage LDO

3.7 Battery Charger

Item	Min.	Typ.	Max.	Unit
Input Voltage	4.5	5	6.5	V
Charge Current (CC Mode)	25		400	mA
Trickle Charge Current		8		mA
Trickle to CC Charge Threshold Voltage		3		V
Recharge Battery Hysteresis Voltage		200		mV

Table 3-7 Battery Charger

3.8 Typical Current Consumption

Core Supply Voltage = 1.8V (buck output) @ 25℃ unless other specified.

Item	Condition	Min.	Typ.	Max.	Unit
Transmit	Peak Current		TBD		mA
Receive	Peak Current		TBD		mA
Sniff mode	10 ms		TBD		mA
	100 ms		TBD		mA
	1.28 s		TBD		mA
Deep sleep (disconnected, link loss state, wake on interrupt)	buck off, wake on by all GPIOs		2		uA

Table 3-8 Typical Current Consumption

The transmit and the receive current consumptions were measured directly on the buck output (1.8V at 25°C), while the sniff mode and deep sleep current was measured at battery output

3.9 Radio Characteristics

3.9.1 Transmitter

Basic Data Rate

Core Supply Voltage = 1.8V @ 25℃

Item		Min.	Typ.	Max.	Unit
Maximum RF transmit Power*1			4		dBm
Maximum RF transmit Power (Low power)			0		dBm
RF power control range			25		dB
20dB bandwidth for modulated carrier				1000	KHz
Adjacent channel transmit power	+2MHz			-20	dBm
	-2MHz			-20	dBm
	+3MHz			-40	dBm
	-3MHz			-40	dBm
Frequency deviation	Average deviation in payload	115			KHz
	Maximum deviation in payload	140		175	KHz
Initial carrier frequency tolerance		-75		75	KHz
Drift	DH1 packet	-25		25	KHz
	DH3 packet	-40		40	KHz
	DH5 packet	-40		40	KHz
Drift Rate		-20		20	KHz/50us
Harmonic Content			-45		dBm

Table 3-9 Transceiver Basic Data Rate

*1 The maximum RF transmit power could reach 4dBm with appropriate settings

Enhanced Data Rate

Core Supply Voltage = 1.8V @ 25℃

Item	Min.	Typ.	Max.	Unit
Relative transmit power		-1.5		dB
π/4 DQPSK max carrier frequency stability $\|\omega_o\|$	-10		10	KHz
π/4 DQPSK max carrier frequency stability $\|\omega_i\|$	-75		75	KHz
π/4 DQPSK max carrier frequency stability $\|\omega_o+\omega_i\|$	-75		75	KHz
8DPSK max carrier frequency stability $\|\omega_o\|$	-10		10	KHz

8DPSK max carrier frequency stability $\|\omega_i\|$		-75		75	KHz
8DPSK max carrier frequency stability $\|\omega_o+\omega_i\|$		-75		75	KHz
π/4 DQPSK Modulation Accuracy	RMS DEVM			20	%
	99% DEVM	99			%
	Peak DEVM			35	%
8DPSK Modulation Accuracy	RMS DEVM			13	%
	99% DEVM	99			%
	Peak DEVM			25	%
In-band spurious emissions	F > F0 + 3MHz			-40	dBm
	F < F0 - 3MHz			-40	dBm
	F = F0 + 3MHz			-40	dBm
	F = F0 - 3MHz			-40	dBm
	F = F0 + 2MHz			-20	dBm
	F = F0 - 2MHz			-20	dBm
	F = F0 + 1MHz			-26	dBm
	F = F0 - 1MHz			-26	dBm
EDR Differential Phase Encoding		99			%

Table 3-10 Transceiver Enhanced Data Rate

3.9.2 Receiver

Basic Data Rate

Core Supply Voltage = 1.8V @ 25℃

Item		Min.	Typ.	Max.	Unit
Sensitivity at 0.1% BER	2.402GHz		-89		dBm
	2.441GHz		-89		dBm
	2.480GHz		-89		dBm
Sensitivity at 0.1% BER (Low Power)	2.402GHz		-84		dBm
	2.441GHz		-84		dBm
	2.480GHz		-84		dBm
Maximum input power at 0.1% BER		-20			dBm
Co-Channel interference				11	dB
Adjacent channel selectivity	$F = F_0+5MHz$			-40	dB
C/I	$F = F_0+4MHz$			-40	dB

	F = F_0+3MHz			-40	dB
	F = F_0+2MHz			-30	dB
	F = F_0+1MHz			0	dB
	F = F_0			11	dB
Adjacent channel selectivity C/I	F = F_0-1MHz			0	dB
	F = F_0-2MHz			-20	dB
	F = F_0-3MHz (F_{image})			-9	dB
	F = F_0-4MHz			-20	dB
	F = F_0-5MHz			-40	dB
Maximum level of intermodulation interference				-39	dBm
Blocking@Pin=-67dBm with 0.1%BER	30-2000 MHz			-10	dBm
	2000-2400 MHz			-27	dBm
	2500-3000 MHz			-27	dBm
	3000-12750 MHZ			-10	dBm

Table 3-11 Receiver Basic Rate

Enhanced Data Rate

Core Supply Voltage = 1.8V @ 25℃

Item			Min.	Typ.	Max.	Unit
Sensitivity at 0.01% EDR	π/4 DQPSK			-90		dBm
	8DPSK			-81		dBm
Sensitivity at 0.01% EDR (Low power)	π/4 DQPSK			-86		dBm
	8DPSK			-77		dBm
Maximum input power at 0.1% BER	π/4 DQPSK		-20			dBm
	8DPSK		-20			dBm
Co-Channel interference	π/4 DQPSK				13	dB
	8DPSK				21	dB
Adjacent channel selectivity C/I	F = F_0+1MHz	π/4 DQPSK			0	dB
		8DPSK			5	dB
	F = F_0-1MHz	π/4 DQPSK			0	dB
		8DPSK			5	dB
	F = F_0+2MHz	π/4 DQPSK			-30	dB
		8DPSK			-25	dB
	F = F_0-2MHz	π/4 DQPSK			-20	dB

		8DPSK			-13	dB
	F = F_0+3MHz	π/4 DQPSK			-40	dB
		8DPSK			-33	dB
	F = F_{image}	π/4 DQPSK			-7	dB
		8DPSK			0	dB

Table 3-12 Receiver Enhanced Data Rate

4 Function Description

4.1 Radio Transceiver

The AB1112 RF transceiver is a 2.4GHz-band transceiver for the Bluetooth HID applications. There are three main functions – transmitter, receiver, and synthesizer. The enable control signals of these functions are given by the Baseband Processing Unit.

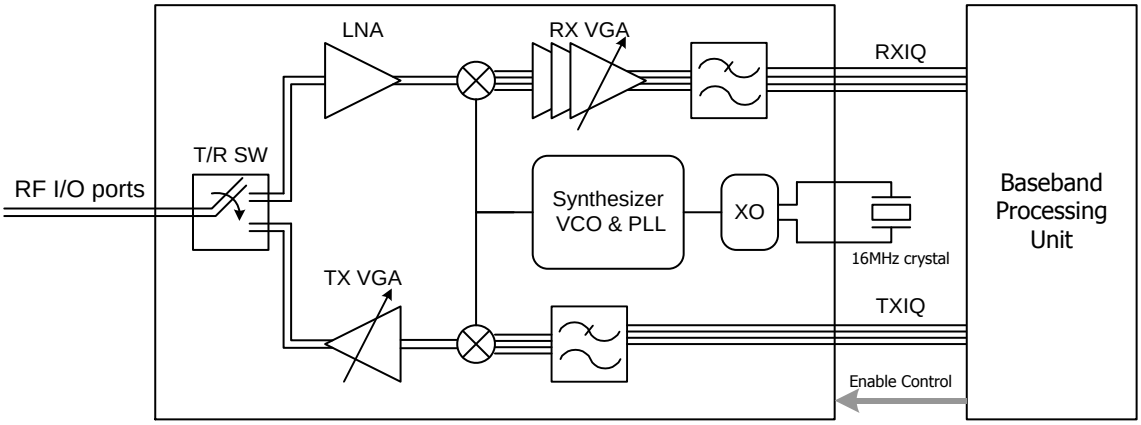


Figure 4-1 AB1112 Transceiver Block Diagram

4.1.1 RF Front End

The RX input ports and TX output ports share the same RF terminals such that no external T/R switch is required. Only a few matching components are placed outside the RF terminals

4.1.2 Receiver

The AB1112 RF receiver is composed of two parts: RF front-end and IF part. The RF front-end part comprises a LNA and a quadrature mixer. The IF part comprises a low-pass filter (LPF) for out-band filtering and a variable gain amplifier (VGA).

The LNA input shares the same RF ports with TX output. The RX front-end gain could be adjusted, and thus reduce the probability of bit errors caused by poor signal-to-noise ratio. The LNA is followed by a quadrature

mixer that down-converts the RF signal to IF band.

At the IF part, the down-converted signal is first low-pass filtered by the LPF, amplified by the VGA, and then forwarded to the ADC for demodulation. The 3dB bandwidth of the LPF could be adjusted through RF registers. The LNA and VGA provide more than 80dB gain control range

4.1.3 Transmitter

The AB1112 RF transmitter comprises a LPF, a modulator and a VGA stage. The TX baseband signals are fed from baseband DAC, generated by the baseband modulators. A LPF is implemented to attenuate the second side lobe of signal spectrum and unwanted oversampling clock or spurious signals. The 3dB bandwidth of the LPF could be adjusted through RF registers. The VGA provides variable gain with more than 25dB dynamic range, and could be controlled through the RF register interface.

4.1.4 Synthesizer

The AB1112 implements a fractional-N synthesizer with embedded VCO and loop filter without the need of external components. AB1112 also integrates an internal crystal oscillator, and only a 16MHz crystal is required externally.

4.2 Baseband Procession Unit

The Baseband Processing Unit (BPU) comprises a Digital-to-Analog Convert (DAC), an Analog-to-Digital Converter (ADC), a digital modulator, a digital demodulator, a Bluetooth Frame Data Processor, and a Timing Processing Unit (TPU).

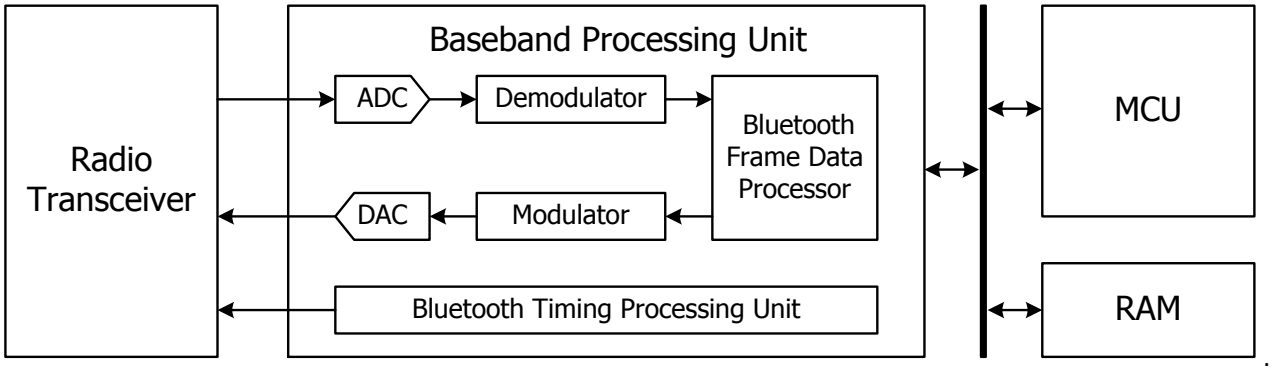


Figure 4-2 AB1112 Baseband Block Diagram

4.2.1 Bluetooth Frame Data Processor

AB1112 baseband processing unit supports all packet types of Bluetooth 1Mbps, 2Mbps and 3Mbps modes. On the transmitter side, the frame data processor can construct Bluetooth data packet according to the packet type given by MCU. The constructed data packet then will be converted to analog modulated signal format by the modulator and DAC.

On the receiver side, the received analog signal will be first converted to digitized data format by the ADC and demodulator, and then the frame data processor will de-construct the received data to several parts and identify if the received signal is a valid Bluetooth packet and if the packet is for the device itself. Only if it is, the received header data and PSDU data will be stored into memory.

Access code check, Header Error Check (HEC) and PSDU CRC checking functions are performed by the frame data processor to see whether or not this received signal is valid and error free. A data whitening circuit and an encryption engine are also included in the frame data processor for both transmitter and receiver paths

4.2.2 Modulator and Demodulator

The modulator can generate GFSK, DQPSK and D8PSK signals according to which data rate is adopted in the frame data. The demodulator can convert the received data signal to digitized data bit format according to the modulation type indicated in the header region

4.2.3 Bluetooth Timing Processing Unit

A Bluetooth Timing Processing Unit (TPU) is embedded in the Baseband processing unit. TPU is in charge of generating RF timing control signals to the RF radio part, such as TX enabling signals and RX enabling signals

4.3 MCU and Memory

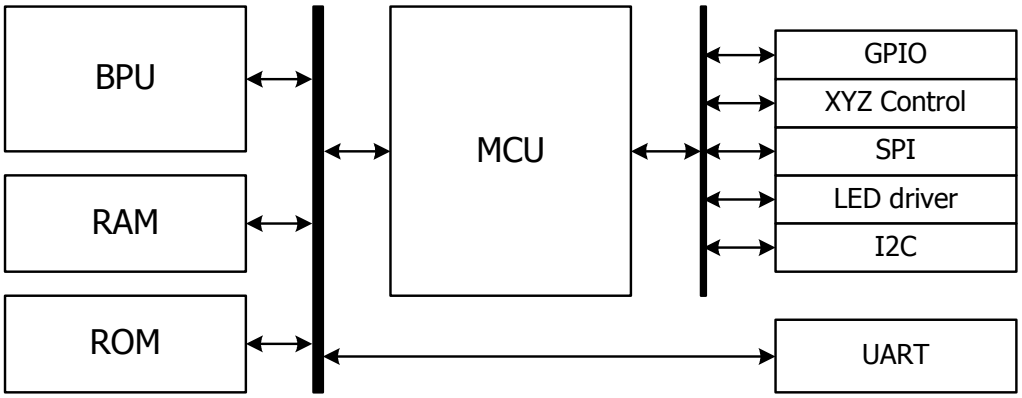


Figure 4-3 AB1112 MCU and Memory

The micro-control unit (MCU) executes the Bluetooth protocol software stack, controls the Bluetooth baseband processing unit (BPU) and Serial Communication Interfaces. 288Kbytes ROM is embedded in AB1112 to store the software stack, and 24Kbytes RAM is provided to support the MCU and baseband data processing.

Data are transferred between MCU, ROM, RAM and BPU with a shared memory bus. The UART interface is also connected to the memory bus for direct access. There is another peripheral bus that connects the peripherals with MCU

4.4 Power Management

AB1112 integrates a Power Management Unit (PMU), one internal switching regulator from VBAT to 1.8V VCC, and one regulator from VBAT to 2.5V~3.2V (selectable) and a Li-ion battery charger.

4.4.1 Buck Regulator

The Buck regulator is embedded to convert VBAT to 1.8V voltage to supply AB1112. When Buck out voltage is 1.8V, it will supply AB1112 core directly. The below block shows the buck circuit with LC component

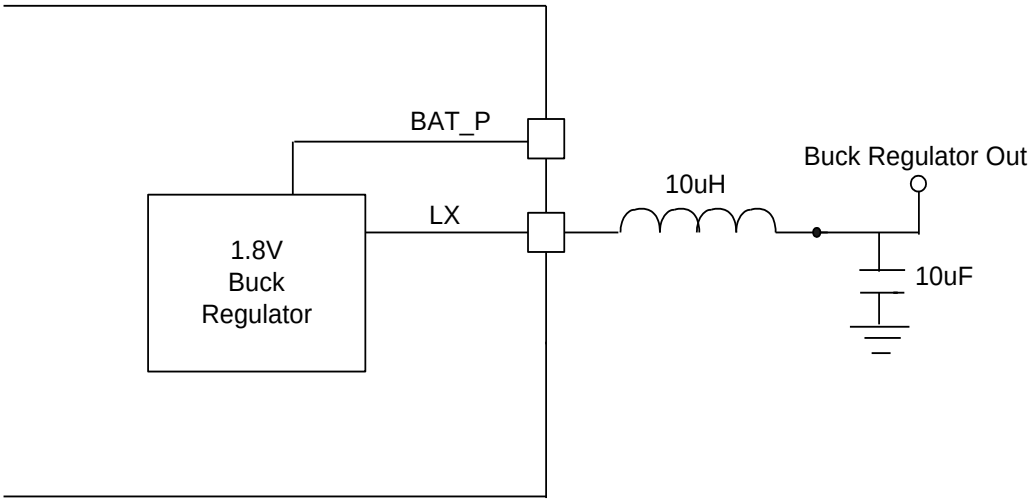


Figure 4-4 Buck Regulator Circuit

4.4.2 LDO Regulator

The LDO Regulator is embedded to convert VBAT to 3V voltage to supply AB1112.The LDO Regulator voltage programming range is 2.5V~3.2V. In some applications, the peripheral may be supplied by the Regulator voltage.

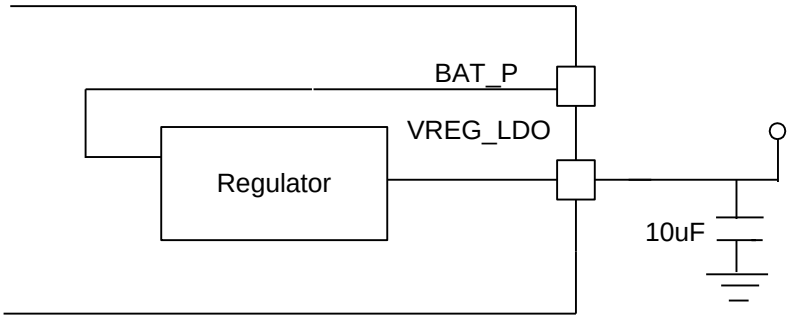


Figure 4-5 LDO Regulator Circuit

4.4.3 Power Management

The PMU is designed in AB1112 for the power management tasks. The PMU controls the Buck and LDO Regulator power in sequence. During general operations, MCU may enter the sleep mode for power saving. During power saving, the PMU monitors the keys and wakes up the MCU if one of the keys is pressed. PMU also monitors the battery voltage and reports to MCU. When the battery charger power supply is connected to the device, PMU will monitor if the voltage is high enough and enable the battery charger circuit to charge the

Li-ion battery.

4.4.4 Li-ion Battery Charger

The Li-mode battery charger of AB1112 supports five modes:

- Trickle mode
- Constant current mode (CC mode)
- Constant voltage mode (CV mode)
- Standby mode
- Error mode

The below block diagram shows the charge circuit. When an external power supply is connected to AB1112 VCHG pin, PMU will first detect if the VCHG voltage is correct and enable the charger circuit.

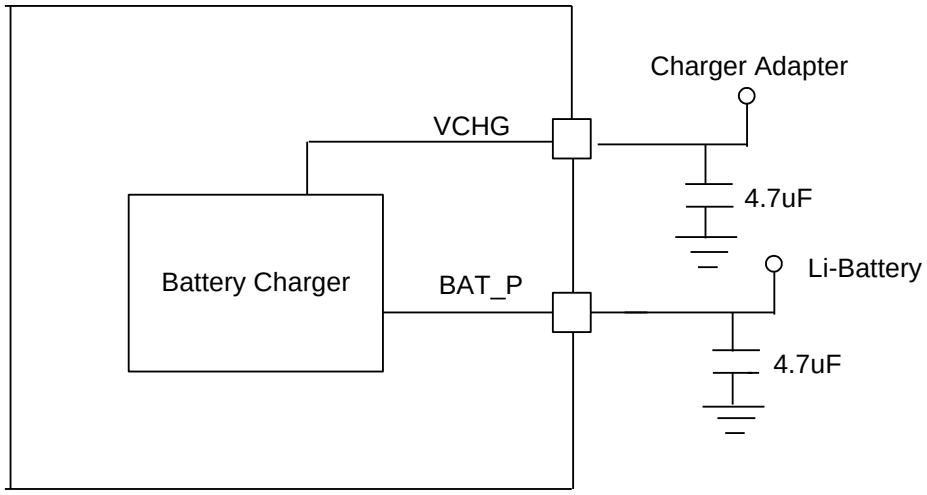


Figure 4-6 Battery Charger Circuit

When the charger circuit is enabled, it will detect the battery voltage and enters the associated mode to charge the battery, i.e. Trickle, CC or CV mode. When the battery voltage reaches a high threshold, the charger will enter the standby mode and keep monitoring the battery voltage. If the battery voltage drops to a low threshold, the charger circuit will re-charge the battery again. The Charge profile is shown as below.

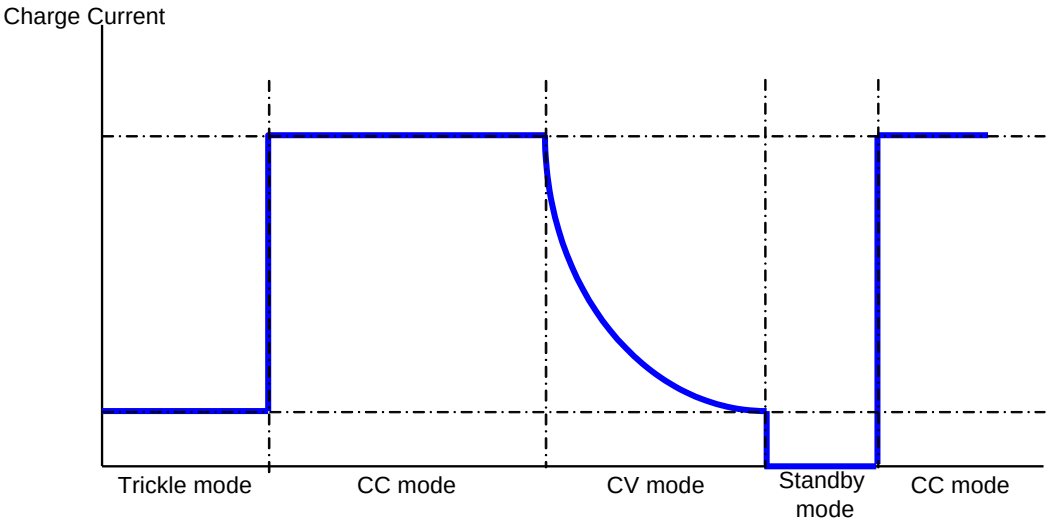


Figure 4-7 Charging Profile

If the MCU cannot read EEPROM setting about the Charge, the charge circuit will enter the Error mode without any charge current to protect the Battery.

5 Software Stack

5.1 Key Features of HID Device Stack

The Airoha AB1112 HID software stack provides total solution of Bluetooth HID profile (device role), including all protocol stacks and profiles defined in HID v1.1. In addition, it has some extra features as shown below:

- Configurable MMI: Customers can modify user interface behavior by setting registers in EEPROM. In additional, AB1112 provides a set of function interfaces in the ARIOHA Customer Code Environment. Customers can re-write these functions to configure their own MMI.
- Support mainstream optical/laser sensors by default, and can be chosen by EEPROM settings. Customers can re-write the MMI using the ARIOHA Customer Code Environment for other sensors.
- Low-power operation based on various hardware-wakeup mechanisms.

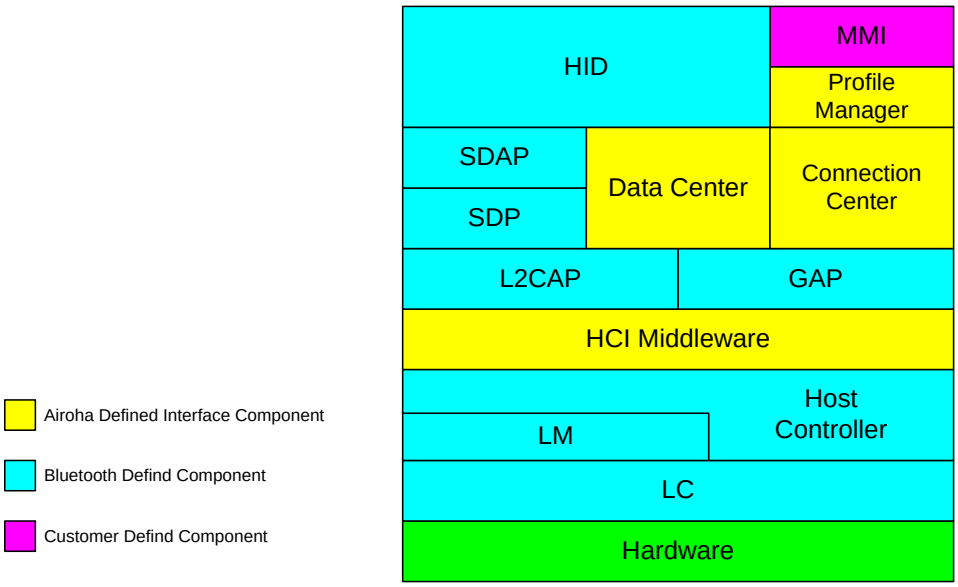


Figure 5-1 AB1112 Software Stack

5.2 Development Environment and Tool

5.2.1 Software Development Environment

AB1112 provides a set of function interfaces in the ARIOHA Customer Code Environment. Customers can rewrite these functions to control their hardware components, such as keypad, LED, SPI, and optical sensor.

5.2.2 Test and Configuration Tools

Various tools are provided for testing and configuration as shown below:

- AB1112 LabTest
  - AB1112 LabTest provides the capability for RF testing and can be used for the HID module testing during mass-production.
- AB1112 Configuration tool
  - AB1112 Configuration tool provides customers with the capability to configure various MMI settings, such as Button I/O, LED behavior, and Battery Parameters stored in EEPROM.

6 Interface Description

The total number of I/O pins of AB1112 is 30, including 3 pins dedicated for input only. Other 27 I/O pins are programmable and support both input and output.

There are also 3 axis' detection IO ports, 4 LED drivers, 1 SPI interface and 1 I2C interface connected to MCU with a peripheral bus. There is also a UART interface for firmware downloading and peripheral control, and one I2S interface could be used to connect to external voice codec for voice input function.

The LED drivers integrate fader function and can drive red and blue LEDs for HID device indication purposes. The I2C interface is used to connect to EEPROM and other peripheral devices such as touch-pad, with 100KHz/400KHz/800KHz bus clock rate at 1.8/3.3V voltage level

6.1 Serial Peripheral Interface

The SPI interface allows AB1112 to communicate with an external HID device controller to exchange the MMI information such as button, etc. Both 3-wire and 4-wire mode SPI interfaces are supported in AB1112. When 3-wire mode is selected, SPI_MOSI is the data I/O pin of the SPI interface. Both the master and the slave modes are supported in AB1112. The SPI interface is shared with GPIOs and there are two groups of GPIOs that can be used as the SPI interface.

6.1.1 SPI Master

The GPIO mapping table for master mode SPI is listed below.

	Four-wire Mode		Three-wire Mode	
PIO14	O	NCS	O	NCS
PIO15	O	MOSI	N/A	
PIO16	I	MISO	I/O	DATA_IO
PIO17	O	SCK	O	SCK

Table 6-1 SPI Master GPIO Mapping Table

The SPI Interface provides the flexibility to fit most SPI slave devices. The polarity and phase of SCK can both be programmed, thus results in four combinations. The NCS to SCK delay, the SCK to NCS delay, and SCK period are also programmed. The timing relationship of the SPI Interface is illustrated below.

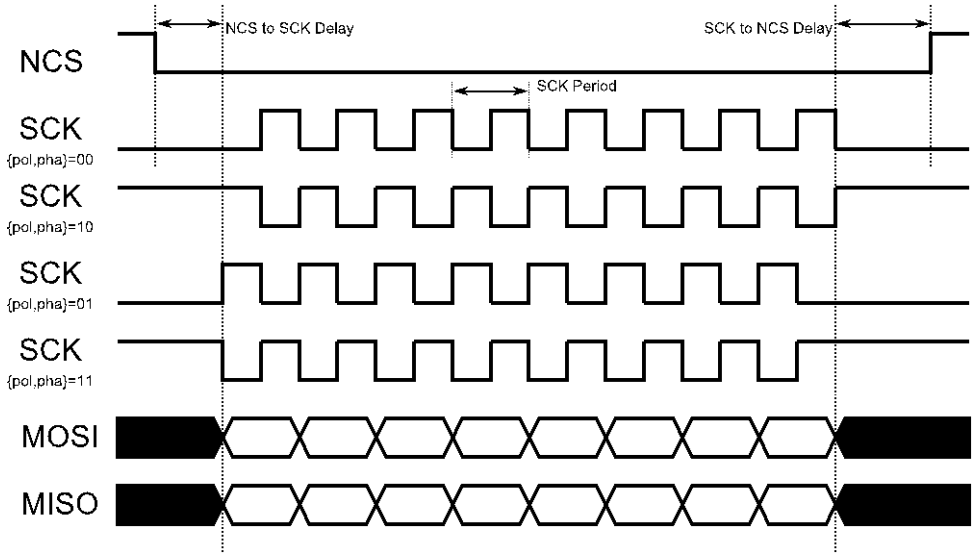


Figure 6-1 SPI Master Timing Diagram

The SPI Interface also supports multiple bytes in a single transfer. Between each byte, a Hold Delay can be set. This is drawn as below

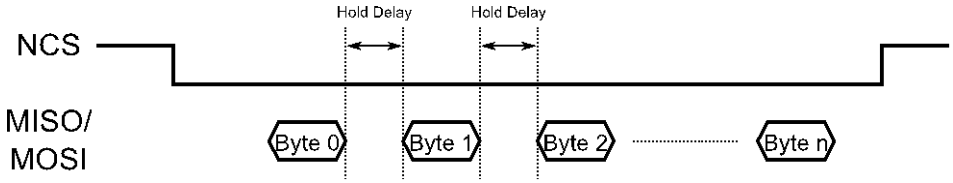


Figure 6-2 SPI Master Multiple Bytes Transfer

6.1.2 SPI Slave

The GPIO mapping table for slave mode SPI is listed below.

	Four-wire Mode		Three-wire Mode	
PIO14	I	NCS	I	NCS
PIO15	I	MOSI	N/A	
PIO16	O	MISO	I/O	DATA_IO
PIO17	I	SCK	I	SCK

Table 6-2 SPI Slave GPIO Mapping Table

The timing diagram for the SPI Slave interface is illustrated below.

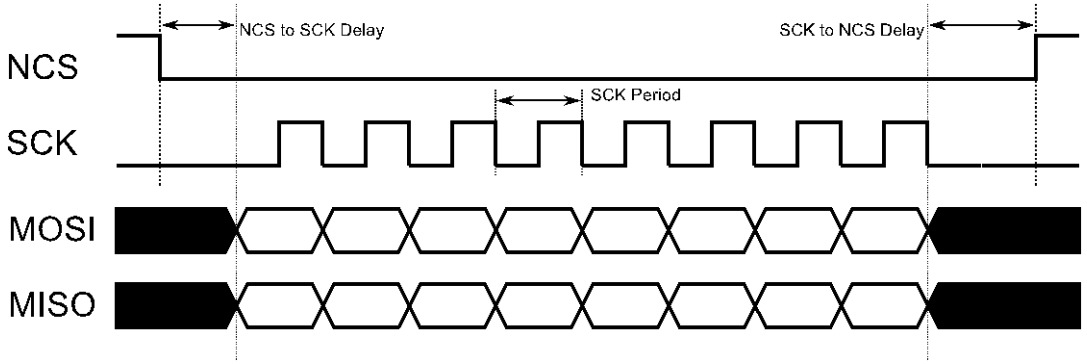


Figure 6-3 SPI Slave Timing Diagram

The SPI slave also supports multiple bytes in a single transfer and up to 32 bytes are allowed.

6.2 UART

AB1112 utilizes a Universal Asynchronous Receiver Transmitter (UART). It supports flexible configurations as listed below. There are local FIFOs and DMA that can achieve high throughput serial communications.

Configuration Parameters	Supported Values
Data Length	8 bits
Flow control	Hardware RTS/CTS None
Parity	Even Odd None
Number of stop bits	1 or 2
Baud rate	1200 2400 4800 9600 19200 38400 57600 76800 1152000 230400 460800

	921600 1843200

Table 6-3 UART Configuration Parameters

6.3 I2C

The I2C in AB1112 is a master interface. It supports 100, 400 and 800 KHz clock rates. For controlling EEPROM, a dedicated write protect (WP) signal is also supported. The I2C interface provides several data formats and can fit various I2C peripherals. Sequential read and write are supported to improve throughputs.

8-bit Register Addressing Mode: Write

Figure 6-4 I2C Write Sequences for 8-bit Register Addressing Mode

8-bit Register Addressing Mode: Read

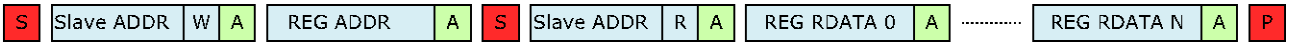


Figure 6-5 I2C Read Sequences for 8-bit Register Addressing Mode

8-bit Register Addressing Mode: Read with Current Address

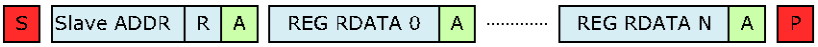


Figure 6-6 I2C Read Sequences with Current Address for 8-bit Register Addressing Mode

16-bit Register Addressing Mode: Write

Figure 6-7 I2C Write Sequences for 16-bit Register Addressing Mode

16-bit Register Addressing Mode: Read

Figure 6-8 I2C Read Sequences for 16-bit Register Addressing Mode

6.4 I2S Slave

The I2S is a simple serial interface for sending stereo audio bit streams. AB1112 supports three data align modes. Timing diagrams for each mode are drawn below.

- Right Justified Mode

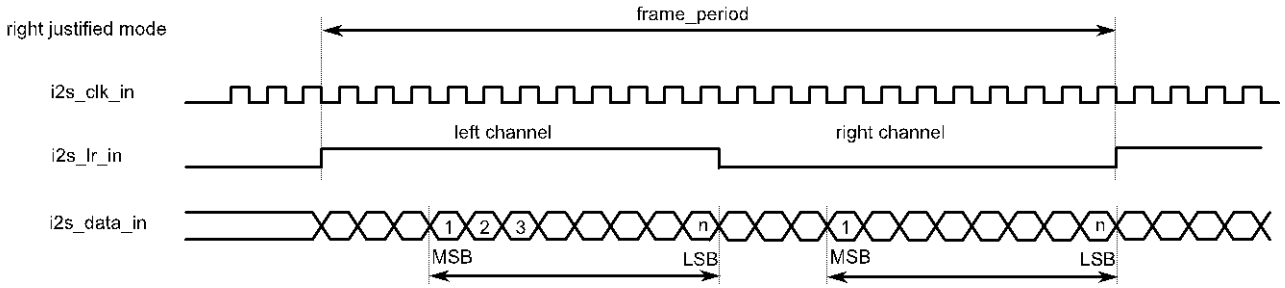


Figure 6-9 Right Justified Mode Timing Diagram

- I2S Justified Mode

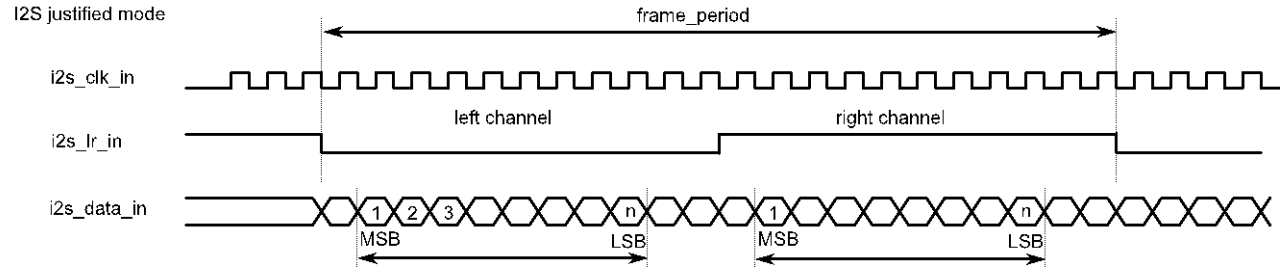


Figure 6-10 I2S Justified Mode Timing Diagram

- Left Justified Mode

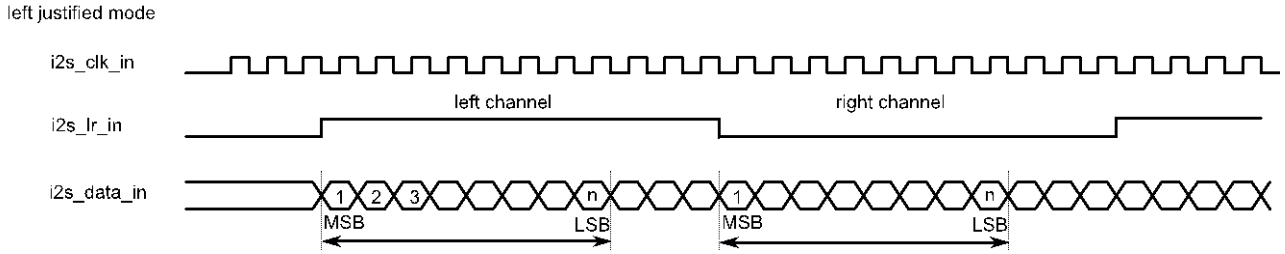


Figure 6-11 Left Justified Mode Timing Diagram

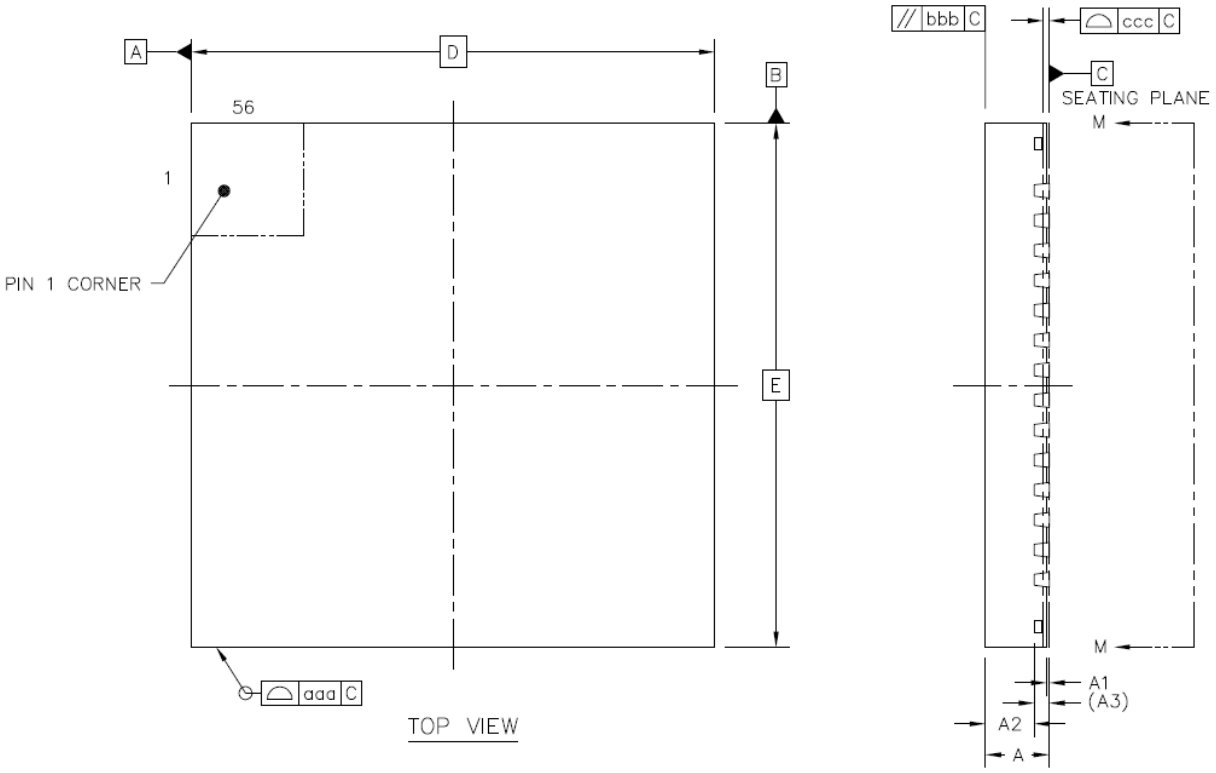
6.5 Key Scanner

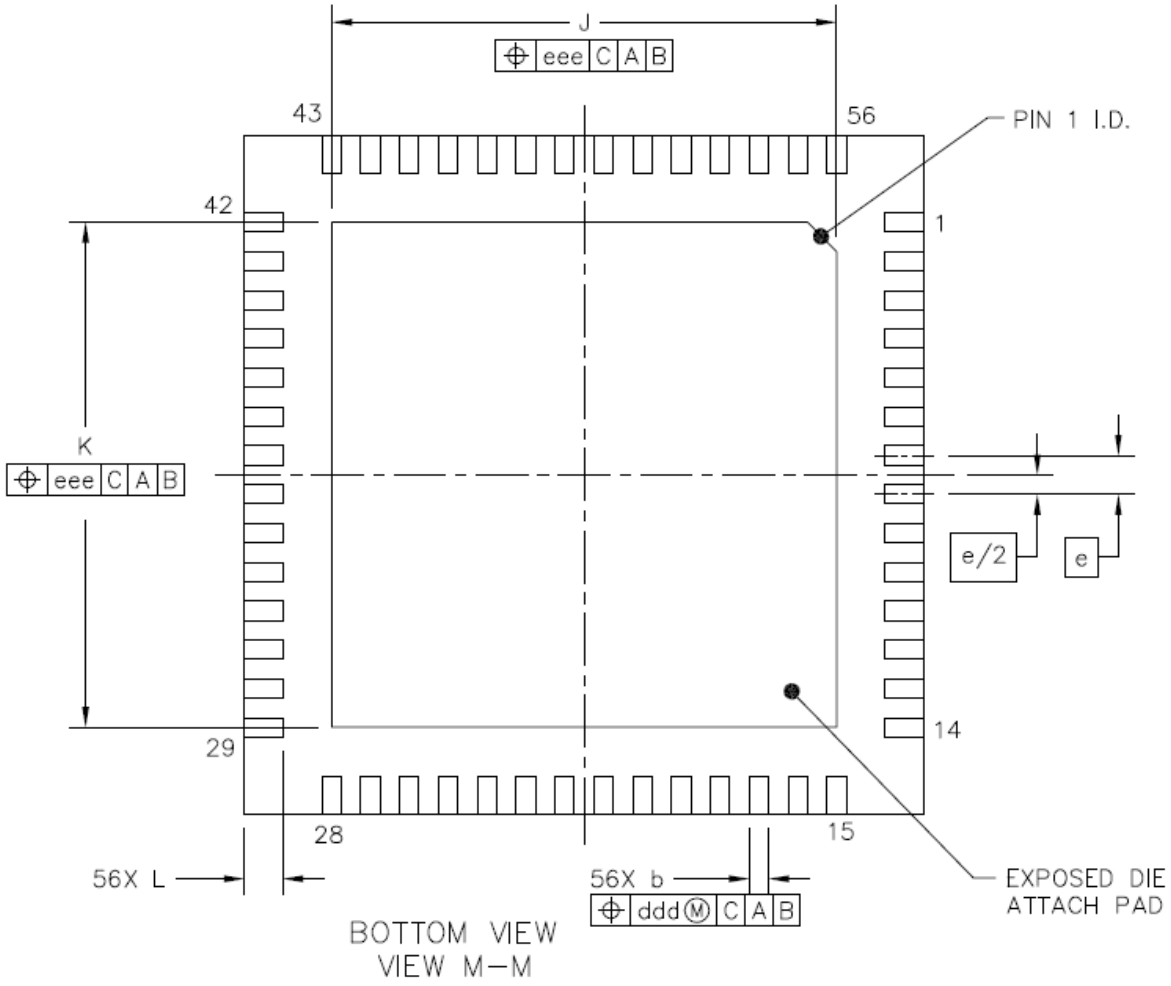
The Key Scanner is designed to optimize the power consumptions for keyboard applications. It scans key events autonomously and stores them in the key buffers. The microcontroller only needs to wait the data in the key buffers and can go to sleep without key events.

The key matrix size, both columns and rows, is programmed. The maximum supported matrix size is 8x18. There are also hardware debouncing and ghost key detection

7 Package Information

7.1 Package Information




J
eee C A B
43
56
PIN 1 I.D.
42
1
K
eee C A B
e/2
e
29
14
28
15
56X L
56X b
ddd M C A B
EXPOSED DIE
ATTACH PAD
BOTTOM VIEW
VIEW M–M

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	5.1	5.2	5.3
	Y	K	5.1	5.2	5.3
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 7-1 Package Dimension