DATASHEET

AB1526

Stereo Headset Solution

For Intensive Audio Applications

Preliminary Specification

VERSION 0.15 1-Apr-2016

Airoha Technology Corp.

Airoha Technology Corp.

TABLE OF CONTENTS

List of Figures

List of Tables

Revision History

Version	Change Summary	Date	Author
0.10	Created	Feb, 26th, 15	Max Lee
0.11	Update Fig. 1-4 Update Table 3-1, 3-2, and 3-8	July, 31st, 15	Max Lee
0.12	Update Table 3-14, 3-15, 3-16, and 4-2 Update Section 1.1, 1.2, and 4.2.3 Add Table 4-3, 4-4, and 4-5 Add Fig. 4-6 and 4-12	Nov, 25th, 15	Max Lee
0.13	Update Table 3-18 Update Section 3.5.2 and 4.3.2	Dec, 9th, 15	Max Lee
0.14	Update Table 2-1, 3-5, 3-6, 3-7, and 3-8 Update Section 4.4.2	Mar, 7th, 16	Max Lee
0.15	Update Table 3-9 Update Section 3.7, 4.4, and 4.4.2	Apr, 1st, 16	Max Lee

Airoha Technology Corp.

1 System Overview

1.1 General Description

AB1526 is an advanced single-chip solution which integrates baseband and radio for intensive audio applications. It is Bluetooth 4.2 dual mode certified and supports wide band speech which is defined at HFP1.6, AAC decoder, and 2-Mic for better noise reduction and echo cancellation performance. AB1526 embeds serial flash which is more flexible for customer SW upgrading and 3rd party SW porting is supported. With optimized MCU structure, interface arrangement and better DSP algorithm, AB1526 provides higher performance and crystal voice and music quality in most of the Bluetooth audio application like Headset and Headphone. With very small BGA package type and only a few outside components, AB1526 can fit the ultra-small type headset application. AB1526 supports “AiroStereo” which two speakers can connect to each other, play left channel in one speaker and play right channel in another speaker as a wireless stereo system. AiroStereo can let end users have great stereo experience without wire connection. AB1526 also supports “ AiroShare” which can relay the music from one audio device to another device wirelessly that users can easily share the music from the same audio source.

1.2 Features

- BT 4.2 dual mode including low energy profiles
- Support EDR function
- A2DP profile version 1.3 compliant
- HFP profile version 1.6 compliant
- HSP profile version 1.2 compliant
- AVRCP profile version 1.5 compliant
- SPP profile version 1.2 compliant
- Multipoint for HFP and A2DP
- Embedded 96MIPS dual-MAC DSP coprocessor
- 2-Mic Noise reduction and Echo cancellation
- Programmable EQ
- Support Packet loss concealment
- Support Wide band speech, wide band voice prompt and customized voice prompt

- Support Voice command
- Support AAC_LC decoder
- Support AiroStereo. AiroShare.
- Support iOS and Android APP
- Support over the air update
- Build in Battery service, proximity profiles
- Integrated Li-ion battery charger supports 250mA fast charging and over-discharging protection

1.3 Applications

- Stereo headsets
- Stereo headphones

The main application of AB1526 is stereo headset. The application block diagram is illustrated as below

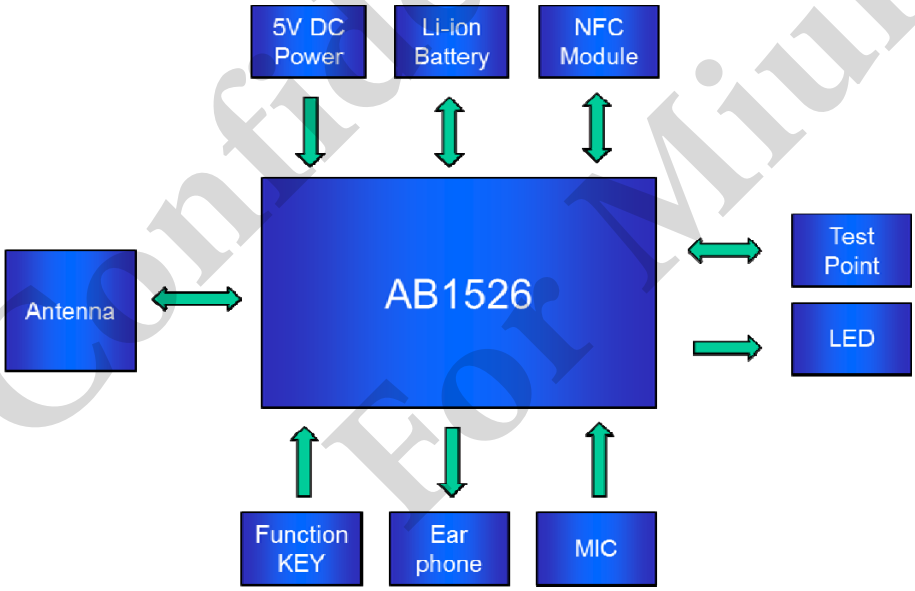


Figure 1-1 Application Block Diagram

The application of AiroStereo is illustrated as below:

Figure 1-2 AiroStereo Application Block Diagram

The application of AiroShare is illustrated as below:

Figure 1-3 AiroShare Headset Application Block Diagram

1.4 Block Diagram

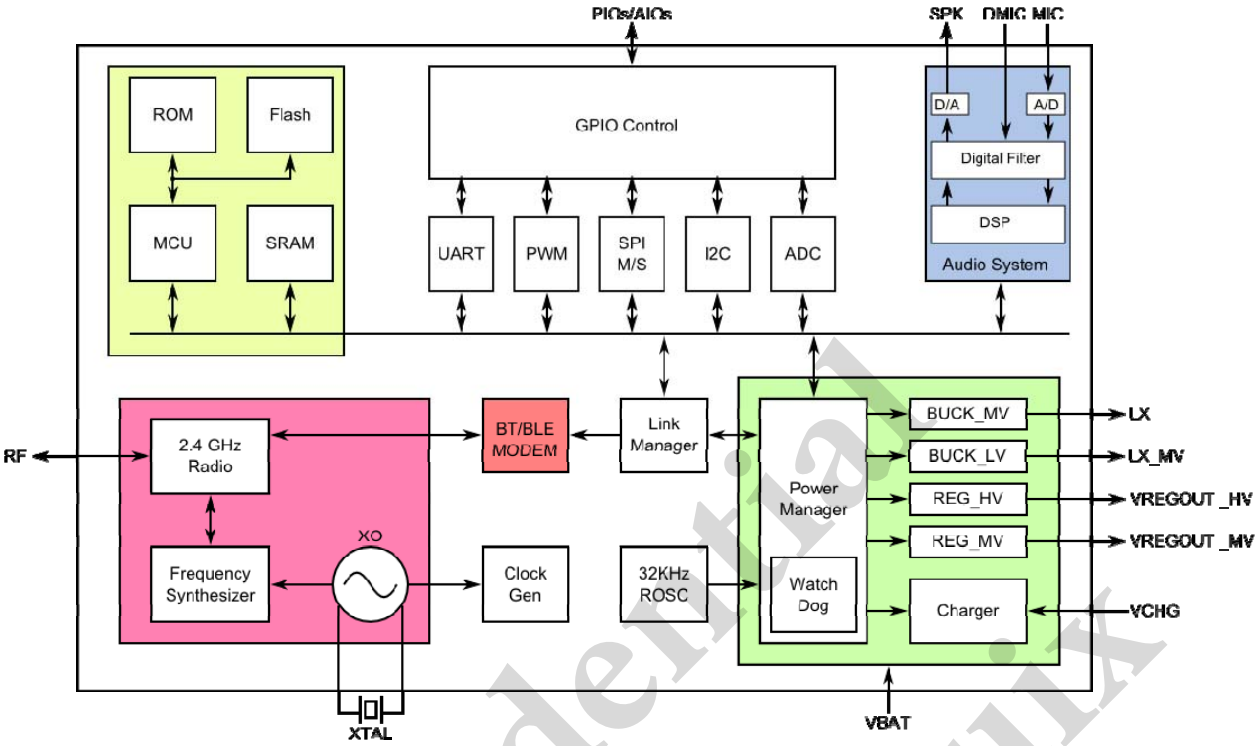


Figure 1-4 Functional Block Diagram

2 Product Description

2.1 Pin Definition

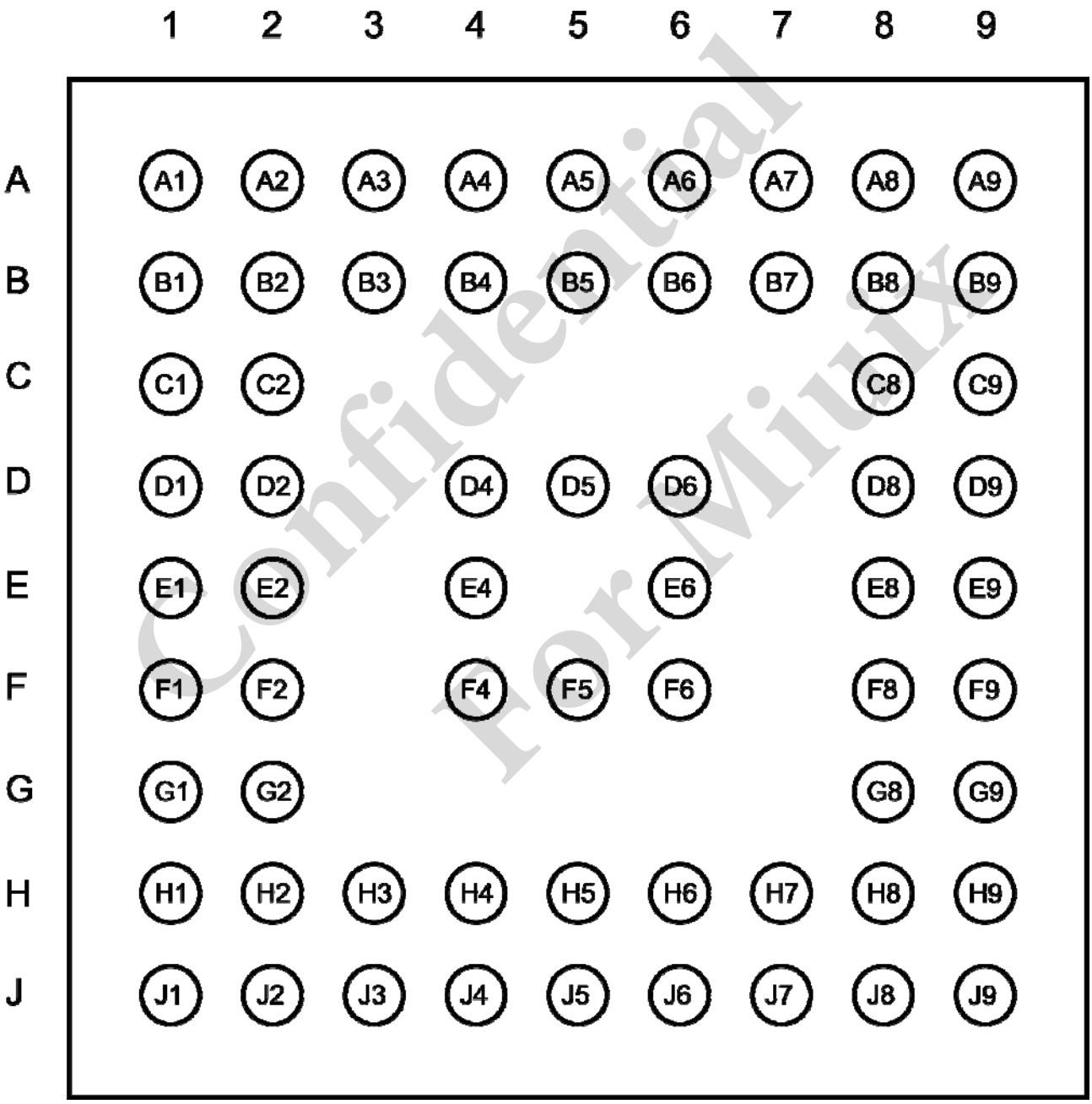


Figure 2-1 Pin Definition

2.2 Pin Description

Audio/Crystal	Ball	Pad Type	Supply Domain	Description	Alternative
XTAL_IN	A1	Analog	VCCXO	Crystal input	
XTAL_OUT	A2	Analog	VCCXO	Crystal output	
AU_REF	B1	Analog	REGHV	Audio reference	
SPK_RN	C1	Analog	VCCSPK	Speaker output RN	
SPK_RP	D1	Analog	VCCSPK	Speaker output RP	
SPK_LP	C2	Analog	VCCSPK	Speaker output LP	
SPK_LN	D2	Analog	VCCSPK	Speaker output LN	
MIC_BIAS	A5	Analog	REGHV	Microphone bias	
MIC1_P	A4	Analog	VCCXO	Microphone 1 P-path	
MIC1_N	B5	Analog	VCCXO	Microphone 1 N-path	
MIC2_P	B4	Analog	VCCXO	Microphone 2 P-path	
MIC2_N	A3	Analog	VCCXO	Microphone 2 N-path	
Radio	Ball	Pad Type	Supply Domain	Description	Alternative
RF_P	F1	RF	VCCRF	RF input/output P	
PIO	Ball	Pad Type	Supply Domain	Description	Alternative
GPIO1	H3	Input only, Digital	VCCIO	Input Pin with 750K pull up	
GPIO2	H1	Input only, Digital	VCCIO	Input Pin with 750K pull up	
GPIO3	J4	Input/Output, Digital	VCCIO	Programmable IO	
GPIO4	E9	Input/Output, Digital	VCCIO	Programmable IO	SPI_NCS / AIO
GPIO5	E8	Input/Output, Digital	VCCIO	Programmable IO	SPI_MOSI / AIO
GPIO6	J6	Input/Output, Digital	VCCIO	Programmable IO	SPI_MISO / AIO
GPIO7	H6	Input/Output, Digital	VCCIO	Programmable IO	SPI_SCK / AIO
GPIO11	H5	Input/Output,	VCCIO	Programmable IO	

		Digital			
GPIO14	J7	Input/Output, Digital	VCCIO	Programmable IO	SPI_NCS
GPIO15	H7	Input/Output, Digital	VCCIO	Programmable IO	SPI_MOSI
GPIO16	J8	Input/Output, Digital	VCCIO	Programmable IO	SPI_MISO
GPIO17	H8	Input/Output, Digital	VCCIO	Programmable IO	SPI_SCK
GPIO24	G9	Input/Output, Digital	VCCIO	Programmable IO	AIO
UART_RX	H4	Input only, Digital	VCCIO	UART RX	
UART_TX	J5	Output only, Digital	VCCIO	UART TX	
SDA	J9	Input/Output, Open Drain	VCCIO	I2C data line	
SCL	H9	Input/Output, Open Drain	VCCIO	I2C clock line	
LED0	F9	Output only, Open Drain	VCCIO	LED driver 0	
LED1	F8	Output only, Open Drain	VCCIO	LED driver 1	
LED2	G8	Output only, Open Drain	VCCIO	LED driver 2	
Power supply	Ball	Pad Type	Description		Alternative
REGEN	F2	Input, Digital	Regulator enable, Input Pin with 100K pull low		
REGMV	A7	Analog	LDO output		
REGHV	B6	Analog	LDO output		
LX_LV	A9	Analog	Switching Regulator output		
LX_MV	A6	Analog	Switching Regulator output		
RST	D8	Input, Digital	Global reset, active high		
VCHG	D9	Supply, 5V	Power for Charger		
BAT_P	C9	Supply	Charger output for battery/ Switching/Linear		

			regulator input	
VCCRF/IF	E2	Supply, 1.25V	VCC for TX/RX front-end	
VCCVCO	J1	Supply, 1.25V	VCC for VCO	
VCCPLL	J3	Supply, 1.25V	VCC for PLL	
VCCIO	B7	Supply, 1.8V~3.3V	VCC for GPIO	
VCCDIG	B9	Supply, 1.25V	VCC for Digital	
VCCXO	B3	Supply, 1.25V	VCC for XO and mic_amp	
VCCSPK	B2	Supply, 3V	VCC for Audio Speaker	
RFGND	G1	Ground	Ground for RF	
GND	A8	Ground	Substrate ground	
GND	B8	Ground	Substrate ground	
GND	C8	Ground	Substrate ground	
GND	D4	Ground	Substrate ground	
GND	D5	Ground	Substrate ground	
GND	D6	Ground	Substrate ground	
GND	E1	Ground	Substrate ground	
GND	E4	Ground	Substrate ground	
GND	E6	Ground	Substrate ground	
GND	F4	Ground	Substrate ground	
GND	F5	Ground	Substrate ground	
GND	F6	Ground	Substrate ground	
GND	G2	Ground	Substrate ground	
GND	H2	Ground	Substrate ground	
GND	J2	Ground	Substrate ground	

Table 2-1 Pin Description

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

AB1526 could be damaged by any stress in excess of the absolute maximum ratings listed below.

ITEM	MIN.	MAX.	UNIT
I/O supply voltage (VCCIO)	-0.3	3.6	V
charger output (BAT_P)	-0.3	4.4	V
Charger supply voltage (VCHG)	-0.3	6.5	V
Operating temperature	-40	+85	°C
Storage temperature	-65	+150	°C

Table 3-1 Absolute Maximum Rating

3.2 Recommended Operating Conditions

Item	Min.	Typ.	Max.	Unit
Core supply voltage (VCCIF, VCCRF, VCCVCO,VCCPLL VCCDIG, VCCXO)		1.25		V
I/O supply voltage (VCCIO)	1.7		3.6	V
charger output (BAT_P)	2.7		4.2	V
Audio Speaker voltage(VCCSPK)	1.8	3	3.3	V
Charger supply voltage (VCHG)	4.5	5	6.5	V

Table 3-2 Recommended Operating Conditions

3.3 Digital Terminals

Item	Min.	Typ.	Max.	Unit
INPUT VOLTAGE LEVELS				
Input logic level low (V_{IL})	0		0.3*VCCIO	V
Input logic level high (V_{IH})	0.7*VCCIO		VCCIO+0.4	V
OUTPUT VOLTAGE LEVELS (1.7V≦VCCIO≦1.9V)				

Output logic level low (V_{OL}), I_O=4.0mA			0.2	V
Output logic level high (V_{OH}), I_O=-4.0mA	VCCIO-0.2			V
OUTPUT VOLTAGE LEVELS (2.7V≦VCCIO≦3.0V)				
Output logic level low (V_{OL}), I_O=4.0mA			0.4	V
Output logic level high (V_{OH}), I_O=-4.0mA	VCCIO-0.4			V

Table 3-3 Digital Terminals

3.4 Reference Clock

Item	Min.	Typ.	Max.	Unit
CRYSTAL REQUIREMENT				
Nominal Frequency		16		MHz
Operating Temperature Range	-40	25	85	℃
Frequency Stability over Operating Temperature Range				ppm
CRYSTAL OSCILLATOR CHARACTERISTICS				
Negative resistance (@ C0 = 0.89pF, CL = 9pF)		-150		Ω

Table 3-4 Reference Clock

3.5 Power

3.5.1 Low-Voltage Switching Regulator

External inductor = 10uH, external capacitor = 10uF

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		2.7	3.7	4.4	V
Output Voltage		1.15	1.25	1.45	V
Rated Output Current (Iout)				200	mA
Switching Frequency			1		MHz
Power Efficiency	@Iout max		80		%

Table 3-5 Low-Voltage Switching Regulator

3.5.2 Medium-Voltage Switching Regulator

External inductor = 10uH, external capacitor = 10uF

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		2.7	3.7	4.4	V
Output Voltage		1.65	1.8	2.2	V
Rated Output Current (Iout)				200	mA
Switching Frequency			1		MHz
Power Efficiency	@Iout max		80		%

Table 3-6 Medium-Voltage Switching Regulator

3.5.3 High-Voltage LDO

External capacitor = 1uF

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		2.7		4.4	V
Output Voltage		2.4	3	3.6	V
Rated Output Current (Iout)	Input voltage = 4.2V			300	mA

Table 3-7 High-Voltage LDO

3.5.4 Medium-Voltage LDO

External capacitor = 1uF

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		2.7		4.4	V
Output Voltage		1.65	1.8	2.2	V
Rated Output Current (Iout)	Input voltage = 4.2V			200	mA

Table 3-8 Medium-Voltage LDO

3.6 Battery Charger

Item	Min.	Typ.	Max.	Unit
Input Voltage	4.5	5	6.5	V
Charge Current (CC Mode)	25		250	mA
Trickle Charge Current		12		mA
Trickle Charge Threshold Voltage		2.92		V

Regulated Output (Float) Voltage		4.2		V

Table 3-9 Battery Charger

3.7 Radio Characteristics

3.7.1 Transmitter

Basic Data Rate

Core Supply Voltage = 1.25V @ 25℃

Item		Min.	Typ.	Max.	Unit
Maximum RF transmit Power*1			8		dBm
RF power control range			20		dB
20dB bandwidth for modulated carrier			900		KHz
Adjacent channel transmit power	+2MHz			-20	dBm
	-2MHz			-20	dBm
	+3MHz			-40	dBm
	-3MHz			-40	dBm
Frequency deviation	Δf1avg Maximum Modulation		165		KHz
	Δf2max Minimum Modulation		140		KHz
	Δf1avg/Δf2avg		0.9		
Initial carrier frequency tolerance		-75		75	KHz
Freq. Drift	DH1 packet	-25		25	KHz
	DH3 packet	-40		40	KHz
	DH5 packet	-40		40	KHz
Freq. Drift Rate		-20		20	KHz/50us
Harmonic Content			-45		dBm

Table 3-10 Transmitter Basic Data Rate

*1 The maximum RF transmit power could reach to 8dBm with appropriate settings

Enhanced Data Rate

Core Supply Voltage = 1.25V @ 25℃

Item	Min.	Typ.	Max.	Unit

Relative transmit power			-1.5		dB
π/4 DQPSK max carrier frequency stability $\|\omega_o\|$		-10		10	KHz
π/4 DQPSK max carrier frequency stability $\|\omega_i\|$		-75		75	KHz
π/4 DQPSK max carrier frequency stability $\|\omega_o+\omega_i\|$		-75		75	KHz
8DPSK max carrier frequency stability $\|\omega_o\|$		-10		10	KHz
8DPSK max carrier frequency stability $\|\omega_i\|$		-75		75	KHz
8DPSK max carrier frequency stability $\|\omega_o+\omega_i\|$		-75		75	KHz
π/4 DQPSK Modulation Accuracy	RMS DEVM			20	%
	99% DEVM	99			%
	Peak DEVM			35	%
8DPSK Modulation Accuracy	RMS DEVM			13	%
	99% DEVM	99			%
	Peak DEVM			25	%
In-band spurious emissions	F > F0 + 3MHz			-40	dBm
	F < F0 - 3MHz			-40	dBm
	F = F0 + 3MHz			-40	dBm
	F = F0 - 3MHz			-40	dBm
	F = F0 + 2MHz			-20	dBm
	F = F0 - 2MHz			-20	dBm
	F = F0 + 1MHz			-26	dB
	F = F0 - 1MHz			-26	dB
EDR Differential Phase Encoding		99			%

Table 3-11 Transmitter Enhanced Data Rate

Low Energy

Core Supply Voltage = 1.25V @ 25℃

Item		Min.	Typ.	Max.	Unit
Maximum RF transmit power[*1]			8		dBm
Peak power – Average power				3	dB
In-band emissions	≥ +3MHz			-30	dBm
	+2MHz			-20	dBm
	-2MHz			-20	dBm
	≤ -3MHz			-30	dBm

Modulation characteristics	Δf1avg	225		275	KHz
	99.9% Δf2max	185			KHz
	Δf1avg/Δf2avg	0.8			
Center freq. deviation, F_n (n = 0,1,2,….k)		-150		150	KHz
Freq. drift, $\|F_0 - F_n\|$ (n = 2,3,4,…k)		-50		50	KHz
Initial freq. drift, $\|F_1 - F_0\|$		-20		20	KHz
Max. freq. drift rate, $\|F_n - F_{n-5}\|$ (n = 6,7,8,…k)		-20		20	KHz/50us
Harmonic content			-45		dBm

Table 3-12 Transmitter Low Energy

*1 The maximum RF transmit power could reach to 8dBm with appropriate settings

3.7.2 Receiver

Basic Data Rate

Core Supply Voltage = 1.25V @ 25℃

Item		Min.	Typ.	Max.	Unit
Sensitivity	2.402GHz		-94		dBm
	2.441GHz		-94		dBm
	2.480GHz		-94		dBm
Maximum input level		-20			dBm
Co-Channel interference, C/I				11	dB
Adjacent channel interference, C/I	$F = F_0$+1MHz			0	dB
	$F = F_0$-1MHz			0	dB
	$F = F_0$+2MHz			-30	dB
	$F = F_0$-2MHz			-20	dB
	$F = F_0$+3MHz			-40	dB
	$F = F_{image}$			-9	dB
Intermodulation		-39			dBm
Blocking	30-2000 MHz	-10			dBm
	2000-2400 MHz	-27			dBm
	2500-3000 MHz	-27			dBm
	3000-12750 MHz	-10			dBm

Table 3-13 Receiver Basic Data Rate

Enhanced Data Rate

Core Supply Voltage = 1.25V @ 25℃

Item			Min.	Typ.	Max.	Unit
Sensitivity	π/4 DQPSK			-94		dBm
	8DPSK			-85		dBm
Maximum input level	π/4 DQPSK		-20			dBm
	8DPSK		-20			dBm
Co-Channel interference, C/I	π/4 DQPSK				13	dB
	8DPSK				21	dB
Adjacent channel interference, C/I	F = F_0+1MHz	π/4 DQPSK			0	dB
		8DPSK			5	dB
	F = F_0-1MHz	π/4 DQPSK			0	dB
		8DPSK			5	dB
	F = F_0+2MHz	π/4 DQPSK			-30	dB
		8DPSK			-25	dB
	F = F_0-2MHz	π/4 DQPSK			-20	dB
		8DPSK			-13	dB
	F = F_0+3MHz	π/4 DQPSK			-40	dB
		8DPSK			-33	dB
	F = F_{image}	π/4 DQPSK			-7	dB
		8DPSK			0	dB

Table 3-14 Receiver Enhanced Data Rate

Low Energy

Core Supply Voltage = 1.25V @ 25℃

Item		Min.	Typ.	Max.	Unit
Sensitivity	2.402GHz		-98		dBm
	2.440GHz		-98		dBm
	2.480GHz		-98		dBm
Maximum input level		-10			dBm
Co-Channel interference, C/I				21	dB

Adjacent channel interference, C/I	F = F_0+1MHz			15	dB
	F = F_0-1MHz			15	dB
	F = F_0+2MHz			-17	dB
	F = F_0-2MHz			-15	dB
	F = F_0+3MHz			-27	dB
	F = F_{image}			-9	dB
Intermodulation		-50			dBm
Blocking	30-2000 MHz	-30			dBm
	2003-2399 MHz	-35			dBm
	2484-2997 MHz	-35			dBm
	3000-12750 MHz	-30			dBm
PER report integrity		50		65.4	%

Table 3-15 Receiver Low Energy

3.8 Audio ADC

Item	Condition	Min.	Typ.	Max.	Unit
SNR	Microphone amplifier (A-Weighted 1kHz@ full scale, microphone input BW=20~20kHz)		90		dB
THD+N	Microphone amplifier gain=42dB (A-Weighted 1kHz@-10dBFS, microphone input BW=20~4kHz)			-55	dB
	Microphone amplifier gain=21dB (A-Weighted 1kHz@-10dBFS, microphone input BW=20~20kHz)		-68		dB
Analog Gain		0		42	dB
Input Full-Scale at MAX gain			2.24		mVrms
Input Full-Scale at Min gain			282		mVrms
Microphone in level	(Microphone input, full scale)			0.8	Vpp
Mic_bias_voltage			2.7		V

Table 3-16 Audio ADC

3.9 Stereo DAC

Item	Condition	Min.	Typ.	Max.	Unit
SNR	With A-weighted		94		dB
THD+N	16 ohm load Analog gain=0dB		0.06		%
Output swing	load=16Ohm SPK_LP--(16Ohm)--SPK_LN SPK_LN--(16Ohm)--SPK_LP speaker gain=0dB		2.1		Vpp
Analog Gain	-36~+9(step=3dB)	-36 (-72)		9	dB
Allow load		8	16		Ohm
Cross talk	Load =16ohm		-70		dB
Noise floor power	Analog gain=0dB		-100		dBV

Table 3-17 Stereo DAC

4 Function Description

4.1 Radio Transceiver

The AB1526 RF transceiver is a 2.4GHz-band transceiver for the Bluetooth Headset applications. There are three main functions – transmitter, receiver, and synthesizer. The enable control signals of these functions are given by the Baseband Processing Unit.

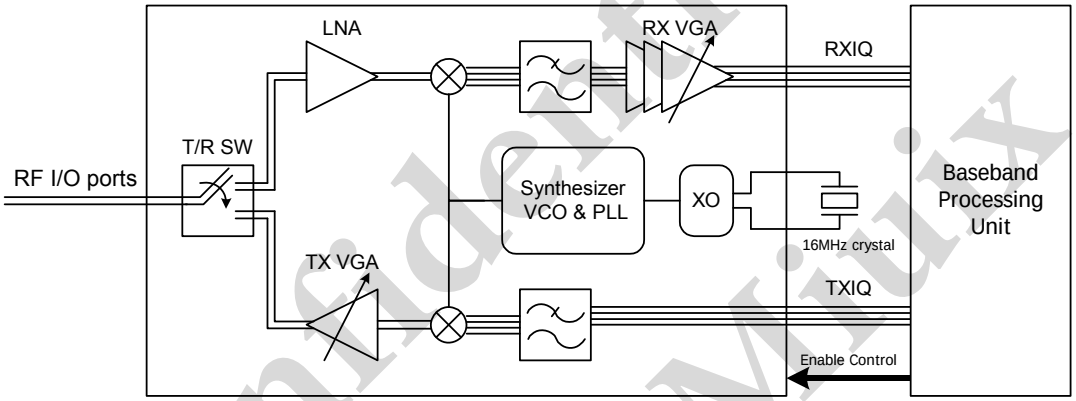


Figure 4-1 Radio Transceiver

4.1.1 RF Front End

The RX input ports and TX output ports share the same RF terminals such that no external T/R switch is required. Only few matching components are placed outside the RF terminals.

4.1.2 Receiver

The AB1526 RF receiver is composed of two parts: RF front-end and IF part. The RF front-end part comprises a LNA and a quadrature mixer. The IF part comprises a low-pass filter (LPF) for out-band filtering and a variable gain amplifier (VGA).

The LNA input shares the same RF ports with TX output. The RX front-end gain could be adjusted, and thus reduce the probability of bit errors caused by poor signal-to-noise ratio. After the LNA is followed by a quadrature mixer that down-converts the RF signal to IF band.

At the IF part, the down-converted signal is first low-pass filtered by the LPF, amplified by the VGA, and then sent to the ADC for demodulation. The 3dB bandwidth of the LPF could be adjusted through RF registers. The LNA and VGA provide more than 80dB gain control range.

4.1.3 Transmitter

The AB1526 RF transmitter comprises a LPF, a modulator and a VGA stage. The TX baseband signals are fed from baseband DAC, generated by the baseband modulators. A LPF is implemented to attenuate the second side-lobe of signal spectrum and unwanted oversampling clock or spurious signals. The 3dB bandwidth of the LPF could be adjusted through RF registers. The VGA provides variable gain with more than 20dB dynamic range, and could be controlled through RF register interface.

4.1.4 Synthesizer

The AB1526 features a fractional-N synthesizer with embedded VCO and loop filter without the need of external components. It also integrates an internal crystal oscillator that only an external 16MHz crystal is required.

4.2 Baseband Processing Unit

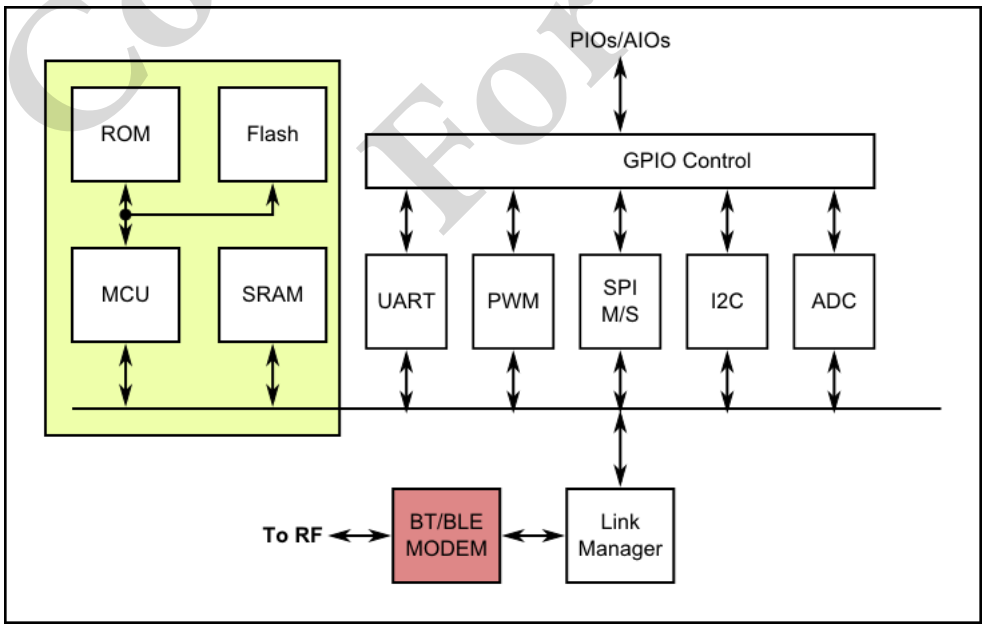


Figure 4-2 Baseband Processing Unit

The baseband processing unit contains a MCU subsystem, a Link Manager and a Modem.

4.2.1 MCU System

The MCU system executes the Bluetooth protocol stacks and supported profiles. It also provides 16M-bits embedded flash for customization. The ROM size is 128K bytes and SRAM size is 32K bytes.

4.2.2 Link Manager

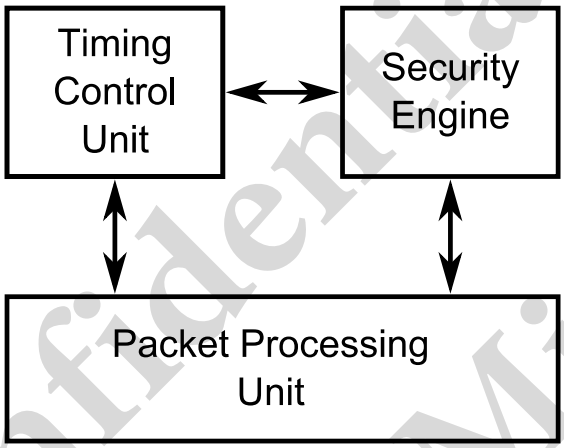


Figure 4-3 Link Manager

The Link Manager has a Timing Control Unit, a Security Engine, and a Packet Processing Unit. The Timing Control Unit generates and keeps the timing information for all Bluetooth links. The Packet Processing Unit assembles and disassembles Bluetooth packets and has dedicated hardware to process data whitening, forward error correction (FEC), and cyclic redundancy check (CRC). The Security Engine is used to encrypt and decrypt the data if the encryption option is turned on.

4.2.3 Modem

The Modem supports basic rate, EDR 2Mbps mode, EDR 3Mbps, and Bluetooth low energy (BLE) mode. It satisfies the requirements of the Bluetooth v4.2 + EDR specification.

4.3 Serial Interfaces

4.3.1 SPI

The SPI is capable of communicating with external devices. Both 3-wire and 4-wire mode SPI interfaces are supported. When 3-wire mode is selected, SPI_MOSI would be data I/O pin of the SPI interface. Only master mode is supported.

The SPI interface is shared with GPIOs and the mapping tables are listed below.

GPIO pins	SPI Master mode 0	SPI Master mode 1
GPIO4	SPI_NCS	
GPIO5	SPI_MOSI	
GPIO6	SPI_MISO	
GPIO7	SPI_SCK	
GPIO14		SPI_NCS
GPIO15		SPI_MOSI
GPIO16		SPI_MISO
GPIO17		SPI_SCK

Table 4-1 SPI GPIO Mapping Table

The SPI Interface provides much flexibility that can fit most SPI slave devices. The polarity and phase of SCK can be both programmed and results in four combinations. The NCS to SCK delay, the SCK to NCS delay, and SCK period are also programmed. The timing relationships of SPI Interface are illustrated below.

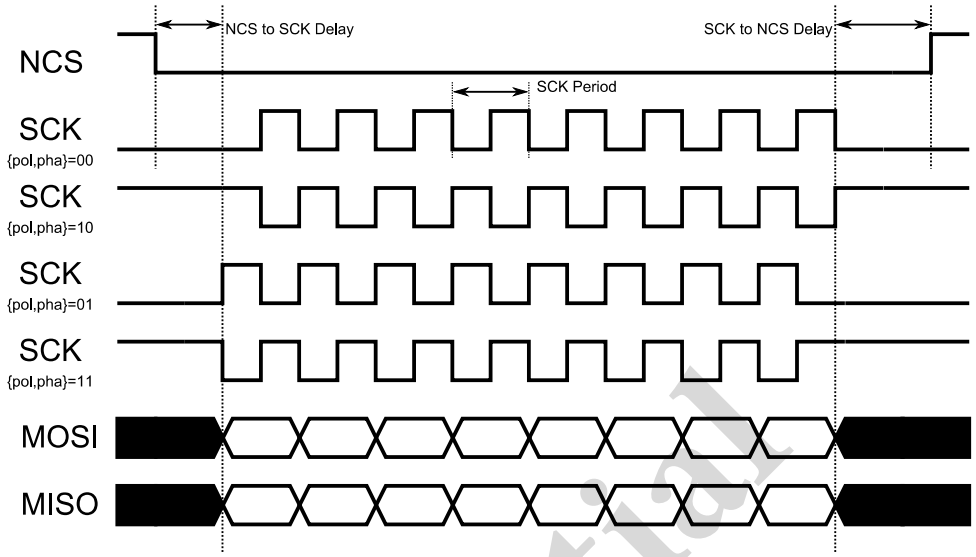


Figure 4-4 SPI Interface Timing Diagram

The SPI Interface also supports multiple bytes in single transfer. Between each byte, a Hold Delay can be set. This is drawn in below.

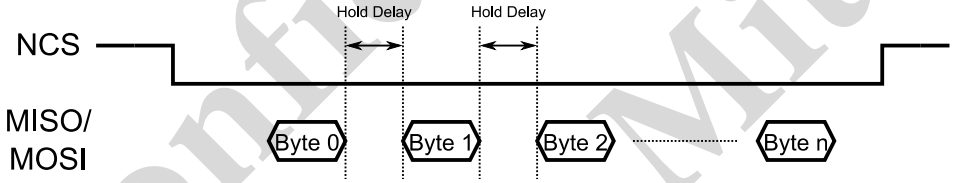


Figure 4-5 SPI Interface Multiple Bytes Transfer

4.3.2 UART

The UART interface supports flexible configurations as listed below. There are local FIFOs and DMA which can achieve high throughputs serial communications. The UART also supports the hardware flow control. When it is enabled, two additional signals, UART_RTS and UART_CTS, are required. To provide the maximum flexibility, both UART_RTS and UART_CTS can be configured via any available GPIOs.

Configuration Parameters	Supported Values
Data Length	8 bits
Flow control	Hardware RTS/CTS None

Parity	Even Odd None
Number of stop bits	1 or 2
Baud rate	1200 2400 4800 9600 19200 38400 57600 76800 115200 230400 460800 921600 1843200 3000000

Table 4-2 UART Configuration Parameters

Baud Rate	Percent Error
1200	-
2400	-
4800	-
9600	-
19200	0.16
38400	0.16
57600	0.16
76800	0.16
115200	0.16
230400	0.16
460800	0.16
921600	7.52
1843200	8.50
3000000	-

Table 4-3 Baud rate accuracy per bit

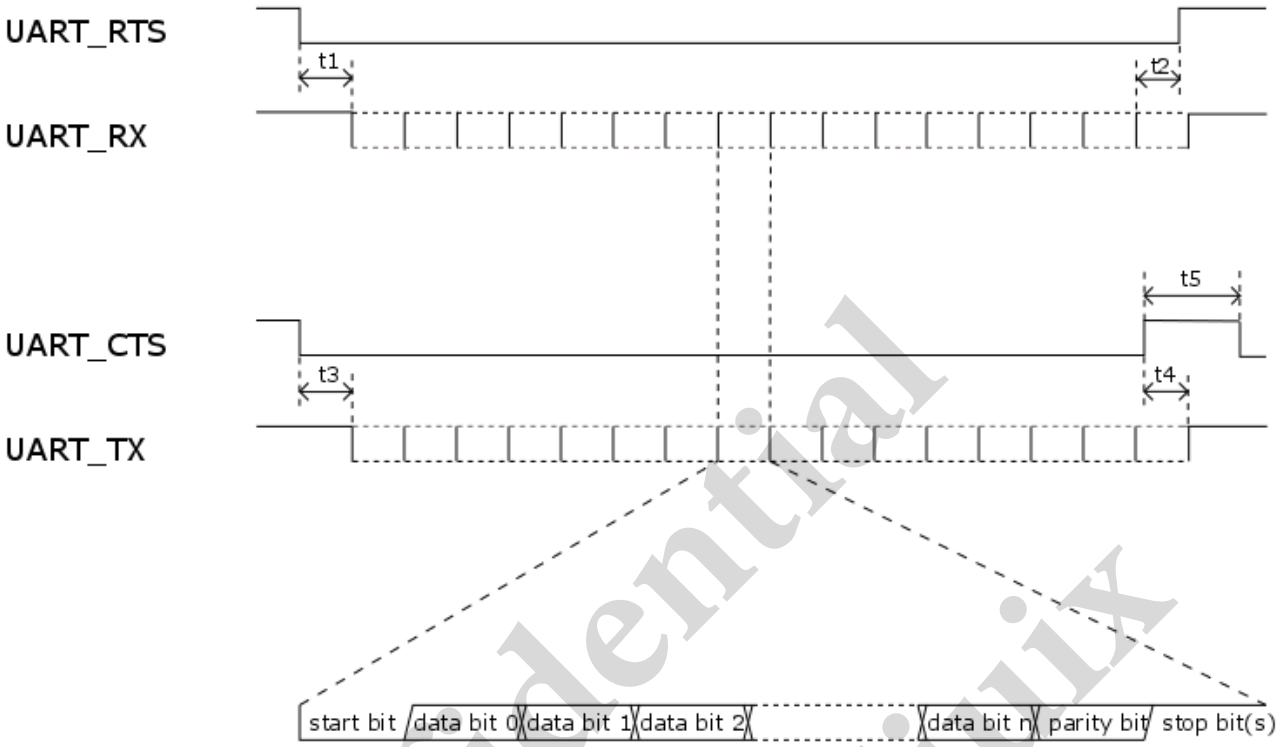


Figure 4-6 UART Timing Diagram

symbol	description	min	max	unit
t1	RTS low to start receiving	0	-	us
t2	Last 2 byte received to RTS high	-	1	byte
t3	CTS low to start transmitting	0.5	1.5	bit
t4	CTS high to stop transmitting	-	1	byte
t5	CTS-high pulse width	1	-	bit

Table 4-4 Description of the symbols in Figure 4-6

4.3.3 I2C

The I2C is a master interface. It supports 100, 400 and 800 KHz clock rates. For controlling EEPROM, a write protect (WP) signal is also supported through GPIO. The I2C interface provides several data formats and can fit various I2C peripherals. Sequential read and write are supported to improve throughputs.

The red S squares mean START or repeated START condition, while the red P squares mean STOP condition of transactions in figure 4-7~ 4-11. The green A squares mean Acknowledge(ACK) or Not

Acknowledge(NACK) bit in figure 4-7~ 4-11. Please note that the ACK or NACK is issued by a receiver. For example, if it's a transmission, ACK or NACK will be issued by the slave. On the other hand, if it's a requesting for data, ACK or NACK will be issued by the master. The W squares, a data bit, mean transmission(WRITE), while R squares mean requesting for data(READ) in figure 4-7~ 4-11. The detailed timing of red S squares, red P square, green A squares, & data bits can be seen in figure 4-12.

Figure 4-7 I2C Write transfer for 8-bit Register Addressing Mode

Figure 4-8 I2C Read transfer for 8-bit Register Addressing Mode

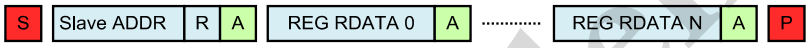


Figure 4-9 I2C Read transfer with Current Address for 8-bit Register Addressing Mode

Figure 4-10 I2C Write transfer for 16-bit Register Addressing Mode

Figure 4-11 I2C Read transfer for 16-bit Register Addressing Mode

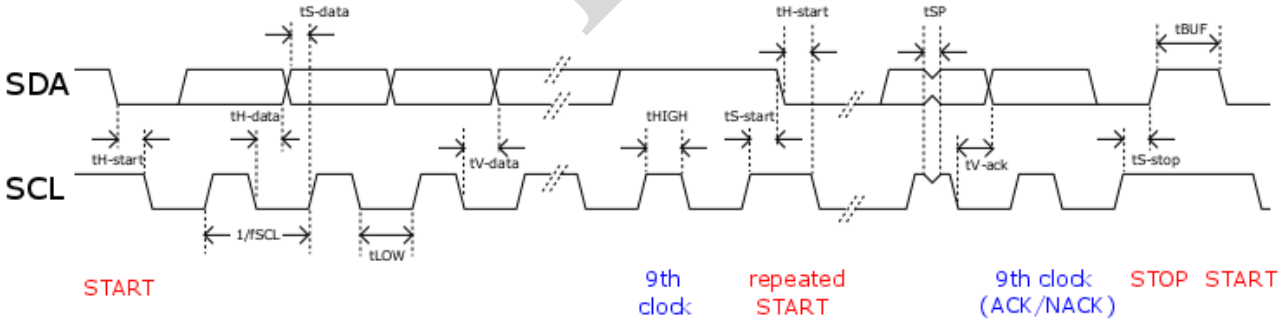


Figure 4-12 Definition of timing on the I^{2}C bus

symbol	description	Standard-mode		Fast-mode		Fast-mode Plus		unit
		min	max	min	max	min	max	
fSCL	SCL clock frequency	0	100	0	400	0	800	KHz
tLOW	LOW period of the SCL clock	5.00	-	1.58	-	0.67	-	us
tHIGH	HIGH period of the SCL clock	5.00	-	0.92	-	0.58	-	us
tS-start	Set-up time for a repeated START condition	6.33	-	1.33	-	0.67	-	us
tH-start	Hold time for a START or repeated START condition	1.33	-	0.50	-	0.25	-	us
tH-data	Hold time for data	0	-	0	-	0	-	us
tS-data	Set-up time for data	250	-	100	-	50	-	ns
tV-data	Data valid time	1.00	1.00	0.58	0.58	0.17	0.17	us
tV-ack	Data valid acknowledge time	1.00	1.00	0.58	0.58	0.17	0.17	us
tS-stop	Set-up time for STOP condition	1.00	8.00	0.50	2.00	0.25	1.00	us
tBUF	Bus free time between a START & STOP condition	3.33	-	0.83	-	0.42	-	us
tSP	Pulse width spikes must be suppressed by the input filer	0	83.3	0	83.3	0	83.3	ns

Table 4-5 Description of the symbols in Figure 4-12

4.4 Power Management / Regulation

AB1526 integrates a Power Management Unit (PMU), two Bulk regulators, two LDO regulators, and a Li-ion battery charger.

4.4.1 Buck Regulator

The Middle/Low Voltage Buck Regulators are embedded to convert VBAT to 1.8V/1.25V voltage to supply AB1526. The Buck out voltage is 1.8V, it will supply AB1526 Audio block directly. The Buck out voltage is 1.25V, it will supply AB1526 core directly. The block shows the buck circuit with LC component.

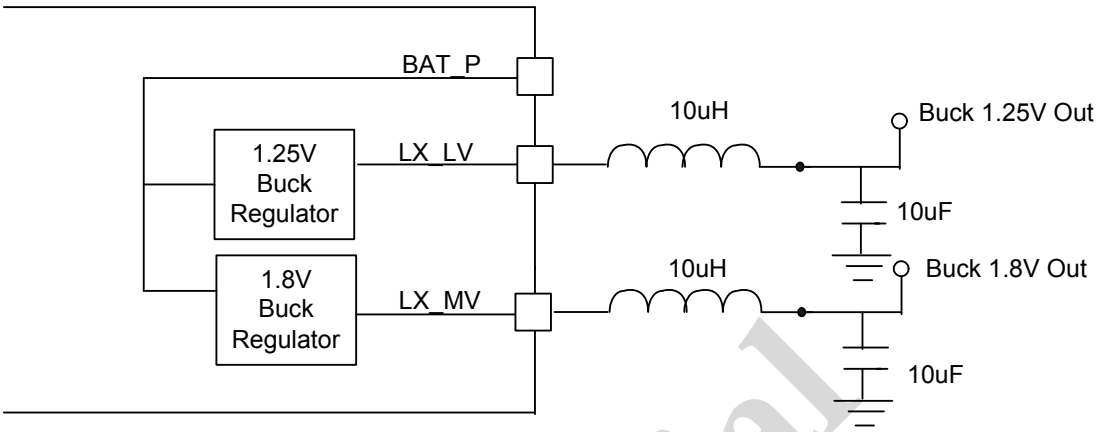


Figure 4-13 Buck Regulator Circuit

4.4.2 LDO Regulator

The High/Medium Voltage Regulators are embedded to convert VBAT to 3V/1.8V voltage to supply AB1526.The HV Regulator voltage programming range is 2.4V~3.6V. MV Regulator voltage programming range is 1.65V~2.2V. In some applications, audio part and peripheral may be supplied by the HV/MV voltages.

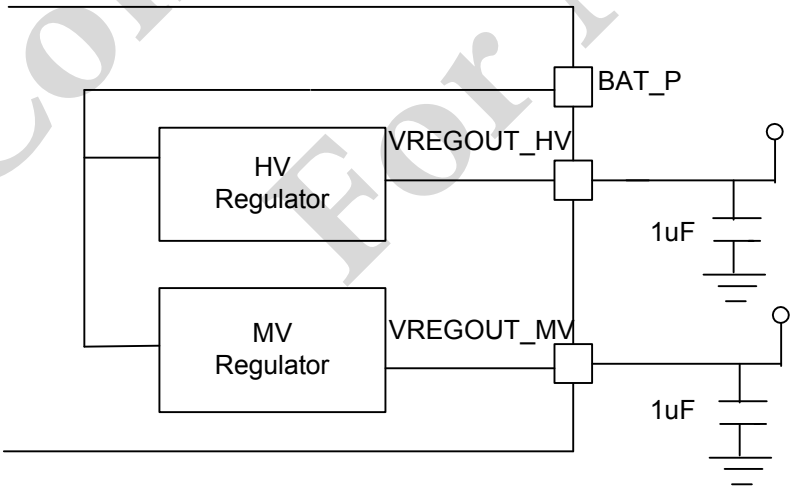


Figure 4-14 LDO Regulator Circuit

4.4.3 Power Management (PMU)

The PMU is designed in AB1526 for the power management tasks. The PMU control the Buck and LDO Regulator power in sequence. During general operations, MCU may get into sleep mode for power saving. During power saving, the PMU monitors the keys and wakes up the MCU if one of the keys is pressed. PMU also monitors the battery voltage and reports to MCU. When the battery charger power supply is connected to the device, PMU will monitor if the voltage is high enough and enable the battery charger circuit to charge the Li-ion battery.

4.4.4 Li-ion Battery Charger

The Li-mode battery charger of AB1526 provides four modes:

- Trickle mode
- Constant current mode (CC mode)
- Constant voltage mode (CV mode)
- Standby mode

The below block diagram shows the charge circuit. When an external power supply is connected to AB1526 VCHG pin, PMU will first detect if the VCHG voltage is correct and enable the charger circuit.

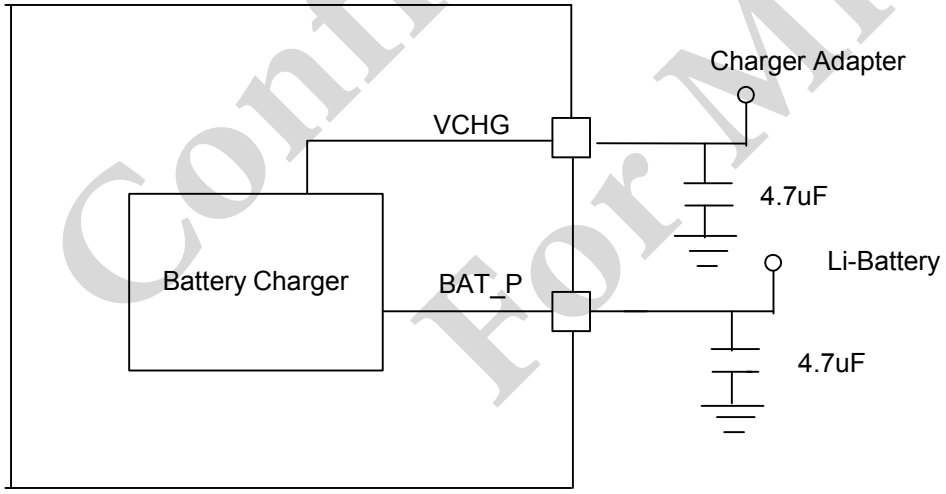


Figure 4-15 Battery Charger Circuit

When Charger circuit is enabled, it will detect the battery voltage and enters the associated mode to charge the battery, i.e. Trickle, CC or CV mode. When the battery voltage reaches a high threshold, the charger will enter standby mode and keep watching the battery voltage. If the battery voltage drops to a lower threshold, charger circuit will re-charge the battery again. The Charge profile is shown as below.

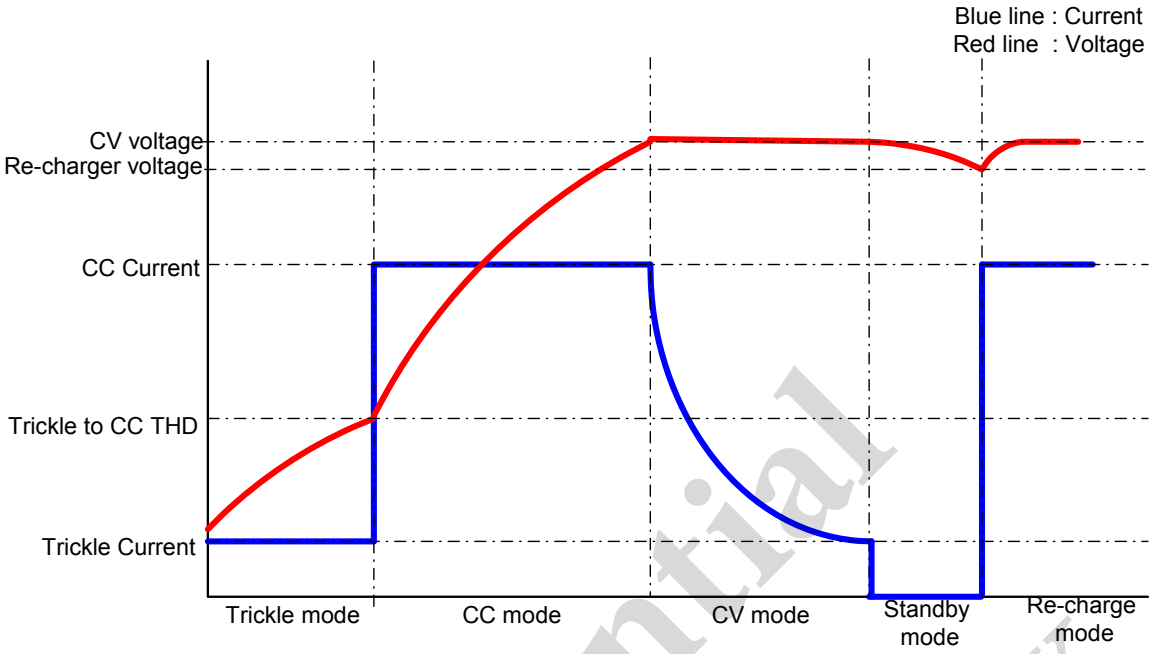


Figure 4-16 Charging Profile

4.5 Audio

The Audio Interface of AB1526 consists of:

- Dual Analog audio inputs
- Dual Analog audio outputs
- Digital Microphone interfaces (DMIC)

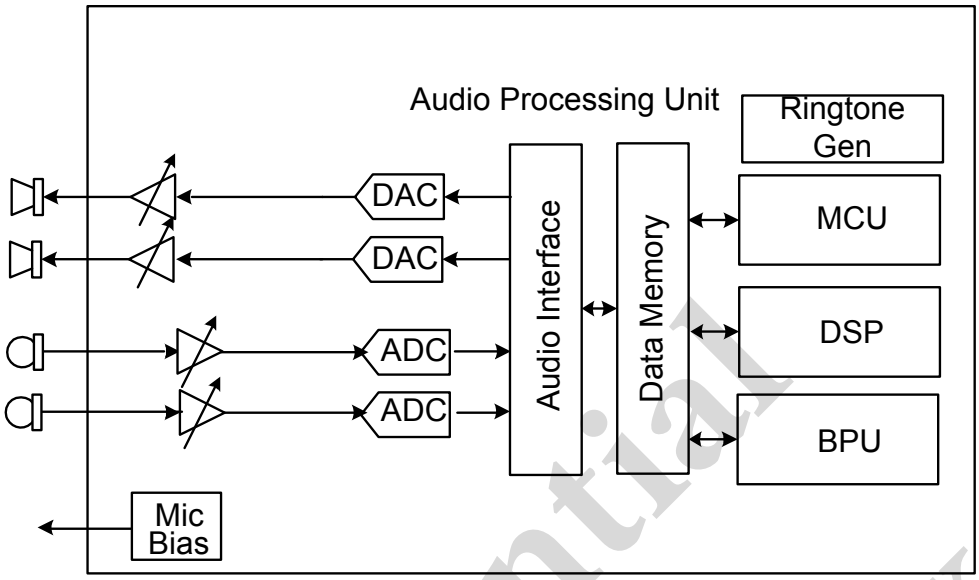


Figure 4-17 Audio Interface

The Audio Processor (APU) of AB1526 includes dual acoustic band ADC and DAC, variable gain amplifiers for external earphone and microphone. A low-noise microphone bias supply and a ring-tone generator are also embedded in AB1526.

4.5.1 Analog Audio Input

There are dual analog audio input ports in AB1526. The analog audio signal from microphone is first amplified by the Microphone Amplify, and converted to digitized data by the ADC. The microphone amplifier is differential end and has programmable gain setting from 42dB to 0dB. The voice codec converts the digitized audio data to associated audio format (A-law/u-law/CVSD) and loads into data Memory through the Audio interface. Either BPU or DSP can access the audio data from data Memory. AB1526 also provide Microphone Bias voltage to Microphone to reduce BOM cost.

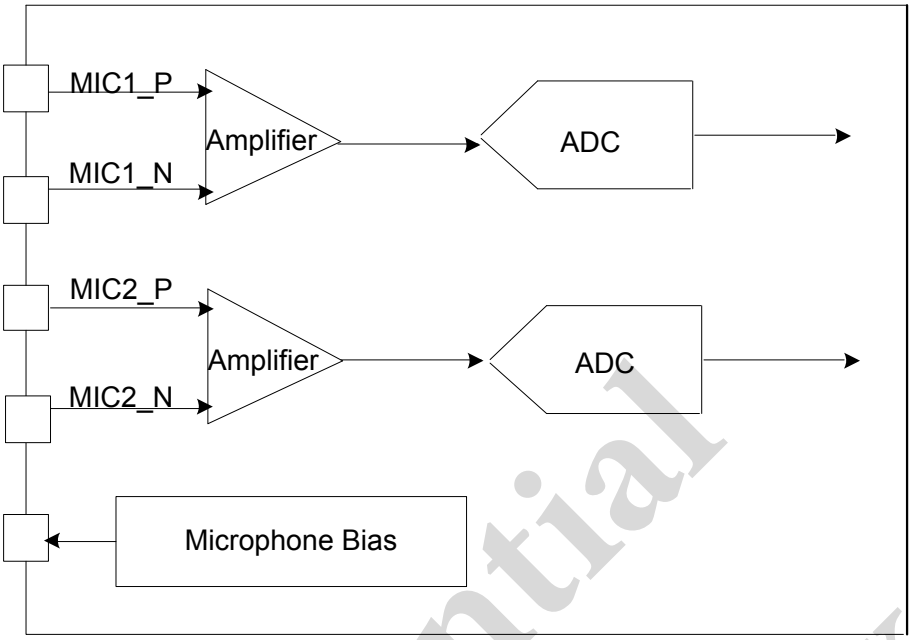


Figure 4-18 Analog Audio Input

4.5.2 Analog Audio Output

There are dual analog audio output ports in AB1526. The DAC loads the audio data from data Memory that is stored by the BPU or DSP. The audio data is decoded by the voice codec or after DSP unit processed then fed into DAC to convert to analog signal format, and amplified by the Ear amplify, and sent to the external speaker. The ear amplifier has programmable gain setting from 9dB to -36dB step is 3dB and extra low gain(-72dB). The ear amplifier out provide LR voltage common DC to reduce external capacitor in application.

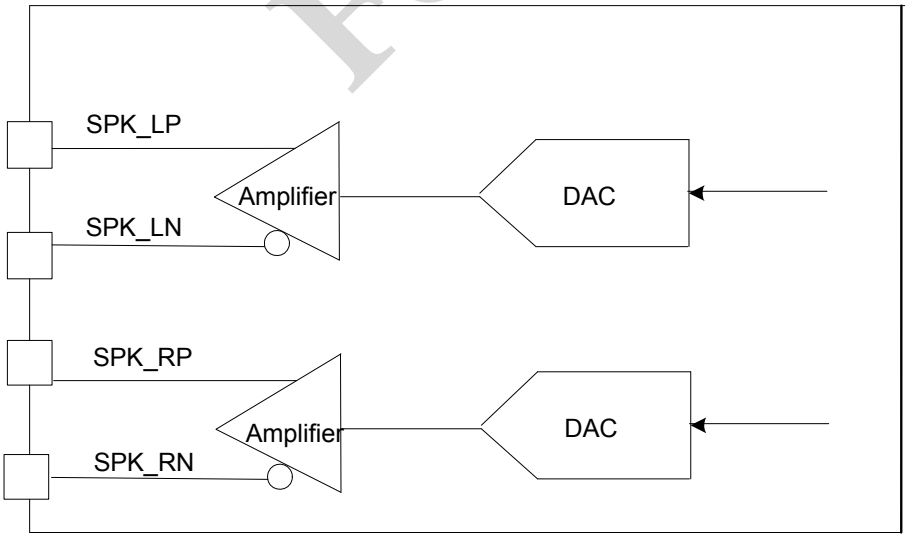


Figure 4-19 Analog Audio Output

The ring tone generator can generate five octave audio tones and play out by the speaker. The whole functions within APU are controlled by MCU.

4.5.3 Digital Microphone (DMIC) Interface

AB1526 supports two sets of DMIC interface which are selectable within GPIO3 to GPIO24. Timing diagrams and interface connection are drawn below.

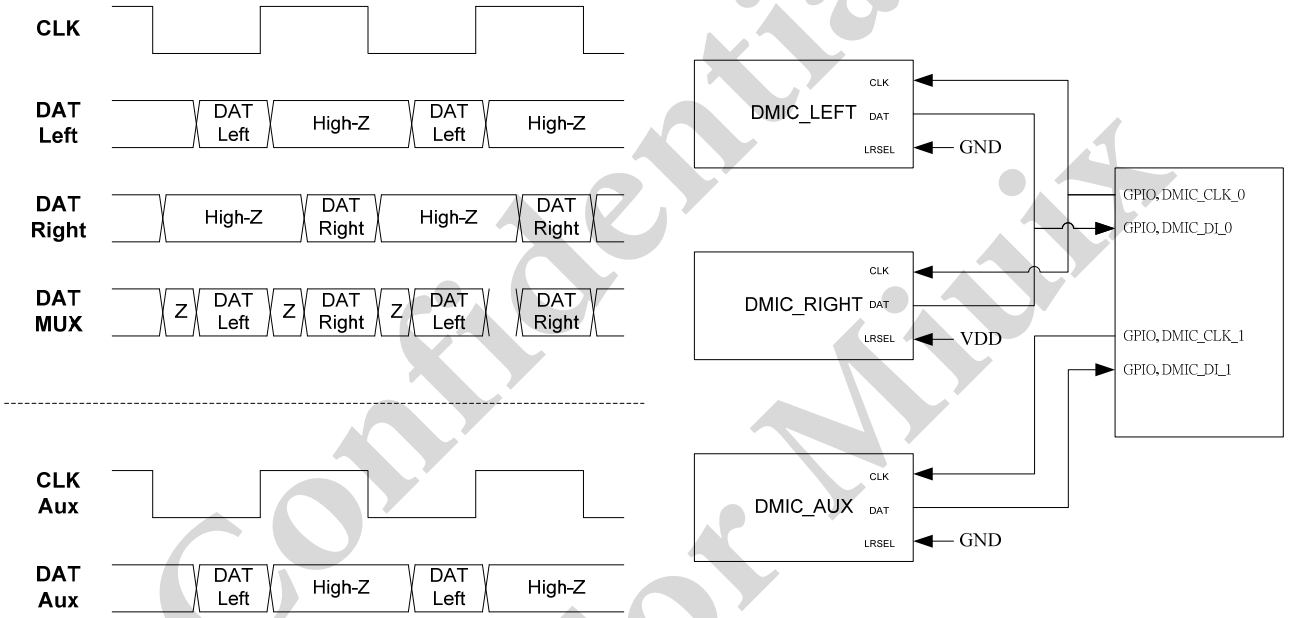


Figure 4-20 DMIC Timing diagram and Interface connection

Following table shows the phase relationship between DATA and CLK of DMIC.

	Valid	Sample Phase	LRSEL
DAT Left	Falling CLK	Rising CLK	GND
DAT Right	Rising CLK	Falling CLK	VDD
DAT Aux	Falling CLK	Rising CLK	GND

Table 4-6 DMIC Data Valid and Sample Phase Table

5 Software

5.1 Protocol Stack

The Airoha AB1526 includes the complete headset software stack as well as BLE stack/profiles. The headset software stack provides a total solution for Bluetooth music streaming and headset/handsfree applications, which include protocol stacks and profiles defined in Bluetooth A2DP, AVRCP, Headset and Handsfree profiles. The BLE stack includes ATT, GATT, Security Manager and standard based profiles such as Battery Service and Find Me Profile. In addition, it has some extra features as shown below:

- The user interface such as key operations, LED flash patterns, ringtones, voice prompt and so on can be easily reconfigured and stored in flash memory.
- Support over eight buttons with power key function.
- Advanced DSP functions for audio and music quality enhancement, and most of the control parameters of the DSP functions can be reconfigured and stored in flash memory.

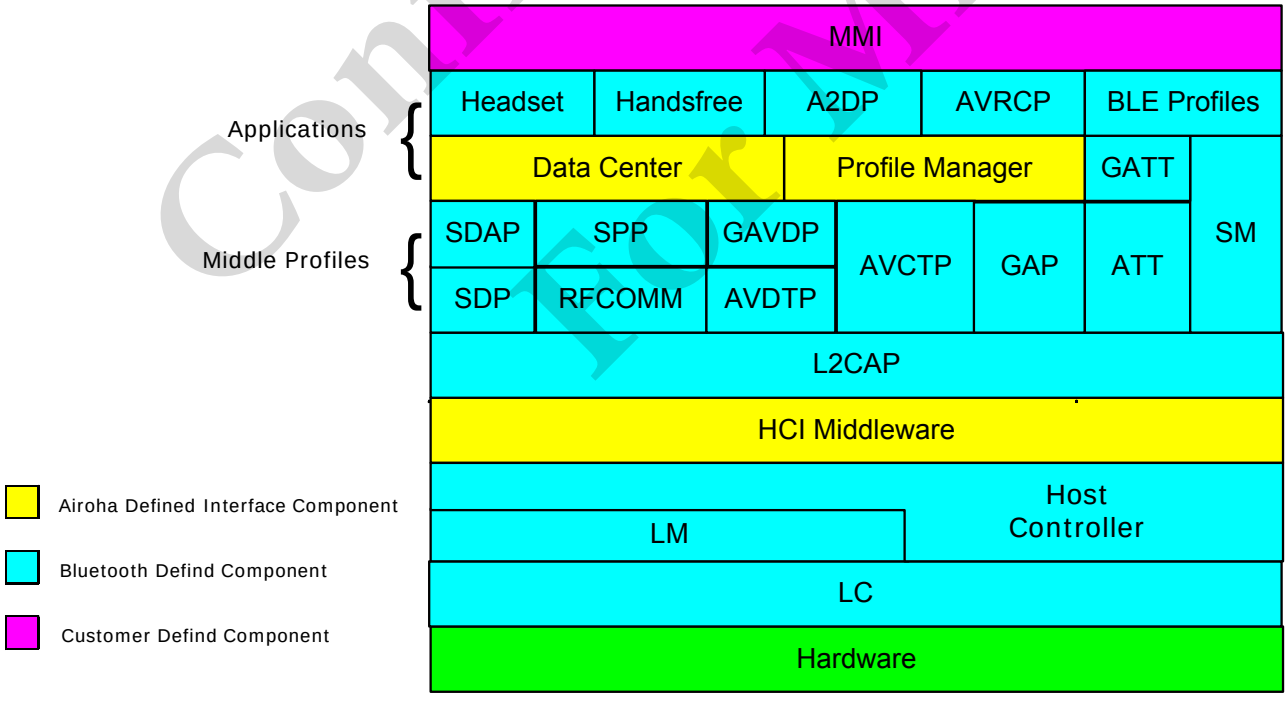


Figure 5-1 AB1526 Software Stack

5.2 Software Development Environment

The AB1526 software architecture allows customers to develop their own software as the application layer very easily. A plug-in architecture allows the customers to process data packets at many different software layers so that very flexible customization can be achieved. Airoha provides all of the necessary source codes, documentations and project files to customers enabling a fast development cycle for customers to create added value and differentiations for their end products.

5.3 Test and Configuration Tools

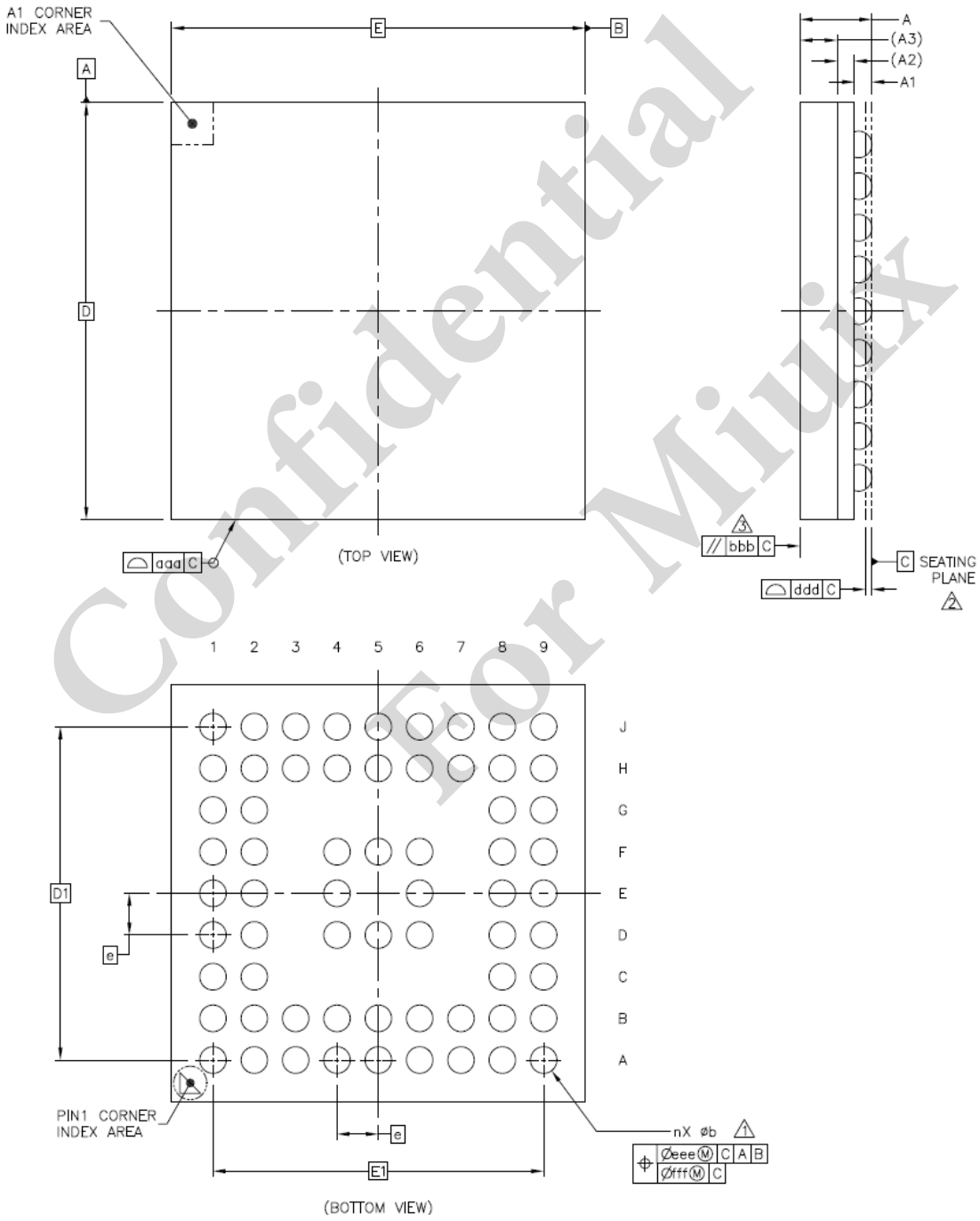
Two tools are provided for manufacture testing and configuration as shown below:

- AB1526 headset configuration tool
    - AB1526 Headset configuration tool provides to customers the capability to configure the various settings, such as Button I/O, LED behavior, Key operations, and Battery Parameters stored in flash memory. Customer code also can be processed by Airoha's AB1526 Headset configuration tool. Customers only need to prepare and compile their program by C compiler, and use the tool to automatically generate the binary data into flash memory.

- AB1526 Mass-Production tool
    - AB1526 Mass-Production tool is used during customer production stage and it provides the capability for downloading/verifying flash memory, testing RF performance, ADC calibration, and updating Bluetooth device address of the headset module. It works with the Airoha provided Test Control Board (TCB) hardware. The Mass-Production tool greatly improves the test and verification efficiency in manufacturing stage.

6 Package Information

6.1 Package Information



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.45	REF
BODY SIZE	D		5	BSC
	E		5	BSC
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.27	---	0.37
BALL PITCH	e		0.5	BSC
BALL COUNT	n		64	
EDGE BALL CENTER TO CENTER	D1		4	BSC
	E1		4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

Figure 6-1 Package Information