



ABS2U THRU ABS10U

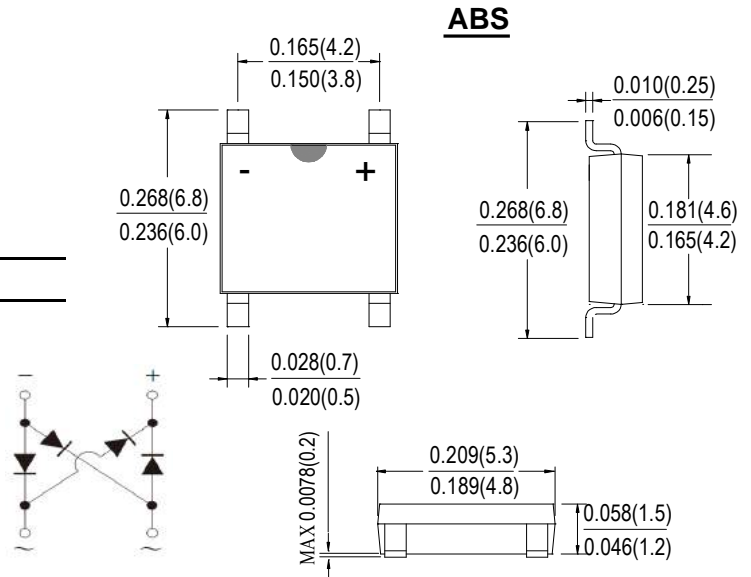
SINGLE PHASE 1.0AMP SURFACE MOUNT GLASS PASSIVATED BRIDGE RECTIFIER

Features

- Glass passivated die construction
- Low forward voltage drop
- High current capability
- High surge current capability
- Designed for surface mount application
- Plastic material-UL flammability 94V-0

Mechanical Data

- Case: SOPA-4, molded plastic ABS
- Terminals: plated leads solderable per MIL-STD-202, Method 208
- Polarity: as marked on case
- Mounting position: Any
- Marking: type number



Dimensions in inches and (millimeters)

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.

Single Phase, half wave, 60Hz, resistive or inductive load.

For capacitive load, derate current by 20%.

TYPE NUMBER	SYMBOL	ABS2U	ABS4U	ABS6U	ABS8U	ABS10U	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	200	400	600	800	1000	V
Working Peak Reverse Voltage	V_{RWM}						
DC Blocking Voltage	V_{DC}						
RMS Reverse Voltage	V_{RMS}	140	280	420	560	700	V
Average Rectified Output Current (Note:1) @ $T_c = 100^\circ C$	$I_{F(AV)}$	1.0					A
Non-Repetitive Peak Forward Surge Current 8.3ms Single half sine-wave superimposed on rated load (JEDEC Method)	I_{FSM}	35					A
I^2t Rating for Fusing ($t < 8.3ms$)	I^2t	5.08					A ² s
Forward Voltage per element @ $I_F=0.5A$ @ $I_F=1.0A$	V_{FM}	0.95			1.0		V
Peak Reverse Current @ $T_J = 25^\circ C$ At Rated DC Blocking Voltage @ $T_J = 125^\circ C$	I_R	5.0			100		μA
Typical Junction Capacitance (Note2)	C_J	15					pF
Typical Thermal Resistance	$R_{\theta JA}$	62.5					$^\circ C/W$
	$R_{\theta JL}$	25					
Operating and Storage Temperature Range	T_J, T_{STG}	-55to+150					$^\circ C$

Note:1. Mounted on glass epoxy PC board with 1.3mm² solder pad.

2. Measured at 1.0 MHz and applied reverse voltage of 4.0V D.C.



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FIG.1 MAXIMUM FORWARD CURRENT DERATING CURVE

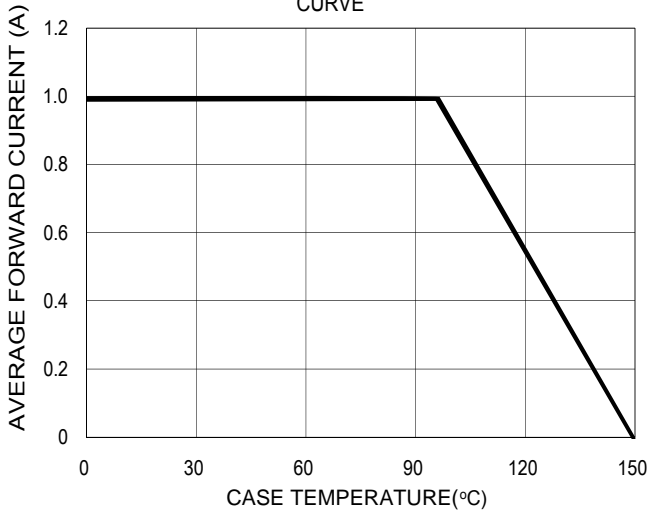


FIG. 2 TYPICAL FORWARD CHARACTERISTIC

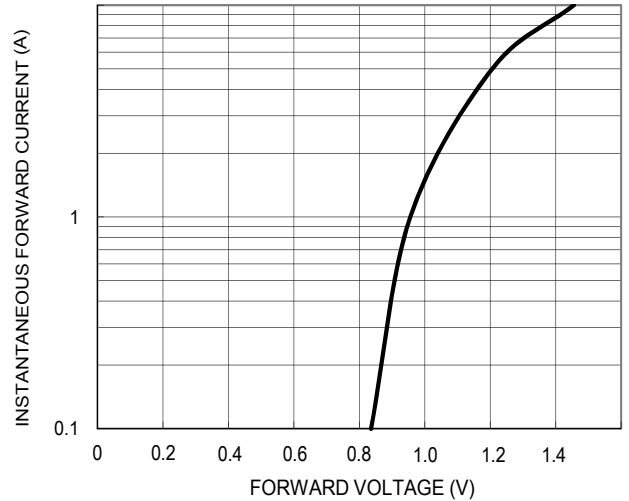


Fig. 3 Maximum Peak Forward Surge Current

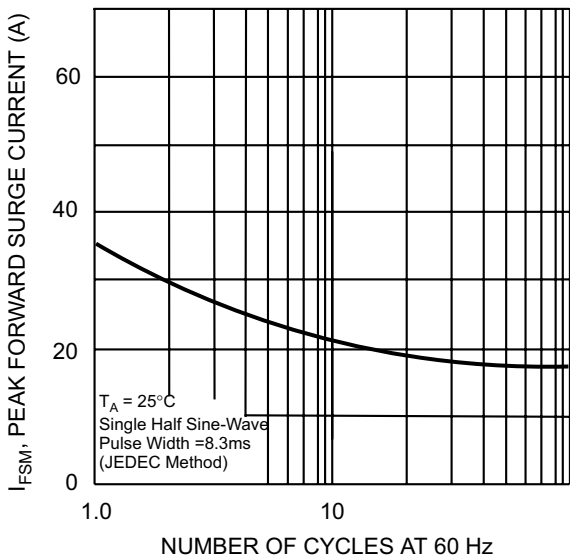


Fig. 4 Typical Reverse Characteristics

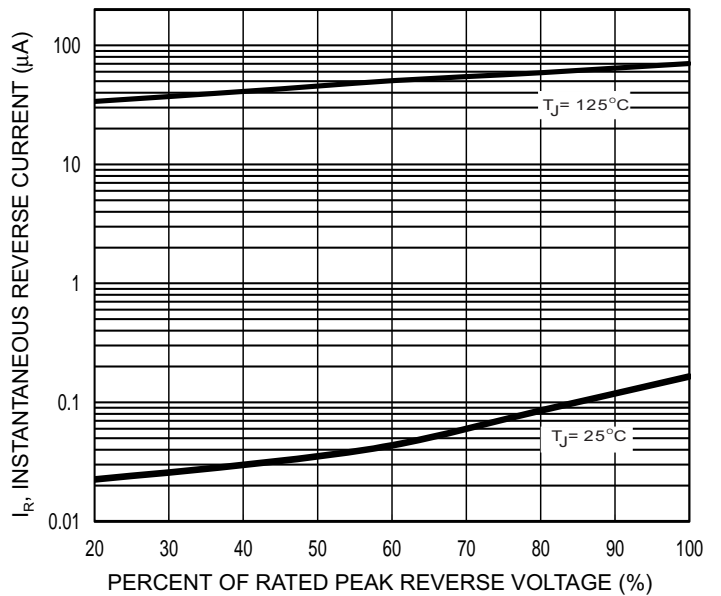
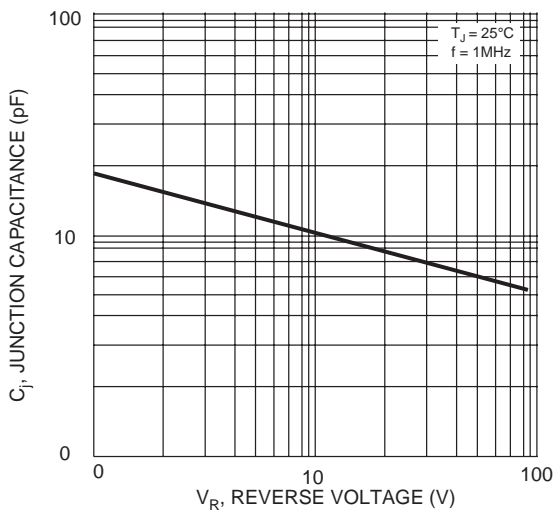
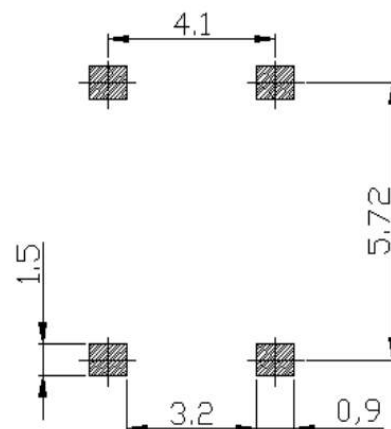


Fig. 5 Typical Junction Capacitance



PAD LAYOUT





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