# AC39LV010

## 1 Megabit (128K x 8) Flash Memory

| | |
|---|---|
| **Single Power Supply**<br>- Full voltage range: 27 to 3.6 volts for both read and write operations<br>- Regulated voltage range : 3.0 to 3.6 volts for both read and write operations | **End-of-Program or End-of-Erase Detection**<br>– Data# Polling<br>– Toggle Bit |
| **Sector-Erase Capability**<br>Uniform 4Kbyte sectors | **CMOS I/O Compatibility** |
| **Read Access Time**<br>Access time: 45, 70 and 90 ns | **JEDEC Standard**<br>Pin-out and software command sets compatible with single-power supply Flash memory |
| **Power Consumption**<br>- Active current: 5 mA (Typical)<br>- Standby current: 1 µA (Typical) | **High Reliability**<br>– Endurance cycles: 100K (Typical)<br>– Data retention: 10 years |
| **Erase/Program Features**<br>- Sector-Erase Time: 40 ms (Typical)<br>- Chip-Erase Time: 40 ms (Typical)<br>- Byte-Program Time: 11µs (Typical)<br>- Chip Rewrite Time: 1.5 seconds (Typical) | **Package Option**<br>– 32-lead PLCC<br>– 32-pin TSOP<br>– 48-pin FBGA |
| **Automatic Write Timing**<br>Internal $V_{PP}$ Generation | |

## PRODUCT DESCRIPTION

The AC39LV010 is an 1M bits Flash memory organized as 128K x 8 bits. The AC39LV010 uses single 3.0 volt-only power supply for both Read and Write functions. Featuring high performance Flash memory technology, the AC39LV010 provides a typical Byte-Program time of 11 µsec and a typical Sector-Erase time of 40 ms. The device uses Toggle Bit or Data# Polling to detect the completion of the Program or Erase operation. To protect against inadvertent write, the device has on-chip hardware and software data protection schemes. The device offers typical 100,000 cycles endurance and a greater than 10 years data retention. The AC39LV010 conforms to JEDEC standard pin outs for x8 memories. The AC39LV010 is offered in package types of 32-lead PLCC, 32-pin TSOP, 48-ball FBGA, and known good die (KGD). For KGD, please contact Actrans System Inc. or its representatives for detailed information.

The AC39LV010 devices are developed for applications that require memories with convenient and economical updating of program, data or configurations, e.g., Networking cards, Card Readers, Graphic cards, Digital TV, MP3, Wireless Phones, etc.

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## ORDERING INFORMATION
## Standard Products

The order number is defined by a combination of the following elements.

| AC39LV010 | -70 | F | W | C |
|---|---|---|---|---|

| Description |
|---|
| **Temperature Range (1 digit)**<br>C = Commercial (0°C to +70°C)<br>I = Industrial (-40°C to +85°C) |
| **Package Type (1-3 digits)**<br>W = FBGA (0.8mm pitch, 6mm x 8mm)<br>E = TSOP (Type 1, die up, 8mm x 14mm)<br>N = 32-pin PLCC<br>KGD = Known Good Die (for wafer or dice sell) |
| **F = PB (Lead) free package** |
| **Speed Option (2-3 digits)**<br>45R = 45ns<br>70 = 70ns<br>90 = 90ns<br>** = VDD = 2.7~3.6V Full voltage range<br>**R = VDD = 3.0~3.6V Regulated voltage range |
| **Device Number/Description**<br>AC39LV010<br>1 Megabit (128K x 8-Bit) Flash Memory |

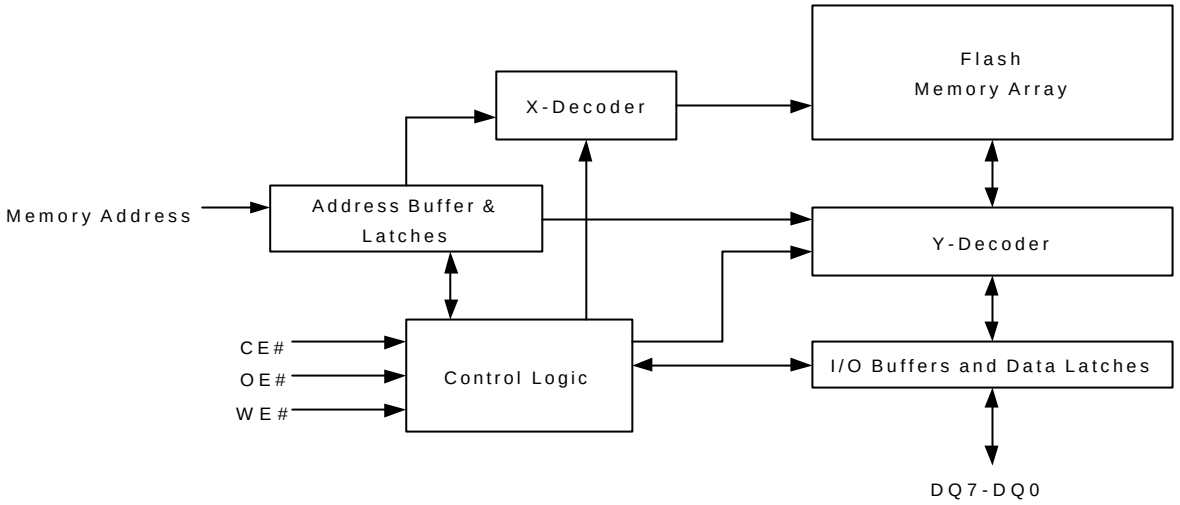
| Valid Combinations for TSOP 32Pin Package | |
|---|---|
| AC39LV010-45R | EC, EI |
| AC39LV010-70 | EC, EI |
| AC39LV010-70R | EC, EI |
| AC39LV010-90 | EC, EI |
| AC39LV010-90R | EC, EI |

| Valid Combinations for PLCC 32Pin Package | |
|---|---|
| AC39LV010-45R | NC, NI |
| AC39LV010-70 | NC, NI |
| AC39LV010-70R | NC, NI |
| AC39LV010-90 | NC, NI |
| AC39LV010-90R | NC, NI |

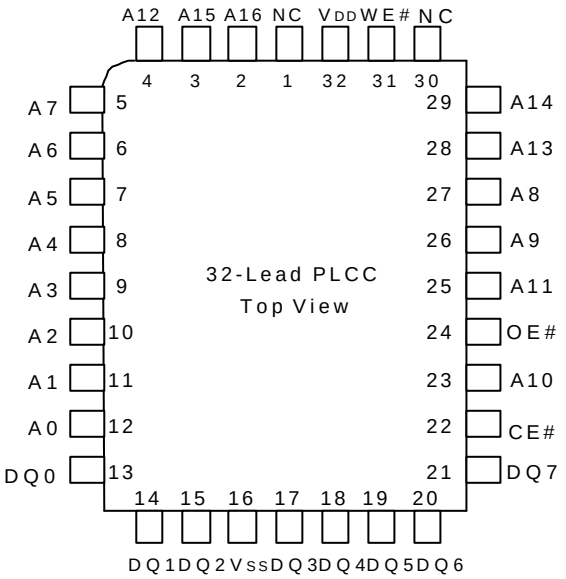
| Valid Combinations for FBGA 48 Ball Package | | | |
|---|---|---|---|
| Order Number | | Package Marking | |
| AC39LV010-45R | WC, WI | V010-45R | C, I |
| AC39LV010-70 | WC, WI | V010-70 | C, I |
| AC39LV010-70R | WC, WI | V010-70R | C, I |
| AC39LV010-90 | WC, WI | V010-90 | C, I |
| AC39LV010-90R | WC, WI | V010-90R | C, I |

**Valid Combinations:** Valid Combinations list the configurations that are supported in volume for this device.

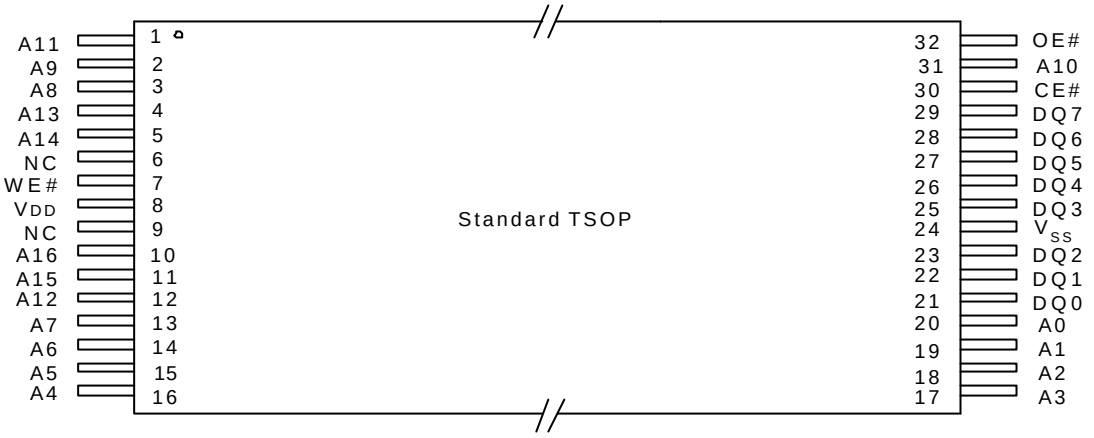
## Functional Block Diagram




## Pin Assignments



## Pin Assignments



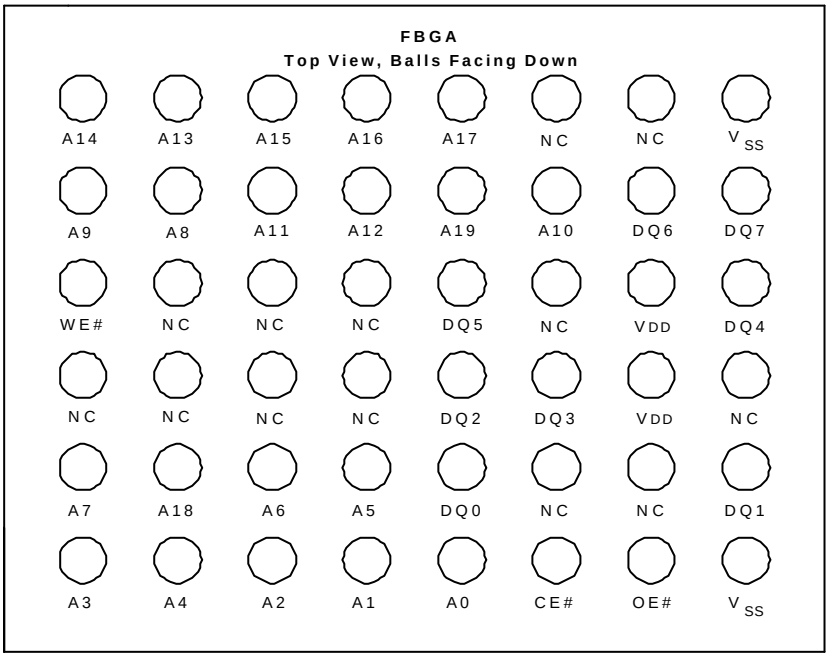



**Table 1. PIN DESCRIPTION**

| Name of the Pin | Function |
|---|---|
| A0–A16 | 17 addresses |
| DQ7–DQ0 | Data inputs/outputs |
| CE# | Chip enable |
| OE# | Output enable |
| WE# | Write enable |
| $V_{DD}$ | 3.0 volt-only single power supply* |
| $V_{SS}$ | Device ground |
| NC | Pin not connected internally |

* Note : see ordering information (page.2) for speed options and voltage supply tolerances

## DEVICE OPERATION

The AC39LV010 uses Commands to initiate the memory operation functions. The Commands are written to the device by asserting WE# Low while keeping CE# Low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

### Read

The Read operation of the AC39LV010 is controlled by CE# and OE#, both have to be Low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram in Figure 1 for further details.

### Byte Program

The AC39LV010 is programmed on a byte-by-byte basis. Before programming, the sector where the byte locates must be erased completely. The Program operation is accomplished in three steps. The first step is a three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last; and the data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 16 µs. See Figures 2 and 3 for WE# and CE# controlled Program operation timing diagrams and Figure 12 for flowchart.

During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored.

**Table 2: AC39LV010 Device Operation**

| Operation | CE# | OE# | WE# | DQ | Address |
|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | $A_{IN}$ |
| Program | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $D_{IN}$ | $A_{IN}$ |
| Erase | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X[1] | Sector address, XXH for Chip-Erase |
| Standby | $V_{IH}$ | X | X | High Z | X |
| Write Inhibit | X | $V_{IL}$ | X | High Z/$D_{OUT}$ | X |
| Write Inhibit | X | X | $V_{IH}$ | High Z/$D_{OUT}$ | X |
| Software Mode | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | | See Table 3 |
| Product Identification | | | | | |

**Note**: X can be $V_{IL}$ or $V_{IH}$, but no other value.

## Write Command/Command Sequence

The AC39LV010 provides two software methods to detect the completion of a Program or Erase cycle in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation. The actual completion of the write operation is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ7 or DQ6. In order to prevent such spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

## Chip Erase

The AC39LV010 provides Chip-Erase feature, which allows the entire memory array to be erased to logic "1" state. The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid reads are Toggle Bit and Data# Polling. See Table 3 for the command sequence, Figure 6 for timing diagram, and Figure 15 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

## Sector Erase

The AC39LV010 offers Sector-Erase mode. The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit method. See Figures 7 for timing waveforms. Any commands issued during the Sector Erase operation are ignored.

## Data# Polling (DQ7)

When the AC39LV010 is in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce the true data. Note that even though DQ7 may have valid data immediately following the completion of an internal Program operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ7 will produce a '0'. Once the internal Erase operation is completed, DQ7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-Erase or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 4 for Data# Polling timing diagram and Figure 13 for a flowchart.

## Toggle Bit (DQ6)

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating 1s and 0s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ6 bit will stop toggling. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-Erase or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 5 for Toggle Bit timing diagram and Figure 13 for a flowchart.

## Data Protection

The AC39LV010 provides both hardware and software features to protect the data from inadvertent write.

## Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

$V_{DD}$ Power Up/Down Detection: The Write operation is inhibited when $V_{DD}$ is less than 1.5V.

Write Inhibit Mode: Forcing OE# Low, CE# High, or WE# High will inhibit the Write operation. This prevents inadvertent write during power-up or power-down.

## Software Data Protection (SDP)

The AC39LV010 provides the JEDEC approved Software Data Protection (SDP) scheme for Program and Erase operations. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, especially during the system power-up or power-down transition. Any Erase operation requires the inclusion of six-byte sequence. See Table 3 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within $T_{RC}$.

## Table 3: Software Command Sequence

| Command Sequence | 1st Bus Write Cycle | | 2nd Bus Write Cycle | | 3rd Bus Write Cycle | | 4th Bus Write Cycle | | 5th Bus Write Cycle | | 6th Bus Write Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Addr[1] | Data | Addr[1] | Data | Addr[1] | Data | Addr[1] | Data | Addr[1] | Data | Addr[1] | Data |
| Byte Program | 5555H | AAH | 2AAAH | 55H | 5555H | A0H | BA[2] | Data | | | | |
| Sector Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | $SA_X$[3] | 30H |
| Chip Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 10H |
| Software ID Entry[4,6] | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | | | | | | |
| Manufacture ID | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | 0000H | 7FH | | | | |
| Manufacture ID | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | 0003H | 7FH | | | | |
| Manufacture ID | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | 0040H | 1FH | | | | |
| Device ID | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | 0001H | A8H | | | | |
| Software ID Exit[5] | XXH | F0H | | | | | | | | | | |
| Software ID Exit[5] | 5555H | AAH | 2AAAH | 55H | 5555H | F0H | | | | | | |

**Note**:

1. Address format A15-A0 (Hex), Addresses A16 can be $V_{IL}$ or $V_{IH}$, but no other value, for the Command sequence.
2. BA = Program byte address.
3. $SA_X$ for Sector-Erase; uses A16-A12 address lines.
4. The device does not remain in Software Product ID mode if powered down.
5. Both Software ID Exit operations are equivalent.
6. Please refer to figure 9 for more information.

**ABSOLUTE MAXIMUM RATINGS** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... –55°C to 125°C

Storage Temperature ..... –65°C to 150°C

D.C. Voltage on Any Pin to Ground Potential ..... –0.5 V to $V_{DD}$+0.5V

Transient Voltage (<20ns) on Any Pin to Ground Potential..... –2.0V to $V_{DD}$ +2.0V

Voltage on A9 Pin to Ground Potential..... –0.5 V to 13.2V

Package Power Dissipation Capability (Ta=25°C)..... 1.0W

Surface Mount Lead Soldering Temperature (3 Seconds)..... 240°C

Output Short Circuit Current (Note 1)..... 50mA

**Note 1:** Output shorted for no more than one second. No more than one output shorted at a time.

## Table 4: Operating Range

| Model Name | Range | Ambient Temperature | $V_{DD}$ |
|---|---|---|---|
| AC39LV010 | Commercial | 0°C to +70°C | Full voltage range : 2.7~3.6V |
| | | | Regulated voltage range : 3.0~3.6V |
| | Industrial | -40°C to +85°C | Full voltage range : 2.7~3.6V |
| | | | Regulated voltage range : 3.0~3.6V |

## AC CONDITIONS OF TEST

Input Rise/Fall Time.....5ns
Output Load.....$C_L$=30pF for 45Rns
Output Load.....$C_L$=100pF for 70ns/90ns
See Figures 10 and 11

### Table 5: DC CHARACTERISTICS (CMOS Compatible)

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Power Supply Current | Address Input =$V_{IL}/V_{IH}$, at f=1/$T_{RC}$ Min, $V_{DD}=V_{DD}$ Max | | | |
| | Read | CE#=OE#=$V_{IL}$, WE#=$V_{IH}$, all I/Os open | | 20 | mA |
| | Program and Erase | CE#=WE#=$V_{IL}$, OE#=$V_{IH}$, | | 30 | mA |
| $I_{SB}$ | Standby $V_{DD}$ Current | CE#=$V_{IHC}$, $V_{DD}=V_{DD}$ Max | | 15 | µA |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$=GND to $V_{DD}$, $V_{DD}=V_{DD}$ Max | | 1 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$=GND to $V_{DD}$, $V_{DD}=V_{DD}$ Max | | 10 | µA |
| $V_{IL}$ | Input Low Voltage | $V_{DD}=V_{DD}$ Min | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | $V_{DD}=V_{DD}$ Max | 0.7 $V_{DD}$ | | V |
| $V_{IHC}$ | Input High Voltage (CMOS) | $V_{DD}=V_{DD}$ Max | $V_{DD}$-0.3 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$=100µA, $V_{DD}=V_{DD}$ Min | | 0.2 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$=-100µA, $V_{DD}=V_{DD}$ Min | $V_{DD}$-0.2 | | V |

### Table 6: Recommended System Power-up Timing

| Parameter | Description | Min | Unit |
|---|---|---|---|
| $T_{PU-READ}$[1] | Power-up to Read Operation | 100 | µs |
| $T_{PU-WRITE}$[1] | Power-up to Program/Erase Operation | 100 | µs |

**Note**: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

### Table 7: Capacitance (Ta=25° C, f=1Mhz, other pins open)

| Parameter | Description | Test Conditions | Max |
|---|---|---|---|
| $C_{I/O}$[1] | I/O Pin Capacitance | $V_{I/O}$=0V | 12pF |
| $C_{IN}$[1] | Input Capacitance | $V_{IN}$=0V | 6pF |

**Note**: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

### Table 8: Reliability Characteristics

| Symbol | Parameter | Min Specification | Unit | Test Method |
|---|---|---|---|---|
| $N_{END}$[1] | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| $T_{DR}$[1] | Data Retention | 10 | Years | JEDEC Standard A103 |
| $I_{LTH}$[1] | Latch Up | 100+$I_{DD}$ | mA | JEDEC Standard 78 |

**Note**: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

## AC CCHARACTERISTICS

### Table 9: Read Cycle Timing Parameters

| Symbol | Parameter | 45REC | | 70REC | | 90REC | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $T_{RC}$ | Read Cycle Time | 45 | | 70 | | 90 | | ns |
| $T_{CE}$ | Chip Enable Access Time | | 45 | | 70 | | 90 | ns |
| $T_{AA}$ | Address Access Time | | 45 | | 70 | | 90 | ns |
| $T_{OE}$ | Output Enable Access Time | | 30 | | 35 | | 45 | ns |
| $T_{CLZ}$[1] | CE# Low to Active Output | 0 | | 0 | | 0 | | ns |
| $T_{OLZ}$[1] | OE# Low to Active Output | 0 | | 0 | | 0 | | ns |
| $T_{CHZ}$[1] | CE# High to High-Z Output | | 15 | | 25 | | 30 | ns |
| $T_{OHZ}$[1] | OE# High to High-Z Output | | 15 | | 25 | | 30 | ns |
| $T_{OH}$[1] | Output Hold from Address Change | 0 | | 0 | | 0 | | ns |

| Symbol | Parameter | 45EC | | 70EC | | 90EC | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $T_{RC}$ | Read Cycle Time | 45 | | 70 | | 90 | | ns |
| $T_{CE}$ | Chip Enable Access Time | | 45 | | 70 | | 90 | ns |
| $T_{AA}$ | Address Access Time | | 45 | | 70 | | 90 | ns |
| $T_{OE}$ | Output Enable Access Time | | 30 | | 35 | | 45 | ns |
| $T_{CLZ}$[1] | CE# Low to Active Output | 0 | | 0 | | 0 | | ns |
| $T_{OLZ}$[1] | OE# Low to Active Output | 0 | | 0 | | 0 | | ns |
| $T_{CHZ}$[1] | CE# High to High-Z Output | | 15 | | 25 | | 30 | ns |
| $T_{OHZ}$[1] | OE# High to High-Z Output | | 15 | | 25 | | 30 | ns |
| $T_{OH}$[1] | Output Hold from Address Change | 0 | | 0 | | 0 | | ns |

**Note**: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

### Table 10: Program/Erase Cycle Timing Parameter

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{BP}$ | Byte-Program Time | | 16 | µs |
| $T_{AS}$ | Address Setup Time | 0 | | ns |
| $T_{AH}$ | Address Hold Time | 30 | | ns |
| $T_{CS}$ | WE# and CE# Setup Time | 0 | | ns |
| $T_{CH}$ | WE# and CE# Hold Time | 0 | | ns |
| $T_{OES}$ | OE# High Setup Time | 0 | | ns |
| $T_{OEH}$ | OE# High Hold Time | 10 | | ns |
| $T_{CP}$ | CE# Pulse Width | 40 | | ns |
| $T_{WP}$ | WE# Pulse Width | 40 | | ns |
| $T_{WPH}$[1] | WE# Pulse Width High | 30 | | ns |
| $T_{CPH}$[1] | CE# Pulse Width High | 30 | | ns |
| $T_{DS}$ | Data Setup Time | 40 | | ns |
| $T_{DH}$[1] | Data Hold Time | 0 | | ns |
| $T_{IDA}$[1] | Software ID Access and Exit Time | | 150 | ns |
| $T_{SE}$ | Sector Erase | | **60** | ms |
| $T_{SCE}$ | Chip Erase | | **60** | ms |

**Note**: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

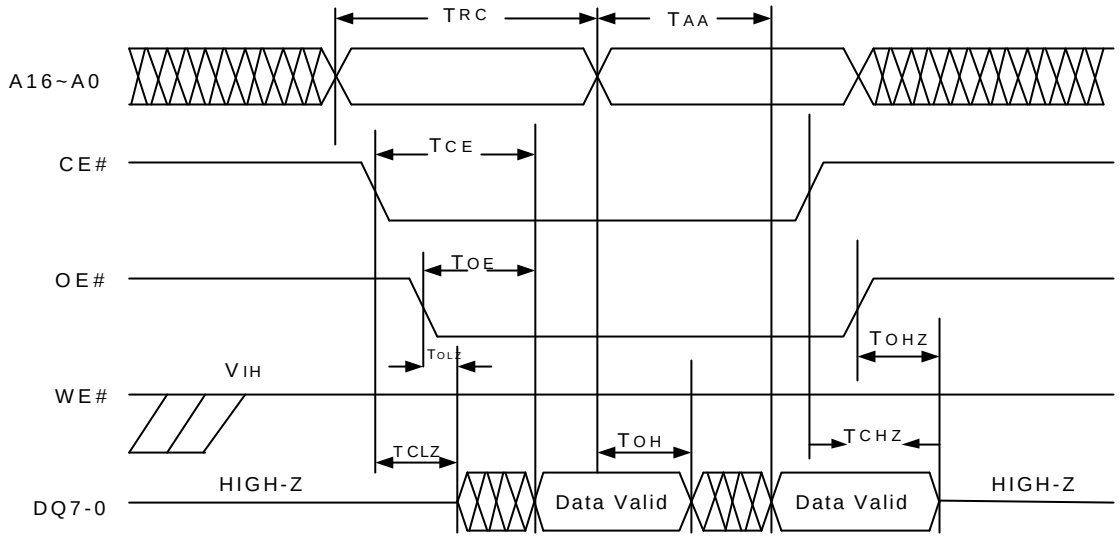



**Figure 1. Read Cycle Timing Diagram**

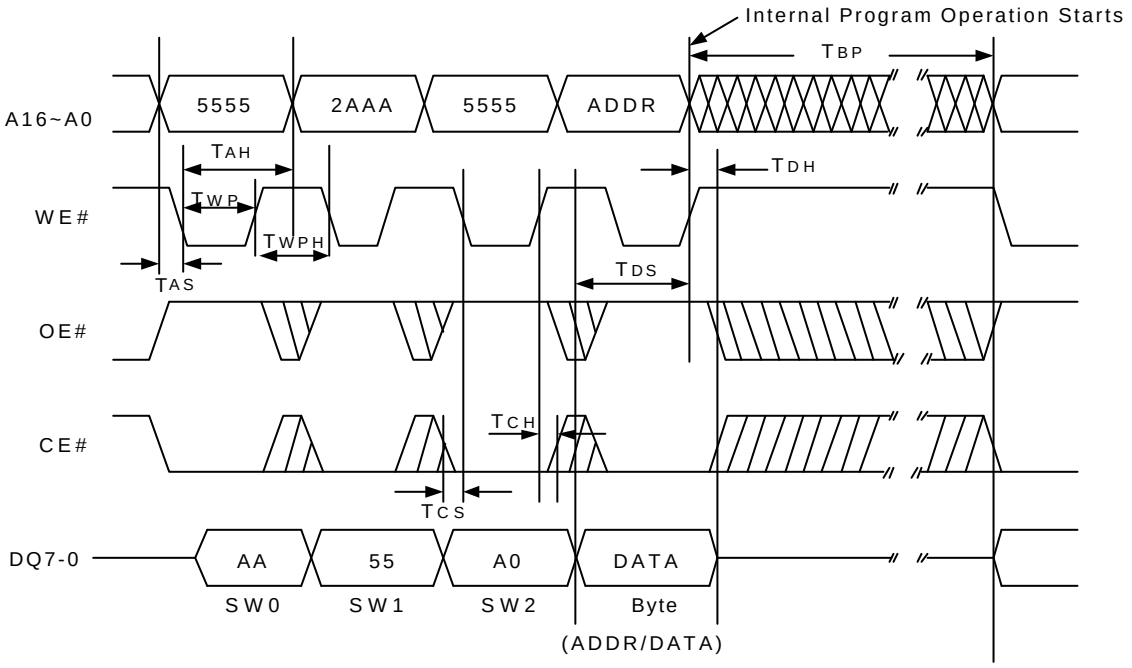



**Figure 2. WE# Controlled Program Cycle Timing Diagram**

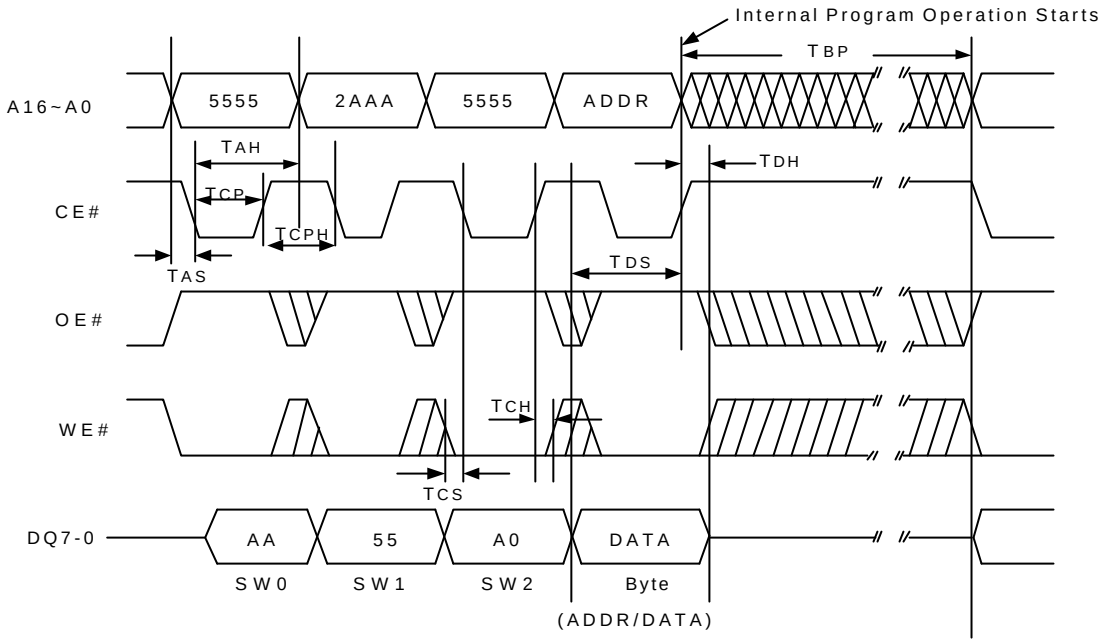



**Figure 3. CE# Controlled Program Cycle Timing Diagram**

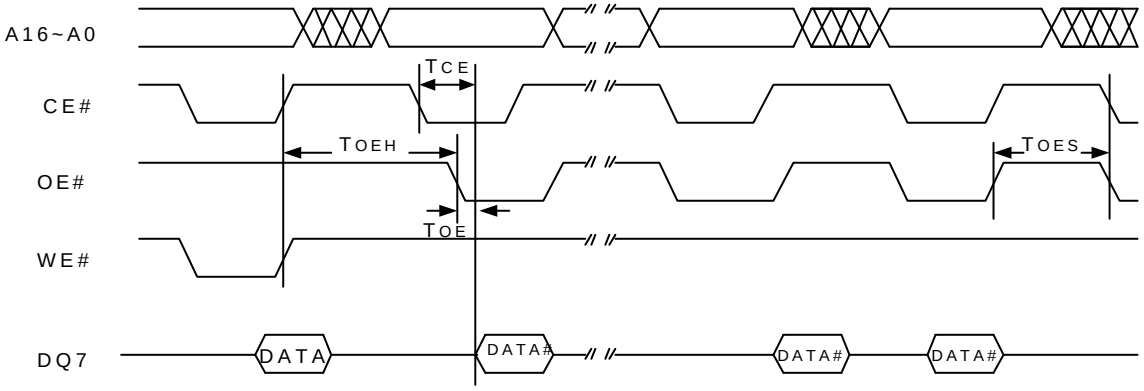



**Figure 4. Data# Polling Timing Diagram**

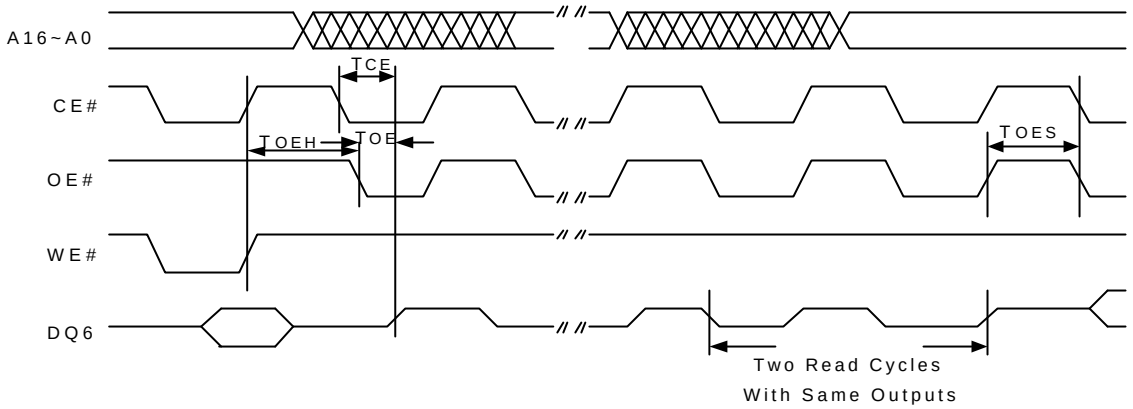
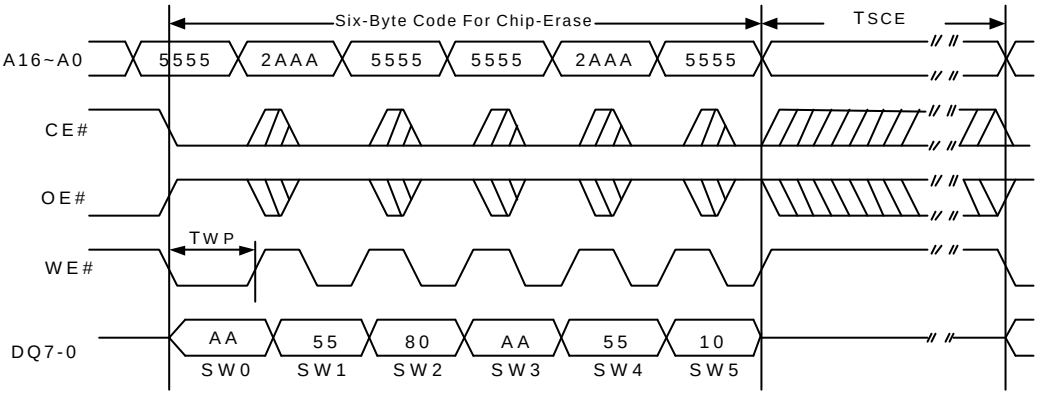
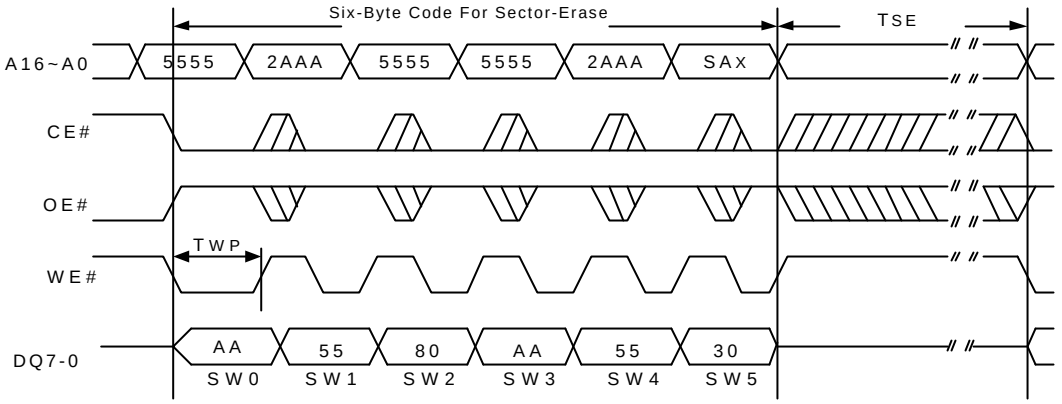



**Figure 5. Toggle Bit Timing Diagram**




Note: This device also supports CE# controlled Chip-Erase operation. The WE#and CE# signals are interchageable as long as minimum timings are met. (See Table 10)

**Figure 6. WE# Controlled Chip-Erase Timing Diagram**




Note: This device also supports CE# controlled Sector-Erase operation. The WE#and CE# signals are interchageable as long as minimum timings are met. (See Table 10)

SAX=Sector Address

X can be VIL or VIH, but no other value.

**Figure 7. WE# Controlled Sector-Erase Timing Diagram**

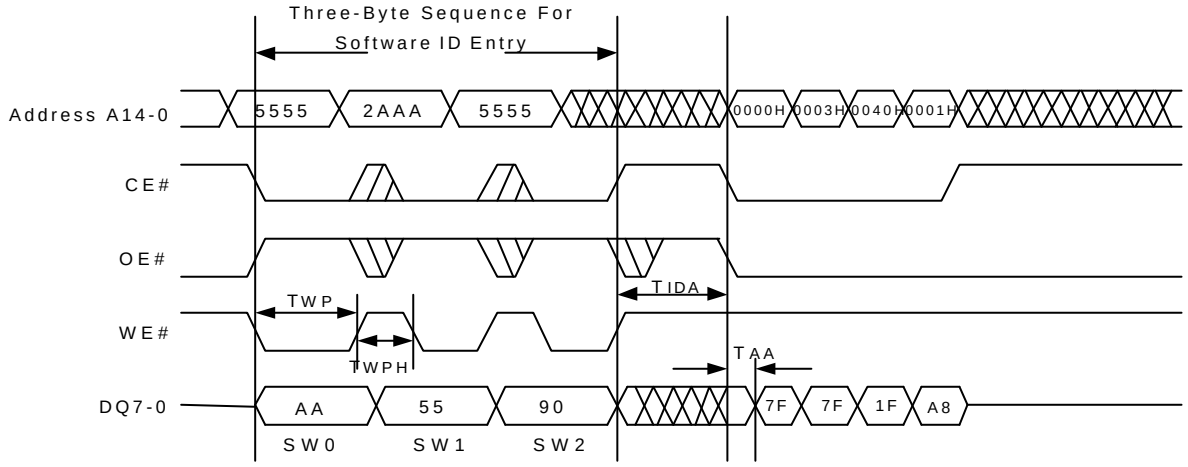



**Figure 8. Software ID Entry and Read**

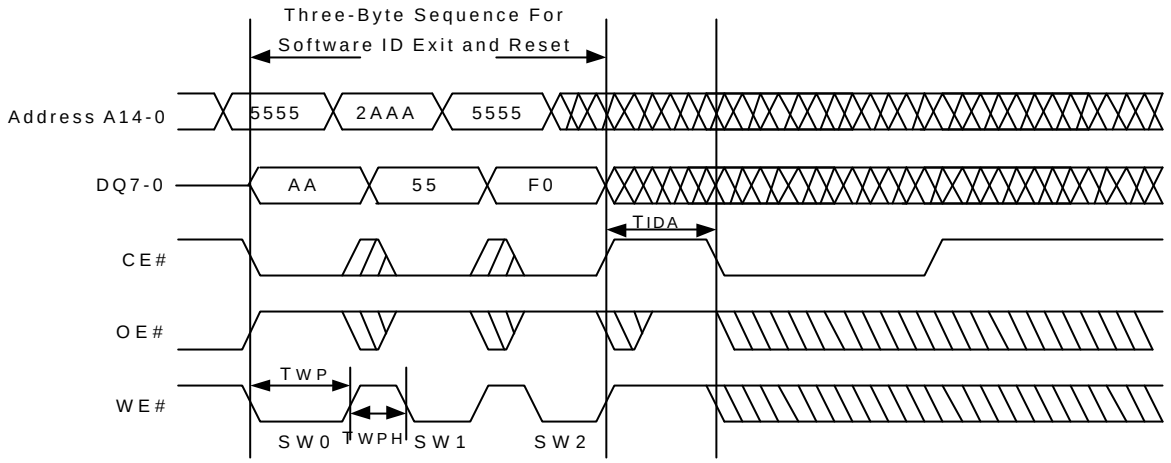
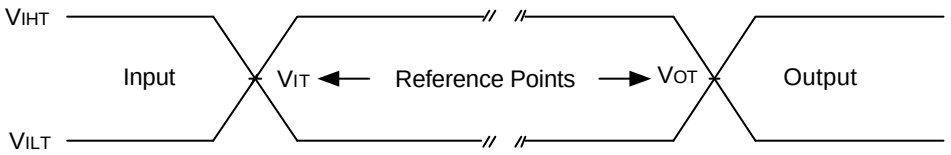



**Figure 9. Software ID Exit and Reset**




AC test inputs are driven at $V_{IHT}$ (0.9 $V_{DD}$) for a logic "1" and $V_{ILT}$(0.1 $V_{DD}$) for a logic "0". Measurement reference points for inputs and outpputs are $V_{IT}$(0.5 $V_{DD}$) and $V_{OT}$(0.5 $V_{DD}$). Input rise and fall times(10% - 90% ) are <5ns

Note: $V_{IT}$ = Vinput Test
$V_{OT}$ = Voutput Test
$V_{IHT}$ = Vinput HIGH Test
$V_{ILT}$ = Vinput LOW Test

**Figure 10. AC Input/Output Reference Waveforms**

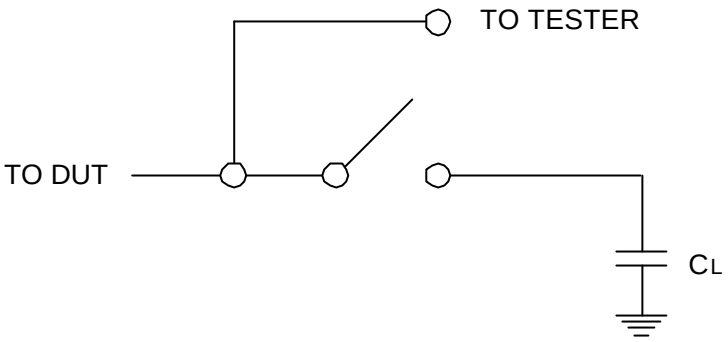



**Figure 11. A Test Load Example**

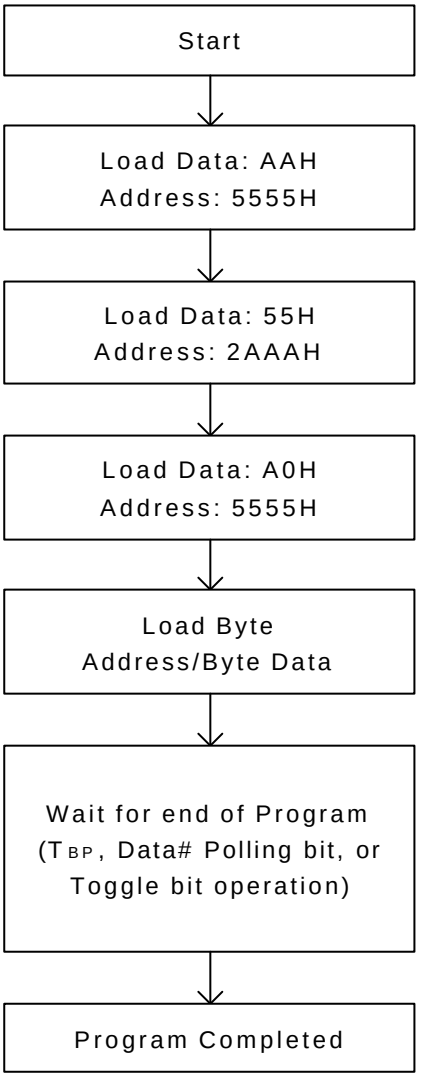



**Figure 12. Byte-Program Algorithm**





**Figure 20. Temporary Sector Unprotect Timing Diagram**

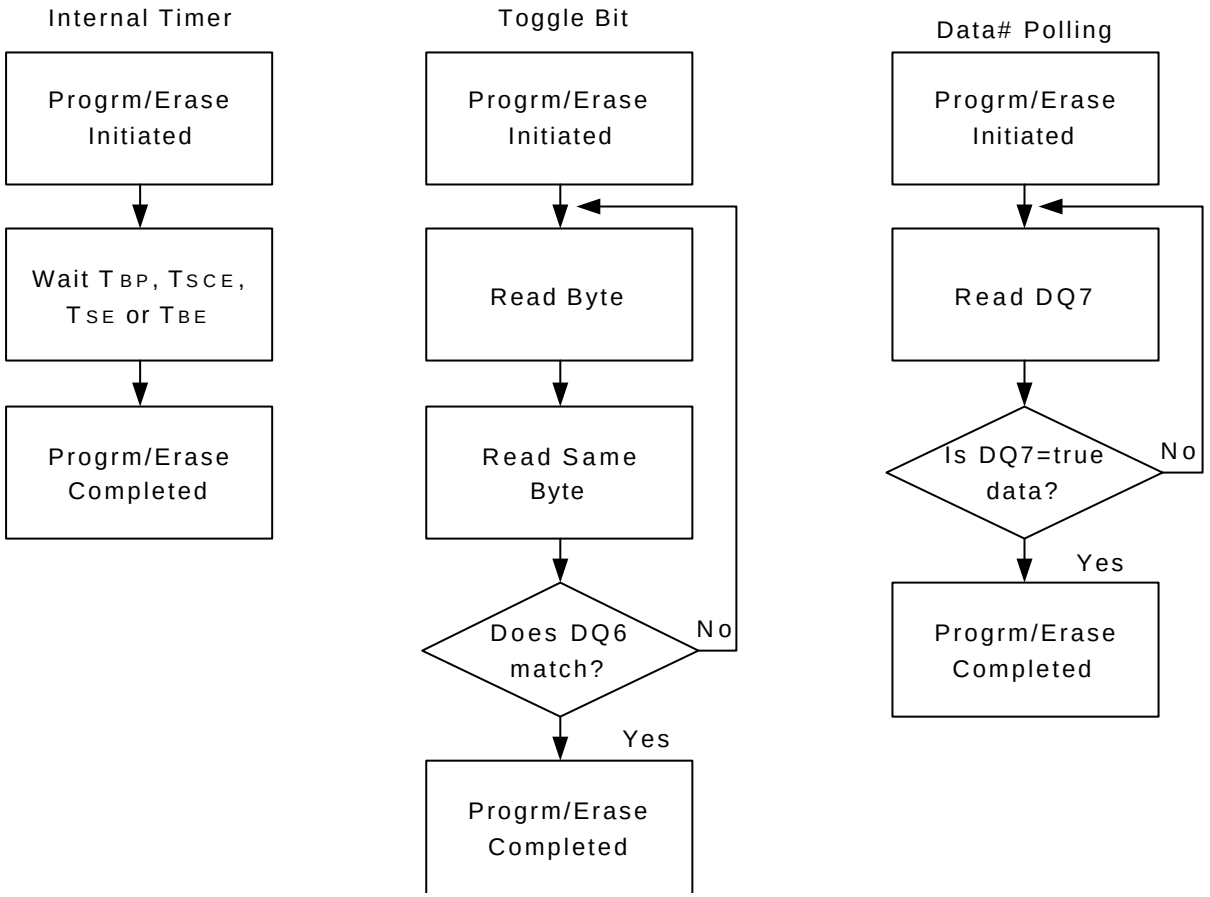
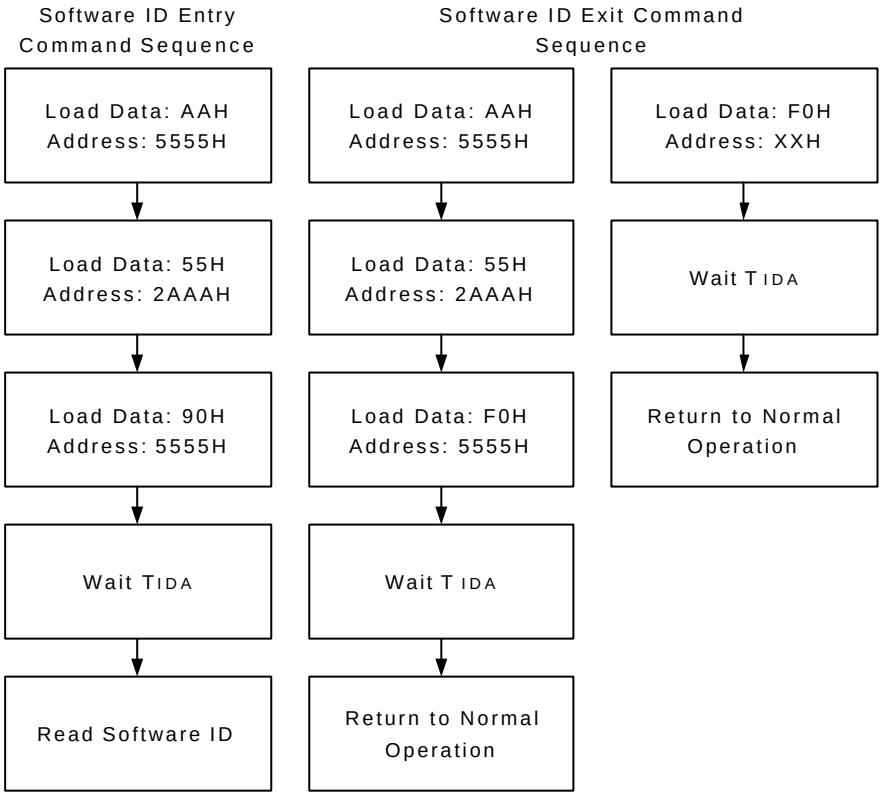
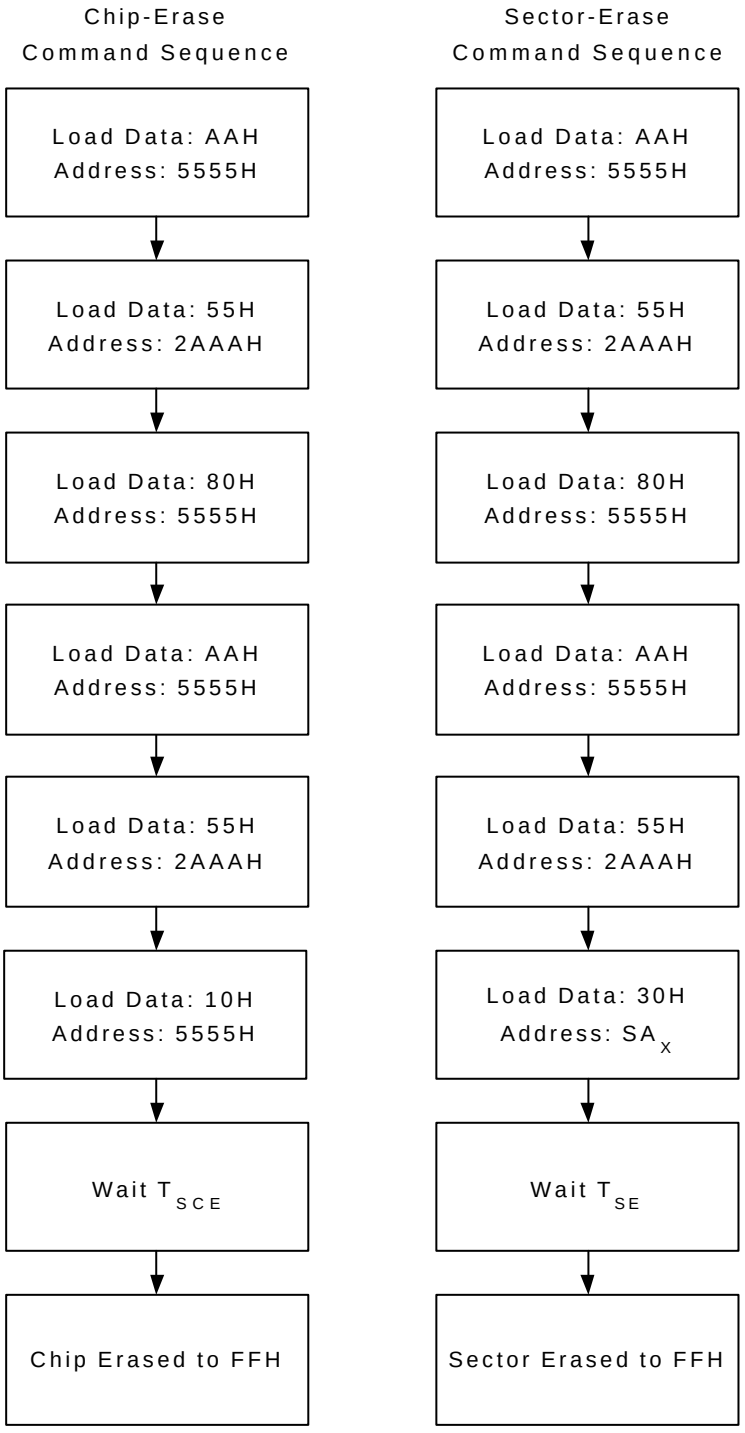



**Figure 13. Wait Options**




X can be VIL or VIH, but no other value.

**Figure 14. Software ID Command Flowcharts**




X can be $V_{IL}$ or $V_{IH}$, but no other value.

**Figure 15. Erase Command Sequence**