

◆ INTRODUCTION

AC780S is a LCD driver & controller LSI which is fabricated by low power CMOS technology. It can display 2 lines x 8 (5 x 8 dot format) characters or 1 lines x 8 (5 x 8 or 5 x 11 dot format) characters. It is ideal for multi-language application.

Standard code AC780S can support up to 240 fonts. Customized codes are available.

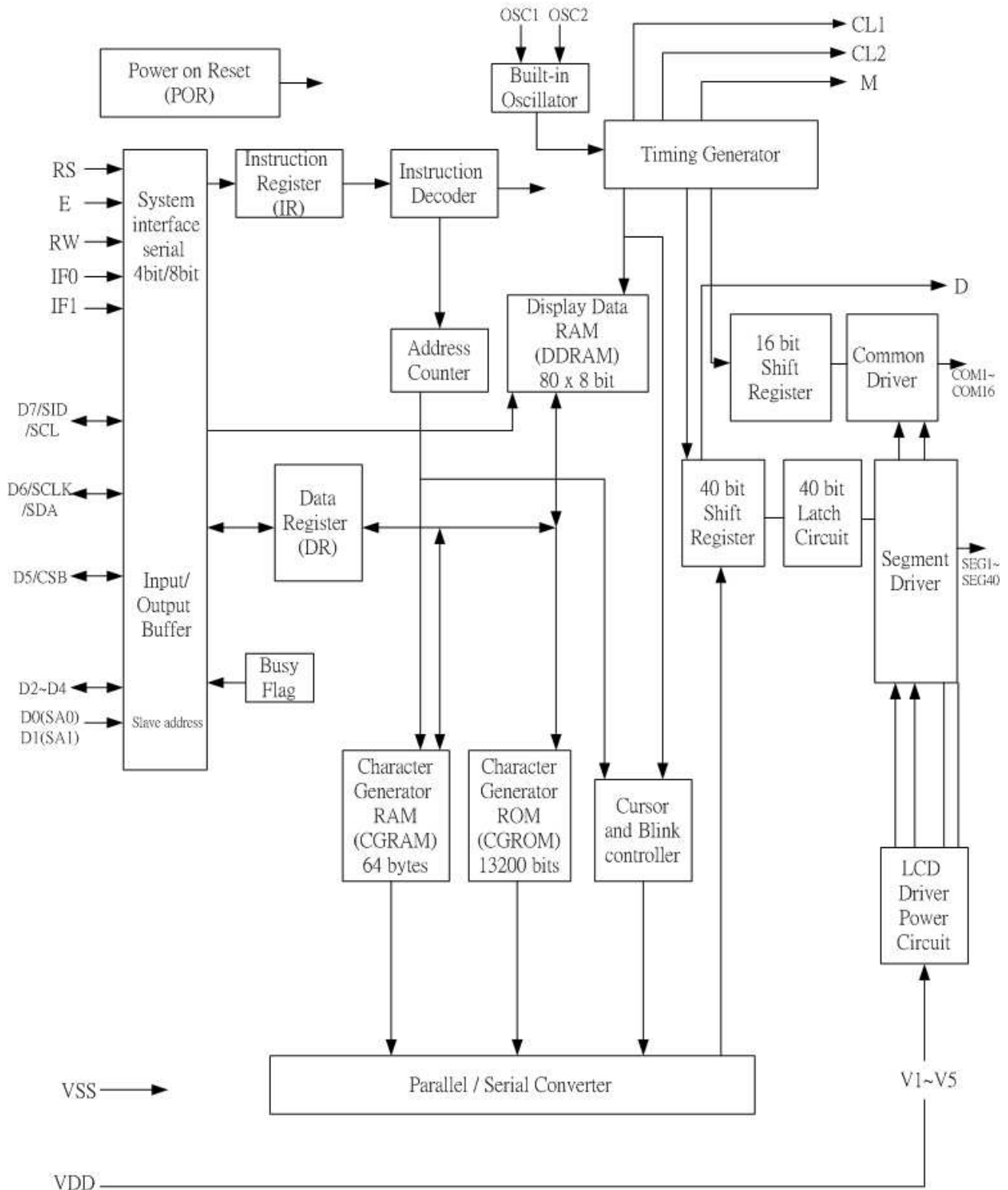
◆ FUNCTIONS

- Character type dot matrix LCD driver & controller
- Internal drivers: 16common and 40 segment for 2 line display, 1/16 duty (N=1, F=0).
11common and 40 segment for 1 line display, 1/11 duty (N=0, F=1).
8 common and 40 segment for 1 line display, 1/8 duty (N=0, F=0).
- Easy interface with 4-bit or 8-bit 68 series MPU or 4 lines SPI / IIC serial peripheral interface
- 5 x 8 dot matrix font or 5 x 11 dot matrix font
- Various instruction functions
- Automatic power on reset
- Double Frequency, half instruction time

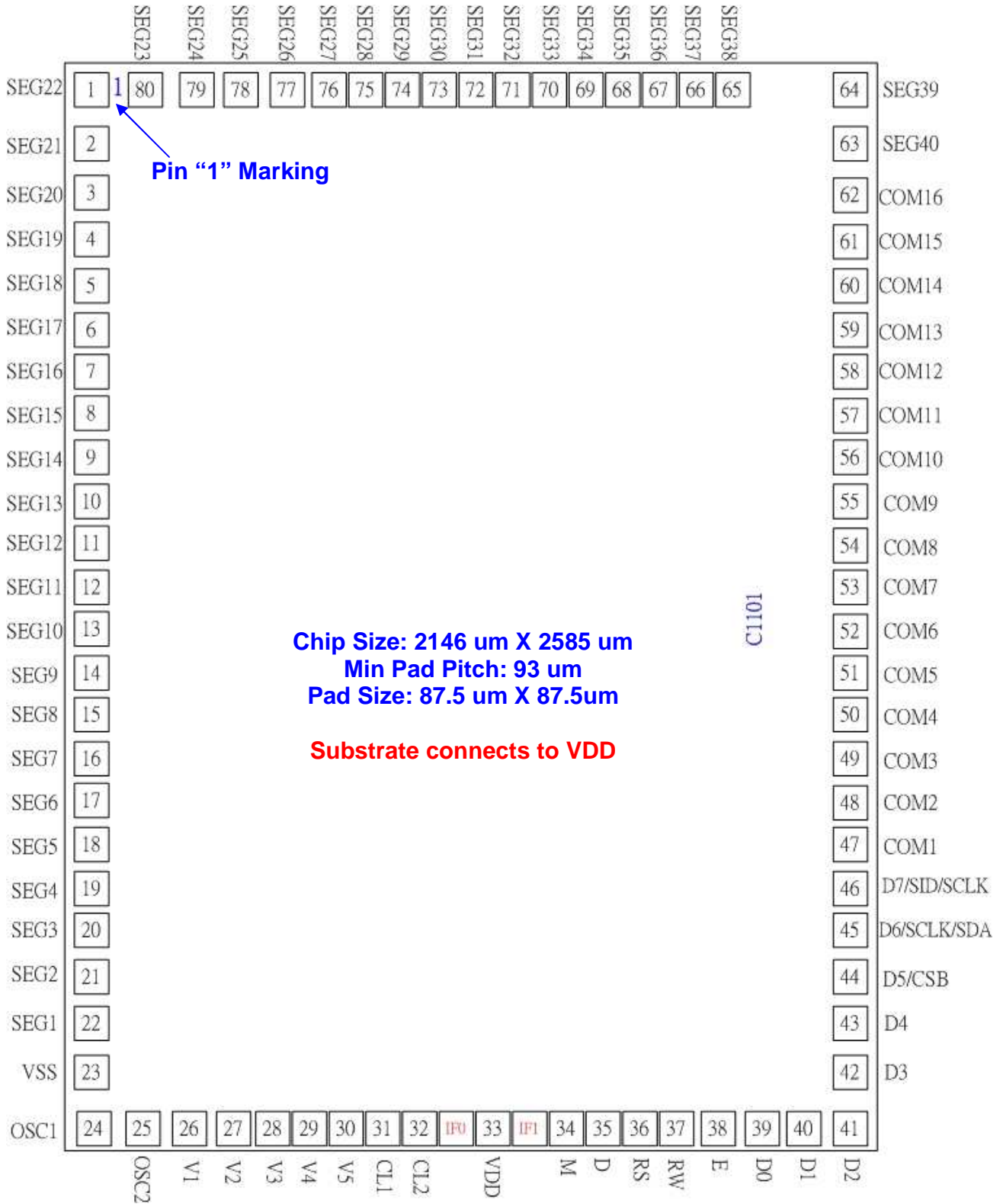
◆ FEATURES

- Internal Memory
- Character Generator ROM (CGROM): 13200 bits (240 characters: 5 x 8 dot or 5 x 11 dots)
- Character Generator RAM (CGRAM): 64 x 8 bits (8 characters x 5 x 8 dot or 4 characters x 5 x 11)
- Display Data RAM (DDRAM): 80 x 8 bits (80 characters max.)
- Power supply voltage range: 2.7 ~ 5.5 V (VDD)
- LCD Drive voltage range: 3.0 ~ 7.0V (VDD – V5)
- CMOS process
- Programmable duty cycle: 1/16, 1/11, 1/8 (refer to Table1)
- Low power consumption
- Bare chip available

◆ BLOCK DIAGRAM

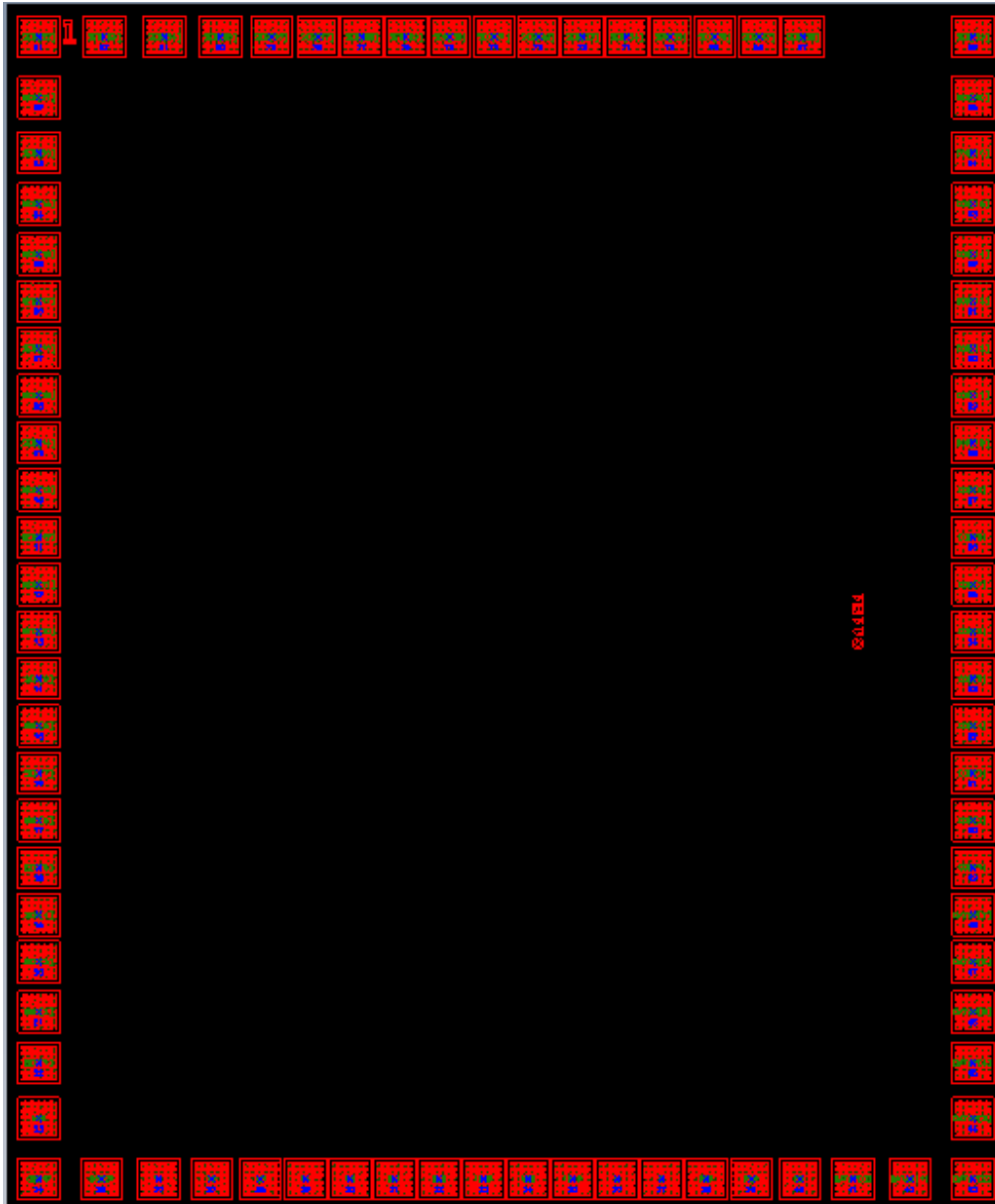


◆ PAD CONFIGURATION



◆ CHIP LAYOUT

PIN1 →



◆ PAD LOCATION

Unit: um

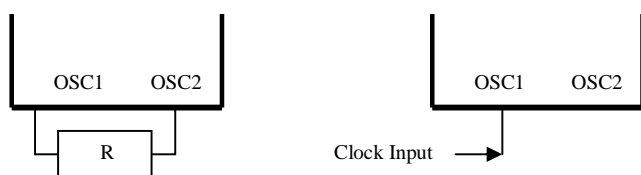
| Pad No. | Pin Name | X | Y | Pad No. | Pin Name | X | Y |
|---------|----------|--------|---------|---------|-------------|--------|---------|
| 1 | SEG[22] | -984.3 | 1203.8 | 40 | D1(SA1) | 851.8 | -1203.8 |
| 2 | SEG[21] | -984.3 | 1076.3 | 41 | D2 | 984.3 | -1203.8 |
| 3 | SEG[20] | -984.3 | 958.8 | 42 | D3 | 984.3 | -1076.6 |
| 4 | SEG[19] | -984.3 | 851.3 | 43 | D4 | 984.3 | -959.1 |
| 5 | SEG[18] | -984.3 | 746.1 | 44 | D5(CSB) | 984.3 | -851.6 |
| 6 | SEG[17] | -984.3 | 646.6 | 45 | D6/SCLK/SDA | 984.3 | -746.4 |
| 7 | SEG[16] | -984.3 | 547.1 | 46 | D7/SID/SCLK | 984.3 | -646.9 |
| 8 | SEG[15] | -984.3 | 447.6 | 47 | COM[1] | 984.3 | -547.4 |
| 9 | SEG[14] | -984.3 | 348.1 | 48 | COM[2] | 984.3 | -447.9 |
| 10 | SEG[13] | -984.3 | 248.6 | 49 | COM[3] | 984.3 | -348.4 |
| 11 | SEG[12] | -984.3 | 149.1 | 50 | COM[4] | 984.3 | -248.9 |
| 12 | SEG[11] | -984.3 | 49.6 | 51 | COM[5] | 984.3 | -149.4 |
| 13 | SEG[10] | -984.3 | -49.9 | 52 | COM[6] | 984.3 | -49.9 |
| 14 | SEG[9] | -984.3 | -149.4 | 53 | COM[7] | 984.3 | 49.6 |
| 15 | SEG[8] | -984.3 | -248.9 | 54 | COM[8] | 984.3 | 149.1 |
| 16 | SEG[7] | -984.3 | -348.4 | 55 | COM[9] | 984.3 | 248.6 |
| 17 | SEG[6] | -984.3 | -447.9 | 56 | COM[10] | 984.3 | 348.1 |
| 18 | SEG[5] | -984.3 | -547.4 | 57 | COM[11] | 984.3 | 447.6 |
| 19 | SEG[4] | -984.3 | -646.9 | 58 | COM[12] | 984.3 | 547.1 |
| 20 | SEG[3] | -984.3 | -746.4 | 59 | COM[13] | 984.3 | 646.6 |
| 21 | SEG[2] | -984.3 | -851.6 | 60 | COM[14] | 984.3 | 746.1 |
| 22 | SEG[1] | -984.3 | -959.1 | 61 | COM[15] | 984.3 | 851.3 |
| 23 | VSS | -984.3 | -1076.6 | 62 | COM[16] | 984.3 | 958.8 |
| 24 | OSC1 | -984.3 | -1203.8 | 63 | SEG[40] | 984.3 | 1076.3 |
| 25 | OSC2 | -851.8 | -1203.8 | 64 | SEG[39] | 984.3 | 1203.8 |
| 26 | V1 | -731.9 | -1203.8 | 65 | SEG[38] | 626.4 | 1203.8 |
| 27 | V2 | -619.4 | -1203.8 | 66 | SEG[37] | 533.4 | 1203.8 |
| 28 | V3 | -516.9 | -1203.8 | 67 | SEG[36] | 440.4 | 1203.8 |
| 29 | V4 | -422.6 | -1203.8 | 68 | SEG[35] | 347.4 | 1203.8 |
| 30 | V5 | -328.7 | -1203.8 | 69 | SEG[34] | 254.4 | 1203.8 |
| 31 | CL1 | -234.8 | -1203.8 | 70 | SEG[33] | 161.4 | 1203.8 |
| 32 | CL2 | -140.9 | -1203.8 | 71 | SEG[32] | 68.4 | 1203.8 |
| | IF0 | -47.0 | -1203.8 | 72 | SEG[31] | -24.6 | 1203.8 |
| 33 | VDD | 47.0 | -1203.8 | 73 | SEG[30] | -117.6 | 1203.8 |
| | IF1 | 140.9 | -1203.8 | 74 | SEG[29] | -210.6 | 1203.8 |
| 34 | M | 234.8 | -1203.8 | 75 | SEG[28] | -303.6 | 1203.8 |
| 35 | D | 328.7 | -1203.8 | 76 | SEG[27] | -396.6 | 1203.8 |
| 36 | RS | 422.6 | -1203.8 | 77 | SEG[26] | -494.2 | 1203.8 |
| 37 | RW | 516.9 | -1203.8 | 78 | SEG[25] | -601.7 | 1203.8 |
| 38 | E | 619.4 | -1203.8 | 79 | SEG[24] | -719.2 | 1203.8 |
| 39 | D0(SA0) | 731.9 | -1203.8 | 80 | SEG[23] | -846.7 | 1203.8 |

◆ PAD DESCRIPTION

| PAD | INPUT/OUTPUT | DESCRIPTION | | INTERFACE |
|------------|--------------|--------------------|---|---|
| VDD | - | Power supply | 2.7V ~ 5.5V | Power supply |
| VSS | | | 0V | |
| V1-V5 | | | Bias voltage level for LCD driving | |
| SEG1-SEG40 | O | Segment output | Segment signal output for LCD drive | LCD |
| COM1-COM16 | O | Common output | Common signal output for LCD drive | LCD |
| OSC1 | I | Oscillator | When oscillation is performed, a resistor must be connected externally. OSC1 also can be the external clock input pin when external clock mode used, OSC2 keep open while external clock input mode. | External Clock input pin (OSC1) Reference Note |
| OSC2 | O | Oscillator | | |
| RS | I | Register select | In bus mode, used as register selection input. When RS = "High", Date register is selected. When RS = "Low", Instruction register is selected. | MPU |
| E | I | Read. Write enable | In bus mode, used as read write enable signal. | MPU |
| RW | I | Read. Write | In bus mode, used as read / write selection input. When RW = "High", read operation. When RW = "Low", write operation. | MPU |

Note:

- VDD >= V1 >= V2 >= V3 >= V4 >= V5 must be maintained
- Two clock input mode

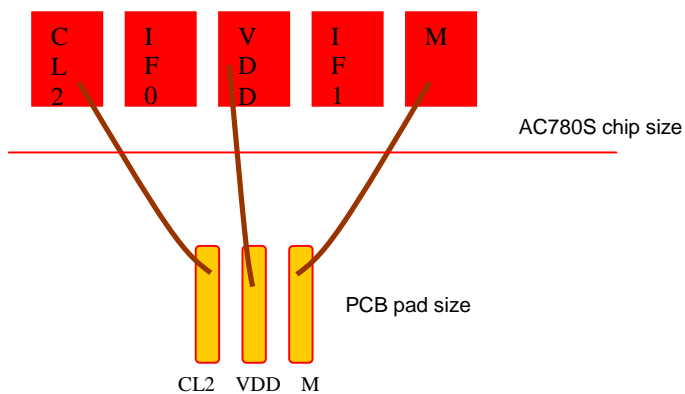


| PAD | INPUT/OUTPUT | DESCRIPTION | | INTERFACE |
|---------------|--------------|--|--|-----------|
| DB0-DB3 | I/O | Data bus 0~3/Slave address for IIC(DB1,DB0) | In 8-bit bus mode, used as low order bi-directional data bus. During 4-bit bus mode or serial mode, open these pins. | MPU |
| | | | In IIC interface ,DB1(SA1) and DB0(SA0) are used for Slave address, must be connect to VDD or VSS. | |
| DB4 | I/O | Data bus 4 | In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. | MPU |
| DB5/CSB | I/O | Data bus 5/ Chip select | In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. In 4-SPI serial mode, used as chip selection input. In I2C serial mode, used as chip selection input. When CSB = "Low", selected When CSB = "High", not selected. (Low access enable) | MPU |
| DB6/SCLK /SDA | I/O | Data bus 6/ Serial clock input/Serial input data | In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. | MPU |
| | | | When the 4-Line serial interface selected: SCLK: serial clock input | |
| | | | When the IIC interface selected: SDA: serial input data | |
| DB7/SID /SCL | I/O | Data bus 7/ Serial data input/Serial clock input | In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output. | MPU |
| | | | When the 4-Line serial interface selected: SID: serial data input | |
| | | | When the IIC interface selected: SCL: serial clock input | |

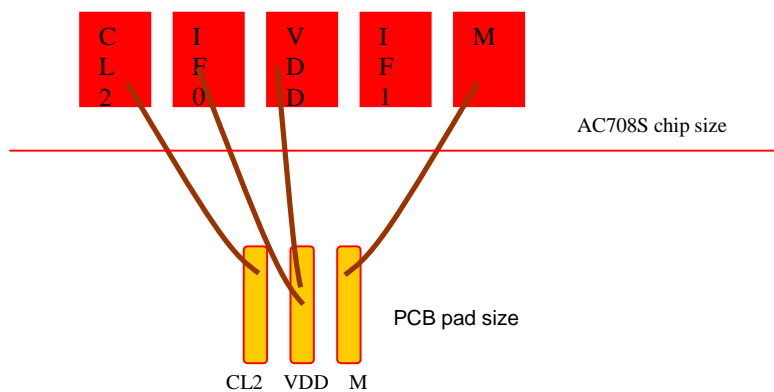
| PAD | INPUT/OUTPUT | DESCRIPTION | | | INTERFACE | | | | | | | | | | | | | |
|----------------|--------------|-----------------------|---|----------------|-----------|-----|-----|-----------|------|------|------|------|----------------|-----|----------------|------|------|-----|
| IF1,IF0 | I | Interface select pins | <table border="1"> <thead> <tr> <th>IF1</th> <th>IF0</th> <th>Interface</th> </tr> </thead> <tbody> <tr> <td>open</td> <td>open</td> <td>6800</td> </tr> <tr> <td>open</td> <td>Bonding to VDD</td> <td>IIC</td> </tr> <tr> <td>Bonding to VDD</td> <td>open</td> <td>4SPI</td> </tr> </tbody> </table> | | | IF1 | IF0 | Interface | open | open | 6800 | open | Bonding to VDD | IIC | Bonding to VDD | open | 4SPI | MPU |
| | | | IF1 | IF0 | Interface | | | | | | | | | | | | | |
| | | | open | open | 6800 | | | | | | | | | | | | | |
| | | | open | Bonding to VDD | IIC | | | | | | | | | | | | | |
| Bonding to VDD | open | 4SPI | | | | | | | | | | | | | | | | |
| M | O | Extension driver | Output the alternating signal to convert LCD driver waveform to A.C. | | | | | | | | | | | | | | | |
| D | O | Extension driver | Outputs extension driver data (the 41 st dot's area) | | | | | | | | | | | | | | | |
| CL1 | O | Extension driver | Extension driver latch clock | | | | | | | | | | | | | | | |
| CL2 | O | Extension driver | Extension driver shift clock | | | | | | | | | | | | | | | |

◆ Interface select bonding Note for IF1,IF0

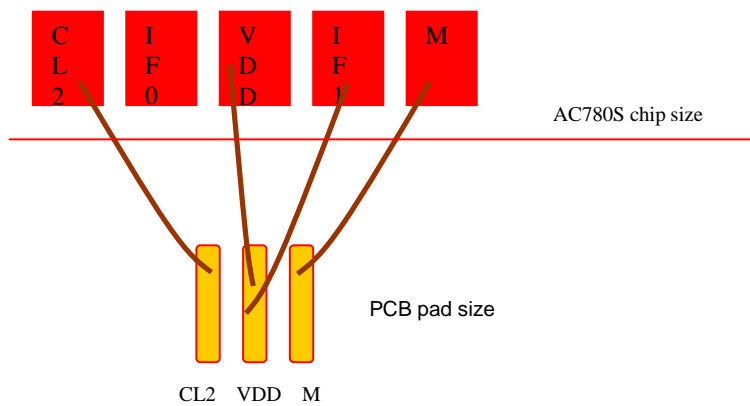
1. 6800 series MPU interface (IF0=open 、IF1=open)



2. IIC Interface Select (IF0=VDD 、IF1=open)



3. 4SPI Interface Select (IF0=open 、IF1=VDD)



◆ FUNCTION DESCRIPTION

● SYSTEM INTERFACE (Parallel 8-bit bus and 4-bit bus)

This chip has all four kinds interface type with MPU: IIC, 4SPI, 4-bit bus and 8-bit bus. Serial and parallel buses (4-bit/8-bit) are selected by IF1 and IF0 input pins, and 4-bit bus and 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR); the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.

So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

IR: Instruction Register.

DR: Data Register.

| RS | R/W | Operation |
|----|-----|---|
| 0 | 0 | Instruction write operation (MPU writes Instruction code into IR) |
| 0 | 1 | Read busy flag (DB7) and address counter (DB0 - DB6) |
| 1 | 0 | Data write operation (MPU writes data into DR) |
| 1 | 1 | Data read operation (MPU reads data from DR) |

● BUSY FLAG (BF) (only support parallel 8-bit bus and 4-bit bus)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R / W = High (Read Instruction Operation); through DB7 before executing the next instruction, be sure that BF is not High.

● DISPLAY DATA RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to Figure 1.)

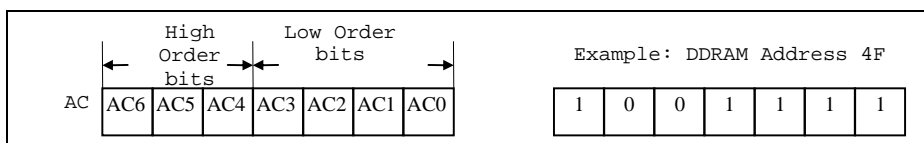


Figure 1 DDRAM Address

➤ **1-line display (N = 0) (Figure 2)**

When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the AC780S, 8 characters are displayed. See Figure 3.
 When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

| | | | | | | | | | | |
|--------------------------|----|----|----|----|----|----|-------|----|----|----|
| Display Position (Digit) | 1 | 2 | 3 | 4 | 5 | 6 | | 78 | 79 | 80 |
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | | 4D | 4E | 4F |

Figure 2 1-Line Display

| | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|
| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 |
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 |
| For Shift Right | 4F | 00 | 01 | 02 | 03 | 04 | 05 | 06 |

Figure 3 1-Line by 8-Character Display Example

➤ **2-line display (N = 1) (Figure 4)**

Case 1: When the number of display characters is less than 40 x 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the AC780S is used, 8 characters x 2 lines are displayed. See Figure 5.

When display shift operation is performed, the DDRAM address shifts. See Figure 5.

| | | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|-------|----|----|----|
| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | | 38 | 39 | 40 |
| DDRAM Address (hexadecimal) | 00 | 01 | 02 | 03 | 04 | 05 | | 25 | 26 | 27 |
| | 40 | 41 | 42 | 43 | 44 | 45 | | 65 | 66 | 67 |

Figure 4 2-Lines Display

| | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|
| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 |
| | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
| For Shift Right | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 |
| | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 |

Figure 5 2-Lines by 8-Character Display Example

Case 2: For a 16-character x 2-line display, the AC780S can be extended using one 40-output extension driver. See Figure 6.

When display shift operation is performed, the DDRAM address shifts. See Figure 6.

Figure 6 2-Lines by 16-Character Display Example

| | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F |
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 |
| | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 |
| For Shift Right | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E |
| | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E |

- **TIMING GENERATION CIRCUIT**

Timing generation circuit generates clock signals for the internal operations.

- **ADDRESS COUNTER (AC)**

Address Counter (AC) stores DDRAM/CGRAM address, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0-DB6

- **CURSOR/BLINK CONTROL CIRCUIT**

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

- **LCD DRIVER CIRCUIT**

LCD Driver circuit has 16 common and 40 segment signals for 2-line display (N=1) or 8 common and 40 segments for 1-line display (N=0) for LCD driving.

Data from CGRAM/CGROM is transferred to 40 bit segment latches serially, and then it is stored to 40 bit shift latch.

- **CGROM (CHARACTER GENERATOR ROM)**

CGROM has 240 characters (5 x 8 dot)

- **CGRAM (CHARACTER GENERATOR RAM)**

CGRAM has up to 5 × 8 dots 8 characters. By writing font data to CGRAM, user defined character can be used (refer to Table 2).

➤ 5 x 8 dots Character Pattern

Table 2. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

| Character Code (DDRAM data) | | | | | | | | CGRAM Address | | | | CGRAM Data | | | | | | | | Pattern Number | | |
|-----------------------------|----|----|----|----|----|----|----|---------------|----|----|----|------------|----|----|----|----|----|----|----|----------------|----|-----------|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A5 | A4 | A3 | A2 | A1 | A0 | P7 | P6 | P5 | P4 | P3 | P2 | | P1 | P0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | 0 | 1 | 1 | 1 | 0 | Pattern 1 |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 0 | 0 | 1 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 0 | 1 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 0 | 1 | 1 | - | - | - | 1 | 1 | 1 | 1 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 1 | 0 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 1 | 0 | 1 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 1 | 1 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 0 | 0 | 0 | - | - | - | 1 | 1 | 1 | - | - | - | 0 | 0 | 0 | 0 | 0 | |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | X | X | X | 1 | 0 | 0 | 0 | 1 | Pattern 8 |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 0 | 0 | 1 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 0 | 1 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 0 | 1 | 1 | - | - | - | 1 | 1 | 1 | 1 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 1 | 0 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 1 | 0 | 1 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 1 | 1 | 0 | - | - | - | 1 | 0 | 0 | 0 | 1 | |
| - | - | - | - | - | 1 | 1 | 1 | - | - | - | 1 | 1 | 1 | - | - | - | 0 | 0 | 0 | 0 | 0 | |

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 2, CGRAM character patterns are selected when character code bits 4 to 7 are all 0 and MW=0. However, since character code bit 3 has no effect, the H display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.
“-”: Indicates no effect.

◆ INSTRUCTION DESCRIPTION

Instruction Table:

| Instruction | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Description | Description Time (540KHz) |
|-----------------------------------|----|----|------------|-----|-----|-----|-----|-----|-----|-----|---|---------------------------|
| Read display data | 1 | 1 | Read data | | | | | | | | Read data from DDRAM/CGRAM | 18.5us |
| Write display data | 1 | 0 | Write data | | | | | | | | Write data into DDRAM/CGRAM | 18.5us |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM, and set DDRAM address to "00H" from AC | 0.76ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 0.76ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Assign cursor moving direction and specify display shift. These operations are performed during data read and write. I/D="1": increment I/D="0": decrement | 18.5us |
| Display ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Set Display /Cursor/Blink On/OFF D="1": display on D="0": display off C="1": cursor on C="0": cursor off B="1": blink on B="0": blink off | 18.5us |
| Cursor or Display shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | Cursor or display shift S/C="1": display shift S/C="0": cursor shift R/L="1": shift to right R/L="0": shift to left | 18.5us |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | F | X | X | Set Interface Data Length DL= 8-bit interface/ 4-bit interface N = 2-line/1-line display F= 5x8 Font Size / 5x11Font Size | 18.5us |
| Set CGRAM Address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter | 18.5us |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter | 18.5us |
| Read Busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Can know internal operation is ready or not by reading BF. The contents of address counter can also be read. BF="1": busy state BF="0": ready state | 0us |

Note : 1. When an MPU program with Busy Flag(DB7) checking is made, 1/2 FOSC (is necessary) for executing the next instruction by the " E " signal after the Busy Flag (DB7) goes to " Low ".

2. "X" Don't care

- **Clear Display**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status; namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

- **Return Home:**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X |

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. A content of DDRAM does not change.

- **Entry Mode Set:**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

Set the moving direction of cursor and display.

I/D: Increment/decrement of DDRAM address (cursor or blink)

I/D = 1: cursor/blink moves to right and DDRAM address is increased by 1.

I/D = 0: cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same as DDRAM, when read/write from or to CGRAM

S: Shift of entire display

When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed.

If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1": shift left, I/D = "0": shift right).

| S | I/D | Description |
|---|-----|--------------------------------|
| H | H | Shift the display to the left |
| H | L | Shift the display to the right |

● Display ON/OFF

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit.

D = 1: entire display is turned on.

D = 0: display is turned off, but display data is remained in DDRAM.

C: Cursor ON/OFF control bit.

C = 1: cursor is turned on.

C = 0: cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON/OFF control bit.

B = 1: cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 540 kHz frequency, blinking has 185 ms interval.

B = 0: blink is off.

● Cursor or Display Shift

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | - | - |

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data (refer to Table 4). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.

Note that display shift is performed simultaneously by the shift enable instruction. When displayed data is shifted repeatedly, all display lines shifted simultaneously. When display shift is performed, the contents of address counter are not changed.

Table 4. Shift Patterns According to S/C and R/L Bits

| S/C | R/L | Operation |
|-----|-----|---|
| 0 | 0 | Shift cursor to the left, address counter is decreased by 1 |
| 0 | 1 | Shift cursor to the right, address counter is increased by 1 |
| 1 | 0 | Shift all the display to the left, cursor moves according to the display |
| 1 | 1 | Shift all the display to the right, cursor moves according to the display |

● Function Set

| | | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 1 | DL | N | F | X | X |

DL: Interface data length control bit

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

IF using IIC and 4-SPI interface \ DL bit must be setting to "1"

N: Display line number control bit

When N = "Low", it means 1-line display mode.

When N = "High", 2-line display mode is set.

F: Display font type control bit

When F = "Low", it means 5 x 8 dots format display mode

When F = "High", 5 x11 dots format display mode.

| N | F | No. of Display Lines | Character Font | Duty Factor |
|---|---|----------------------|----------------|-------------|
| L | L | 1 | 5x8 | 1/8 |
| L | H | 1 | 5x11 | 1/11 |
| H | x | 2 | 5x8 | 1/16 |

● Set CGRAM Address

| | | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

● Set DDRAM Address

| | | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N=0), DDRAM address is from "00H" to "4FH"

In 2-line display mode (NW = 0), DDRAM address in the 1st line is from "00H" - "27H", and DDRAM address in the 2nd line is from "40H" - "67H".

- **Read Busy Flag and Address** (only support parallel 8-bit bus and 4 bit bus)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

This instruction shows whether AC780S is in internal operation or not. If the resultant BF is “high”, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

- **Write Data to RAM**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

- **Read Data from RAM** (only support parallel 8-bit bus and 4 bit bus)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

- **OUTLINE**

To overcome the speed difference between internal clock of AC780S and MPU clock, AC780S performs internal operation by storing control information to IR (Instruction Register) or DR (data Register). The internal operation is determined according to the signal from MPU, composed of read/write and data bus.

Instruction can be divided largely four kinds;

- AC780S function set instructions (set display methods, set data length, etc.)
- Address set instructions to internal RAM
- Data transfer instructions with internal RAM
- Others

The address of internal RAM is automatically increased or decreased by 1.

NOTE: During internal operation, Busy Flag (DB7) is read high. Busy Flag check must be preceded the next instruction.
Busy flag check must be proceeded the next instruction.
When an MPU program with Busy Flag (DB7) checking is made, $1/2 F_{osc}$ (is necessary) for executing the next instruction by the falling edge of the "E" signal after the Busy Flag (DB7) goes to "Low".

◆ INTERFACE WITH MPU

AC780S can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU.

In case of 4-bit bus mode, data transfer is performed by two times to transfer 1 byte data.

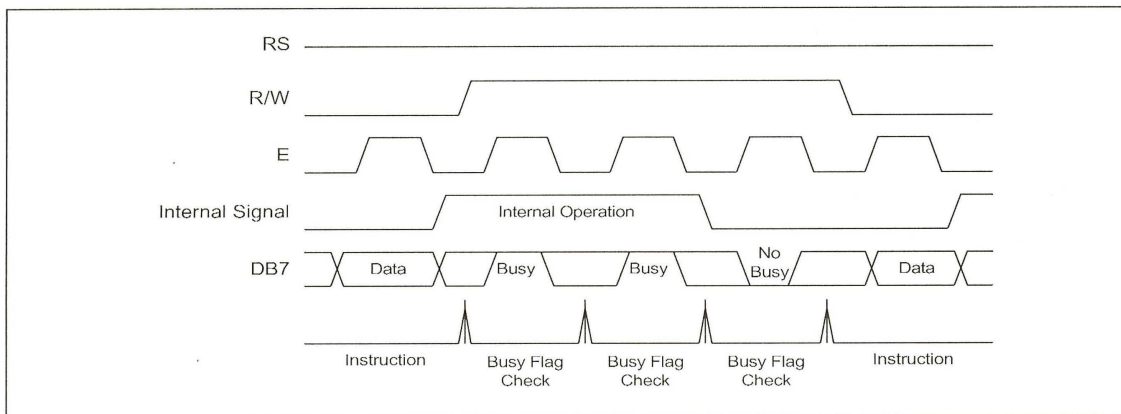
- When interfacing data lengths are 4-bit, only 4 ports, from DB4 - DB7, are used as data bus.
At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times. Busy Flag outputs "High" after the second transfer are ended.
- When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 - DB7.
- Interface is selected by IF1,IF0 pins (refer to **Bonding Note for IF1, IF0** on Page 10)

| IF1 | IF0 | Interface select |
|----------------|----------------|------------------|
| open | open | 6800 8/4 bit |
| open | Bonding to VDD | IIC |
| Bonding to VDD | open | 4-line SPI |

◆ INTERFACE WITH MPU IN BUS MODE

● Interface with 8-bit MPU

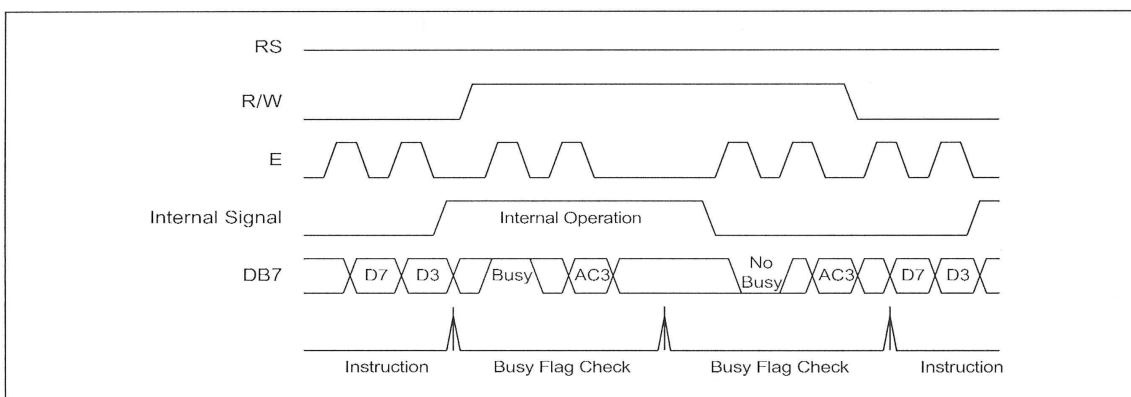
If 8-bits MPU is used, AC780S can connect directly with that. In this case, port E, RS, R/W and DB0 to DB7 need to interface each other. Example of timing sequence is shown below.



Example of 8-bit Bus Mode Timing Sequence

● Interface with 4-bit MPU

If 4-bit MPU is used, AC780S can connect directly with this. In this case, port E, RS, R/W and DB4 - DB7 need to interface each other. The transfer is performed by two times. Example of timing sequence is shown below.

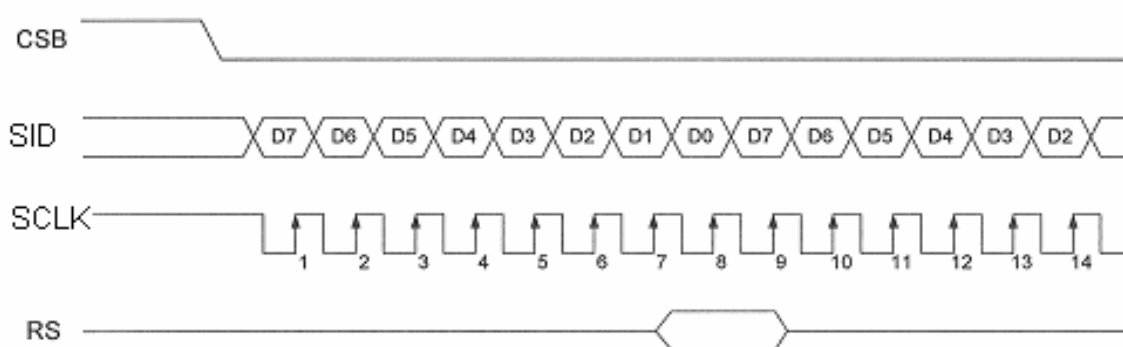


Example of 4-bit Bus Mode Timing Sequence

- For serial interface data, bus lines (DB5 to DB7) are used. 4-Line SPI

If 4-Pin SPI mode is used, CSB (DB5), SID (DB7), SCLK (DB6), and RS are used. They are chip selection; serial input data, serial clock input, and data/instruction section, relatively. The example of timing sequence is shown below.

➤ Example of timing sequence



Note: Following is the master SPI clock mode of MPU.

Idle state for clock is a high level › data transmitted on rising edge of SCLK, and data is hold during low level.

- For serial interface data, bus lines (DB5(CSB) · DB6(SDA) and DB7(SCL)) are used. IIC interface

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.

The IIC Interface is for bi-directional, two-line communication between different ICs or modules. Serial data line SDA (DB6) and a Serial clock line SCL (DB7) must be connected to a positive supply via a pull-up resistor.

Data transfer may be initiated only when the bus is not busy.

*The CSB (DB5) Pin must be setting to "VSS".

* When IIC interface is selected, the DL register must be set to "1".

➤ BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.9.1

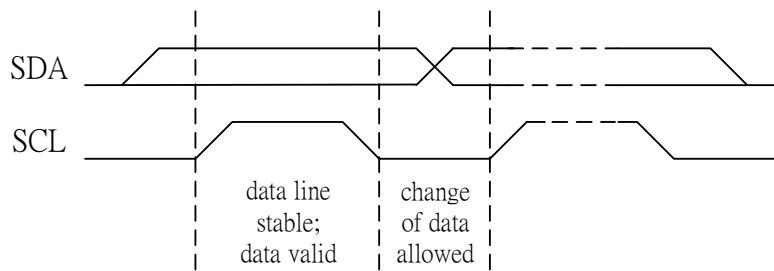


Fig .9.1 Bit transfer

➤ START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.9.2

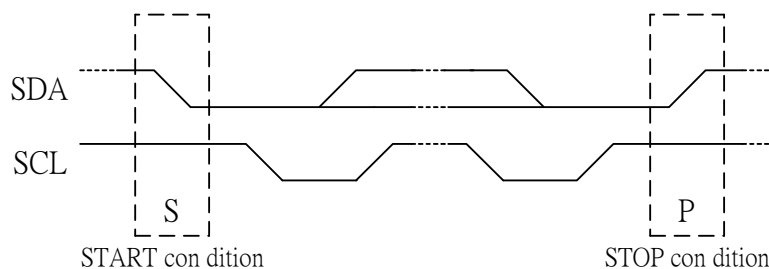


Fig .9.2 Definition of START and STOP conditions

➤ SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.9.3

- Transmitter: the device, which sends the data to the bus
- Receiver: the device, which receives the data from the bus
- Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

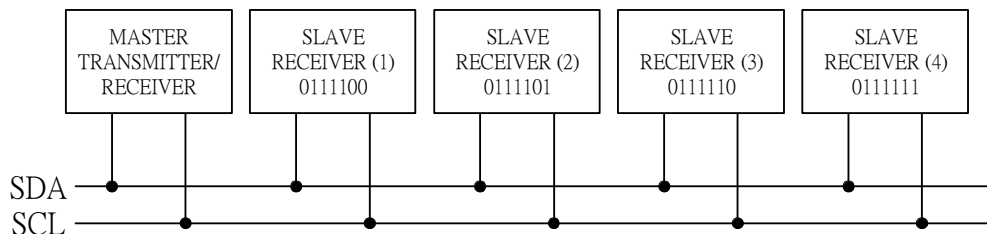


Fig .9.3 System configuration

➤ ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge after the reception of each byte. A master receiver must also generate an Acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the Acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an Acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Fig.9.4

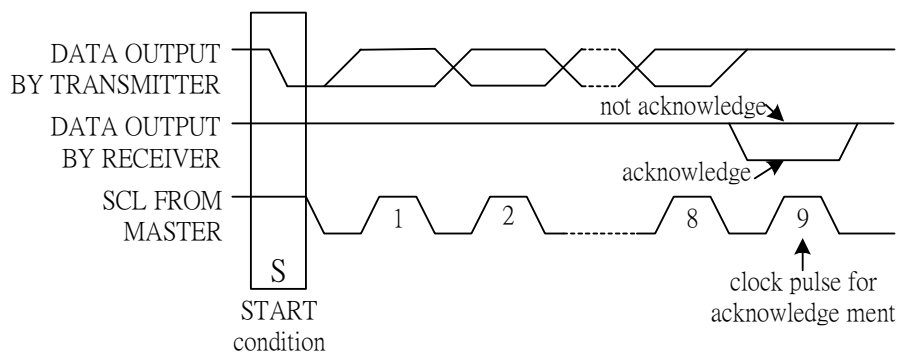


Fig .9.4 Acknowledgement on the 2-line Interface

IIC Interface protocol

The AC780S supports command, data write addressed slaves on the bus.

Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first.

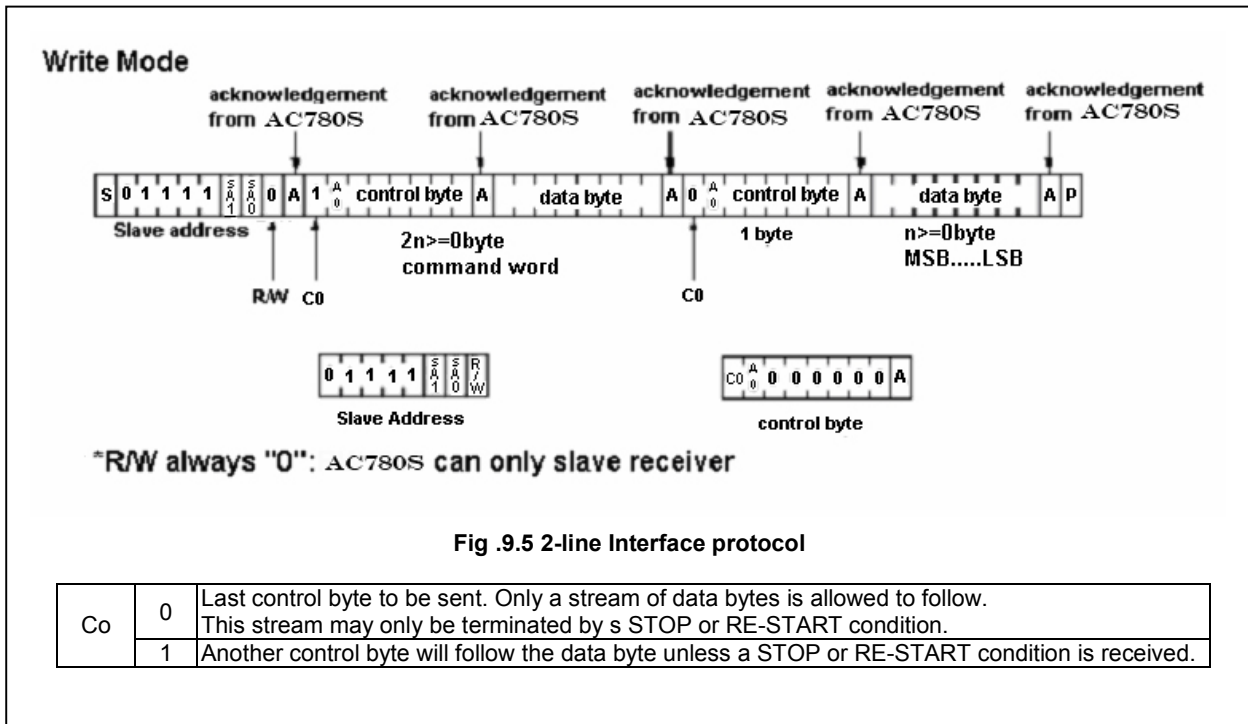
Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the AC780S. The least significant bit of the slave address is set by connecting the input SA0 (DB0) and SA1 (DB1) to either logic 0 (VSS) or logic 1 (VDD).

The IIC Interface protocol is illustrated in Figure.9.5

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

A command word consists of a control byte, which defines Co and A0, plus a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended AC780S device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC interface-bus master issues a STOP condition (P). If no acknowledgement is generated by the master after a byte, the driver stops transferring data to the master.



◆ INITIALIZING**● INITIALIZING BY INTERNAL RESET CIRCUIT**

When the power is turned on, AC780S is initialized automatically by power on reset circuit.

During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High"(busy state) to the end of initialization.

● Clear Display Instruction

Write "20H" to all DDRAM

● Set Functions Instruction

DL = 1: 8-bit bus mode

N = 0: 1-line display

F = 0: 5 x 8 dot character font

● Display ON/OFF Instruction

D = 0: Display OFF

C = 0: Cursor OFF

B = 0: Blink OFF

● Set Entry Mode Instruction

I/D = 1: Increment by 1

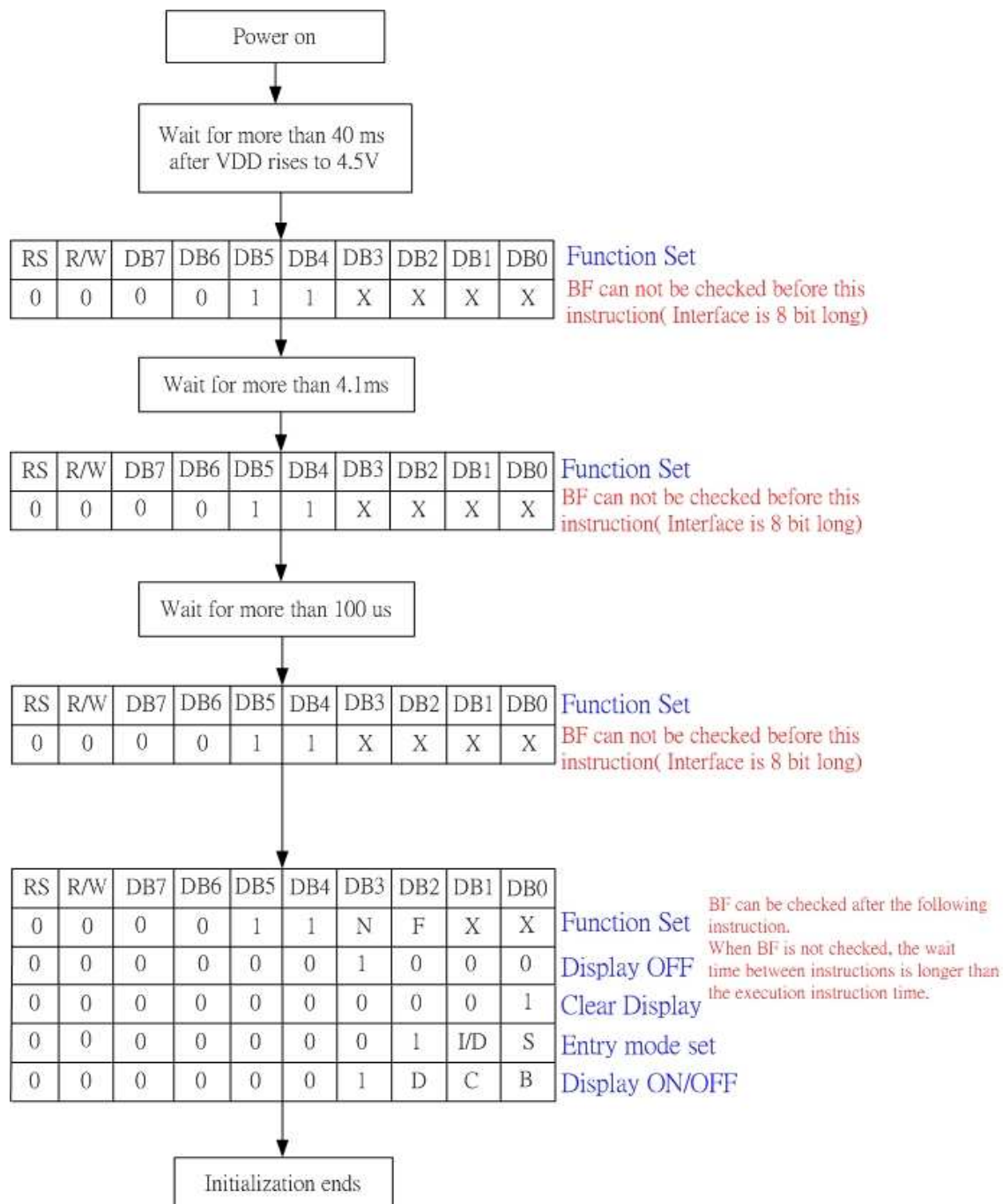
S = 0: No entire display shift

Note:

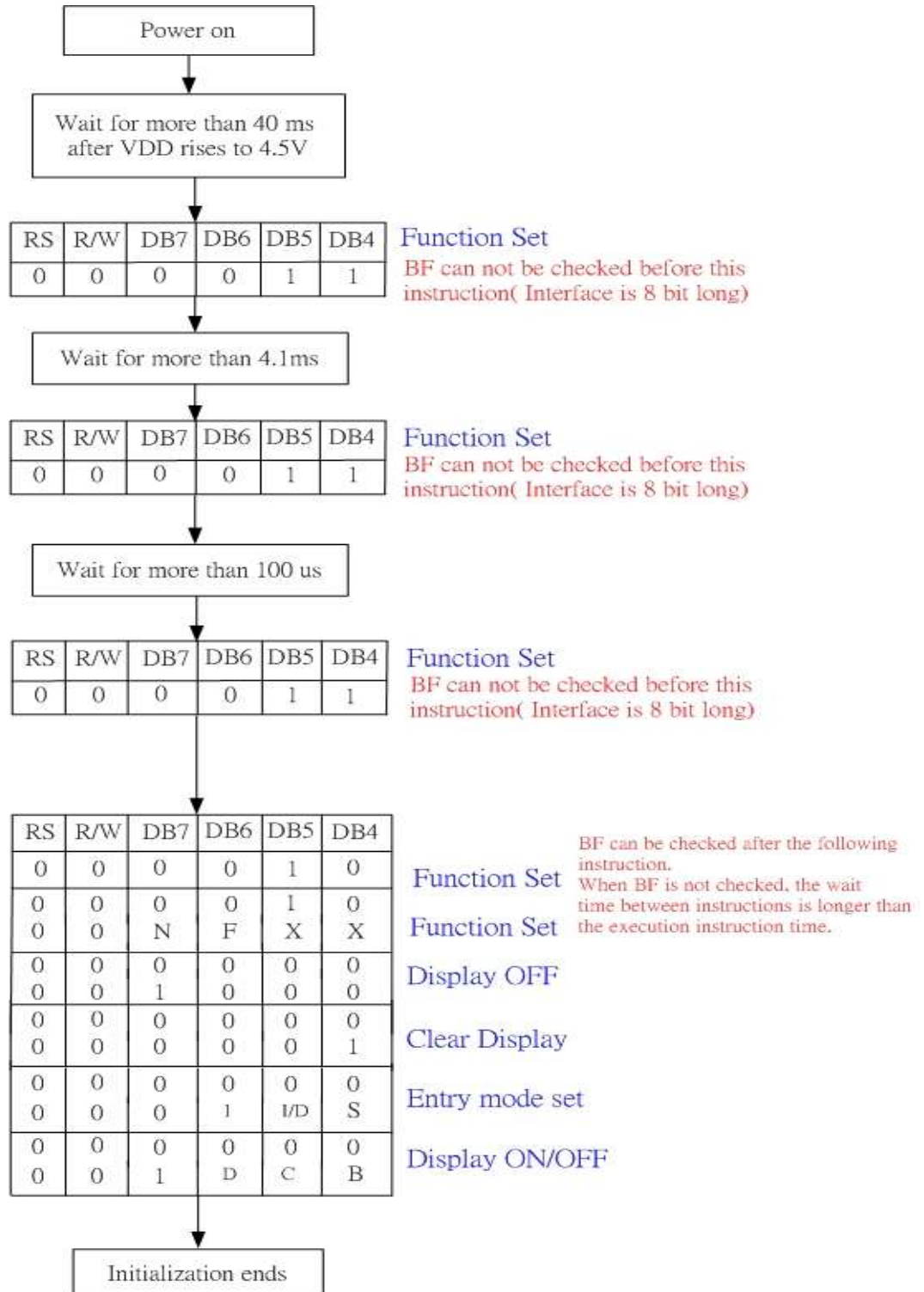
If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the AC780S. For such a case, initialization must be performed by the MPU as explain by the following figure.

◆ INITIALIZING BY INSTRUCTION

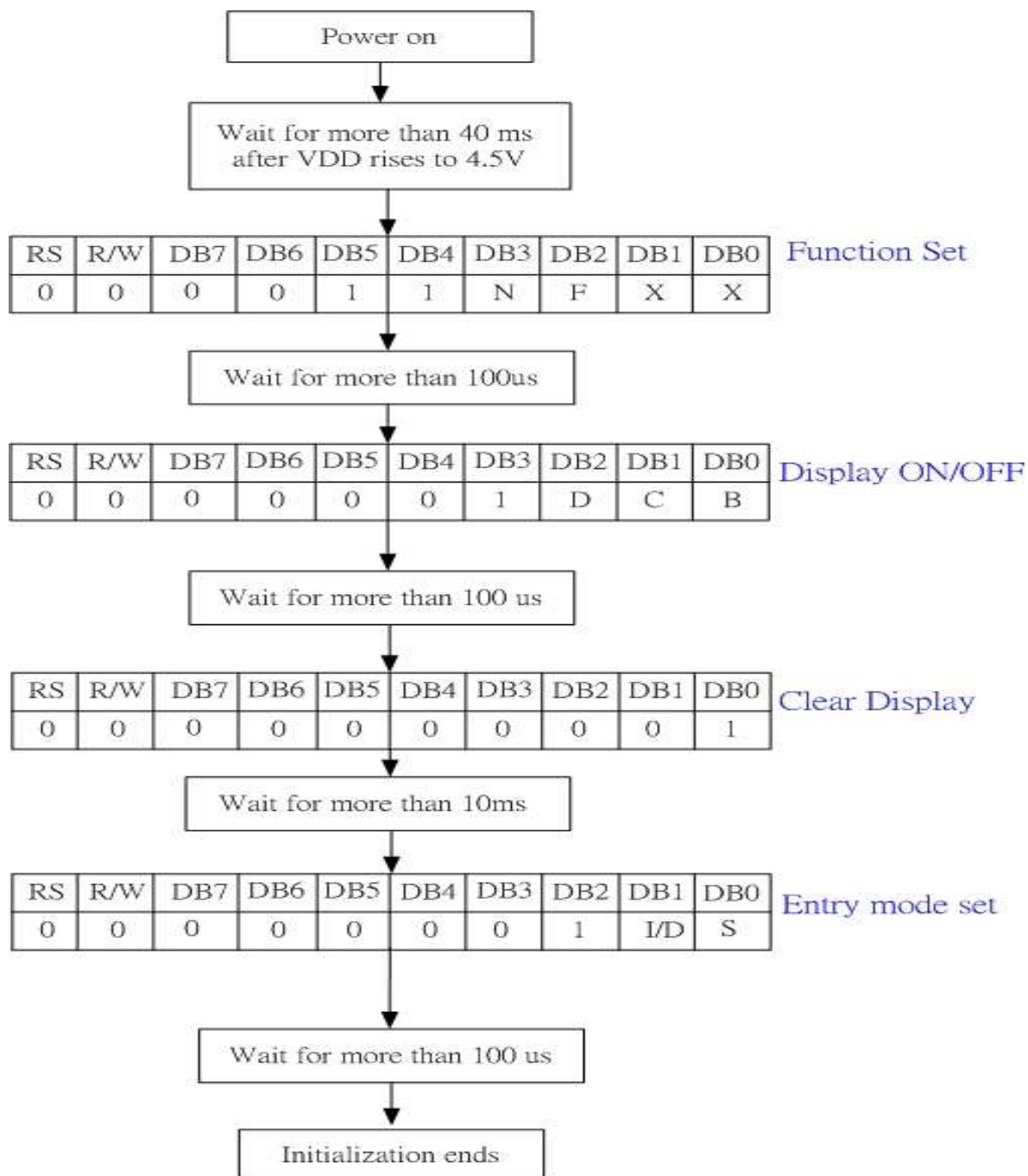
- 8 bit interface (Fosc=540KHz)



- 4 bit interface (Fosc=540KHz)



- Serial Interface code (Fosc=540KHz)

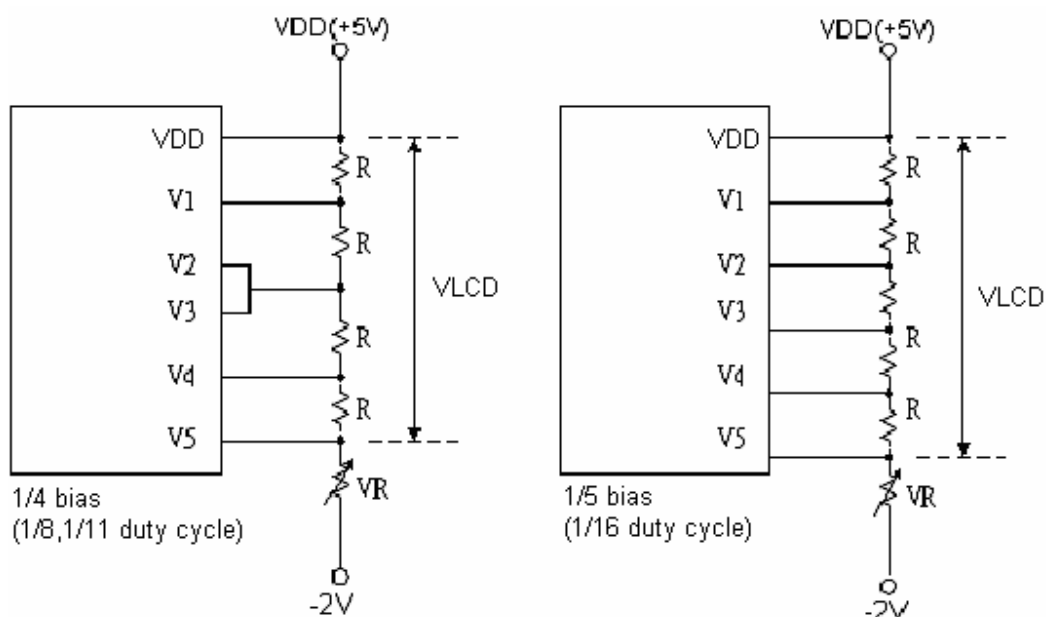


◆ Supply Voltage for LCD Drive

There are different voltages that supply to AC780S' s pin (V1 - V5) to obtain LCD drive waveform.

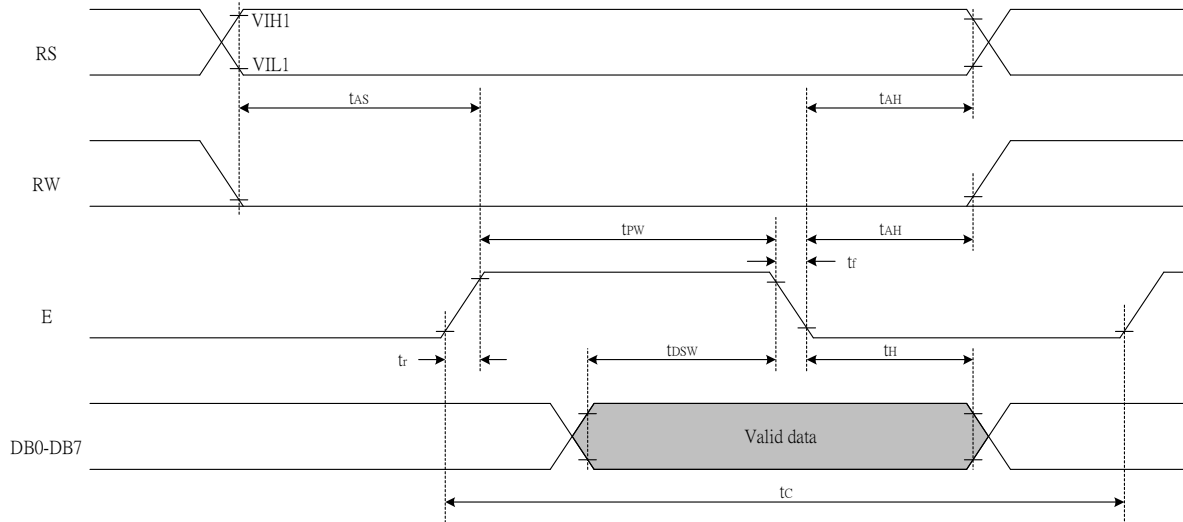
The relations of the bias, duty factor and supply voltages are shown as below:

| Supply Voltage | Duty Factor | |
|----------------|--------------------|--------------------|
| | 1/8, 1/11 | 1/16 |
| | Bias | |
| | 1/4 | 1/5 |
| V1 | $VDD - 1/4V_{LCD}$ | $VDD - 1/5V_{LCD}$ |
| V2 | $VDD - 1/2V_{LCD}$ | $VDD - 2/5V_{LCD}$ |
| V3 | $VDD - 1/2V_{LCD}$ | $VDD - 3/5V_{LCD}$ |
| V4 | $VDD - 3/4V_{LCD}$ | $VDD - 4/5V_{LCD}$ |
| V5 | $VDD - V_{LCD}$ | $VDD - V_{LCD}$ |

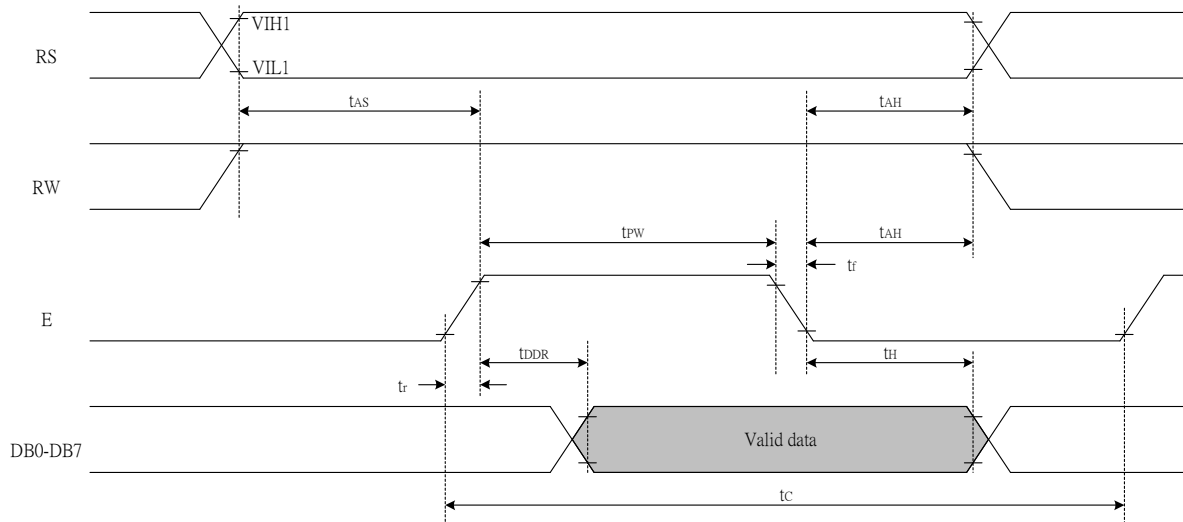


◆ Timing Characteristics

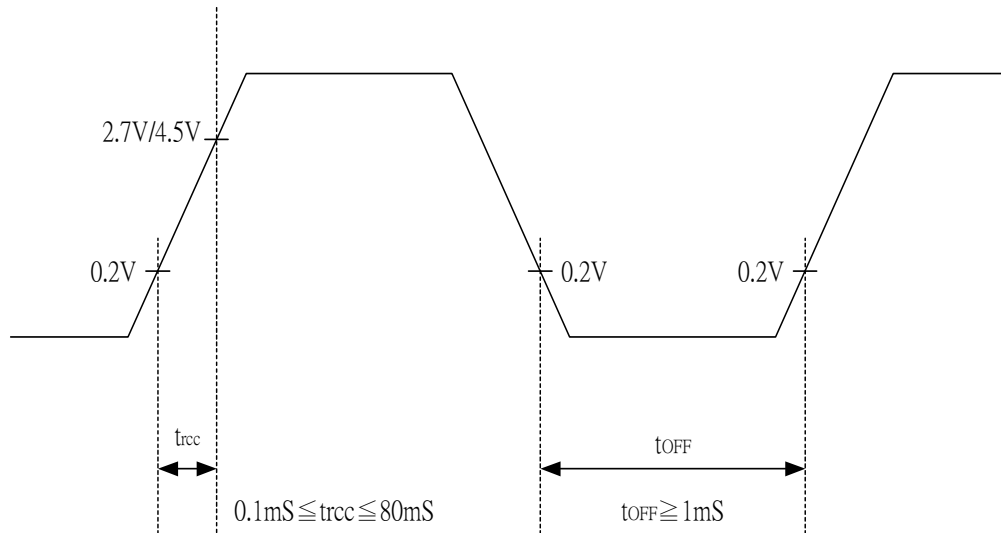
● Writing data from MPU to AC780S (Parallel 8-bit bus and 4-bit bus)



● Reading data from AC780S to MPU(Parallel 8-bit bus and 4-bit bus)



- Internal Power Supply Reset



Notes:

- t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
- Specified at 4.5V for 5V operation, and at 2.7V for 3V operation.
- For if 4.5V is not reached during 5V operation, the internal reset circuit will not operate normally.

◆ AC Characteristics
In 6800 interface (TA = 25°C, VDD = 2.7V)

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|---|-----------------------|---------------------------------|------|------|------|------|
| <i>Internal Clock Operation</i> | | | | | | |
| f _{OSC} | OSC Frequency | RF=75K | 380 | 540 | 700 | KHz |
| <i>External Clock Operation</i> | | | | | | |
| f _{EX} | External Frequency | - | 380 | 540 | 700 | KHz |
| | Duty Cycle | - | 45 | 50 | 55 | % |
| T _R ,T _F | Rise/Fall Time | - | - | - | 0.2 | μs |
| <i>Write Mode (Writing data from MPU to AC780S)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E (except clear display) | 1000 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 450 | - | - | ns |
| T _R ,T _F | Enable Rise/Fall Time | Pin E | - | - | 25 | ns |
| T _{AS} | Address Setup Time | Pins: RS,RW,E | 60 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS,RW,E | 20 | - | - | ns |
| T _{DSW} | Data Setup Time | Pins: DB0 - DB7 | 195 | - | - | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 10 | - | - | ns |
| <i>Read Mode (Reading Data from AC780S to MPU)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E | 1000 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 450 | - | - | ns |
| T _R ,T _F | Enable Rise/Fall Time | Pin E | - | - | 25 | ns |
| T _{AS} | Address Setup Time | Pins: RS,RW,E | 60 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS,RW,E | 20 | - | - | ns |
| T _{DDR} | Data Setup Time | Pins: DB0 - DB7 | - | - | 360 | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 5 | - | - | ns |

In 6800 interface (TA = 25°C, VDD = 5V)

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|---|-----------------------|---------------------------------|------|------|------|------|
| <i>Internal Clock Operation</i> | | | | | | |
| f _{OSC} | OSC Frequency | RF=91K | 380 | 540 | 700 | KHz |
| <i>External Clock Operation</i> | | | | | | |
| f _{EX} | External Frequency | - | 380 | 540 | 700 | KHz |
| | Duty Cycle | - | 45 | 50 | 55 | % |
| T _R ,T _F | Rise/Fall Time | - | - | - | 0.2 | μs |
| <i>Write Mode (Writing data from MPU to AC780S)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E (except clear display) | 500 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 230 | - | - | ns |
| T _R ,T _F | Enable Rise/Fall Time | Pin E | - | - | 20 | ns |
| T _{AS} | Address Setup Time | Pins: RS,RW,E | 40 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS,RW,E | 10 | - | - | ns |
| T _{DSW} | Data Setup Time | Pins: DB0 - DB7 | 80 | - | - | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 10 | - | - | ns |
| <i>Read Mode (Reading Data from AC780S to MPU)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E | 500 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 230 | - | - | ns |
| T _R ,T _F | Enable Rise/Fall Time | Pin E | - | - | 20 | ns |
| T _{AS} | Address Setup Time | Pins: RS,RW,E | 40 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS,RW,E | 10 | - | - | ns |
| T _{DDR} | Data Setup Time | Pins: DB0 - DB7 | - | - | 120 | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 5 | - | - | ns |

◆ Absolute Maximum Ratings

| Characteristics | Symbol | Value |
|-----------------------|-----------|------------------------------|
| Power Supply Voltage | V_{DD} | -0.3 to +5.5 |
| LCD Driver Voltage | V_{LCD} | $V_{SS}+7.0$ to $V_{SS}-0.3$ |
| Input Voltage | V_{IN} | -0.3 to $V_{DD}+0.3$ |
| Operating Temperature | T_A | -40°C to + 90°C |
| Storage Temperature | T_{STO} | -55°C to + 125°C |

◆ DC Characteristics

($T_A = 25^\circ\text{C}$, $V_{DD} = 2.7\text{ V} - 4.5\text{ V}$)

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|------------|---|---|--------------|------|-------------|---------------|
| V_{DD} | Operating Voltage | - | 2.7 | - | 4.5 | V |
| V_{LCD} | LCD Voltage | $V_{DD} - V_5$ | 3.0 | - | 7.0 | V |
| I_{DD} | Power Supply Current | $f_{OSC}=540\text{KHz}$ $V_{DD}=3.0\text{V}, \text{RF}=75\text{K}$ | - | 0.25 | 0.45 | mA |
| V_{IH1} | Input High Voltage (Except OSC1) | - | $0.7V_{DD}$ | - | V_{DD} | V |
| V_{IL1} | Input Low Voltage (Except OSC1) | - | - 0.3 | - | 0.6 | V |
| V_{IH2} | Input High Voltage (OSC1) | - | $0.7V_{DD}$ | - | V_{DD} | V |
| V_{IL2} | Input Low Voltage (OSC1) | - | - | - | $0.2V_{DD}$ | V |
| V_{OH1} | Output High Voltage (DB0 - DB7) | $I_{OH} = -0.1\text{mA}$ | $0.75V_{DD}$ | - | - | V |
| V_{OL1} | Output Low Voltage (DB0 - DB7) | $I_{OL} = 0.1\text{mA}$ | - | - | $0.2V_{DD}$ | V |
| V_{OH2} | Output High Voltage (Except DB0 - DB7) | $I_{OH} = -0.04\text{mA}$ | $0.8V_{DD}$ | - | V_{DD} | V |
| V_{OL2} | Output Low Voltage (Except DB0 - DB7) | $I_{OL} = 0.04\text{mA}$ | - | - | $0.2V_{DD}$ | V |
| R_{COM} | Common Resistance | $V_{LCD} = 4\text{V}, I_d = 0.05\text{mA}$ | - | 2 | 20 | K Ω |
| R_{SEG} | Segment Resistance | $V_{LCD} = 4\text{V}, I_d = 0.05\text{mA}$ | - | 2 | 30 | K Ω |
| I_{LEAK} | Input Leakage Current | $V_{IN} = 0\text{V to } V_{DD}$ | -1 | - | 1 | μA |
| I_{PUP} | Pull Up MOS Current | $V_{DD} = 3\text{V}$ | 10 | 60 | 120 | μA |

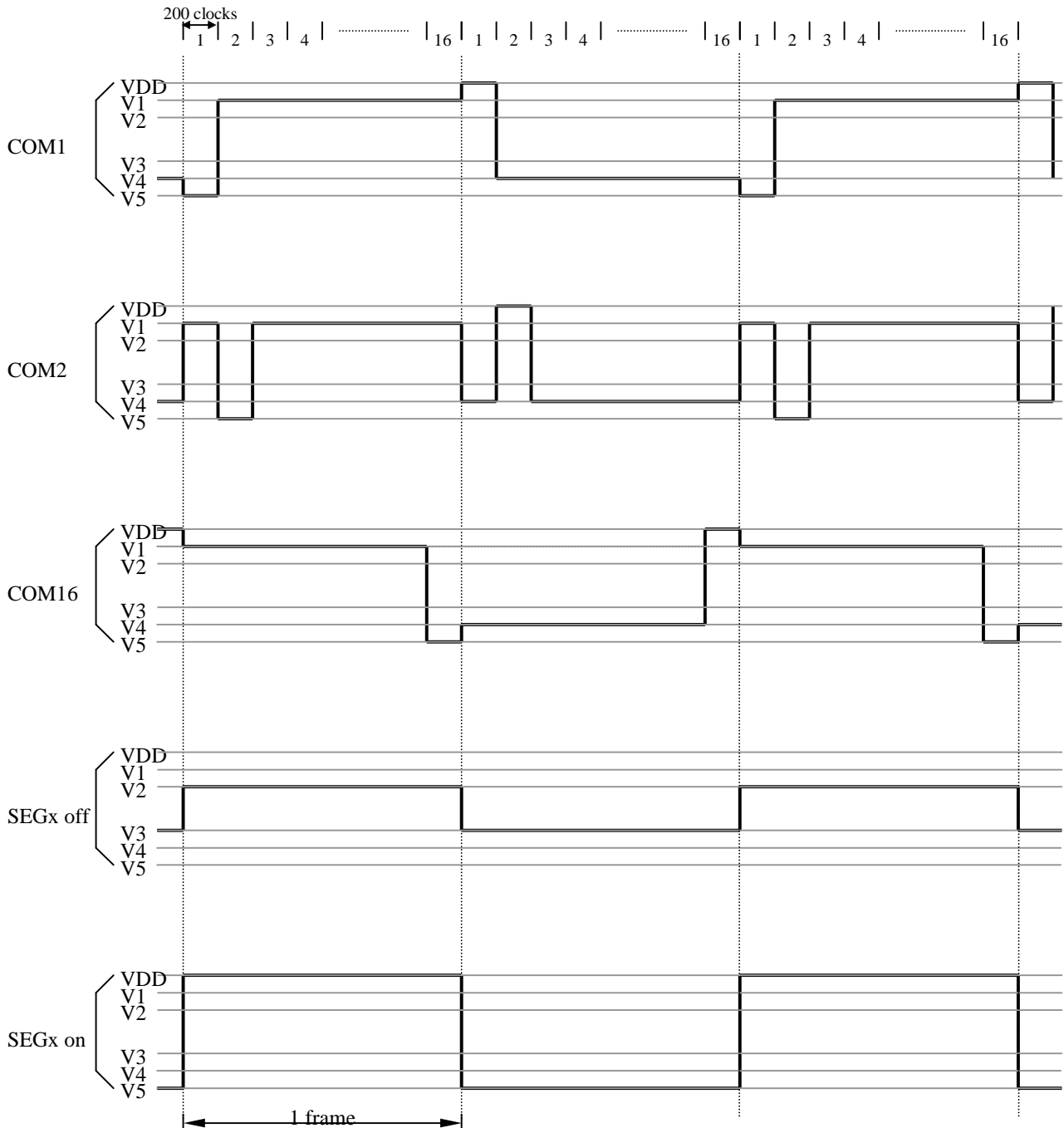
◆ DC Characteristics

(TA = 25°C, V_{DD} = 4.5 V - 5.5 V)

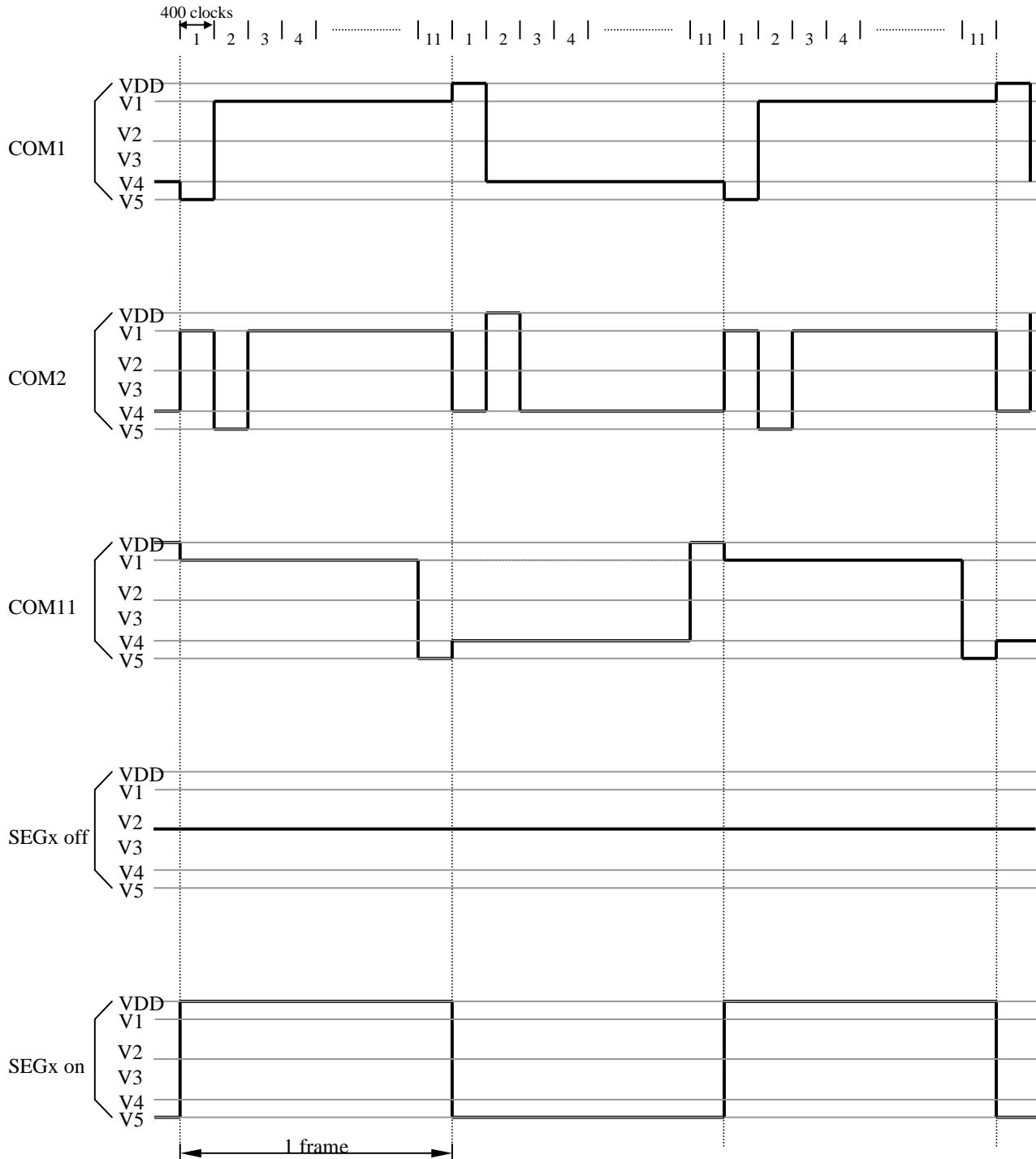
| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|-------------------|---|---|---------------------|------|---------------------|------|
| V _{DD} | Operating Voltage | - | 4.5 | - | 5.5 | V |
| V _{LCD} | LCD Voltage | V _{DD} - V5 | 3.0 | - | 7.0 | V |
| I _{DD} | Power Supply Current | f _{OSC} = 540KHz V _{DD} = 5.0V, RF = 91K | - | 0.35 | 0.55 | mA |
| V _{IHI} | Input High Voltage (Except OSC1) | - | 2.5 | - | V _{DD} | V |
| V _{ILI} | Input Low Voltage (Except OSC1) | - | -0.3 | - | 0.55 | V |
| V _{IH2} | Input High Voltage (OSC1) | - | V _{DD} - 1 | - | V _{DD} | V |
| V _{IL2} | Input Low Voltage (OSC1) | - | - | - | 0.2 V _{DD} | V |
| V _{OHI} | Output High Voltage (DB0 - DB7) | I _{OH} = -0.1mA | 3.9 | - | V _{DD} | V |
| V _{OLI} | Output Low Voltage (DB0 - DB7) | I _{OL} = 0.1mA | - | - | 0.4 | V |
| V _{OH2} | Output High Voltage (Except DB0 - DB7) | I _{OH} = -0.04mA | 0.9V _{DD} | - | V _{DD} | V |
| V _{OL2} | Output Low Voltage (Except DB0 - DB7) | I _{OL} = 0.04mA | - | - | 0.1V _{DD} | V |
| R _{COM} | Common Resistance | V _{LCD} = 4V, I _d = 0.05mA | - | 2 | 20 | KΩ |
| R _{SEG} | Segment Resistance | V _{LCD} = 4V, I _d = 0.05mA | - | 2 | 30 | KΩ |
| I _{LEAK} | Input Leakage Current | V _{IN} = 0V to V _{DD} | -1 | - | 1 | μA |
| I _{PUP} | Pull Up MOS Current | V _{DD} = 5V | 90 | 200 | 330 | μA |

◆ LCD Frame Frequency

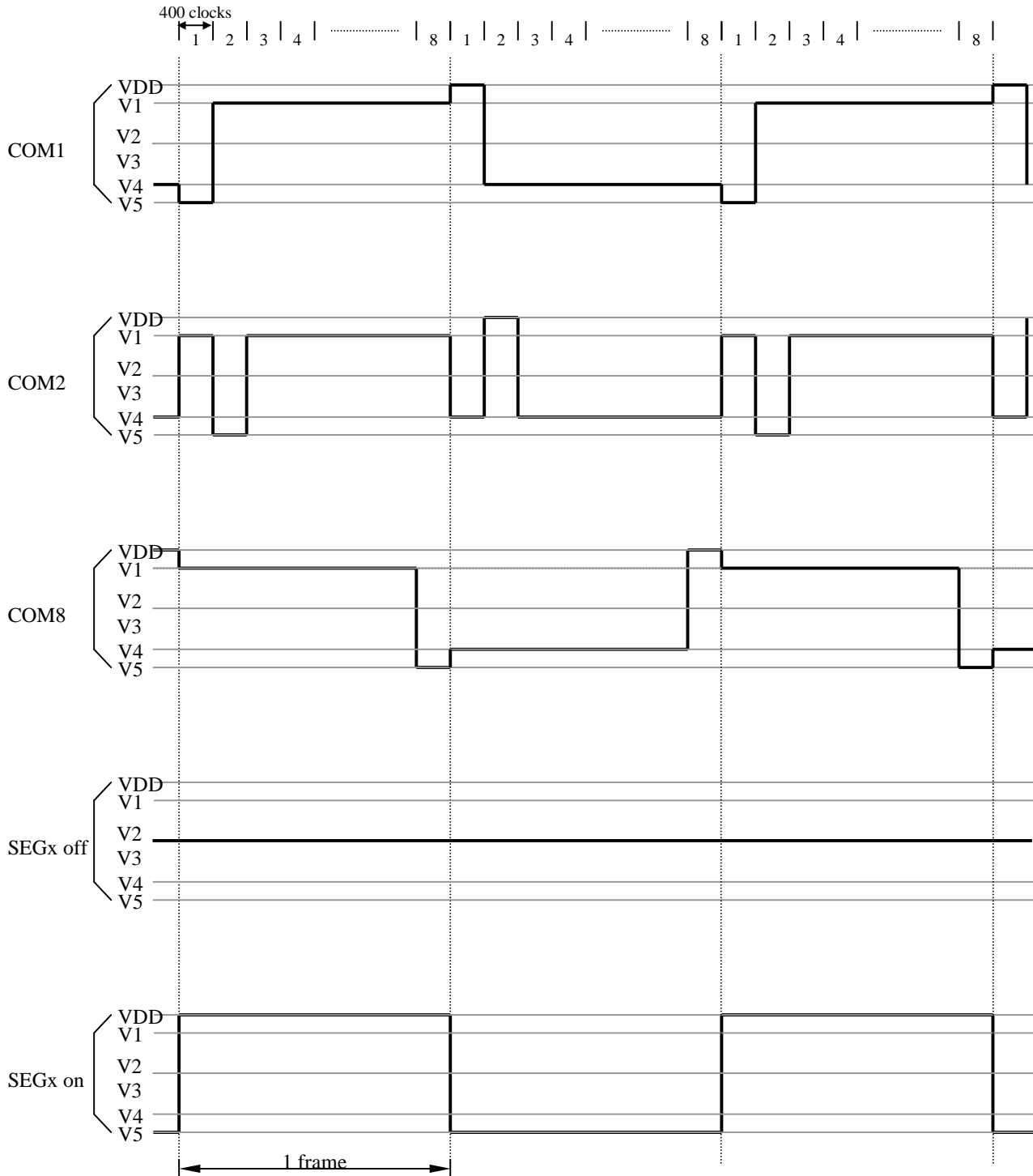
- Assume the oscillation frequency is 540KHz, 1 clock cycle time = 1.85us, 1/16 duty; 1/5 bias, 1 frame = 1.85us x 200 x 16 = 5920us=5.92ms (168.9Hz)



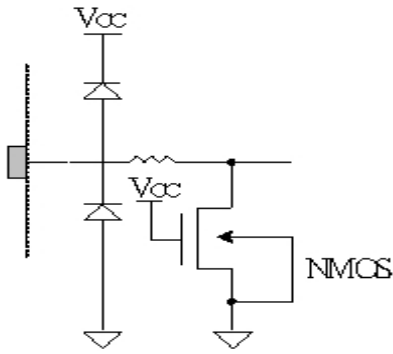
- Assume the oscillation frequency is 540KHz, 1 clock cycle time = 1.85us, 1/11 duty; 1/4 bias, 1 frame = 1.85us x 400 x 11 = 8140us=8.14ms (122.8Hz)



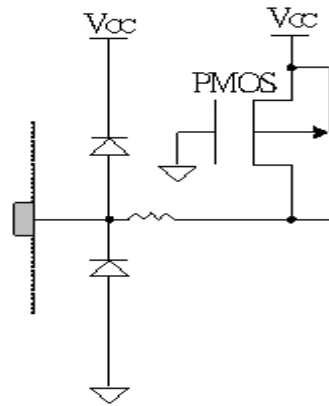
- Assume the oscillation frequency is 540KHz, 1 clock cycle time = 1.85us, 1/8 duty; 1/4 bias, 1 frame = 1.85us x 400 x 8 = 5920us=5.92ms (168.9Hz)



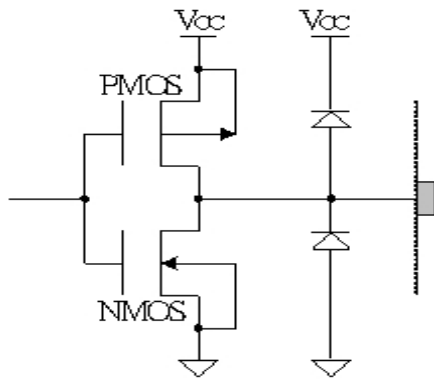
◆ I/O Pad Configuration



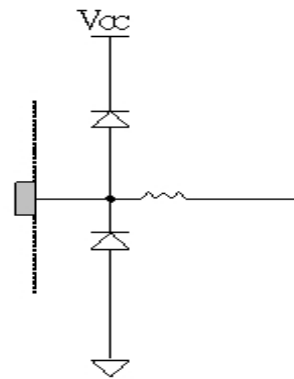
Input PAD:E
(with Pull-down in Serial interface)



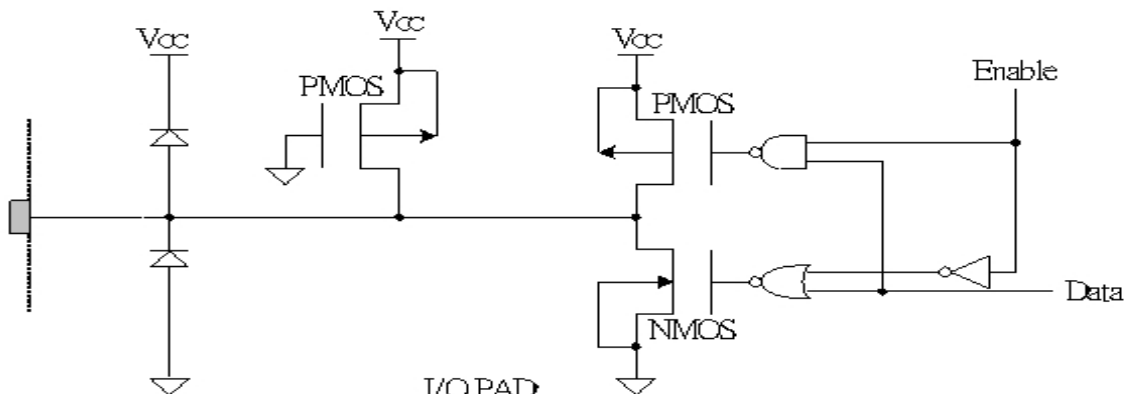
Input PAD:RW (with Pull-up)
RS (with Pull-up in parallel and IIC interface)



Output PAD:CL1,CL2,M,D



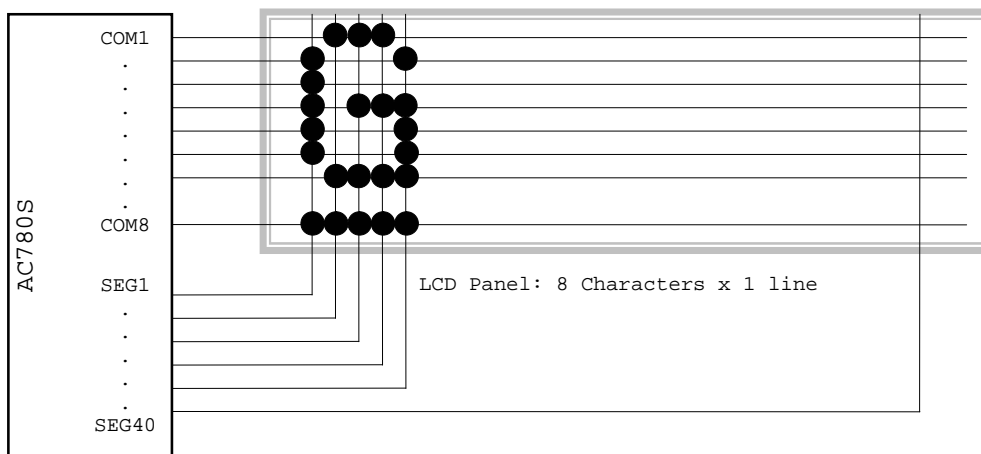
Input PAD:IF0,IF1



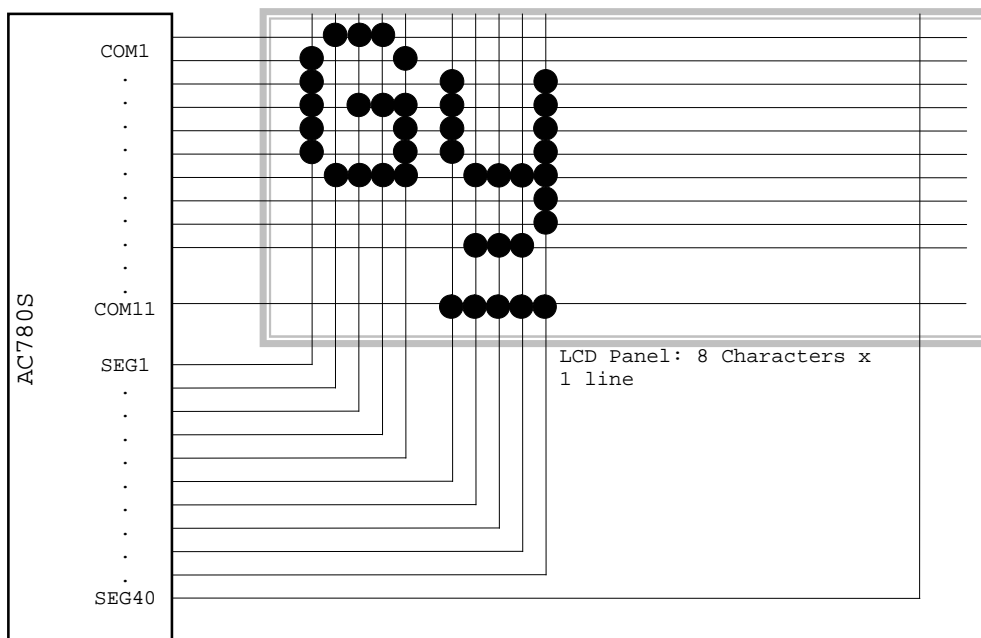
I/O PAD:
DB0-DB7 with Pull-up in parallel interface
D2,D3,D4,D5 with Pull-up in IIC interface
D0-D4 with Pull-up in 4SPI interface

◆ LCD and AC780S Connection

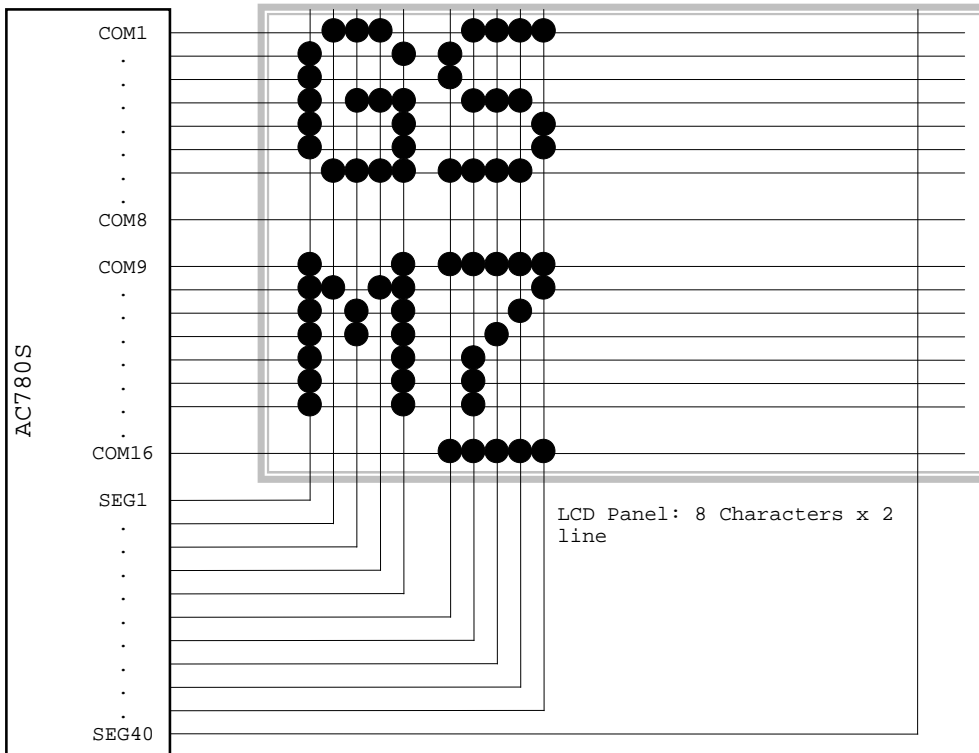
A. 5x8 dots, 8 characters x 1 line (1/4 bias, 1/8 duty)



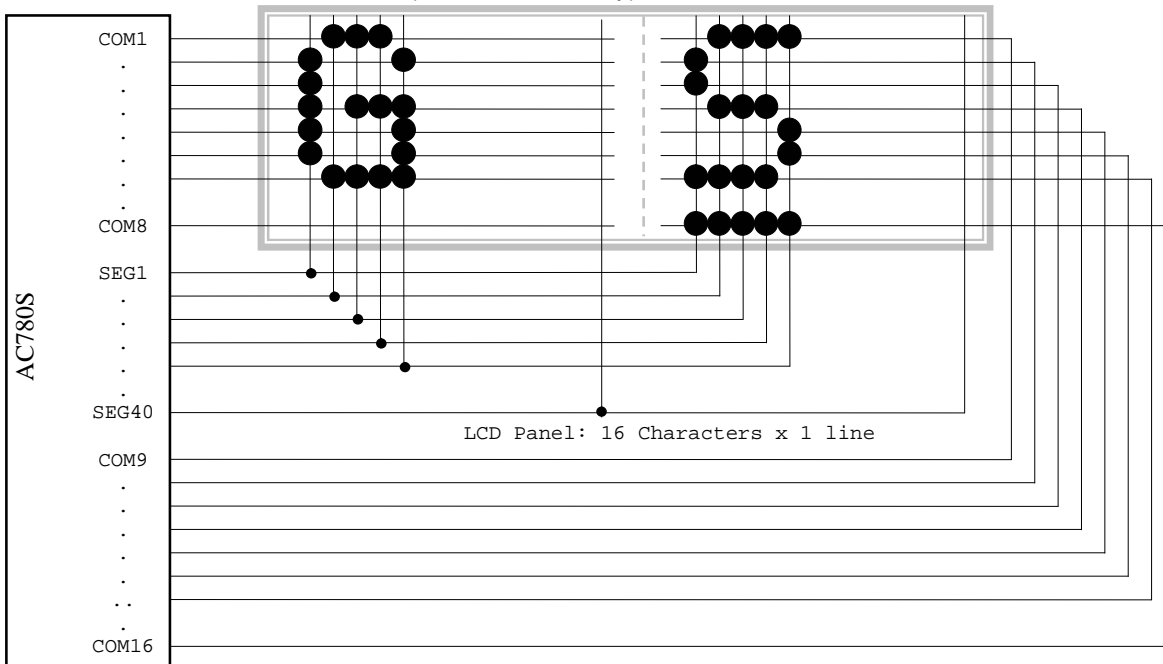
B. 5x11 dots, 8 characters x 1 line (1/4 bias, 1/11 duty)



C. 5x8 dots, 8 characters x 2 line (1/5 bias, 1/16 duty)



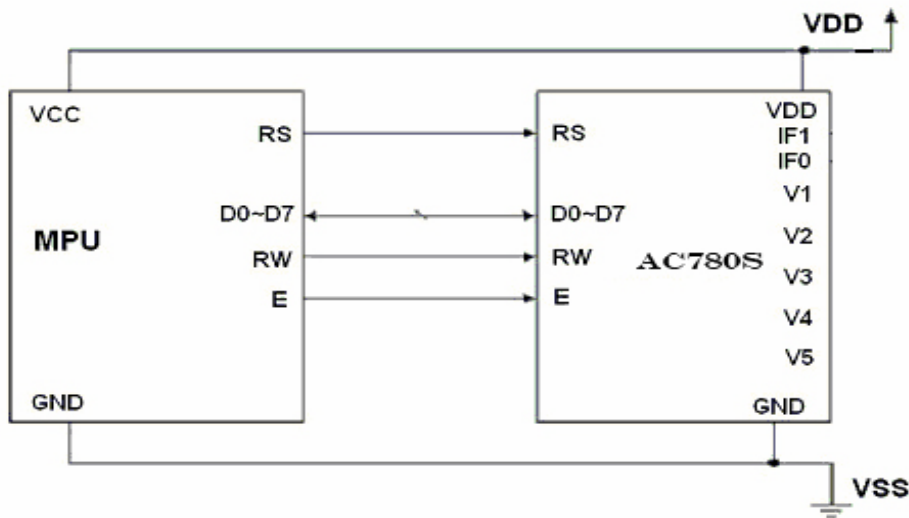
D. 5x8 dots, 16 characters x 1 line (1/5 bias, 1/16 duty)



THE MPU INTERFACE CIRCUIT

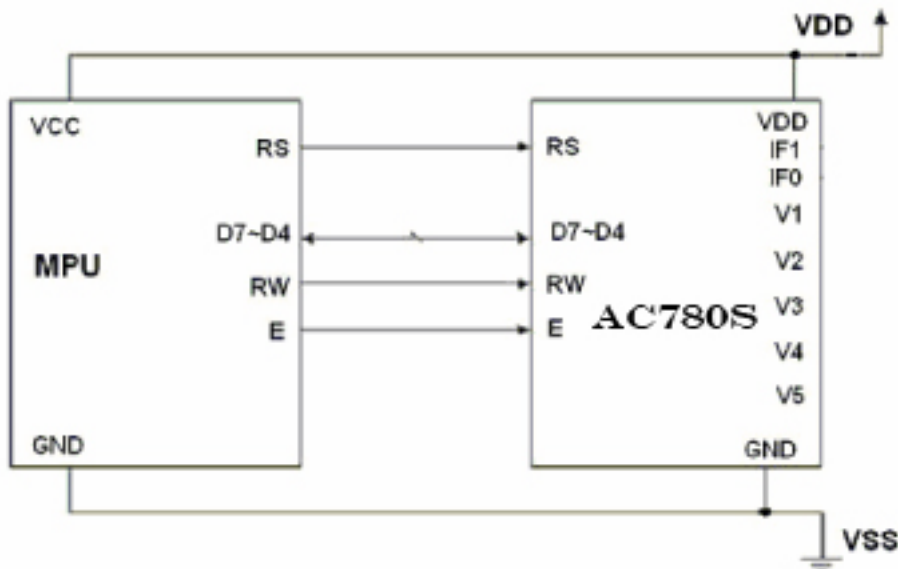
The AC780S Series can be connected to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the AC780S series chips with fewer signal lines. The display area can be enlarged by using multiple AC780S Series chips. When this is done, the chip select signal can be used to select the individual lcs to access.

(1) 6800 8 bits Series MPUs



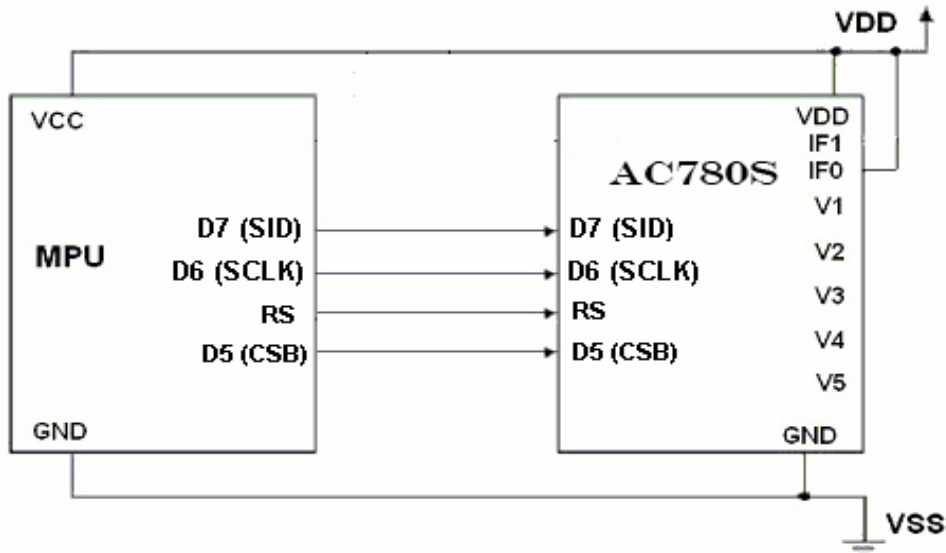
IF0, IF1: opened

(2) 6800 4 bits Series MPUs



IF0, IF1: opened
D0~D3: opened

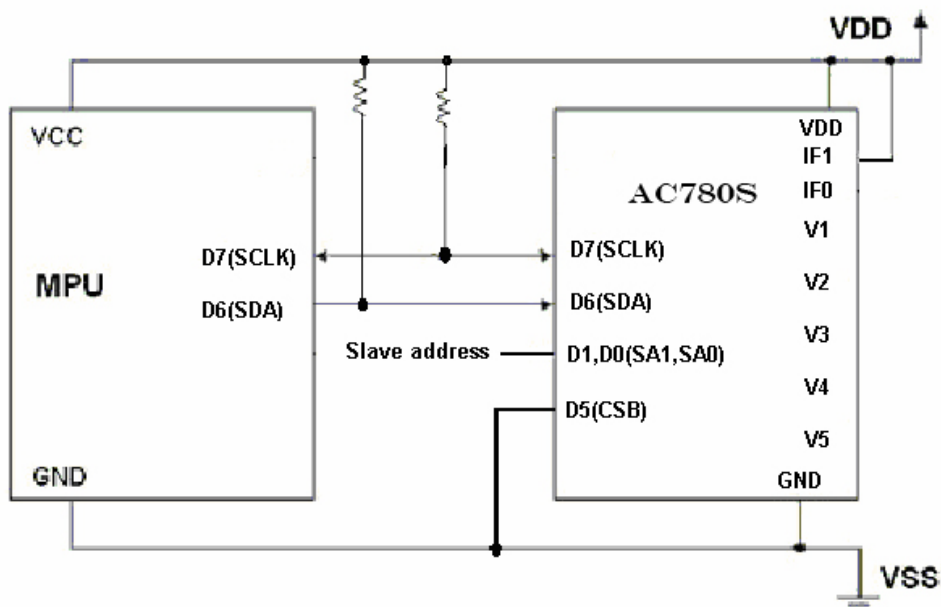
(3) Using the Serial Interface—For 4 SPI



IF0: bonding to VDD
 IF1: opened
 D0~D4: opened
 RW、E: opened

(4) Using the Serial Interface—For IIC Interface

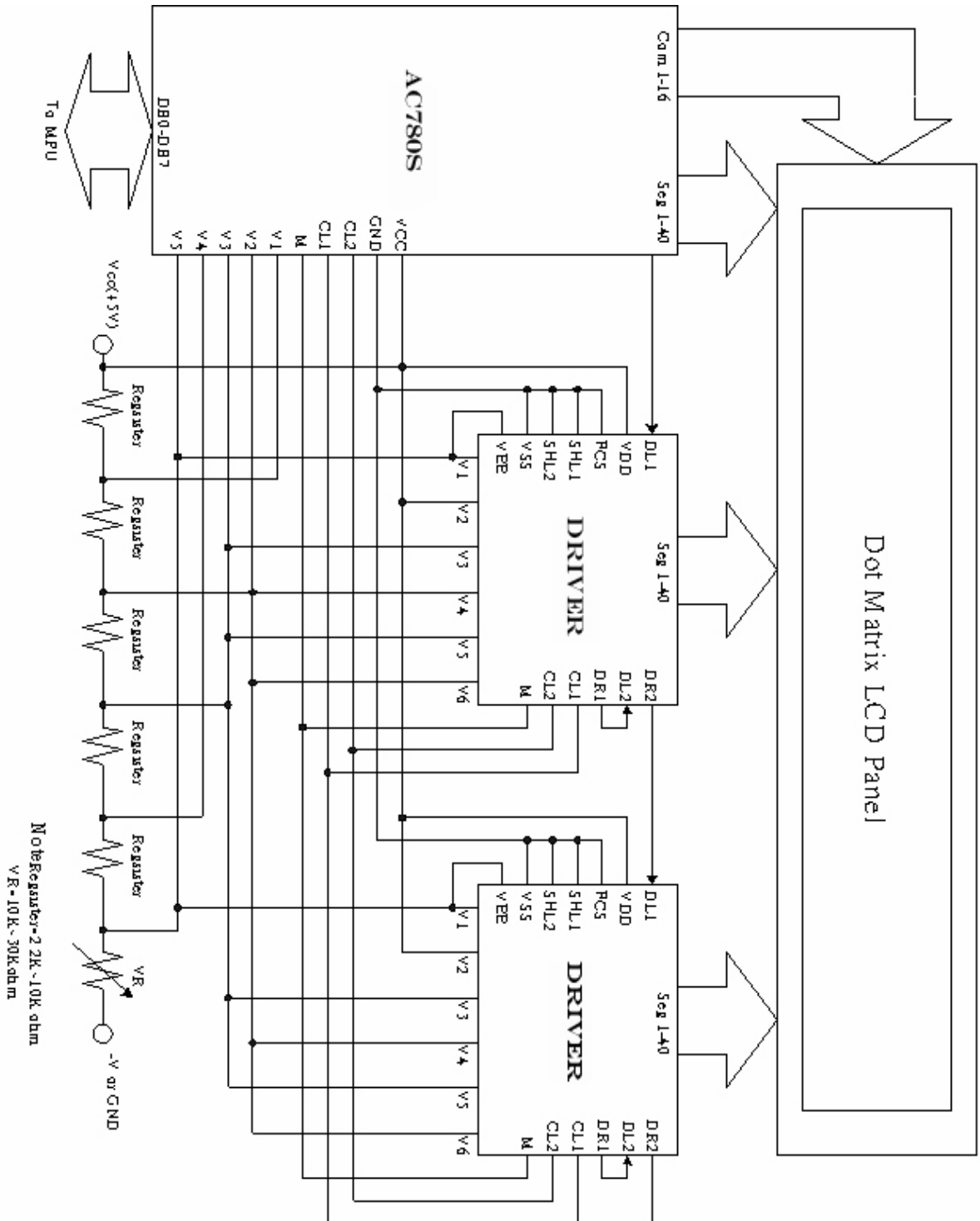
R=2.2K
 Pull-high resistor



IF0: opened
 IF1: bonding to VDD
 D0、D1: Slave address
 D2~D4: opened
 RW、E: opened

Application Circuit

(2 Line x 24 Characters)



AC780S FONT TABLE (0A-001)

| $\frac{b7 \sim 4}{b3 \sim 0}$ | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|-------------------------------|-------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | CG RAM [00] | | | 0 | a | P | \ | P | | | | 一 | 9 | 3 | 0 | P |
| 0001 | CG RAM [01] | | ! | 1 | A | Q | a | 9 | | | . | 7 | + | 4 | 3 | 9 |
| 0010 | CG RAM [02] | | " | 2 | B | R | b | r | | | 7 | 4 | 9 | + | P | 0 |
| 0011 | CG RAM [03] | | # | 3 | C | S | c | s | | | J | 0 | T | E | 0 | 0 |
| 0100 | CG RAM [04] | | \$ | 4 | D | T | d | t | | | \ | T | T | P | H | 0 |
| 0101 | CG RAM [05] | | % | 5 | E | U | e | u | | | - | * | * | 1 | 0 | 0 |
| 0110 | CG RAM [06] | | & | 6 | F | V | f | v | | | 9 | 0 | 2 | 3 | P | 2 |
| 0111 | CG RAM [07] | | ' | 7 | G | W | g | w | | | 7 | + | + | 9 | 9 | π |
| 1000 | CG RAM [00] | | (| 8 | H | X | h | x | | | 4 | 0 | * | U | + | + |
| 1001 | CG RAM [01] | |) | 9 | I | Y | i | y | | | 5 | 0 | J | U | + | Y |
| 1010 | CG RAM [02] | | * | 0 | J | Z | j | z | | | 2 | 0 | 0 | U | J | + |
| 1011 | CG RAM [03] | | + | 1 | K | L | k | l | | | * | 0 | E | 0 | + | π |
| 1100 | CG RAM [04] | | , | < | L | Y | l | l | | | 0 | 0 | 0 | 0 | 0 | π |
| 1101 | CG RAM [05] | | - | = | M | N | m | n | | | 2 | + | + | U | + | + |
| 1110 | CG RAM [06] | | . | > | N | n | n | + | | | a | 0 | 0 | + | 0 | |
| 1111 | CG RAM [07] | | / | ? | 0 | L | o | e | | | w | U | + | + | 0 | ■ |