# 2020
# Power Management Chip

The PMC™ 2020 is designed to reduce the total power consumption of a Notebook computer system with an easy-to-use interface. By minimizing power consumption, the 2020 extends the battery life of a PC Notebook system.

## Features

* Provides eight trigger input channels for monitoring activities such as keyboard, video, hard disk, floppy disk, and user defined device.
* Provides eight power control outputs
* Each power control output status can be determined by the combinations of the eight trigger inputs
* Provides eight user programmable time-out timers.
* Flexible timer scales:

  2 timers from 1/8 second to 14 seconds
  4 timers from 1 minute to 15 minutes
  1 timer from 2 minutes to 210 minutes
  1 timer from 4 minutes to 7 hours
* Each trigger input can select one of the two timer scales
* No glitch CPU clock switching functions
* Supports CPU clock up to 66 MHz
* Generates 16 MHz clock for AT Bus
* Generates 32.768 KHz for both RTC and ACC2020 by using 32.768 KHz crystal
* Supports Modem ring power-on
* Supports scheduled power-on
* Supports cover switch power-down/on
* Supports Suspend and Resume
* Provides six operation modes:

  Full Operation mode
  Rest mode
  Standby mode
  Shutdown mode
  Freeze mode
  Off mode
* Predefined mode transition among Normal Rest, and Standby modes
* Programmable transitions of operation modes
* Provides interrupt request for suspend/resume operation
* Interrupt request output can be masked
* Supports Programmable Slow Refresh in Shutdown and Freeze modes
* Supports CAS before RAS refresh
* 80-pin QFP


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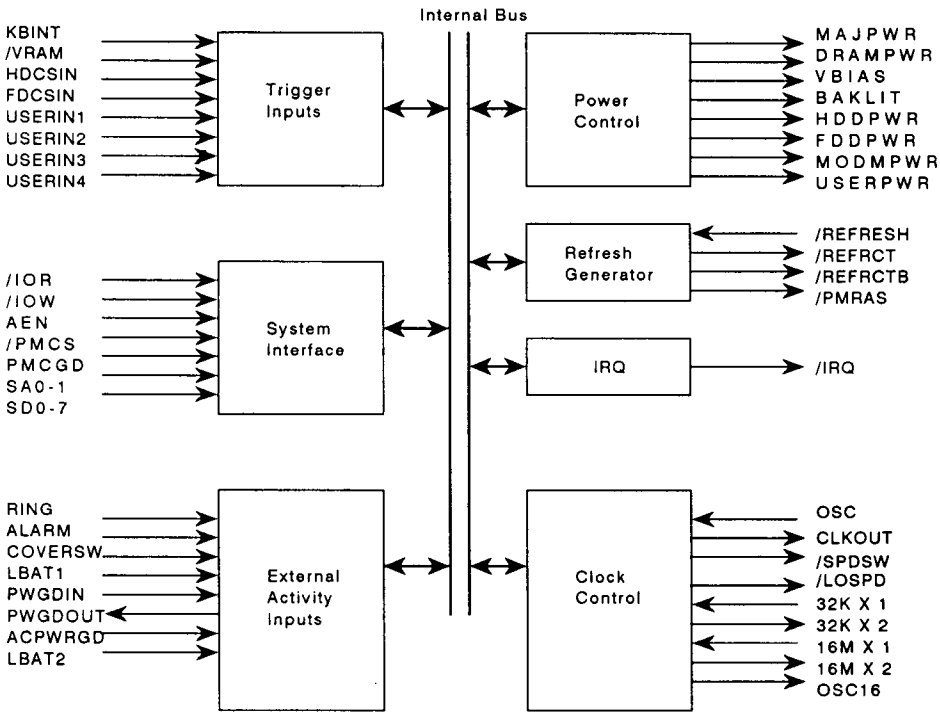
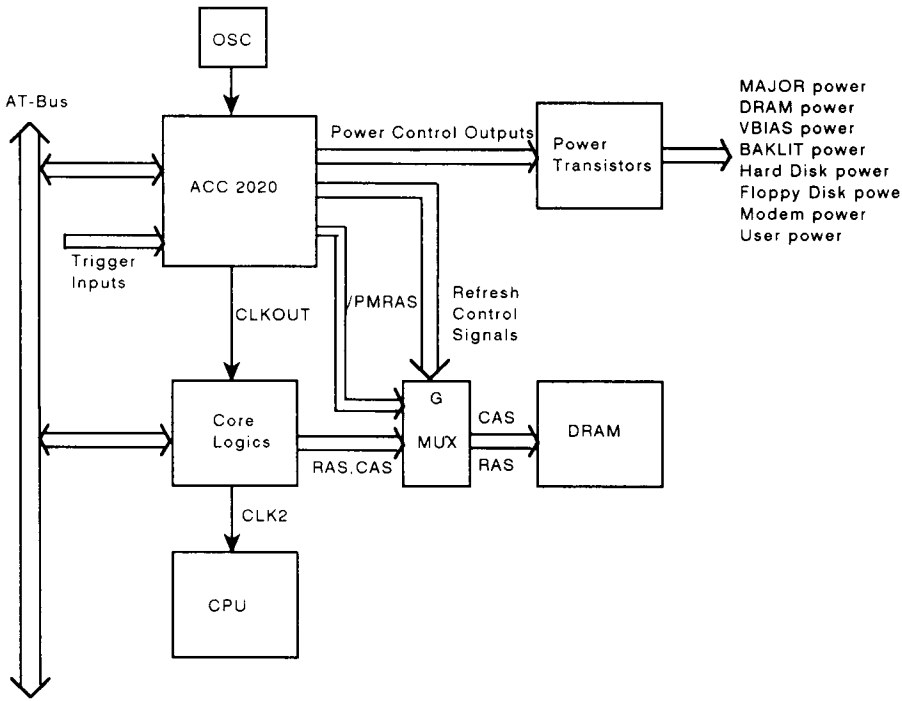
## Functional Block Diagram



## System Block Diagram



## Functional Description

The 2020 is a smart solution for a PC notebook system design where power consumption is a major consideration. The 2020 allows the system to maximize its performance with minimum power consumption. The 2020 has eight trigger inputs and timers to facilitate a PC notebook system intelligently identify when the system can be running at lower speed and which device is not in use.

When the areas where power can be saved are identified, the 8 power control outputs can restrain them from consuming power. The 2020 internal state machine provides an automatic mode transition mechanism to further reduce the system's power consumption without sacrificing the performance of a PC notebook system. The default value of this state machine has been set in such a way that no software efforts are required for the power management control system to work.

The 2020 supports Suspend and Resume function in three power down modes (Freeze, Shutdown, and Off modes) to give the system designer maximum flexibility to conserve battery life. In Freeze or Shutdown mode, the system DRAM refresh control is assumed by 2020, and CAS before RAS refresh is implemented to consume minimum power.

## Trigger Inputs

The 2020 has 8 trigger inputs to monitor activities for keyboard, video, hard disk, floppy and other peripherals. The status of these 8 inputs are latched internally. These latches are sampled and monitored at regular intervals to control the programmed time-out timers. The 2020 trigger inputs accept pulse signals (low-to-high transition), such as interrupts or chip-select signals of the monitored devices.

All trigger inputs are CMOS inputs i.e. $V_{IL}$ = 0.2 VCC, $V_{IH}$ = VCC with input leakage less than 1 mA.

Four trigger inputs are predefined to monitor system activities. They are IRQ1 for keyboard activity, /VRAM for video access activity, IRQ14 for hard disk activity and IRQ6 for floppy drive activity.

An example of the eight trigger inputs is as follows:

| Pin Name | Monitor | Purpose |
|---|---|---|
| KBINT | IRQ1 | monitor keyboard activity |
| /VRAM | /VRAM of 2036 | monitor video activity |
| HDCSIN | IRQ14 or SCSI | monitor hard disk activity |
| FDCSIN | IRQ6 | monitor floppy activity |
| USERIN1 | | defined by user |
| USERIN2 | | defined by user |
| USERIN3 | | defined by user |
| USERIN4 | | defined by user |

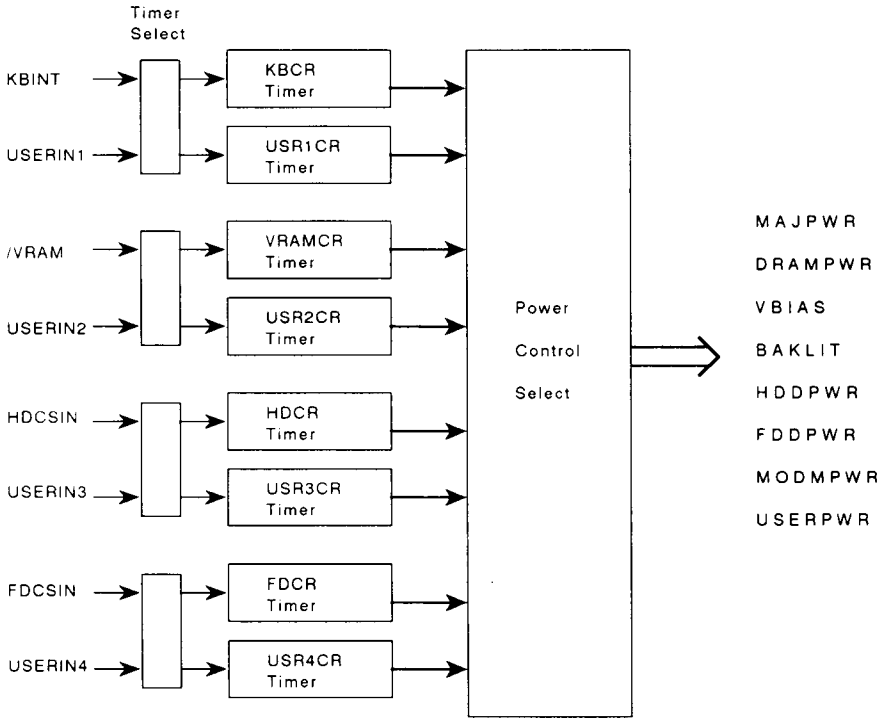



**Figure 1: Internal Timer Block Diagram**

## Internal Timers

There are 12 timers in the 2020. Eight internal timers are used to generate time out signal for each of the eight trigger inputs and 4 timers are used by the internal state machine.

A positive pulse at the trigger input will start the corresponding timer. The timer will generate a time-out signal when there is no other following pulse coming in at the trigger input for a programmed time period. If the trigger input pulse comes in again the timer will restart.

The 8 trigger input timers are KBCR timer, USER1CR timer, VRAMCR timer, USR2CR timer, HDCR timer, USR3CR timer, FDCR timer, and USR4CR timer. Refer to the table 1.1 for each timer's scale. Each trigger input has a corresponding default timer. For instance, the KBINT pin default timer is KBCR timer and USERIN1 pin default timer is USER1CR timer.

To provide flexibility, a pair of trigger inputs share the same two timers. Bits 3-0 of Register 7Ah are the timer select registers which can be programmed to assign the timers between the pairs. For instance, when Bit 0 is changed from default 0 to 1, KBINT is the trigger input pin for USR1CR timer, and USERIN1 is the trigger input pin for KBCR timer. Refer to Figure 1, Internal Timer Block Diagram for the relationship of other trigger input pairs.

**Table 1.1 2020 Timer Scales**

| Timer | Time-out | Default |
|---|---|---|
| KBCR timer | 1/8 - 14 secs. | 8 secs. |
| USR1CR timer | 1 - 15 mins. | 2 mins. |
| VRAMCR timer | 1/8 - 14 secs. | 8 secs. |
| USR2CR timer | 1 - 15 mins. | 2 mins. |
| HDCR timer | 1 - 15 mins. | 4 mins. |
| USR3CR timer | 2 - 210 mins. | 4 mins. |
| FDCR timer | 1 - 15 mins. | 2 mins. |
| USR4CR timer | 4 mins. - 7 hrs. | 4 mins. |
| TP1CR timer | 1/8 - 14 secs. | 4 secs. |
| TP2CR timer | 1 - 15 mins. | Disable |
| TP3CR timer | 1/8 - 14 secs. | Disable |
| TP4CR timer | 1 - 15 mins. | Disable |

TP1CR timer, TP2CR timer, TP3CR timer, and TP4CR timer are used by the internal state machine. Refer to state machine timer in the section of Mode Transitions for the details.

## Power Control Outputs

The 2020 supports 8 power control outputs. These power control outputs are used to control the power of peripheral devices by enabling or disabling power transistors. When the power transistor is disabled, the power of the peripheral device is removed.

To determine the turn-off condition of a peripheral device, each power control output can be controlled by combinations of trigger inputs. Refer to Figure 1. The power control output pin will go to logic low level to disable the power transistor, when all corresponding trigger inputs are timed out. When any of the trigger input has renewed activity, the corresponding power control output pin will go to logic high level to enable the power transistor and resume the power of the corresponding peripheral device.

The logic state for power control pins MAJPWR and DRAMPWR are controlled by the 2020 internal state machine. There are two display power control outputs. BAKLIT is controlled by USERIN3 trigger input and VBIAS has a time delay from BAKLIT preset by Bits 3-0 of Register 5Ch. Registers BAKLITCR, HDDCR, FDDCR, MODMCR, USRCR determine the combination of trigger inputs for power control pins BAKLIT, HDDPWR, FDDPWR, MODMPWR, USERPWR respectively. The default for Power Control output pins are as follows:

| Pin Name | Default Control Source |
|---|---|
| MAJPWR | controlled by 2020 |
| DRAMPWR | controlled by 2020 |
| VBIAS | time delay from BAKLIT |
| BAKLIT | USERIN3 for 4 minutes of inactivity |
| HDDPWR | HDCSIN for 4 minutes of inactivity |
| FDDPWR | FDCSIN for 2 minutes of inactivity |
| MODMPWR | USERIN1 for 2 minutes of inactivity |
| USERPWR | USERIN2 for 2 minutes of inactivity |

## Mode of Operation

The 2020 supports 6 sequencing operation modes to conserve the CPU and peripheral power consumptions. Refer to Table 1.2 for the pin status in each mode.

**FULL OPERATION mode:**

In this mode, CPU is operating at normal or turbo speed, all peripherals in the systems are powered.

**REST mode:**

In this mode, CPU speed is operating at 8 MHz. This mode is desirable when the speed of system application is not critical.

**STANDBY mode:**

In this mode, most peripherals are powered off except the CPU, system controller, DRAM and 2020. CPU speed can be programmed from 8-0 MHz.

**FREEZE mode:**

In this mode, most peripherals are powered off except the CPU, system controller, DRAM and 2020. CPU will operate at 0 Hz, that means CPUCLK is kept at High or Low level. 2020 will take over DRAM refresh while CPU is operated at 0Hz.

**SHUTDOWN mode:**

In this mode, the CPU, system controller and all peripherals are powered off except 2020 and DRAM. 2020 will take over DRAM refresh while CPU is powered off.

**OFF mode:**

Only 2020 is powered. The others are powered off.

**Table 1.2 2020 Control Pin Status in each Operation Mode**

| MODE | CLK-OUT | OSC-16 | MAJ-PWR | DRAM-PWR | VBIAS | BAK-LIT | HDD-PWR | FDD-PWR | MODM-PWR | USER-PWR | /LO-SPD | REF-RCT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Full Operation | OSC | 16 MHz | On | On | P* | P | P | P | P | P | High | High |
| Rest | 8 MHz | 16 MHz | On | On | P | P | P | P | P | P | High | High |
| Standby | 8/4/2/1 MHz | 16 MHz | On | On | Off | Off | Off | Off | P | Off | Low | High |
| Freeze | 0Hz | 0Hz | On | On | Off | Off | Off | Off | P | Off | Low | Low |
| Shutdown | 0Hz | 0Hz | Off | On | Off | Off | Off | Off | P | Off | Low | Low |
| Off | 0Hz | 0Hz | Off | Off | Off | Off | Off | Off | Off | Off | Low | Low |

* Programmable

## External Activity Inputs

RING is a positive edge sensitive input intended for use with a modem ring line. The numbers of rings required for this input to be triggered is specified in 4 bits of the 7Ah Control Register. The default is one positive edge transition. If these bits are zero, this input is disabled. If Register 7Ah, bits 4-7 are enabled, a pre-defined number of positive edge transitions on this input will wake up the 2020 to Full Operation mode or Rest mode. Refer to Register 7Ah.

ALARM is a positive edge sensitive input, intended for use with a real time clock wakeup alarm. A positive transition on this input will wake up 2020 to Full Operation mode.

COVERSW is an input connected to the external switch and is intended for use with the casecover switch. A level transition on this input will force 2020 to Standby and then into power down mode, or from power down mode to Full Operation mode. Refer to the section of Transitions of Mode Operations.

ACPWR is an active high signal that indicates the system is powered by AC line power. When ACPWR is active, all the internal timers except USR3CR timer for BAKLIT are reset to zero. No mode transitions will occur and the 2020 continues to operate at Full Operation mode. When ACPWR is removed, the values of all registers are not cleared and the 2020 starts its power management function.

PWGDIN is the power on reset signal from power supply. When the system is reset, the PWGDIN pin will be active and will send a power good signal (PWGDOUT) to reset the CPU and core logic.

The PMCGD is the reset signal for 2020 from the battery.

## State Machine Events and Timers

The 2020 has a built-in state machine to automatically control the transitions of mode operations. There are two events and four timers used by the state machine to facilitate the transitions of mode operations.

The OROUT is an event that occurs when all the timers of the trigger inputs defined by Register 5Ah are timed out. The default trigger inputs are KBINT and /VRAM.

The RSOUT is an event that will occur when all the timers of the trigger inputs defined by Register 5Bh are timed out. The default trigger inputs are KBINT, USERIN3, HDCSIN, and FDCSIN pins.

TP1CR timer, TP2CR timer, TP3CR timer, and TP4CR timer are used by the state machine. These timers are used to provide a time delay preset by the Registers 58h and 59h.

TP1CR timer will provide a time delay for entering Standby mode when the case cover is closed or RSOUT occurs in Rest mode.

TP2CR timer will provide a time delay for starting TP4CR timer when entering power down mode from Standby mode because OROUT occurs. When TP2CR is timed out, TP2OUT status register bit will be set to 1.

TP3CR timer will provide a time delay for starting TP4CR timer when entering power down mode from Standby mode because the case cover is closed. When TP3CR timer is timed out, TP3OUT status register bit will be set to 1.

TP4CR timer will provide a time delay when either TP2CR timer or TP3CR timer is timed out when entering into one of the power down modes from Standby mode.

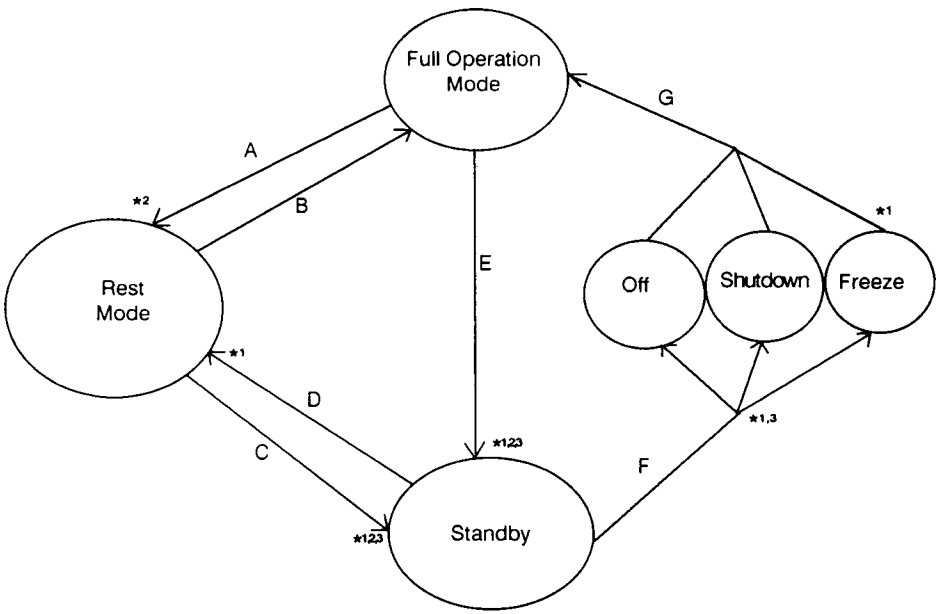
## Transition of Operation Modes

The programmable state machine is preset in such a way that no BIOS effort is required for the system to run in one of the power saving modes when conditions described below are met. Figure 2, 2020 Transition Modes explains the basic state machine sequences.

A: In Full Operation mode, when COVERSW is high (case cover is open) and the event OROUT occurs, the state machine will enter into Rest mode.

B: In Rest mode, when COVERSW is high (case cover is open) and any activity on the trigger inputs defined by Register 5Ah is detected, the state machine goes back to Full Operation mode.

C: In Rest mode, when either COVERSW is low (case cover is closed) or event RSOUT occurs, the state machine will enter into Standby mode. Refer to TP1CR timer register. An /IRQ output will be generated.




*1 Generate /IRQ output

*2 /SPDSW output pin will send a rising pulse when the transition is done

*3 /LOSPD output pin will send an active low signal when the transition is done.

**Figure 2: 2020 Transition of Operation Modes**

D: In Standby mode, three activities let the system go back to Rest mode:

D1. Case cover is opened again and any activity on the trigger inputs defined by Register 5Bh is detected, or
D2. Modem Ring comes in (as described in External Activity Inputs), or
D3. ALARM comes in.

When system goes into Rest mode from Standby mode, an /IRQ output will be generated.

E: In Full Operation mode, when COVERSW is low (case cover is closed) the system will go into Standby mode. Refer to TP1CR timer register 58h. An /IRQ output will be generated.

F: In default setting, the system can stay in Standby Mode as long as the conditions for going back to Rest mode do not occur. To further reduce the power consumption, a user can change the TP2CR and TP3CR default value to let the system go into one of the following power down modes: Off, Shutdown, or Freeze.

Bits 1 and 0 of Register 7Bh selects the power down mode as follows:

| Bit 1 | Bit 0 | Mode |
|---|---|---|
| 0 | 0 | Freeze mode |
| 0 | 1 | Shutdown mode |
| 1 | 0 | Off mode |

In Standby mode, there are two activities to let the system go into power down modes:

F1. The event RSOUT continues to exist for the time set by TP2CR timer, or

F2. After the case is closed for the time set by TP3CR timer. Either TP2CR and TP3CR time out will trigger TP4CR timer. When TP4CR timer is time out the state machine will go into one of the power down modes and 2020 will generate an /IRQ output signal.

G: The following activities will let the system go into Full Operation mode from power down mode:

G1. Case cover is opened again while TP3CR timer is timed out, or
G2. While case cover is open, the cover switch is toggled, or
G3. Modem Ring comes in, or
G4. ALARM comes in, or
G5. Scheduled power-on occurs

The 2020 will generate an /IRQ output signal when changed from Freeze mode to Full Operation Mode.

## 2020 Clock Generation

The 2020 controls the necessary clock sources for the CPU, NPU, AT core logic, etc.

The OSC pin is the 2020 oscillator input pin. This clock source frequency is two times of CPU clock frequency and can be anywhere from 16 MHz to 66 MHz. Pin 16M x 1 and 16M x 2 are the 16 MHz crystal input and output pins providing a 16 MHz OSC16 output for the use of AT Bus clock (SYSCLK) and power down operation. Pin 32K x 1 and pin 32K x 2 are the 32.768 KHz crystal input and output pins for the use of internal timer. The pin 32K x 2 also provides the 32.768 KHz for the use of RTC clock.

The CLKOUT provides the operating frequency for the CPU and core logic. The CLKOUT frequency source can be switched between OSC and the 16Mx1.

In Full Operation mode, the CLKOUT clock source is OSC.

In Rest mode the CLKOUT source is switched to 16 MHz crystal.

In Standby mode, the clock source of CLKOUT is also from 16 MHz crystal. Register 7Dh, Bits 7 and 6 can be programmed to determine the CLKOUT frequency (Refer to Table 1.3 ).

In Freeze mode, the CLKOUT frequency is stopped at 0Hz.

The OSC16 frequency source is the 16 MHz crystal. In Full Operation mode, Rest mode, and Standby mode, the OSC16 output frequency is fixed at 16 MHz and can be used for SYSCLK clock source. In Standby mode, since OSC16 still provides SYSCLK with a steady 16 MHz clock source, any I/O access is still allowed. When in Freeze mode, the OSC16 frequency is stopped at 0 MHz, no I/O access will be allowed.

Some AT core logics have two clock sources, Turbo and Normal, for CPU operation. With the Turbo clock source connected to CLKOUT, /SPDSW signal generated by 2020 can be used to control the core logics' clock switch circuit, such that, Turbo clock for the core logics is enabled when 2020 changes the mode from Full Operation mode to Rest or Standby mode.

During Standby mode and power down modes (Off, Freeze, and Shutdown), the /LOSPD will stay at low to trigger the peripherals into the power saving mode.

## Scheduled Power-on

The 2020 supports scheduled power-on function when the system is in power down modes. Programmable timers are provided in the 2020 to set scheduled power-on time. Register 7Bh, bits 7-5 set the days; Register 7Dh, bits 5-0 set the hours; Register 7Eh, bits 6-0 set the minutes.

**Table 1.3 Standby mode output frequency**

| Mode | Clock source | Register 7Dh Bit 7 | Bit 6 | Divisor | CLKOUT |
|---|---|---|---|---|---|
| Standby Mode | 16 MHz crystal | 0 | 0 | 16 | 1 MHz |
| | | 0 | 1 | 8 | 2 MHz. (Default) |
| | | 1 | 0 | 4 | 4 MHz |
| | | 1 | 1 | 2 | 8 MHz |

## /IRQ

The 2020 generates /IRQ output in mode transitions and battery low to notify the system interrupt handler to perform the necessary hardware or BIOS functions for power management activities. The system interrupt handler can detect the source of /IRQ by examining the mode status of Registers 7Ch and 7Bh. Please refer to Tables 1.4 and 1.5 for distinguishing /IRQ source. The system interrupt handler needs to clear the /IRQ status bit (Bit 5 of 7Ch) before proceeding with the system functions. For example, the /IRQ can be connected to the ACC Micro 2036 NMIIN pin, or the CPU NMI input directly. If desired, the /IRQ can be masked by programming Bit 4 of Register 7Bh.

**Table 1.4 /IRQ Source from Mode Transition**

| /IRQ Source | Register 7Ch | | | Register 7Bh | |
|---|---|---|---|---|---|
| | Bit 7 | Bit 6 | Bit 5 | Bit 1 | Bit 0 |
| From Rest mode to Standby mode | 0 | 1 | 1 | X* | X |
| From Standby mode to Rest mode | 1 | 0 | 1 | X | X |
| From Full Operation mode to Standby mode | 0 | 1 | 1 | X | X |
| From Standby mode to Off mode | 1 | 1 | 1 | 1 | 0 |
| From Standby mode to Shutdown mode | 1 | 1 | 1 | 0 | 1 |
| From Standby mode to Freeze mode | 1 | 1 | 1 | 0 | 0 |
| Resume from Freeze mode to Full Operation mode | 0 | 0 | 1 | 0 | 0 |

**Table 1.5 /IRQ Source from External Activity**

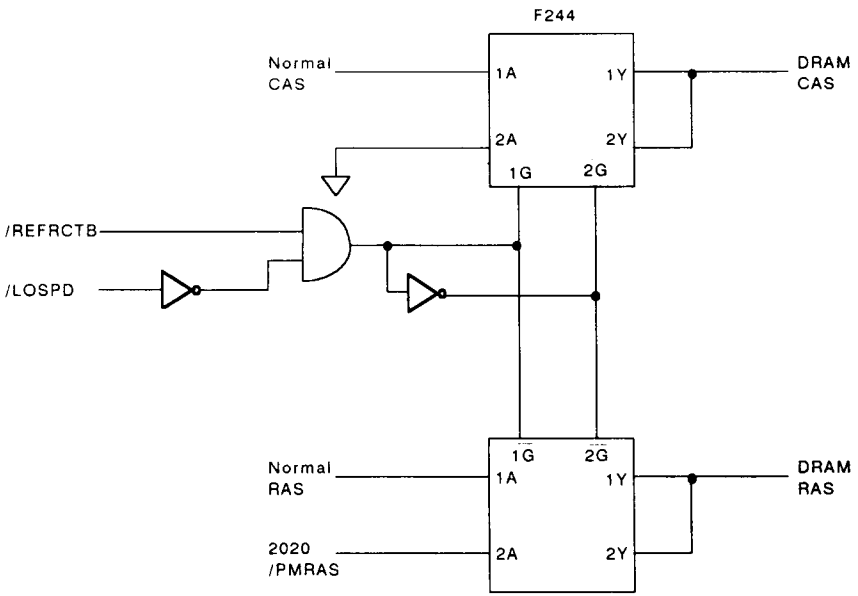
| /IRQ Source | Register 7Ch | Register 7Ch | | | |
|---|---|---|---|---|---|
| | Bit 5 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| From primary battery low | 1 | 1 | X | X | X |
| From secondary battery low | 1 | X | 1 | X | X |
| From Ring | 1 | X | X | 1 | X |
| From Alarm | 1 | X | X | X | 1 |

* X = don't care

## Suspend DRAM Refresh

When the system goes into Freeze or Shutdown mode, the 2020 assumes control of the DRAM refresh. The input pin from the system bus, /REFRESH, is driven active low to activate the 2020 to take over memory refresh function. The 2020 RAS signal for refresh is /PMRAS. The 2020 will perform a CAS before RAS DRAM refresh. The 2020 asserts /REFRCT and /REFRCTB signals to take over the RAS and CAS timing. Fegure 3 is an example of DRAM CAS and RAS generation.

**Figure 3: System RAS and CAS connection to 2020**



## Suspend and Resume Support

Suspend and Resume function is a system feature that allows the user to start an application program (at power up) from where it left off (at power down).

The state machine of 2020 in the default setting will be switching among Full Operation mode, Rest mode, and Standby mode as follows.

### Suspend Sequence

In **Full Operation mode**, the system is running at full system speed. When conditions described in the section on Mode of Transitions are met, the 2020 state machine will go into Rest mode. In the Rest mode, the system is running at 8 MHz. When conditions described in the section on Transitions of Mode Operations are met, the 2020 state machine will go into Standby mode.

In **Standby mode**, the CPU and core logics run at a minimum frequency of 1 MHz. All the register status in CPU and core logics are retained. In such a case, Suspend function is achieved without special BIOS effort, while CPU and AT core logics are running at 1 MHz and memory is refreshed by AT core logics.

To further conserve power, the user can program the 2020 Register 7Bh to go into one of the power down modes: Off, Shutdown, or Freeze.

When the system goes into Standby mode, the 2020 will issue an /IRQ signal, the BIOS can distinguish the /IRQ status and source, then start to perform the power down modes suspend sequence if user desires to further conserve power. The TP2CR timer and TP3CR timer can be programmed to accommodate the time needed for the execution of this power down mode suspend sequence.

In **Off mode**, the DRAM is shut down totally. To support the Suspend and Resume function, the BIOS has to perform suspend sequence to store the contents of all system status on disk while the system goes into Standby mode. When the system goes into Standby mode, the 2020 will issue an /IRQ signal, the BIOS can distinguish the /IRQ status source, then start to perform the Off mode suspend sequence. The timer TP2CR timer and TP3CR timer can be programmed to accommodate the time needed for the execution of this BIOS off mode suspend sequence.

In **Freeze mode**, the DRAM refresh function is assumed by the 2020. As the power supply to CPU and core logic is still on (running at 0Hz) in Freeze mode, the register status for CPU and core logics are also retained if all the registers are implemented in CMOS static circuits such as in the case of ACC Micro 2036. Therefore, there is no need for the system BIOS to issue a suspend sequence to store the system register status.

In the **Shutdown mode**, the DRAM refresh function is also assumed by the 2020. However, the power to the CPU and core logics are off. If the user selects the Shutdown Mode as power down, the BIOS needs to do suspend sequence to save the status of the machine into either disk or memory before entering Shutdown mode.

### Resume Sequence

If the system wakes up from the **Shutdown Mode** when the system is powered up, the PWGOUT will reset the system 0.5 seconds after power on, the AT core logic will take over the refresh from 2020, and the BIOS will execute a resume sequence which will restore the system and core logics registers back from either disk or memory. The resume sequence will restore the system status to the point

where it left off. Refer to Figure 4 for the Resume Power on Sequence from Shutdown mode.

In **Freeze mode**, as the system and core logic status is retained when the system is powered up, there is no reset signal issued. No BIOS resume sequence is required. To resume from the Freeze mode, the 2020 will start providing the turbo frequency for CPU and core logic first, and then the core logic will take over DRAM refresh and issue an IRQ signal to notify the BIOS that the BIOS can begin to access the DRAMs. Refer to Figure 5 for Resume power on Sequence from Freeze mode.

Resume from **Off mode**, is the same as from Shutdown mode, the BIOS will execute a resume sequence to restore CPU and core logic status from disk. Refer to Figure 6 for Resume power on Sequence from Off mode.

**Figure 4: Resume Power on Sequence from Shutdown Mode**

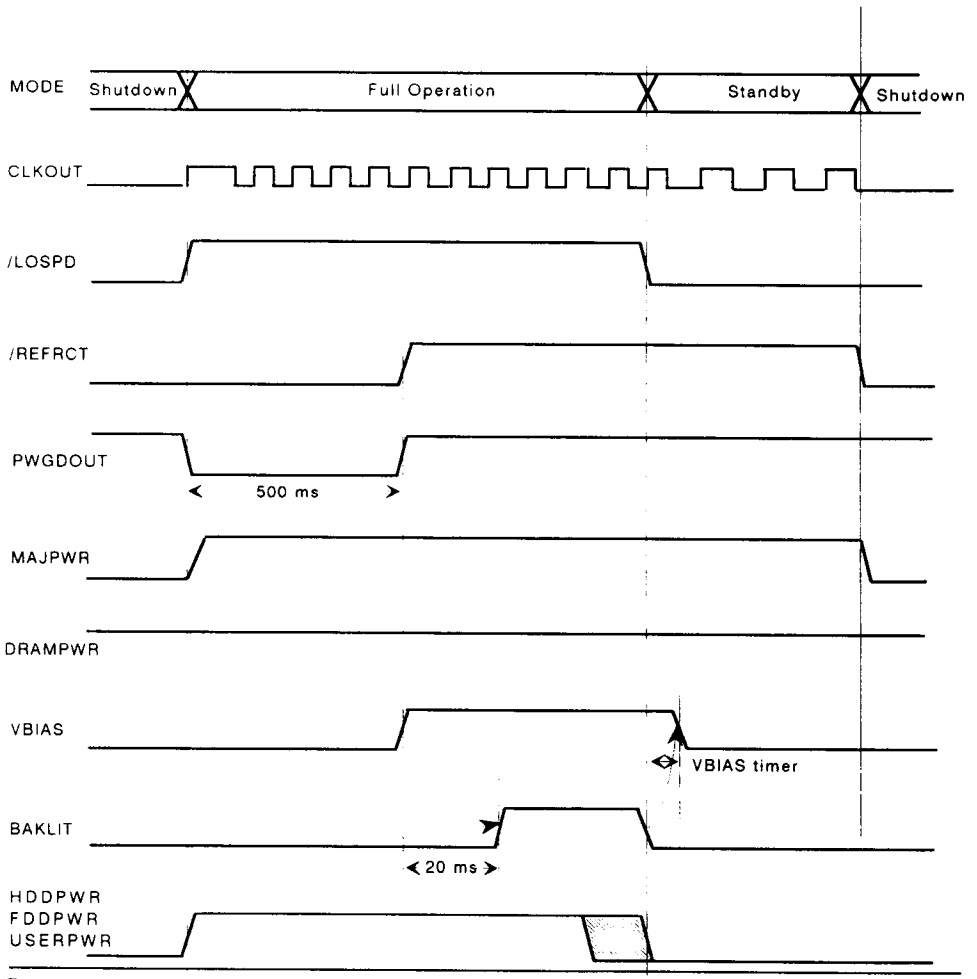


**Figure 5: Resume Power on Sequence from Freeze Mode**

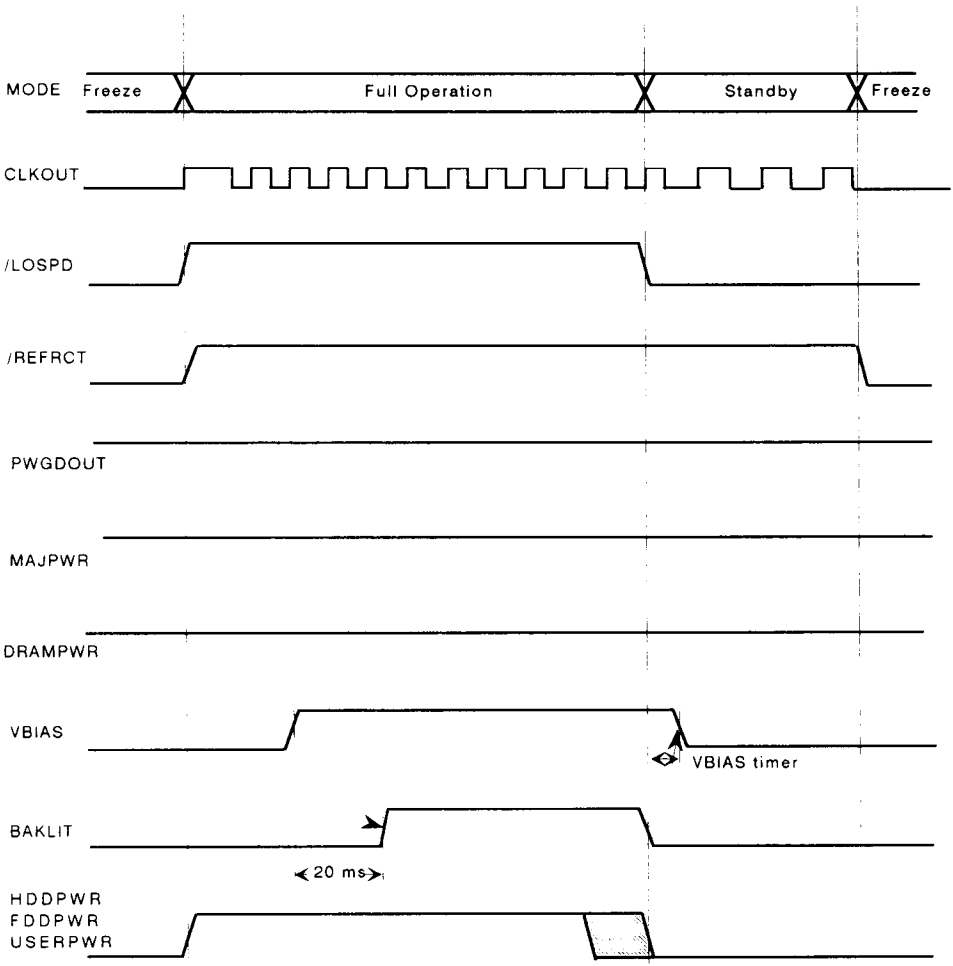
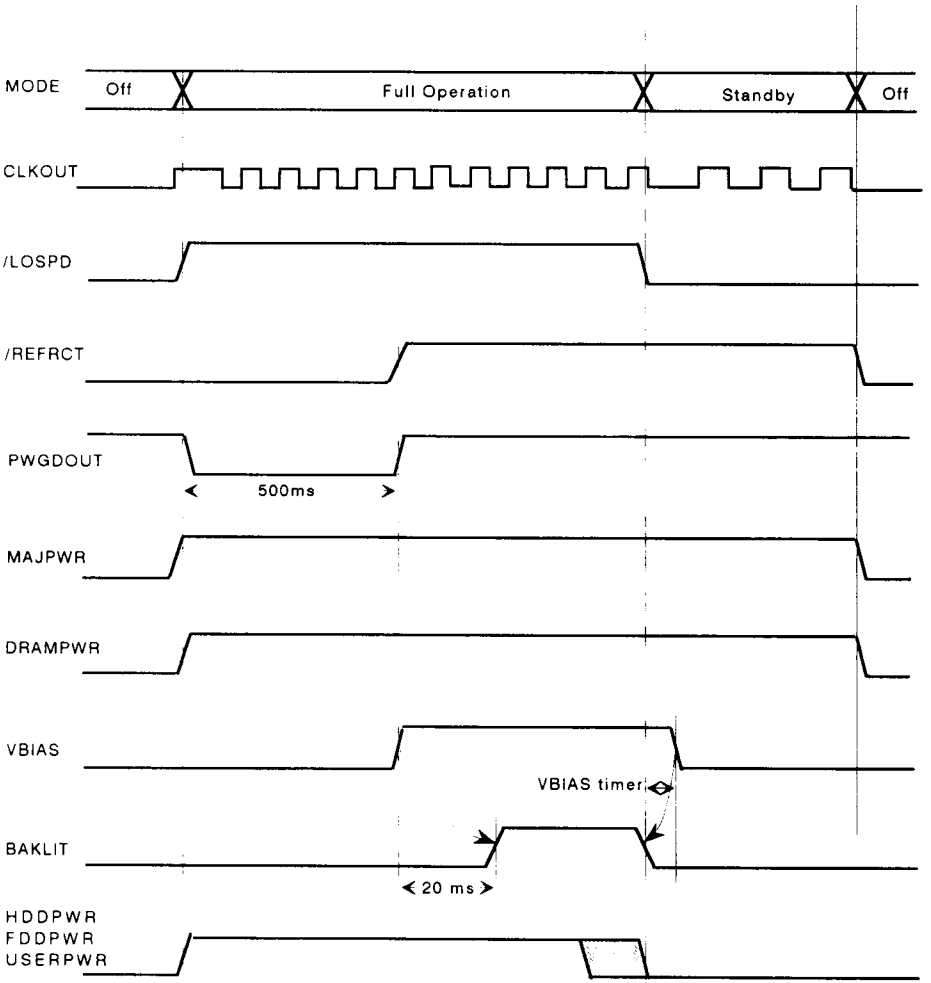


**Figure 6: Resume Power on Sequence from Off Mode**



## Configuration Registers

The 2020 contains 20 configuration registers which provide a variety of functions. Configuration registers are programmed with an indirect addressing scheme. An index register, and a content register are used in this addressing scheme.

The 2020 inputs, SA0, SA1 and /PMCS, define the I/O address for the index register and content register. /PMCS is connected to a chip select signal which will decode address lines from A9 to A2. SA1 and SA0 define the decoded address as an index register (SA1 = 1, SA0 = 0) or a content register (SA1 = 1, SA0 = 1).

For instance, when /PMCS has a decoded (SA9-SA2) chip select signal (0011100) comes in, F2 is selected as the Index register address, F3 is selected as the content register address.

To write a value of "12" into configuration register 54h, the configuration index register at I/O address F2 must first be written with a value of "54," then register at I/O address F3 with a value of "12."

Table 1.5 contains a summary of configuration registers 54h-7Eh

**Table 1.5 ACC 2020 Configuration Registers 54h-7Fh**

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 54h | < | KBCR timer | | >< | | USR1CR | | > |
| 55h | < | VRAMCR timer | | >< | | USR2CR | | > |
| 56h | < | HDCR timer | | >< | | USR3CR | | > |
| 57h | < | FDCR timer | | >< | | USR4CR | | > |
| 58h | < | TP1CR timer | | >< | | TP2CR | | > |
| 59h | < | TP3CR timer | | >< | | TP4CR | | > |
| 5Ah | < | | OROUT trigger source | | | | | > |
| 5Bh | < | | RSOUT trigger source | | | | | > |
| 5Ch | < | Reserved | > | TP2OUT | < | VBIAS timer | | > |
| 5Dh | < | | BAKLIT trigger source | | | | | > |
| 5Eh | < | | HDDPWR trigger source | | | | | > |
| 5Fh | < | | FDDPWR trigger source | | | | | > |
| 78h | < | | MODMPWR trigger source | | | | | > |
| 79h | < | | USERPWR trigger source | | | | | > |
| 7Ah | < | Modem Ring Counter | | > | < | Trigger Input Timer | | > |
| 7Bh | < | Set Day | > | IRQMASK | <PMC Refresh> | | <Select Modes> | |
| 7Ch | <Mode Status> | | IRQ | TP3OUT | LBAT1 | LBAT2 | Ring | Alarm |
| 7Dh | <Stby. Freq. > | | < | | Set Hours | | | > |
| 7Eh | CLKOUT < | | | | Set Minutes | | | > |

**Timer Register 1, 54h**

| Bit | Function |
|---|---|
| 7-4 | KBCR timer provides 1/8-14 sec. |
| 3-0 | USR1CR timer provides 1-15 mins. |

Bit 7-4 Set the time-out period for KBCR timer from 1/8 second to 14 seconds. The default is 8 seconds. The KBCR timer sets the time-out period for trigger input pin KBINT or USERIN1.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 1/8 sec. |
| 0 | 0 | 1 | 0 | 2/8 sec. |
| 0 | 0 | 1 | 1 | 3/8 sec. |
| 0 | 1 | 0 | 0 | 4/8 sec. |
| 0 | 1 | 0 | 1 | 5/8 sec. |
| 0 | 1 | 1 | 0 | 6/8 sec. |
| 0 | 1 | 1 | 1 | 7/8 sec. |
| 1 | 0 | 0 | 0 | 1 sec. |
| 1 | 0 | 0 | 1 | 2 secs. |
| 1 | 0 | 1 | 0 | 4 secs. |
| 1 | 0 | 1 | 1 | 6 secs. |
| 1 | 1 | 0 | 0 | 8 secs(Default) |
| 1 | 1 | 0 | 1 | 10 secs. |
| 1 | 1 | 1 | 0 | 12 secs. |
| 1 | 1 | 1 | 1 | 14 secs. |

Bit 3-0 Set the time-out period for USR1CR timer ranging from 1 minute to 15 minutes. The default of this timer is 2 minutes. The USR1CR timer sets the time-out period for trigger input pins USERIN1 or KBINT.

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 1 min. |
| 0 | 0 | 1 | 0 | 2 mins(Default) |
| 0 | 0 | 1 | 1 | 3 mins. |
| 0 | 1 | 0 | 0 | 4 mins. |
| 0 | 1 | 0 | 1 | 5 mins. |
| 0 | 1 | 1 | 0 | 6 mins. |
| 0 | 1 | 1 | 1 | 7 mins. |
| 1 | 0 | 0 | 0 | 8 mins. |
| 1 | 0 | 0 | 1 | 9 mins. |
| 1 | 0 | 1 | 0 | 10 mins. |
| 1 | 0 | 1 | 1 | 11 mins. |
| 1 | 1 | 0 | 0 | 12 mins. |
| 1 | 1 | 0 | 1 | 13 mins. |
| 1 | 1 | 1 | 0 | 14 mins. |
| 1 | 1 | 1 | 1 | 15 mins. |

**Timer Register 2, 55h**

| Bit | Function |
|---|---|
| 7-4 | VRAMCR timer from 1/8-14 secs. |
| 3-0 | USR2CR timer from 1-15 mins. |

Bit 7-4 Set the time-out period for VRAMCR timer ranging from 1/8 second to 14 seconds. The default is 8 seconds. This timer sets time-out period for trigger input pin VRAM or USERIN2.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 1/8 sec. |
| 0 | 0 | 1 | 0 | 2/8 sec. |
| 0 | 0 | 1 | 1 | 3/8 sec. |
| 0 | 1 | 0 | 0 | 4/8 sec. |
| 0 | 1 | 0 | 1 | 5/8 sec. |
| 0 | 1 | 1 | 0 | 6/8 sec. |
| 0 | 1 | 1 | 1 | 7/8 sec. |
| 1 | 0 | 0 | 0 | 1 sec. |
| 1 | 0 | 0 | 1 | 2 secs. |
| 1 | 0 | 1 | 0 | 4 secs. |
| 1 | 0 | 1 | 1 | 6 secs. |
| 1 | 1 | 0 | 0 | 8 secs(Default) |
| 1 | 1 | 0 | 1 | 10 secs. |
| 1 | 1 | 1 | 0 | 12 secs. |
| 1 | 1 | 1 | 1 | 14 secs. |

Bit 3-0 Set the time-out period for USR2CR timer ranging from 1 minute to 15 minutes. The default is 2 minutes. This timer sets the time-out period for trigger input pin USERIN2 or VRAM.

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 1 min. |
| 0 | 0 | 1 | 0 | 2 mins(Default) |
| 0 | 0 | 1 | 1 | 3 mins. |
| 0 | 1 | 0 | 0 | 4 mins. |
| 0 | 1 | 0 | 1 | 5 mins. |
| 0 | 1 | 1 | 0 | 6 mins. |
| 0 | 1 | 1 | 1 | 7 mins. |
| 1 | 0 | 0 | 0 | 8 mins. |
| 1 | 0 | 0 | 1 | 9 mins. |
| 1 | 0 | 1 | 0 | 10 mins. |
| 1 | 0 | 1 | 1 | 11 mins. |
| 1 | 1 | 0 | 0 | 12 mins. |
| 1 | 1 | 0 | 1 | 13 mins. |
| 1 | 1 | 1 | 0 | 14 mins. |
| 1 | 1 | 1 | 1 | 15 mins. |

**Timer Register 3, 56h**

| Bit | Function |
|---|---|
| 7-4 | HDCR Timer from 1-15 minutes |
| 3-0 | USR3CR Timer 2-210 minutes |

Bit 7-4 Set the time-out period for HDCR timer ranging from 1 minute to 15 minutes. The default is 2 minutes. The HDCR timer can set the time-out period for trigger input pin, HDCSIN or USERIN3.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 1 min. |
| 0 | 0 | 1 | 0 | 2 mins(Default) |
| 0 | 0 | 1 | 1 | 3 mins. |
| 0 | 1 | 0 | 0 | 4 mins. |
| 0 | 1 | 0 | 1 | 5 mins. |
| 0 | 1 | 1 | 0 | 6 mins. |
| 0 | 1 | 1 | 1 | 7 mins. |
| 1 | 0 | 0 | 0 | 8 mins. |
| 1 | 0 | 0 | 1 | 9 mins. |
| 1 | 0 | 1 | 0 | 10 mins. |
| 1 | 0 | 1 | 1 | 11 mins. |
| 1 | 1 | 0 | 0 | 12 mins. |
| 1 | 1 | 0 | 1 | 13 mins. |
| 1 | 1 | 1 | 0 | 14 mins. |
| 1 | 1 | 1 | 1 | 15 mins. |

Bit 3-0 Set the time-out period for USR3CR timer ranging from 2 minutes to 210 minutes. The default is 4 minutes. The USR3CR timer sets the time-out period for trigger input pin USERIN3 or HDCSIN. Since USERIN3 has a larger time scale than /VRAM, the USERIN3 can be used to disable LCD while /VRAM can be used to detect instant idle for entering Rest mode.

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 2 mins. |
| 0 | 0 | 1 | 0 | 4 mins(Default) |
| 0 | 0 | 1 | 1 | 6 mins. |
| 0 | 1 | 0 | 0 | 8 mins. |
| 0 | 1 | 0 | 1 | 10 mins. |
| 0 | 1 | 1 | 0 | 12 mins. |
| 0 | 1 | 1 | 1 | 14 mins. |
| 1 | 0 | 0 | 0 | 16 mins. |
| 1 | 0 | 0 | 1 | 30 mins. |
| 1 | 0 | 1 | 0 | 60 mins. |
| 1 | 0 | 1 | 1 | 90 mins. |
| 1 | 1 | 0 | 0 | 120 mins. |
| 1 | 1 | 0 | 1 | 150 mins. |
| 1 | 1 | 1 | 0 | 180 mins. |
| 1 | 1 | 1 | 1 | 210 mins. |

| Bit 7 | Bit 6 | Bit 5 | Bit4 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 1 min. |
| 0 | 0 | 1 | 0 | 2 mins(Default) |
| 0 | 0 | 1 | 1 | 3 mins. |
| 0 | 1 | 0 | 0 | 4 mins. |
| 0 | 1 | 0 | 1 | 5 mins. |
| 0 | 1 | 1 | 0 | 6 mins. |
| 0 | 1 | 1 | 1 | 7 mins. |
| 1 | 0 | 0 | 0 | 8 mins. |
| 1 | 0 | 0 | 1 | 9 mins. |
| 1 | 0 | 1 | 0 | 10 mins. |
| 1 | 0 | 1 | 1 | 11 mins. |
| 1 | 1 | 0 | 0 | 12 mins. |
| 1 | 1 | 0 | 1 | 13 mins. |
| 1 | 1 | 1 | 0 | 14 mins. |
| 1 | 1 | 1 | 1 | 15 mins. |

**Timer Register 4, 57h**

| Bit | Function |
|---|---|
| 7-4 | FDCR timer from 1 to 15 mins. |
| 3-0 | USR4CR timer from 4 mins. to 7 hrs. |

Bit 7-4 Set the time-out period for FDCR timer ranging from 1 minute to 15 minutes. The default is 2 minutes. The FDCR timer sets the time-out period for trigger input pin FDCSIN or USERIN4.

Bit 3-0 Set the time-out period for USR4CR timer ranging from 4 minutes to 7 hours. The default is 4 minutes. The USR4CR timer sets the time-out period for trigger input pin USERIN4 or FDCSIN.

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 4 min(Default) |
| 0 | 0 | 1 | 0 | 8 mins. |
| 0 | 0 | 1 | 1 | 12 mins. |
| 0 | 1 | 0 | 0 | 16 mins. |
| 0 | 1 | 0 | 1 | 20 mins. |
| 0 | 1 | 1 | 0 | 24 mins. |
| 0 | 1 | 1 | 1 | 28 mins. |
| 1 | 0 | 0 | 0 | 32 mins. |
| 1 | 0 | 0 | 1 | 1 hr. |
| 1 | 0 | 1 | 0 | 2 hrs. |
| 1 | 0 | 1 | 1 | 3 hrs. |
| 1 | 1 | 0 | 0 | 4 hrs. |
| 1 | 1 | 0 | 1 | 5 hrs. |
| 1 | 1 | 1 | 0 | 6 hrs. |
| 1 | 1 | 1 | 1 | 7 hrs. |

**Timer Register 5, 58h**

| Bit | Function |
|---|---|
| 7-4 | TP1CR timer from 1/8-14 secs. |
| 3-0 | TP2CR timer from 1-15 mins. |

Bit 7-4 Set time-out period for TP1CR timer. The TP1CR timer is used by the internal state machine. The default is 4 seconds.

In Rest mode, there are two conditions to trigger this TP1CR timer. The two events are cover case closed or RSOUT time-out. When TP1CR timer is timed out, the state machine will go into standby mode.

In Full Operation mode, when cover case is closed, the TP1CR timer will be used to determine the delay before the state machine going into the standby mode.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 1/8 sec. |
| 0 | 0 | 1 | 0 | 2/8 sec. |
| 0 | 0 | 1 | 1 | 3/8 sec. |
| 0 | 1 | 0 | 0 | 4/8 sec. |
| 0 | 1 | 0 | 1 | 5/8 sec. |
| 0 | 1 | 1 | 0 | 6/8 sec. |
| 0 | 1 | 1 | 1 | 7/8 sec. |
| 1 | 0 | 0 | 0 | 1 sec. |
| 1 | 0 | 0 | 1 | 2 secs. |
| 1 | 0 | 1 | 0 | 4 secs(Default) |
| 1 | 0 | 1 | 1 | 6 secs. |
| 1 | 1 | 0 | 0 | 8 secs. |
| 1 | 1 | 0 | 1 | 10 secs. |
| 1 | 1 | 1 | 0 | 12 secs. |
| 1 | 1 | 1 | 1 | 14 secs. |

Bit 3-0 Set time-out period for TP2CR timer. The TP2CR timer is used by the internal state machine. When Standby mode is entered because RSOUT is timed out, the 2020 state machine will trigger the TP2CR timer. When TP2CR timer is timed out, TP4CR timer will be triggered.

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable(Default) |
| 0 | 0 | 0 | 1 | 1 min. |
| 0 | 0 | 1 | 0 | 2 mins. |
| 0 | 0 | 1 | 1 | 3 mins. |
| 0 | 1 | 0 | 0 | 4 mins. |
| 0 | 1 | 0 | 1 | 5 mins. |
| 0 | 1 | 1 | 0 | 6 mins. |
| 0 | 1 | 1 | 1 | 7 mins. |
| 1 | 0 | 0 | 0 | 8 mins. |
| 1 | 0 | 0 | 1 | 9 mins. |
| 1 | 0 | 1 | 0 | 10 mins. |
| 1 | 0 | 1 | 1 | 11 mins. |
| 1 | 1 | 0 | 0 | 12 mins. |
| 1 | 1 | 0 | 1 | 13 mins. |
| 1 | 1 | 1 | 0 | 14 mins. |
| 1 | 1 | 1 | 1 | 15 mins. |

**Timer Register 6, 59h**

| Bit | Function |
|---|---|
| 7-4 | TP3CR timer from 1/8-14 sec. |
| 3-0 | TP4CR timer from 1-15 mins. |

Bit 7-4 Set time-out period for TP3CR timer ranging from 1/8- second to 14 seconds. The default is disabled. When Standby mode is entered because the COVERSW is activated, the 2020 state machine will trigger the TP3CR timer right away. When TP3CR timer is timed out, TP4CR timer will be triggered.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable(Default) |
| 0 | 0 | 0 | 1 | 1/8 sec. |
| 0 | 0 | 1 | 0 | 2/8 sec. |
| 0 | 0 | 1 | 1 | 3/8 sec. |
| 0 | 1 | 0 | 0 | 4/8 sec. |
| 0 | 1 | 0 | 1 | 5/8 sec. |
| 0 | 1 | 1 | 0 | 6/8 sec. |
| 0 | 1 | 1 | 1 | 7/8 sec. |
| 1 | 0 | 0 | 0 | 1 sec. |
| 1 | 0 | 0 | 1 | 2 secs. |
| 1 | 0 | 1 | 0 | 4 secs. |
| 1 | 0 | 1 | 1 | 6 secs. |
| 1 | 1 | 0 | 0 | 8 secs. |
| 1 | 1 | 0 | 1 | 10 secs. |
| 1 | 1 | 1 | 0 | 12 secs. |
| 1 | 1 | 1 | 1 | 14 secs. |

Bit 3-0 Set time-out period for TP4CR .

The default is 5 minutes. TP4CR timer will be triggered, when either TP2CR or TP3CR timer is timed out.

When TP4CR timer is to provide a time delay defined by the user before entering into Off, Shutdown or Freeze mode.

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Time-out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 1 min. |
| 0 | 0 | 1 | 0 | 2 mins. |
| 0 | 0 | 1 | 1 | 3 mins. |
| 0 | 1 | 0 | 0 | 4 mins. |
| 0 | 1 | 0 | 1 | 5 mins(Default) |
| 0 | 1 | 1 | 0 | 6 mins. |
| 0 | 1 | 1 | 1 | 7 mins. |
| 1 | 0 | 0 | 0 | 8 mins. |
| 1 | 0 | 0 | 1 | 9 mins. |
| 1 | 0 | 1 | 0 | 10 mins. |
| 1 | 0 | 1 | 1 | 11 mins. |
| 1 | 1 | 0 | 0 | 12 mins. |
| 1 | 1 | 0 | 1 | 13 mins. |
| 1 | 1 | 1 | 0 | 14 mins. |
| 1 | 1 | 1 | 1 | 15 mins. |

**OROUT Register, 5Ah**

| Bit | Function |
|---|---|
| 7 | Set 1 to select USERIN4 as input . Default 0. |
| 6 | Set 1 to select USERIN3 as input. Default 0. |
| 5 | Set 1 to select USERIN2 as input. Default 0. |
| 4 | Set 1 to select USERIN1 as input. Default 0. |
| 3 | Set 1 to select FDCSIN as input. Default 0. |
| 2 | Set 1 to select HDCSIN as input. Default 0. |
| 1 | Set 1 to select VRAM as input . Default 1. |
| 0 | Set 1 to select KBINT as input. Default 1. |

Register 5Ah defines the trigger inputs for the OROUT event. The default sources are the KBINT and VRAM trigger inputs.

**RSOUT Register, 5Bh**

| Bit | Function |
|---|---|
| 7 | Set 1 to select USERIN4 as input activity monitoring source, Default 0. |
| 6 | Set 1 to select USERIN3 as input activity monitoring source, Default 1. |
| 5 | Set 1 to select USERIN2 as input activity monitoring source, Default 0. |
| 4 | Set 1 to select USERIN1 as input activity monitoring source, Default 0. |
| 3 | Set 1 to select FDCSIN as input activity monitoring source, Default 1. |
| 2 | Set 1 to select HDCSIN as input activity monitoring source, Default 1. |
| 1 | Set 1 to select VRAM as input activity monitoring source, Default 0. |
| 0 | Set 1 to select KBINT as activity monitoring source, Default 1. |

Register 5Bh defines the trigger inputs for the RSOUT event. The default sources are KBINT, USERIN3, HDCSIN, and FDCSIN.

**VBIASCR Register, 5Ch**

| Bit | Function |
|---|---|
| 7-5 | Reserved |
| 4 | TP2OUT |
| 3-0 | VBIAS time delay register |

Bit 4 This bit is the timeout status bit of TP2CR timer. When power down mode is entered because TP2CR timer is timed out, this bit is set to one. Default is zero.

Bit 3-0 VBIASCR register sets the delay time after the video backlit is timed out for VBIAS output pin to be active low to turn off the LCD BIAS. The default time is 16 milliseconds.

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Delay time |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 4 ms. |
| 0 | 0 | 1 | 0 | 8 ms. |
| 0 | 0 | 1 | 1 | 12 ms. |
| 0 | 1 | 0 | 0 | 16 ms(Default) |
| 0 | 1 | 0 | 1 | 20 ms. |
| 0 | 1 | 1 | 0 | 24 ms. |
| 0 | 1 | 1 | 1 | 28 ms. |
| 1 | 0 | 0 | 0 | 32 ms. |
| 1 | 0 | 0 | 1 | 36 ms. |
| 1 | 0 | 1 | 0 | 40 ms. |
| 1 | 0 | 1 | 1 | 44 ms. |
| 1 | 1 | 0 | 0 | 48 ms. |
| 1 | 1 | 0 | 1 | 52 ms. |
| 1 | 1 | 1 | 0 | 56 ms. |
| 1 | 1 | 1 | 1 | 60 ms. |

**BAKLITCR Register, 5Dh**

| Bit | Function |
|---|---|
| 7 | Set 1 to select USERIN4 as input. Default 0. |
| 6 | Set 1 to select USERIN3 as input. Default 1. |
| 5 | Set 1 to select USERIN2 as input. Default 0. |
| 4 | Set 1 to select USERIN1 as input. Default 0. |
| 3 | Set 1 to select FDCSIN as input. Default 0. |
| 2 | Set 1 to select HDCSIN as input. Default 0. |
| 1 | Set 1 to select VRAM as input. Default 0. |
| 0 | Set 1 to select KBINT as input. Default 0. |

The BAKLITCR Register defines the trigger inputs which control the BAKLIT output pin. The default is the USERIN3 trigger input . When all the trigger inputs of BAKLIT pin are timed out, the BAKLIT pin will change to low to turn off the LCD's back light. If there is any pulse at the trigger input again, the BAKLIT pin state will go back to high to turn on the LCD's back light.

**HDDCR Register, 5Eh**

| Bit | Function |
|---|---|
| 7 | Set 1 to select USERIN4 as input . Default 0. |
| 6 | Set 1 to select USERIN3 as input. Default 0. |
| 5 | Set 1 to select USERIN2 as input. Default 0. |
| 4 | Set 1 to select USERIN1 as input. Default 0. |
| 3 | Set 1 to select FDCSIN as input. Default 0. |
| 2 | Set 1 to select HDCSIN as input. Default 1. |
| 1 | Set 1 to select VRAM as input. Default 0. |
| 0 | Set 1 to select KBINT as input. Default 0. |

HDDCR Register defines the trigger inputs which control the HDDPWR output pin. The default is the HDCSIN input signal.

When all the trigger inputs of HDDPWR pin are timed out, the HDDPWR pin will change to low to turn off the hard disk drive. If there is any pulse at the trigger input again, HDDPWR will change the state to high immediately to turn on the hard disk drive.

**FDDCR Register, 5Fh**

| Bit | Function |
|---|---|
| 7 | Set 1 to select USERIN4 as input. Default 0. |
| 6 | Set 1 to select USERIN3 as input. Default 0. |
| 5 | Set 1 to select USERIN2 as input . Default 0. |
| 4 | Set 1 to select USERIN1 as input . Default 0. |
| 3 | Set 1 to select FDCSIN as input. Default 1. |
| 2 | Set 1 to select HDCSIN as input. Default 0. |
| 1 | Set 1 to select VRAM as input. Default 0. |
| 0 | Set 1 to select KBINT as input. Default 0. |

FDDCR Register defines the trigger inputs which control the FDDPWR output pin. The default is the FDCSIN input signal.

When all the trigger inputs of the FDDPWR pin are timed out, the FDDPWR pin will change to low to turn off the floppy disk drive. If there is any pulse at the trigger input again, FDDPWR will change the state to high immediately to turn on the floppy disk drive.

**MODMCR Register, 78h**

| Bit | Function |
|---|---|
| 7 | Set 1 to select USERIN4 as input. Default 0. |
| 6 | Set 1 to select USERIN3 as input. Default 0. |
| 5 | Set 1 to select USERIN2 as input . Default 0. |
| 4 | Set 1 to select USERIN1 as input. Default 1. |
| 3 | Set 1 to select FDCSIN as input. Default 0. |
| 2 | Set 1 to select HDCSIN as input. Default 0. |
| 1 | Set 1 to select VRAM as input. Default 0. |
| 0 | Set 1 to select KBINT as input. Default 0. |

MODMCR Register defines the trigger inputs which control the MODMPWR output pin. The default source is USERIN1 signal.

When all the trigger inputs of the MODMPWR pin are timed out, the MODMPWR pin will change the state to low to turn off the modem. If there is any pulse at the trigger input again, MODMPWR will change the MODMPWR state to high immediately.

**USRCR Register, 79h**

| Bit | Function |
|---|---|
| 7 | Set 1 to select USERIN4 as input. Default 0. |
| 6 | Set 1 to select USERIN3 as input. Default 0. |
| 5 | Set 1 to select USERIN2 as input. Default 1. |
| 4 | Set 1 to select USERIN1 as input. Default 0. |
| 3 | Set 1 to select FDCSIN as input. Default 0. |
| 2 | Set 1 to select HDCSIN as input. Default 0. |
| 1 | Set 1 to select VRAM as input. Default 0. |
| 0 | Set 1 to select KBINT as input. Default 0. |

USRCR Register defines the trigger inputs which control the USERPWR output pin. The default is the USERIN2 signal.

When all the trigger inputs of USERPWR pin are timed out, the USERPWR pin will change the state to low. If there is any pulse at the trigger input again, USERPWR will change the USERPWR pin state to high immediately.

**RINGCR Register, 7Ah**

| Bit | Function |
|---|---|
| 7-4 | Modem Ring Counter |
| 3-0 | Input Trigger source for timers |

Bit 7-4 Defines the numbers of positive edge transitions on the Ring input pin to wake up the 2020 to Full Operation mode.

These bits need to be read first to be ready to count the incoming Ring pulses. After the Modem Ring Counter is accessed, the read only Modem Ring status bit needs to be cleared to prepare the Modem Ring counter to be used next time.

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Count |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable |
| 0 | 0 | 0 | 1 | 1 time.Default |
| 0 | 0 | 1 | 0 | 2 times |
| 0 | 0 | 1 | 1 | 3 times |
| 0 | 1 | 0 | 0 | 4 times |
| 0 | 1 | 0 | 1 | 5 times |
| 0 | 1 | 1 | 0 | 6 times |
| 0 | 1 | 1 | 1 | 7 times |
| 1 | 0 | 0 | 0 | 8 times |
| 1 | 0 | 0 | 1 | 9 times |
| 1 | 0 | 1 | 0 | 10 times |
| 1 | 0 | 1 | 1 | 11 times |
| 1 | 1 | 0 | 0 | 12 times |
| 1 | 1 | 0 | 1 | 13 times |
| 1 | 1 | 1 | 0 | 14 times |
| 1 | 1 | 1 | 1 | 15 times |

Bit 3 Set 0, select FDCSIN as the trigger input for FDCR timer, USERIN4 for USR4CR timer.

Set 1, select USERIN4 as the trigger input for FDCR timer, FDCSIN for USR4CR timer.

Default = 0.

Bit 2 Set 0, select HDCSIN as the trigger input for HDCR timer, USERIN3 pin for USR3CR timer.

Set 1, select USERIN3 as the trigger input source for HDCR timer, HDCSIN for USR3CR timer.

Default = 0.

Bit 1 Set 0, select /VRAM as the trigger input for VRAMCR timer, USERIN2 pin for USR2CR timer.

Set 1, select USERIN2 as the input trigger for VRAMCR timer, /VRAM pin for USR2CR timer.

Default = 0.

Bit 0 Set 0, select KBINT as the trigger input which controls timer KBCR,KBINT for timer USR1CR.

Set 1, select USERIN1 as the input trigger which controls KBCR timer.

Default = 0.

**Control Register 1, 7Bh**

| Bit | Function |
|---|---|
| 7-5 | Set day for scheduled power on |
| 4 | /IRQ mask bit |
| 3-2 | Select PMC refresh period |
| 1-0 | Select Freeze/Shutdown/Off Mode |

Bit 7-5 These bits can be used to set the day for scheduled power on as shown in table below

| Bit 7 | Bit 6 | Bit 5 | Day |
|---|---|---|---|
| 0 | 0 | 0 | Disable. (Default) |
| 0 | 0 | 1 | 1 day |
| 0 | 1 | 0 | 2 days |
| 0 | 1 | 1 | 3 days |
| 1 | 0 | 0 | 4 days |
| 1 | 0 | 1 | 5 days |
| 1 | 1 | 0 | 6 days |
| 1 | 1 | 1 | 7 days |

Bit 4 This is the /IRQ mask bit. When set to one, this bit disables interrupt request output. Default is zero.

Bit 3-2 These bits can be used to set the refresh period.

| Bit 3 | Bit 2 | Refresh Period |
|---|---|---|
| 0 | 0 | 15 us. (Default) |
| 0 | 1 | 30 us |
| 1 | 0 | 60 us |
| 1 | 1 | 120 us |

Bit 1-0 These bits select the power down modes.

| Bit 1 | Bit 0 | Mode |
|---|---|---|
| 0 | 0 | Freeze Mode. (Default) |
| 0 | 1 | Shutdown Mode |
| 1 | 0 | Off Mode |
| 1 | 1 | Reserved |

**Mode Status Register, 7Ch (Read Only)**

| Bit | Function |
|---|---|
| 7-6 | Mode status |
| 5 | /IRQ status |
| 4 | TP3OUT status |
| 3 | LBAT1 |
| 2 | LBAT2 |
| 1 | Ring |
| 0 | Alarm |

Bit 7-6 These bits indicate the mode status as shown in table below.

| Bit 7 | Bit 6 | Mode |
|---|---|---|
| 0 | 0 | Full Operation Mode.(Default) |
| 0 | 1 | Standby Mode |
| 1 | 0 | Rest Mode |
| 1 | 1 | Shutdown/Freeze/Off Mode |

Each status bit 5-0 needs to be cleared after being accessed. Write any value to 7Ch to clear bits 5-0 of 7Ch.

Bit 5 This bit indicates /IRQ status. When /IRQ is generated during some of the state transitions, this bit will be set to one. Default is zero.

Bit 4 This bit is the timeout status of TP3CR timer. When power down mode is entered because TP3CR timer is timed out, this bit is set to one. Default is zero.

Bit 3 This bit is set to one, when the main battery power is low. Default is zero.

Bit 2 This bit is set to one, when the battery power of 2020 is low. Default is zero.

Bit 1 When RING is counted and finished, this bit is set to one. Default is zero.

Bit 0 When ALARM is active, this bit is set to one. Default is zero.

**Control Register 2, 7Dh**

| Bit | Function |
|---|---|
| 7-6 | Select standby frequency |
| 5-0 | Set hours for schedule power down |

Bit 7-6 These bits can be programmed to select the Standby mode frequency.

| Bit 7 | Bit 6 | Frequency |
|---|---|---|
| 0 | 0 | 1 MHz. |
| 0 | 1 | 2 MHz. (Default) |
| 1 | 0 | 4 MHz. |
| 1 | 1 | 8 MHz. |

Bit 5-0 These bits can be porgrammed to select the elapsed time for scheduled power on.

| Bit 5 | Bit 4 | Time |
|---|---|---|
| 0 | 0 | Disable. (Default) |
| 0 | 1 | 10 hours |
| 1 | 0 | 20 hours |
| 1 | 1 | Reserved |

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Time |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable.(Default) |
| 0 | 0 | 0 | 1 | 1 hr. |
| 0 | 0 | 1 | 0 | 2 hrs |
| 0 | 0 | 1 | 1 | 3 hrs |
| 0 | 1 | 0 | 0 | 4 hrs |
| 0 | 1 | 0 | 1 | 5 hrs |
| 0 | 1 | 1 | 0 | 6 hrs |
| 0 | 1 | 1 | 1 | 7 hrs |
| 1 | 0 | 0 | 0 | 8 hrs |
| 1 | 0 | 0 | 1 | 9 hrs |
| 1 | 0 | 1 | 0 | Reserved |
| 1 | 0 | 1 | 1 | Reserved |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

**Control Register 3, 7Eh**

| Bit | Function |
|---|---|
| 7 | CLKOUT 0Hz level, set 1 to high and set 0 to low. Default = 0. |
| 6-0 | Set minutes for scheduled power-on |

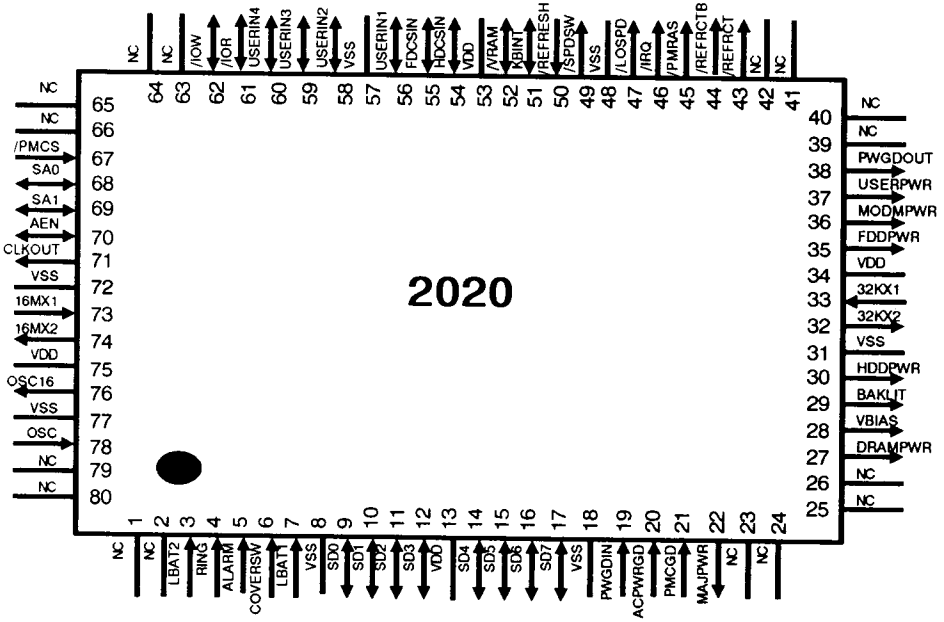
Bit 7 When set to one, the CLKOUT 0 Hz level is high. In Freeze/Shutdown/Off mode, if this bit is set to one, the clock will remain at high level. Default is zero.

Bit 6-0 These bits can be used to set the minutes for scheduled power on as indicated in table below.

| Bit 6 | Bit 5 | Bit 4 | Time |
|---|---|---|---|
| 0 | 0 | 0 | Disable. Default |
| 0 | 0 | 1 | 10 mins. |
| 0 | 1 | 0 | 20 mins. |
| 0 | 1 | 1 | 30 mins. |
| 1 | 0 | 0 | 40 mins. |
| 1 | 0 | 1 | 50 mins. |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Time |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disable(Default) |
| 0 | 0 | 0 | 1 | 1 min. |
| 0 | 0 | 1 | 0 | 2 mins. |
| 0 | 0 | 1 | 1 | 3 mins. |
| 0 | 1 | 0 | 0 | 4 mins. |
| 0 | 1 | 0 | 1 | 5 mins. |
| 0 | 1 | 1 | 0 | 6 mins. |
| 0 | 1 | 1 | 1 | 7 mins. |
| 1 | 0 | 0 | 0 | 8 mins. |
| 1 | 0 | 0 | 1 | 9 mins. |
| 1 | 0 | 1 | 0 | Reserved |
| 1 | 0 | 1 | 1 | Reserved |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

## Pin Diagram


2020
1 NC
2 NC
3 LBAT2
4 RING
5 ALARM
6 COVERSW
7 LBAT
8 VSS
9 SD0
10 SD1
11 SD2
12 SD3
13 VDD
14 SD4
15 SD5
16 SD6
17 SD7
18 VSS
19 PWGDIN
20 ACPWRGD
21 PMCGD
22 MAJPWR
23 NC
24 NC
25 NC
26 NC
27 NC
28 DRAMPWR
29 VBIAS
30 BAKLIT
31 HDDPWR
32 VSS
33 32KX2
34 32KX1
35 VDD
36 FDDPWR
37 MODMPWR
38 USERPWR
39 PWGDOUT
40 NC
41 NC
42 NC
43 NC
44 /REFRCT
45 /REFRCTB
46 /PMRAS
47 /IRQ
48 /LOSPD
49 VSS
50 /SPDSW
51 /REFRESH
52 XBINT
53 /VRAM
54 VDD
55 HDCSIN
56 FDCSIN
57 USERIN1
58 VSS
59 USERIN2
60 USERIN3
61 USERIN4
62 /IOR
63 /IOW
64 NC
65 NC
66 NC
67 /PMCS
68 SA0
69 SA1
70 AEN
71 CLKOUT
72 VSS
73 16MX1
74 16MX2
75 VDD
76 OSC16
77 VSS
78 OSC
79 NC
80 NC

## Pin Descriptions

| Symbol | Pin | Type | Description |
|---|---|---|---|
| **Trigger Inputs** | | | |
| KBINT | 51 | I/O | Monitors keyboard activity. Driven low in Shutdown/Off mode. |
| /VRAM | 52 | I/O | Monitors video activity. Driven low in Shutdown/Off mode. This is an active low pin that is connected to the 2036. |
| HDCSIN | 54 | I/O | Monitors hard disk activity. Driven low in Shutdown/Off mode. |
| FDCSIN | 55 | I/O | Monitor floppy activity. Driven low in Shutdown/Off mode. |
| USERIN1 | 56 | I/O | This pin to be defined by user. Driven low in Shutdown/ Off mode. |
| USERIN2 | 58 | I/O | This pin to be defined by user. Driven low in Shutdown/ Off mode. |
| USERIN3 | 59 | I/O | This pin to be defined by user. Driven low in Shutdown/ Off mode. |
| USERIN4 | 60 | I/O | This pin to be defined by user. Driven low in Shutdown/ Off mode. |
| **Power control Outputs** | | | |
| MAJPWR | 22 | O | Major power control. |
| DRAMPWR | 27 | O | Power control for DRAM. |
| VBIAS | 28 | O | Power control for LCD Bias supply. There is time delay from BAKLIT to turn off VBIAS. |
| BAKLIT | 29 | O | Power control for LCD Backlight. |
| HDDPWR | 30 | O | Power control for hard disk drive. |

## Pin Descriptions

| Symbol | Pin | Type | Description |
|---|---|---|---|
| FDDPWR | 35 | O | Power control for floppy disk drive. |
| MODMPWR | 36 | O | Power control for modem. |
| USERPWR | 37 | O | Power control defined by user. |
| **External Activity Inputs** | | | |
| RING | 4 | I | Used with a modem ring indicator input. Wakes up the system into the Full Operation Mode from the Shutdown/ Freeze/Off Mode. |
| ALARM | 5 | I | Used with a real time clock wakeup alarm. A rising transition wakes up the 2020 to Full Operation Mode. |
| COVERSW | 6 | I | An external switch input used with casecover switch. This input forces PMC to Standby or Shutdown/Freeze/ Off Mode. |
| LBAT1 | 7 | I | Provides warning when main battery low is detected. |
| LBAT2 | 3 | I | Provides warning when PMC battery low is detected. |
| PWGDIN | 19 | I | Power good signal connected from power supply. |
| PWGDOUT | 38 | O | Power good signal connected to the core chip logic. This pin is driven low during Shutdown/Off Mode. |
| ACPWRGD | 20 | I | This signal indicates connection to AC power supply. Disables internal activity timers except the LCD backlight timer. If unused, this pin should be tied low. |

## Pin Descriptions

| Symbol | Pin | Type | Description |
|---|---|---|---|
| **CPU Interface** | | | |
| /IOR | 61 | I/O | Input/Output read strobe. Driven low in Shutdown/Off mode. |
| /IOW | 62 | I/O | Input/Output write strobe. Driven low in Shutdown/Off Mode. |
| AEN | 70 | I/O | Bus hold acknowledge. When asserted, I/O devices ignore address bus. This pin is driven low during Shutdown/Off Mode. |
| /PMCS | 67 | I | Programmable Chip select. |
| PMCGD | 21 | I | PMC power good input. |
| SA0 | 68 | I/O | Local address bus. Driven low during Shutdown/Off Mode. |
| SA1 | 69 | | |
| SD0 | 9 | I/O | System data bus. Driven low during Shutdown/Off Mode. |
| SD1 | 10 | | |
| SD2 | 11 | | |
| SD3 | 12 | | |
| SD4 | 14 | | |
| SD5 | 15 | | |
| SD6 | 16 | | |
| SD7 | 17 | | |
| **Refresh Control** | | | |
| /REFRCT | 43 | O | Signal used to control DRAM refresh during Shutdown/ Freeze Mode. |
| /REFRCTB | 44 | O | Negative signal used to control DRAM refresh during Shutdown/Freeze Mode. |

## Pin Descriptions

| Symbol | Pin | Type | Description |
|---|---|---|---|
| /PMRAS | 45 | O | RAS signal for DRAM refresh during Shutdown/Freeze Mode. |
| /REFRESH | 50 | I | DRAM refresh cycle. Active low. |
| **/IRQ Generator** | | | |
| /IRQ | 46 | O | Interrupt request to the CPU. Driven low in Shutdown/ Off Mode. |
| **Clock Control** | | | |
| OSC | 78 | I | System clock oscillator input. |
| CLKOUT | 71 | O | System clock oscillator output for core logic. |
| /SPDSW | 49 | O | Active high signal to force the system core logic using Turbo clock source. |
| /LOSPD | 47 | O | Active low signal to engage peripheral into power saving mode. |
| 32K x 1 | 33 | I | 32.768 KHz crystal input. |
| 32K x 2 | 32 | O | 32.768 KHz crystal output. |
| 16M x 1 | 73 | I | 16 MHz crystal input. |
| 16M x 2 | 74 | O | 16 MHz crystal output. |
| OSC16 | 76 | O | 16 MHz clock output for core logic. |
| VDD | 13,34, 53,75 | | +5 Volts |
| VSS | 8,18, 31,48, 57,72,77 | | Ground |
| NC | 1,2,23, 24,25,26, 39,40, 41, 42,63,64, 65,66,79,80 | | |

## Rating Specifications

**Absolute Maximum Ratings***

TA = 25° C

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Power supply voltage | VDD | -0.5 | 6.5 | V |
| Input, Output voltage | Vin<br>Vout | -0.3 | VDD +0.3 | V |
| DC Current Drain per Pin any input or output | I | | 25 | mA |
| DC Current Drain VSS and VDD Pins | I | | 100 | mA |
| Storage Temperature | Tstg | -65 | 150 | °C |
| Lead Temperature less than 10sec. solder | TI | | 250 | °C |
| Operating Temperature Commercial | Toper | 0 | 70 | °C |

* Exposing the device to stresses above those listed can cause permanent damage. The maximum rating is a stress rating only, and functional operation at the maximum is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

## Capacitance

TA = +25° C, VDD = 5 V

| Parameter | Symbol | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| Input Capacitance | Cin | | 10 | pF | fc = 1 MHz unmeasured pins to ground |
| Output Capacitance | Cout | | 10 | pF | |
| I/O Capacitance | Ci/o | | 10 | pF | |

## DC Specifications

TA = 0° C to +70° C, VDD = +5 V +/- 10%

LBAT2, LBAT1, OSC, RING, ALARM, COVERSW, PWGDIN, ACPWRGD, PMCGD

| Parameter | Symbol | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| Input low voltage | VIL | | 0.8 | V | VDD = 5 +/- 10% |
| Input high voltage | VIH | 2.0 | | V | VDD = 5 +/- 10% |
| Input low current | IIL | | -10.0 | uA | VIN = 0.0V |
| Input high current | IIH | | 10.0 | uA | VIN = 5V |

MAJPWR, DRAMPWR, VBIAS, BAKLIT, HDDPWR, FDDPWR, MODMPWR, USERPWR

| Parameter | Symbol | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| Output low voltage | VOL | | 0.4 | V | IOL=2mA |
| Output high voltage | VOH | 2.4 | | V | IOH=-2mA |

PWGDOUT, /REFRCT, /REFRCTB, /PMRAS, /IRQ, /LOSPD, /SPDSW, OSC16

| Parameter | Symbol | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| Output low voltage | VOL | | 0.4 | V | IOL=6mA |
| Output high voltage | VOH | 2.4 | | V | IOH=-6mA |

CLKOUT

| Parameter | Symbol | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| Output low voltage | VOL | | 0.4 | V | IOL=12mA |
| Output high voltage | VOH | 2.4 | | V | IOH=-12mA |

SD0-SD7

| Parameter | Symbol | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| Input low voltage | VIL | | 0.8 | V | DD =5V±10% |
| Input high voltage | VIH | 2.0 | | V | VDD=5V±10% |
| Input low current | IIL | | -10 | uA | VIN=VSS |
| Input high current | IIH | | 10 | uA | VIN=VDD |
| Output low voltage | VOL | | 0.4 | V | IOL=12mA |
| Output high voltage | VOH | 2.4 | | V | IOH=-12mA |
| Tristate output leakage current | IOZ | -10 | 10 | uA | VSS<VOUT<VDD |

/REFRESH, KBINT, /VRAM, HDCSIN, FDCSIN, USERIN1, USERIN2, USERIN3, USERIN4, /IOR, /IOW, /PMCS, SA0, SA1, AEN

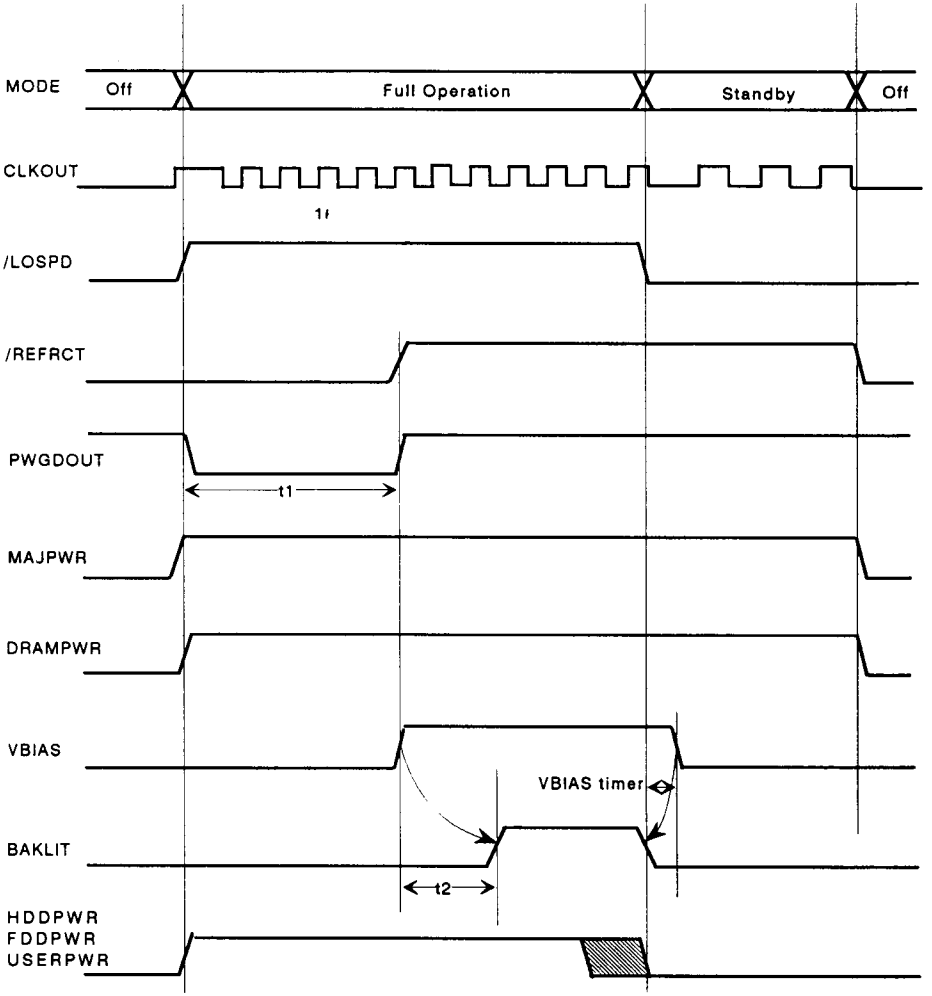
| Parameter | Symbol | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| Input low voltage | VIL | | 0.8 | V | VDD=5V±10% |
| Input high voltage | VIH | 2.0 | | V | VDD=5V±10% |
| Input low current | IIL | | -10 | uA | VIN=VSS |
| Input high current | IIH | | 10 | uA | VIN=VDD |
| Output low voltage | VOL | | 0.4 | V | IOL=2mA |
| Output high voltage | VOH | 2.4 | | V | IOH=-2mA |
| Tristate output leakage current | IOZ | -10 | 10 | uA | VSS<VOUT<VDD |

## AC Specifications

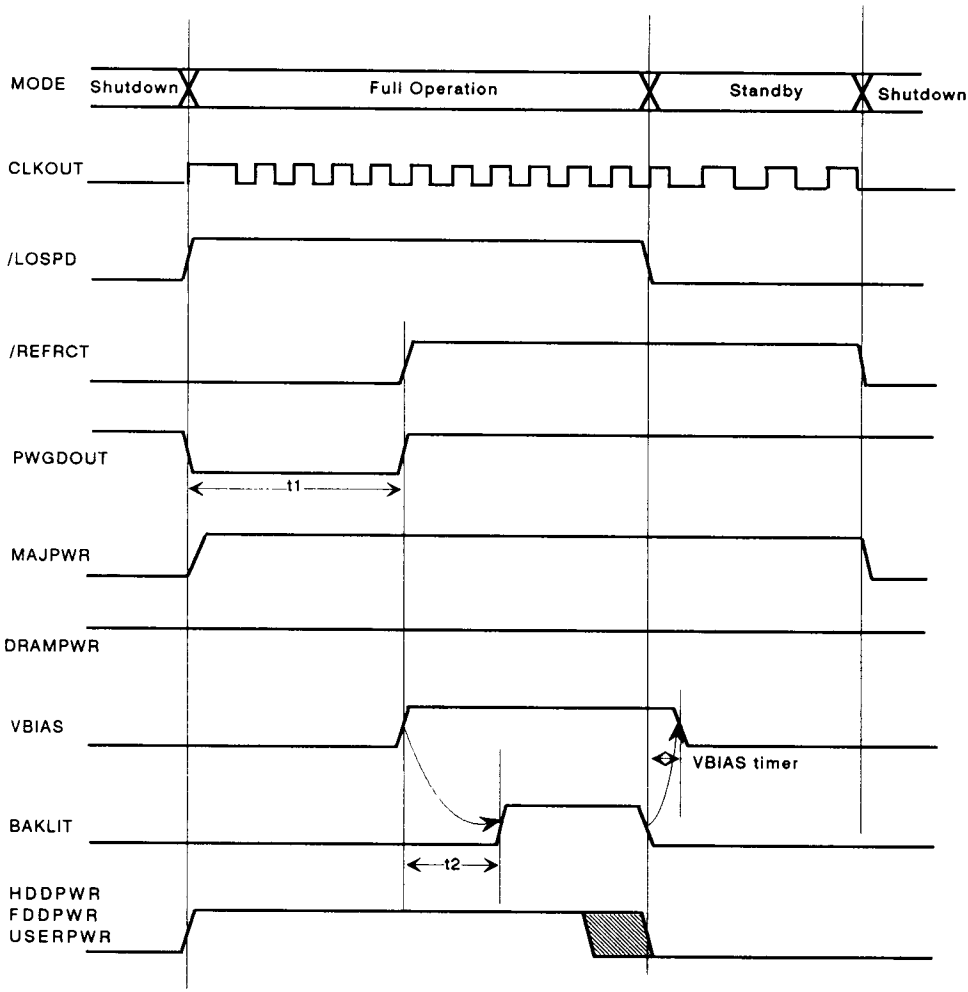
**TA = 0°C to 70°C, VCC = +5V ± 10%**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| t1 | PWGDOUT width | 500 | 1000 | ms |
| t2 | BAKLIT delay time from VBIAS | 15.625 | 31.25 | ms |
| t3 | OSC to CLKOUT delay time | 4 | 13.6 | ns |
| t4 | High pulse width | 7 | | ns |
| t5 | Low pulse width | 7 | | ns |
| t6 | Trigger input pulse width | 20 | | ns |
| t7 | Write data setup time | 12 | | ns |
| t8 | Write data hold time | 5 | | ns |
| t9 | Valid read data time | 9 | 30 | ns |
| t10 | Read data hold time | 5 | 20 | ns |
| t11 | Mode switch delay time from COVERSW | | 30 | us |
| t12 | COVERSW low pulse width for mode switch | 720 | | us |
| t13 | Mode switch delay time from ALARM | | 30 | us |

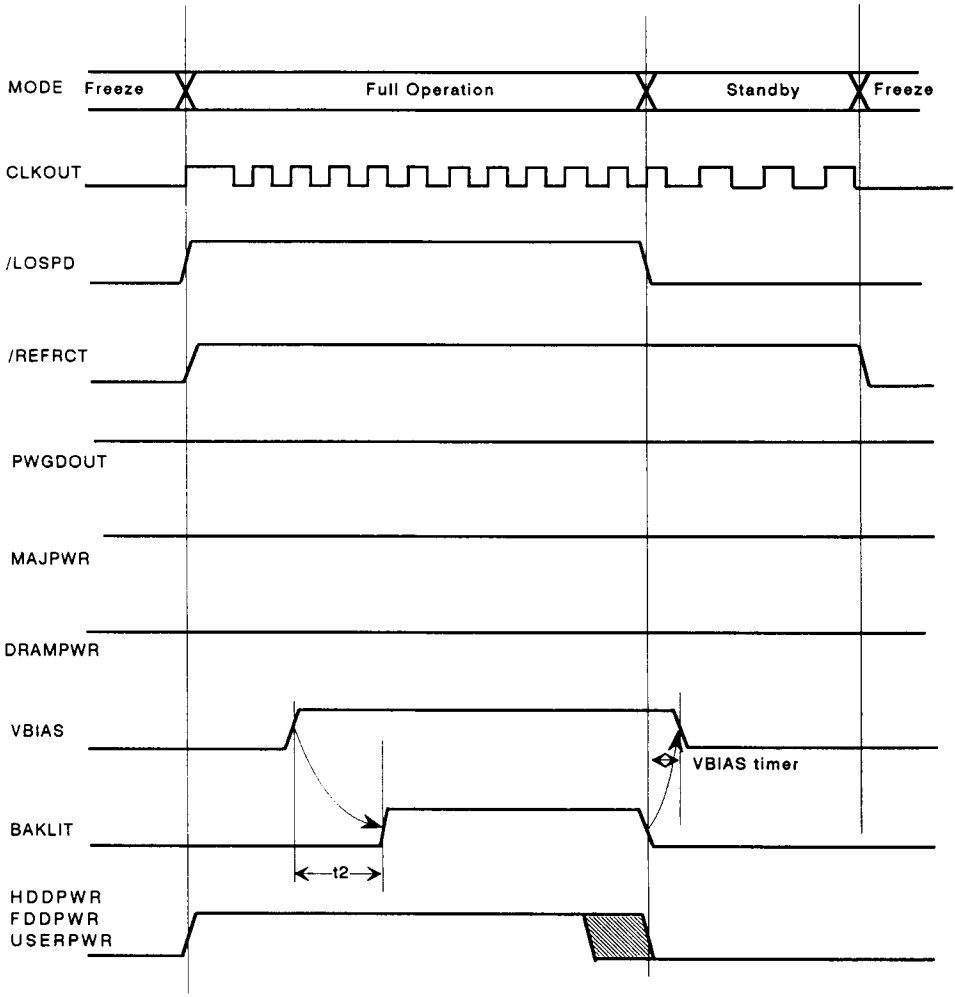
## Off Mode Timing



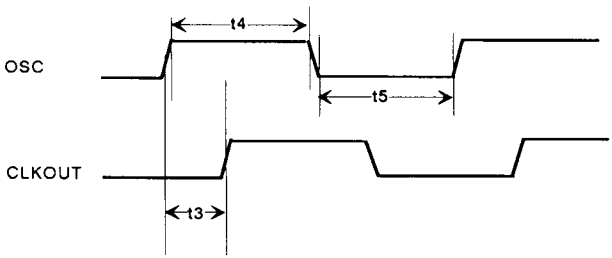
## Shutdown Mode Timing



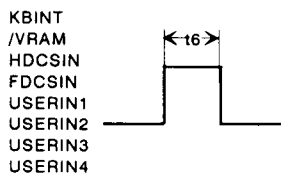
## Freeze Mode Timing



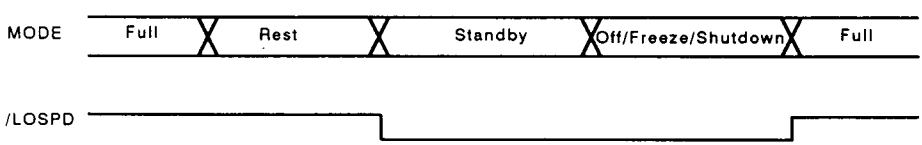
## Clock Timing



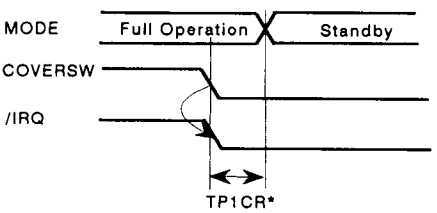

## Trigger Inputs Timing

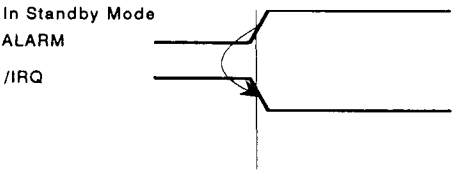


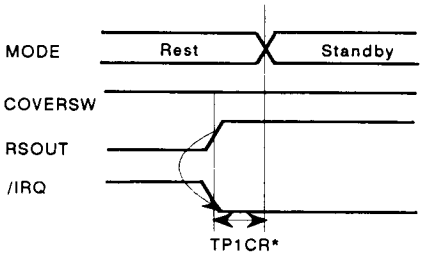

## /LOSPD Timing

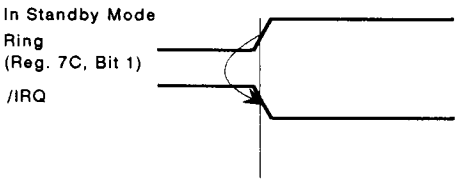


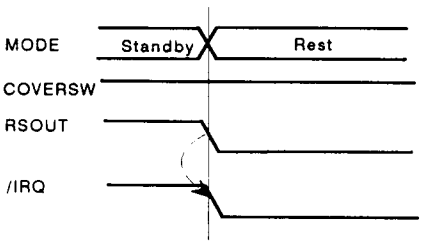
## /IRQ Timing

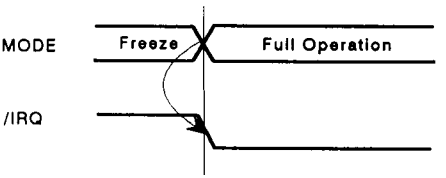


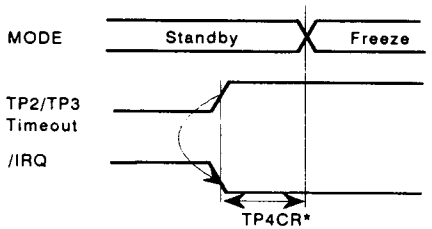



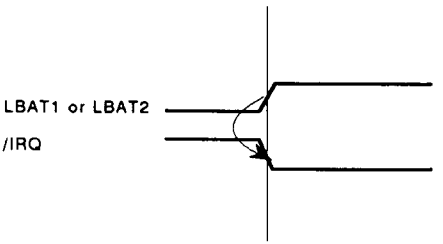



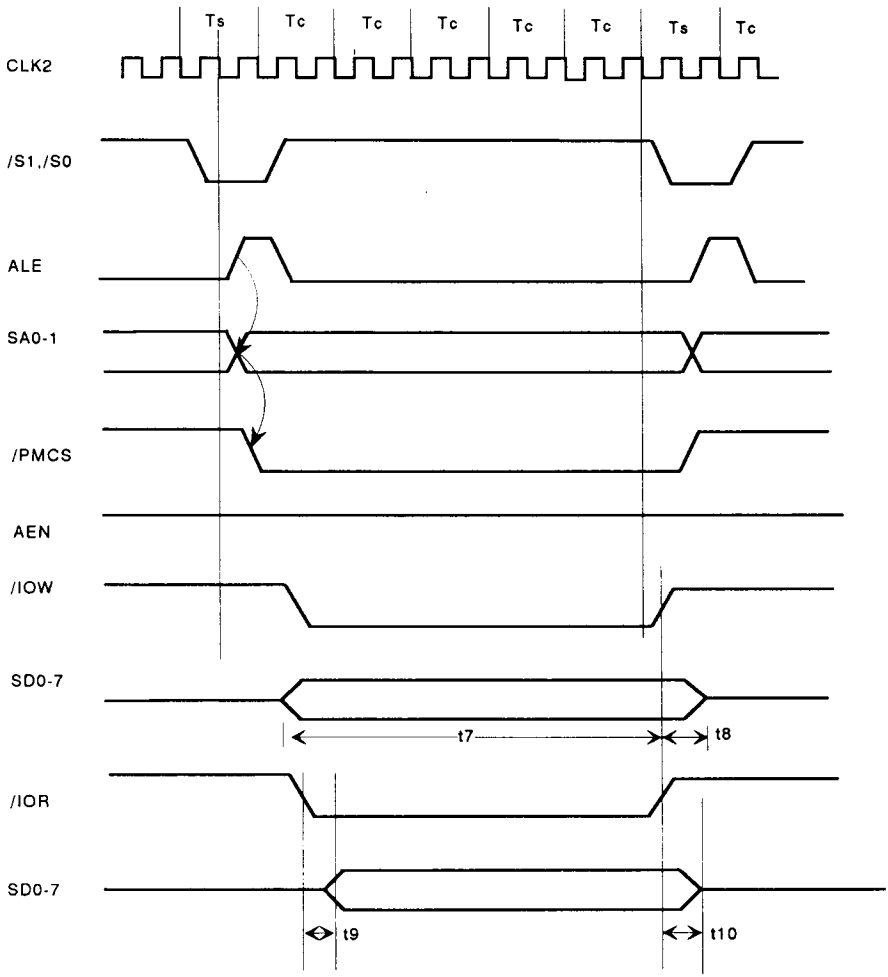



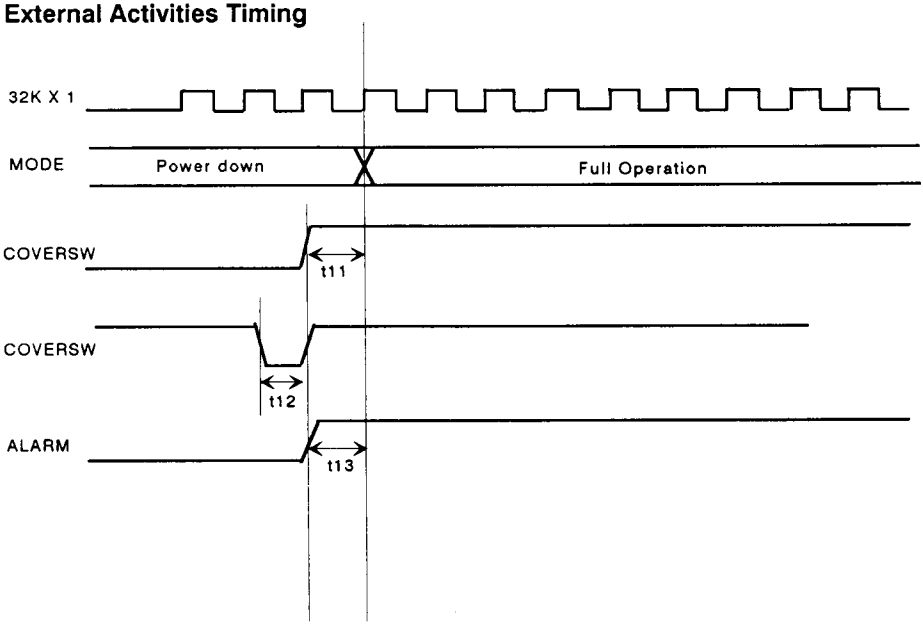




* Programmable delay timer.

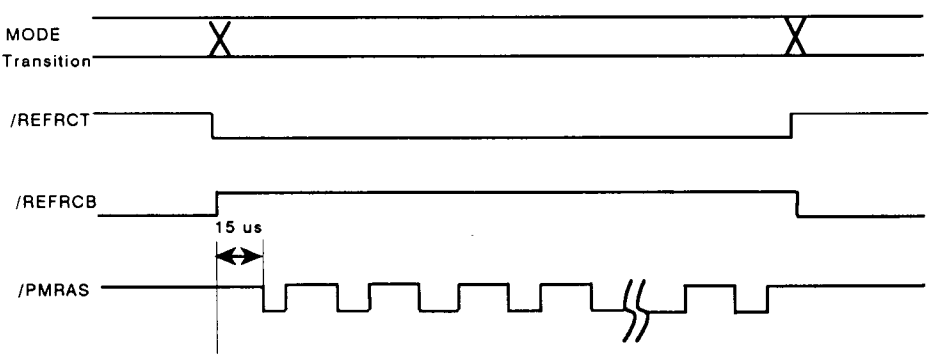
## AT Bus Interface Timing



## External Activities Timing

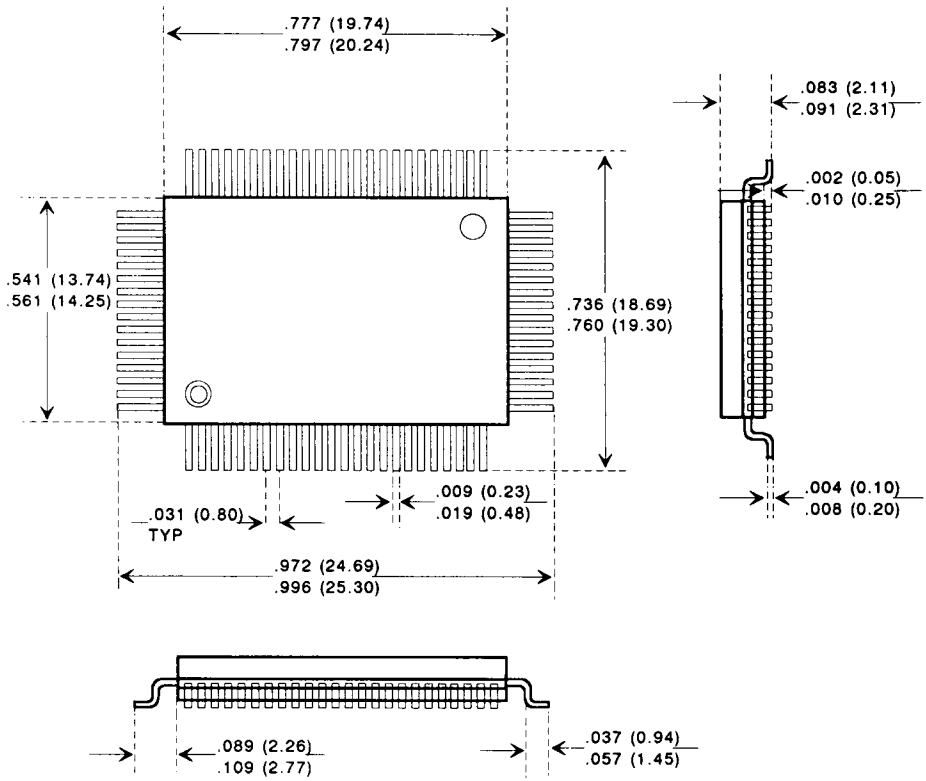



## Refresh Signals Relationship



## Production Package Specification

**Package:** 80-pin PQFP
**Unit:** inches (mm.)
**Chip:** 2020



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P/N 520069 Rev 1.1 2/17/92



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