ACE93C46A/56A/66A
Three-wire Serial EEPROM

Description

The ACE93C46A/56A/66A series are 1024/2048/4096 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM. They are organized as 64/128/256 words of 16 bits each when the ORG pin is connected to VCC (or unconnected) and 128/256/512 words of 8 bits (1 byte) each when the ORG pin is tied to ground. The devices are fabricated with proprietary advanced CMOS process for low power and low voltage applications. These devices are available in standard 8-lead DIP, 8-lead JEDEC SOP, 8-lead TSSOP and 8-lead DFN packages. Our extended V_{CC} range (1.8V to 5.5V) devices enables wide spectrum of applications.

The ACE93C46A/56A/66A is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SCL). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. Once a device begins its self-timed program procedure, the data out pin (DO) can indicate the READY/BUSY status by rising chip select (CS).

Features

- Standard Voltage and Low Voltage Operation:
  ACE 93C46A/56A/66A: VCC = 1.8V to 5.5V
- User Selectable Internal Organization:
  ACE 93C46A:128 x 8 or 64 x 16
  ACE 93C56A:256 x 8 or 128 x 16
  ACE 93C66A:512 x 8 or 256 x 16
- 2 MHz Clock Rate (5V) Compatibility.
- Industry Standard 3-wire Serial Interface.
- Self-Timed ERASE/WRITE Cycles (5ms max including auto-erase).
- Automatic ERAL before WRAL.
- Sequential READ Function.
- High Reliability: Typical 1 Million Erase/Write Cycle Endurance.
- 100 Years Data Retention.
- Industrial Temperature Range (-40o C to 85o C).
- Standard 8-pin DIP/SOP/TSSOP/DFN Pb-free Packages

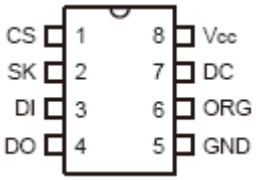
Absolute Maximum Ratings

Industrial operating temperature	-40oC to 85oC
Storage temperature	-50oC to 125oC
Input voltage on any pin relative to ground	-0.3V to VCC + 0.3V
Maximum voltage	8V

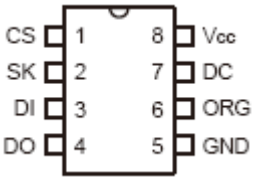
*Notice: Stresses exceed those listed under “Absolute Maximum Rating” may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality.

Packaging Type

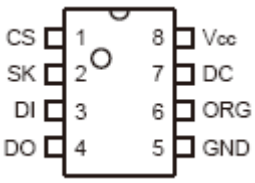
DIP-8



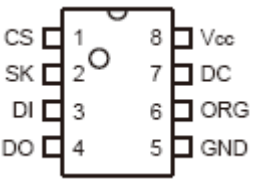
TSSOP-8



SOP-8



DFN-8



Pin Configurations

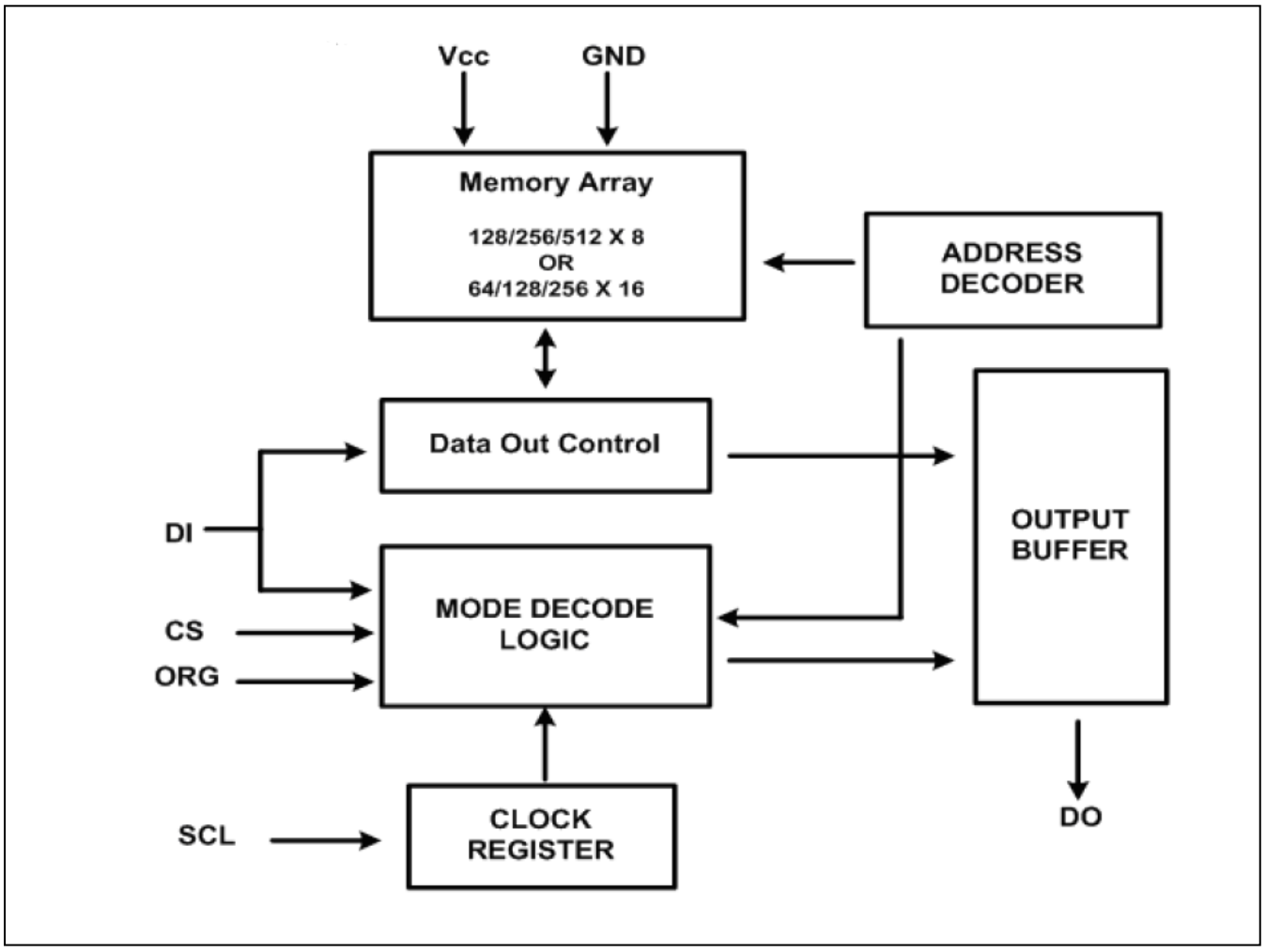
NO	Pin Name	Function
1	CS	Chip select
2	SK	Serial Data Clock
3	DI	Serial Data Input
4	DO	Serial Data Output
5	GND	Ground
6	Vcc	Power Supply
7	ORG	Internal Organization
8	DC	Don’t Connect

Ordering information

ACE93C46A/56A/66A XX + X H

- H : Halogen-free
- X : U : Tube / T : Tape and Reel
- + : Pb - free
- XX : DP : DIP-8 / FM : SOP-8 / TM : TSSOP-8 / DM : TDFN-8

Block Diagram



Pin Descriptions

(A) SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the rising edge of this clock is to clock data out of the EEPROM device.

(B) CHIP SELECT (CS)

This is the chip select input signal for the serial EEPROM device. .

(C) SERIAL DATA INPUT (DI)

This is data input signal for the serial device.

(D) SERIAL DATA OUTPUT (DO)

This is data output signal for the serial device.

(E) INTERNAL ORGANIZATION (ORG)

This is internal organization input signal for the serial EEPROM device. When the ORG pin is connected to VCC or unconnected the EEPROM is organized as 64/128/256 word of 16 bits each and when ORG pin is connected to ground the EEPROM is organized as 128/256/512 byte of 8 bits each. Typically, these signals are hardwired to either V_{IH} or V_{IL}. If left unconnected, they are internally recognized as V_{IH}.

Memory Organization

The ACE93C46A/56A/66A memory is organized either as bytes (x8) or as words (x16). If Internal Organization (ORG) is unconnected (or connected to VCC) the words (x16) organization is selected; When Internal Organization is connected to ground the bytes (x8) organization is selected.

Instruction set

Instruction	Device Type	SB	Op code	Address		Data		Comments
				*8 (1) (2)	*16 (1) (3)	*8	*16	
READ	ACE93C46A ACE93C56A ACE93C66A	1 1 1	10 10 10	A_6-A_0 A_8-A_0 A_8-A_0	A_5-A_0 A_7-A_0 A_7-A_0			Reads date stored in memory, at specified address.
EWEN	ACE93C46A ACE93C56A ACE93C66A	1 1 1	00 00 00	11XXXXX 11XXXXXXX 11XXXXXXX	11XXXX 11XXXXXX 11XXXXXX			Write enable must precede all programming modes.
EWDS	ACE93C46A ACE93C56A ACE93C66A	1 1 1	11 11 11	00XXXXX 00XXXXXXX 00XXXXXXX	00XXXX 00XXXXXX 00XXXXXX			Disables all programming instructions.
ERASE	ACE93C46A	1	01	A_6-A_0	A_5-A_0			Erase memory

	ACE93C56A ACE93C66A	1 1	01 01	A_8-A_0 A_8-A_0	A_7-A_0 A_7-A_0			location A_n- A_0.
WRITE	ACE93C46A ACE93C56A ACE93C66A	1 1 1	00 00 00	A_6-A_0 A_8-A_0 A_8-A_0	A_5-A_0 A_7-A_0 A_7-A_0	D_7-D_0 D_7-D_0 D_7-D_0	D_{15}-D_0 D_{15}-D_0 D_{15}-D_0	Writes memory location A_n-A_0.
ERAL	ACE93C46A ACE93C56A ACE93C66A	1 1 1	00 00 00	10XXXXX 10XXXXXXX 10XXXXXXX	10XXXX 10XXXXXX 10XXXXXX			Erases all memory locations.
WRAL	ACE93C46A ACE93C56A ACE93C66A	1 1 1	00 00 00	01XXXXX 01XXXXXXX 01XXXXXXX	01XXXX 01XXXXX 01XXXXX	D_7-D_0 D_7-D_0 D_7-D_0	D_{15}-D_0 D_{15}-D_0 D_{15}-D_0	Writes all memory locations.

(A) START BIT (SB)

Each instruction is preceded by a rising edge on Chip Select (CS) with Serial Clock (SCL) being held Low.

(B) OPERATION CODE (OP-CODE)

Two op-code bits, read on Serial Data Input (DI) during the rising edge of Serial Clock (SCL).

(C) ADDRESS

The address bits of the byte or word that is to be accessed. For the ACE93C46A, the address is made up of 6 bits for the x16 organization or 7 bits for x8 organization. For the ACE93C56A, the address is made up of 7 bits for the x16 organization or 8 bits for x8 organization. For the ACE 93C66A, the address is made up of 8 bits for the x16 organization or 9 bits for x8 organization.

(D) DATA

The data bits of the byte or word that is to be accessed. For the ACE93C46A/56A/66A, the data is made up of 16 bits (word) for the x16 organization or 8 bits (byte) for x8 organization.

Instruction Sets Description

(A) READ

The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that when a dummy bit (logic “0”) precedes the 8- or 16-bit data output string.

(B) ERASE/WRITE ENABLE

To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

(C) ERASE/WRITE DISABLE

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

(D) ERASE

The Erase (ERASE) instruction programs all bits in the specified memory location to the logical "1" state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{cs}). A logic "1" at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

(E) WRITE

The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{wp}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{tp}). A logic "0" at DO indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A READY/BUSY status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{wp}.

(F) ERASE ALL

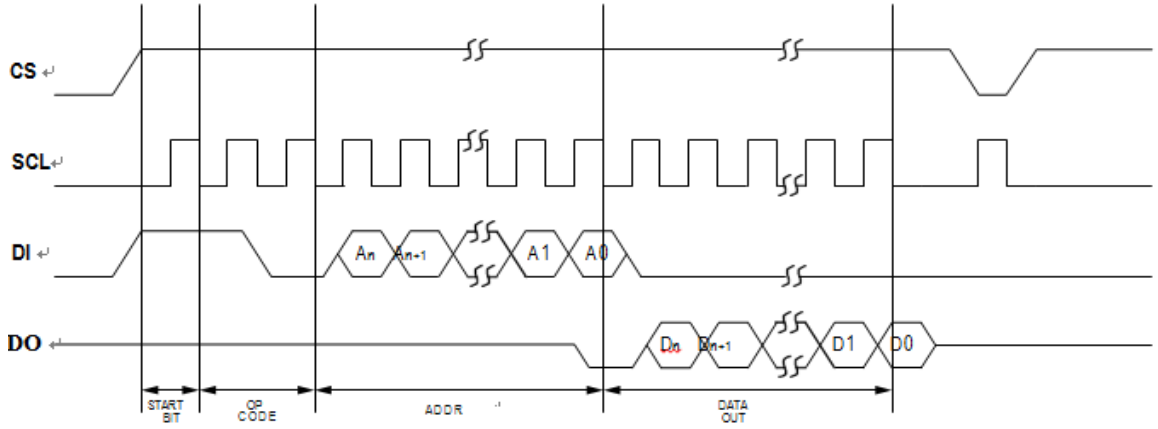
The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ±10%.

(G) WRITE ALL

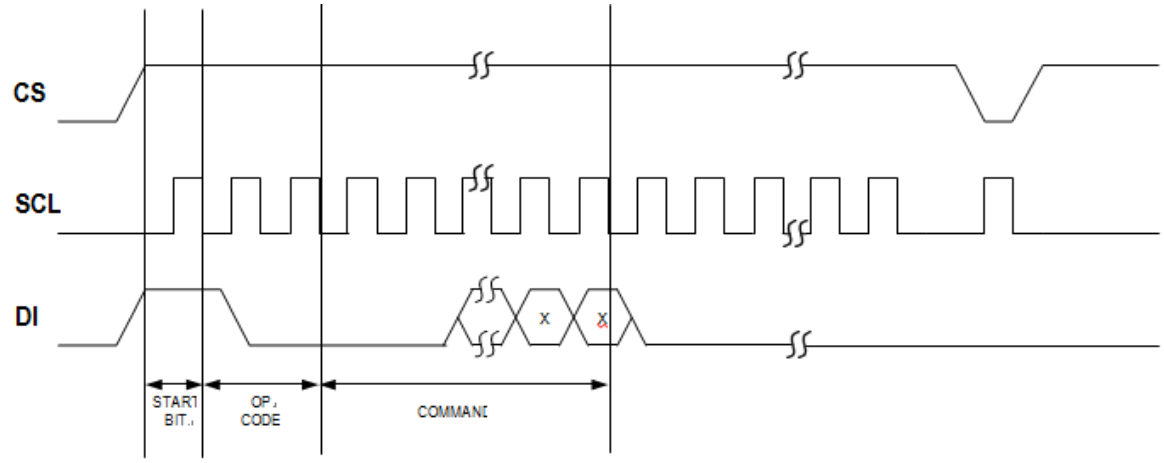
The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

Timing Diagrams

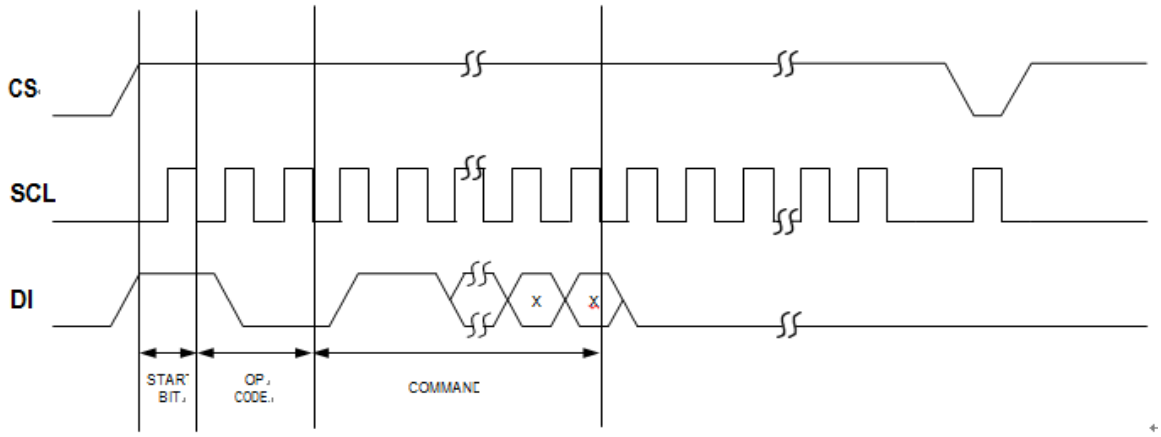
READ Timing



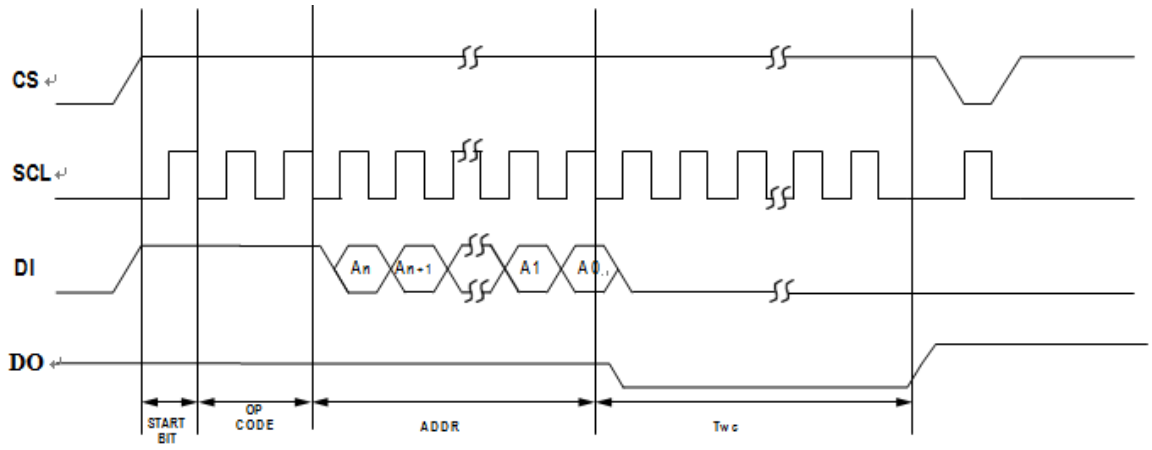
EWDS Timing



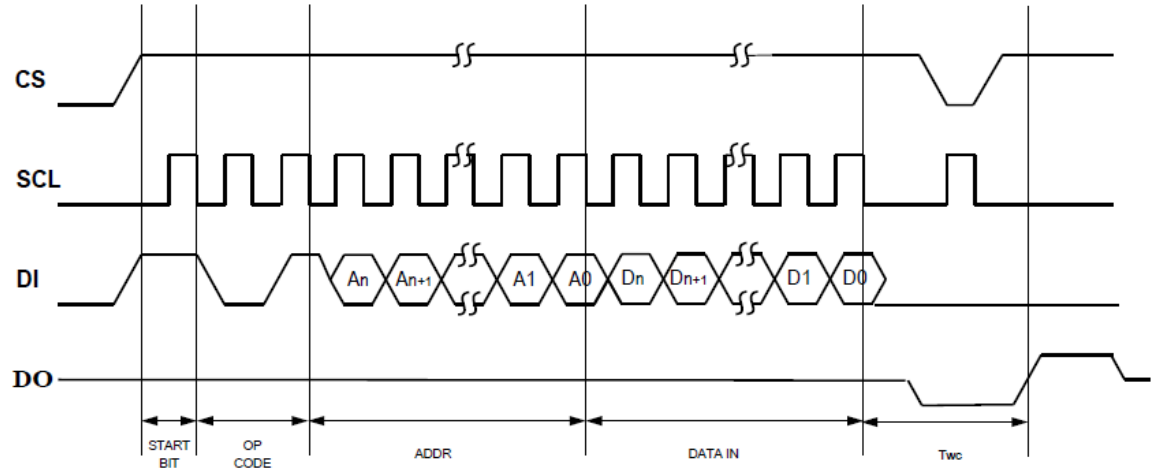
EWEN Timing



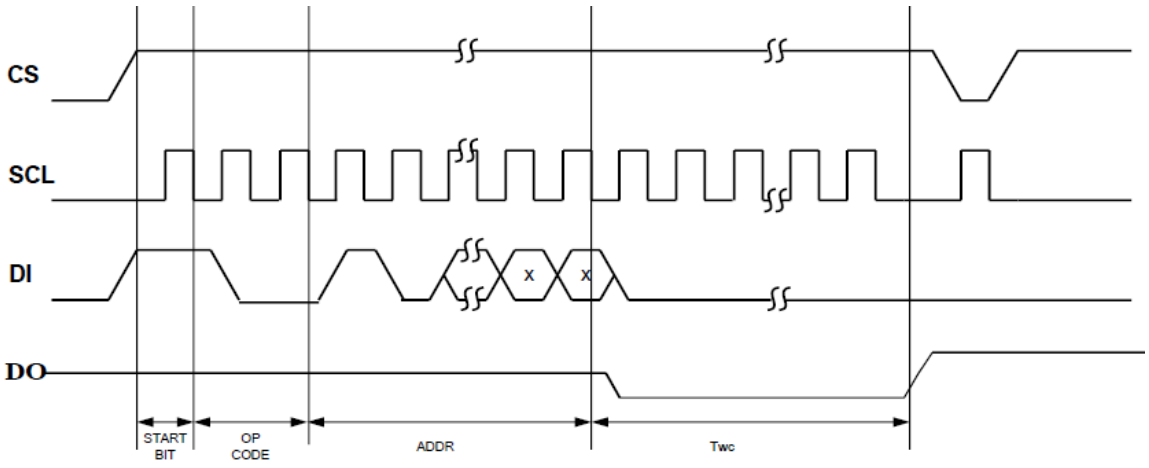
ERASE Timing



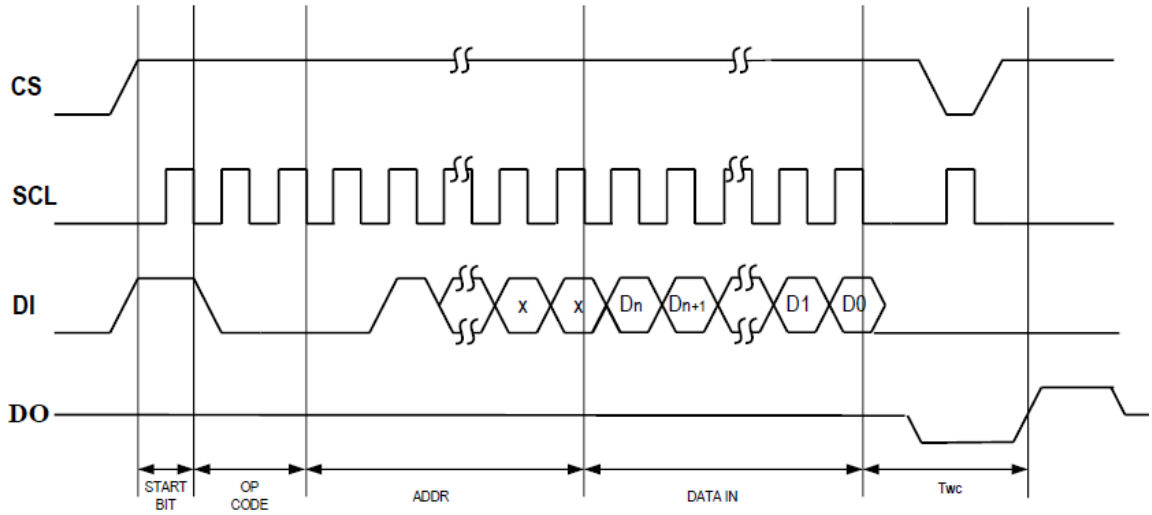
WRITE Timing



ERAL Timing(1)

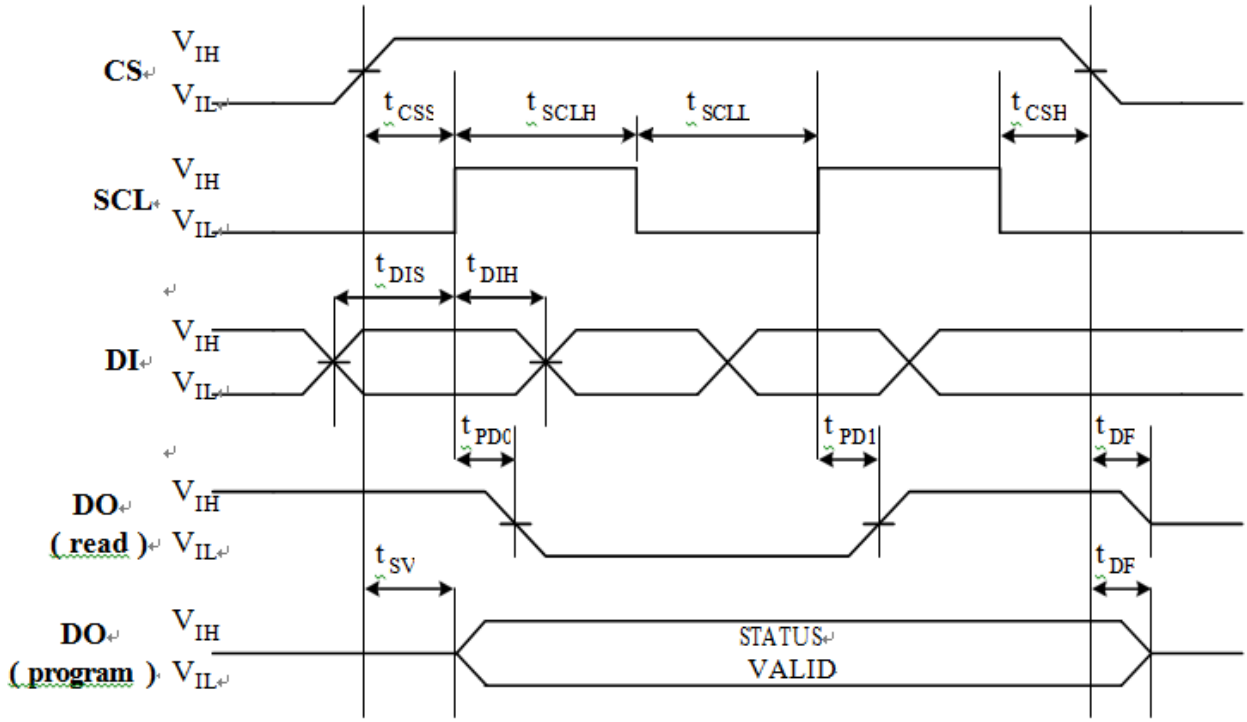


WRAL Timing(2)



Note：1. Valid only at V_{CC}=4.5V to 5.5V
2. Valid only at V_{CC}=4.5V to 5.5V

Synchronous Data Timing



AC characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} =+1.8V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V		0 0 0		2 1 0.25	MH_Z
t_{SHLH}	SCL High Time	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V		250 250 1000			ns
t_{SCLL}	SCL Low Time	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V		250 250 1000			ns
t_{CS}	Minimum CS Low Time	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V		250 250 1000			ns
t_{CSS}	CS Setup Time	Relative to SCL	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V	50 50 200			ns
t_{DIS}	DI Setup Time	Relative to SCL	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V	100 100 400			ns
t_{CSH}	CS Hold Time	Relative to SCL		0			ns
t_{DIH}	DI Setup Time	Relative to SCL	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V	100 100 400			ns
t_{PD1}	Output Delay to"1"	AC Test	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V			250 250 1000	ns
t_{PD0}	Output Delay to"0"	AC Test	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V			250 250 1000	ns
t_{SV}	CS to Status Valid	AC Test	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V			250 250 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS=V_{IL}	4.5V≤V_{CC}≤5.5V 2.7V≤V_{CC}≤5.5V 1.8V≤V_{CC}≤5.5V			100 100 400	ns
t_{WC}	Write Cycle Time		4.5V≤V_{CC}≤5.5V		3	10	ms

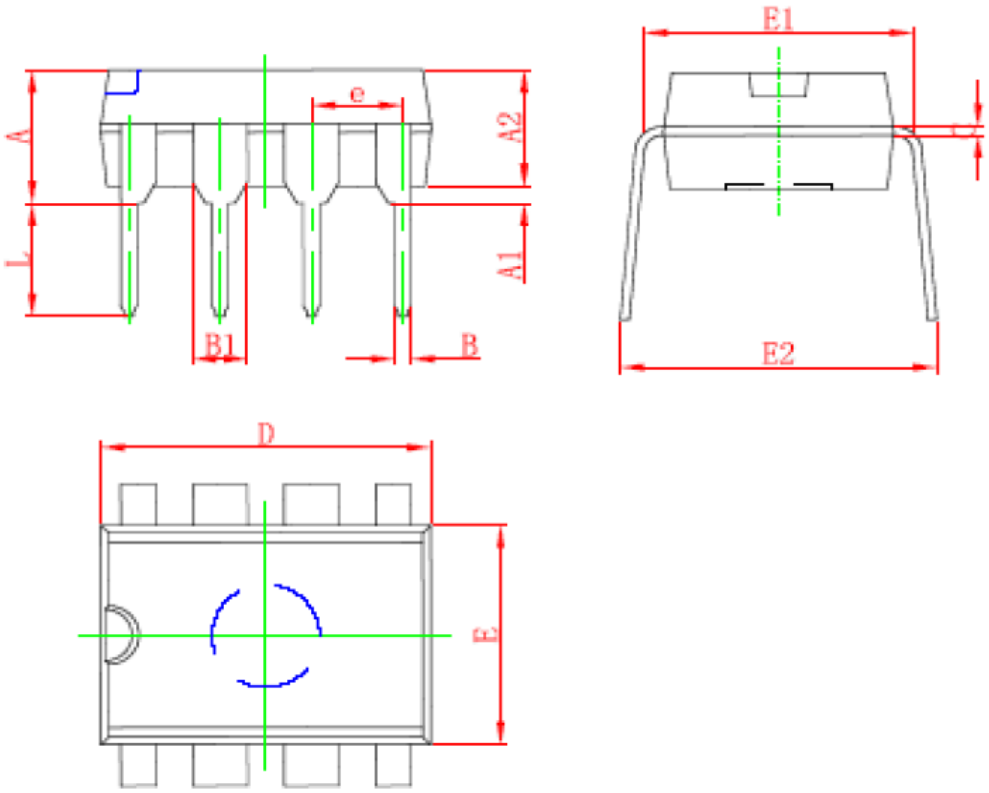
DC characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 $_p$F (unless otherwise noted).

Symbol	Parameter	Test condition		Min	Typ	Max	Units
V_{CC1}	Supply voltage			1.8		5.5	V
V_{CC2}	Supply voltage			2.5		5.5	
V_{CC3}	Supply voltage			2.7		5.5	
V_{CC4}	Supply voltage			4.5		5.5	
I_{CC}	Supply	V_{CC}=5.0V,	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	1.0	mA
I_{SB1}	Standby current	V_{CC}=1.8V	CS=0V			0.1	µA
I_{SB2}	Standby current	V_{CC}=2.5V	CS=0V			1.5	µA
I_{SB3}	Standby current	V_{CC}=2.7V	CS=0V			1.5	µA
I_{SB4}	Standby current	V_{CC}=5.0V	CS=0V			1.5	µA
I_{LI}	Input leakage	V_{in} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output low voltage	V_{in} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1} V_{IH1}	Input low voltage Input high voltage	4.5V ≤V_{CC} ≤ 5.5V		-0.6 2.0		0.8 V_{CC}+1	V
V_{IL2} V_{IH2}	Input low voltage Input high voltage	1.8V ≤V_{CC}≤ 2.7V		-0.6 V_{CC}X0.7		V_{CC}X0.3 V_{CC}+1	V
V_{OL1}	Output low voltage		I_{OL}=2.1mA			0.4	V
V_{OH1}	Output high voltage	4.5V ≤V_{CC} ≤ 5.5V	I_{OH}=-0.4mA	2.4			V
V_{OL12}	Output low voltage		I_{OL}=0.15mA			0.2	V
V_{OH2}	Output high voltage	1.8V ≤V_{CC} ≤ 2.7V	I_{OH}=-100uA	V_{CC}-0.2			V

Packaging information

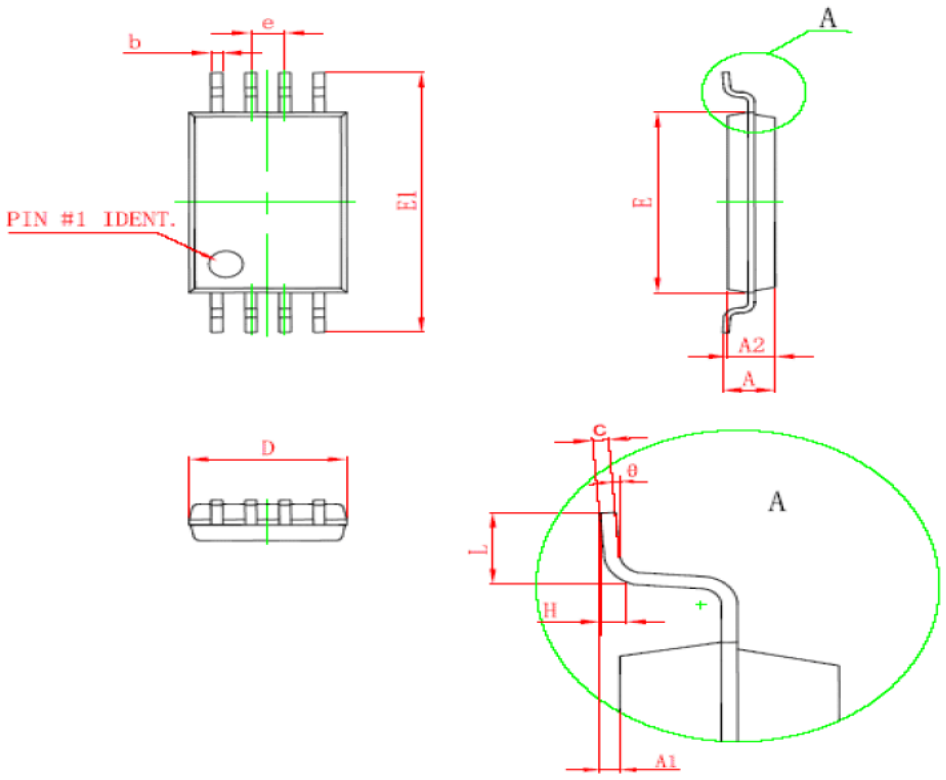
DIP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524（BSC）		0.060（BSC）	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100（BSC）	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

Packaging information

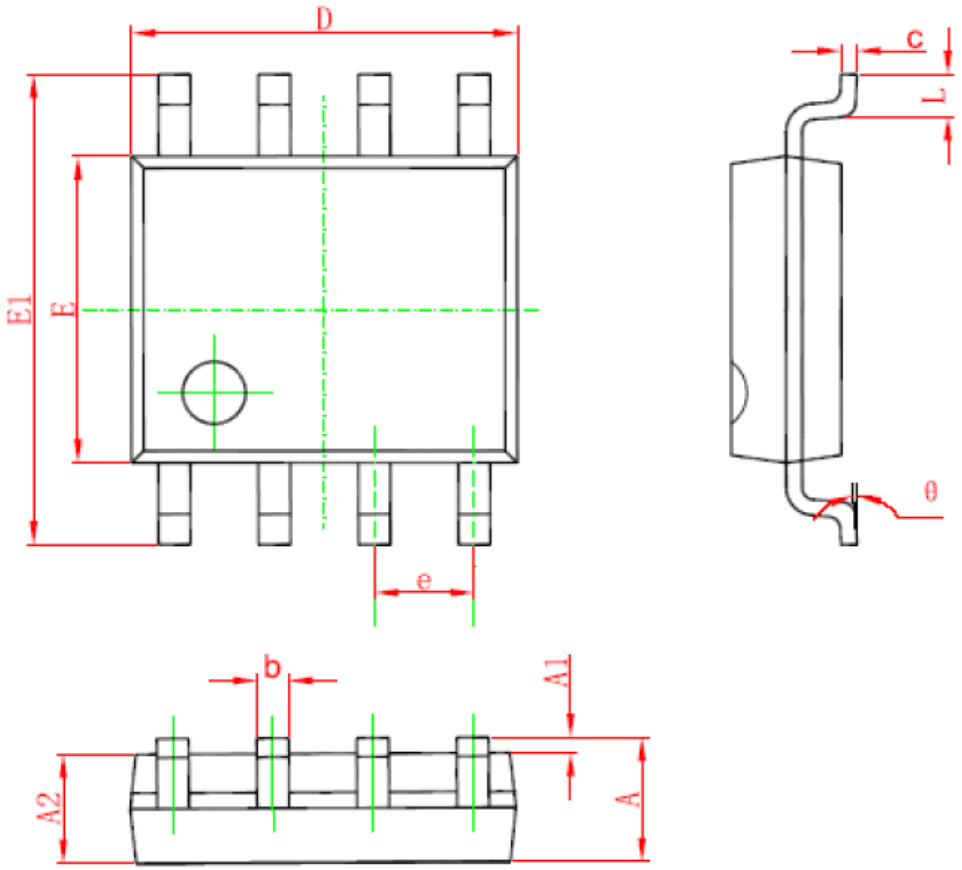
TSSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

Packaging information

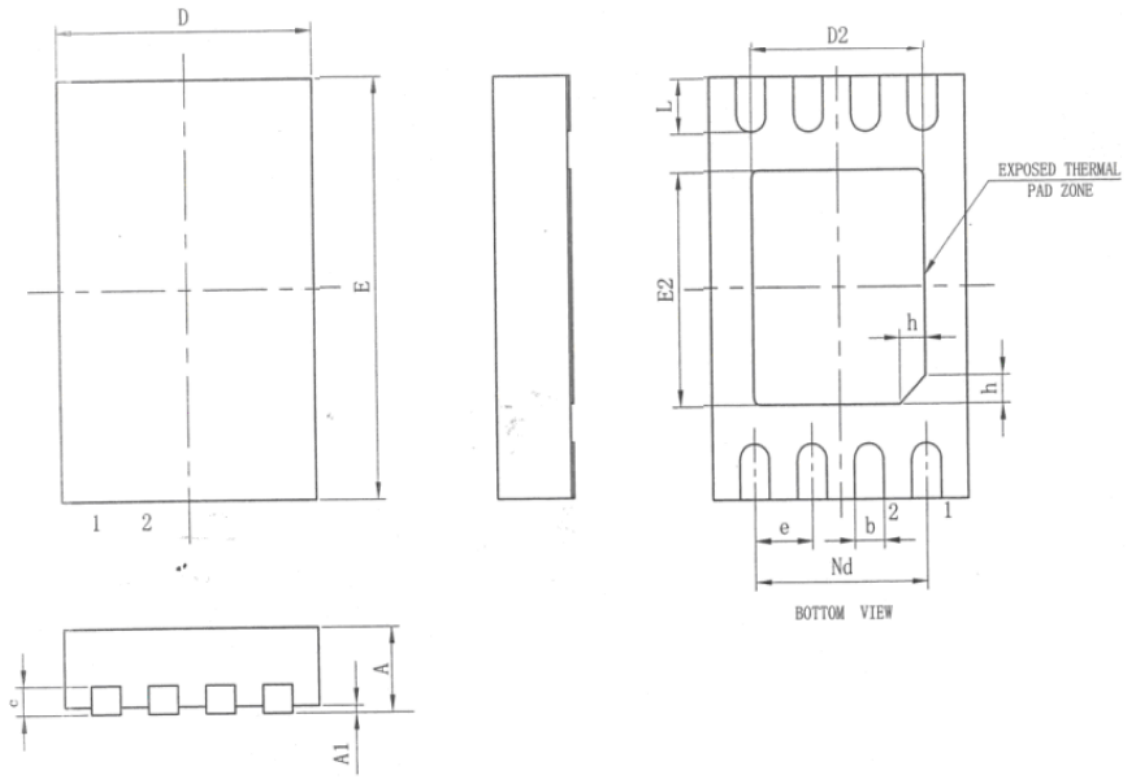
SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Packaging information

TDFN-8



Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1		0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D2	1.50REF		
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.40		1.60
L	0.20		0.40
h	0.20	0.25	0.30

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.