ACM3128A 2×42W Stereo | 1×84W Mono, Analog Input Class-D Audio Amplifier with Ultra Low Power Dissipation, Spread Spectrum and Class-H Control

1. Features

- **Single Supply Voltage**
  - PVDD: 4.5V to 26.4V
  - Built-in LDO output 5V for others
- **Various Output Configurations**
  - 2×32.5W, 1% THD+N, 24V, 8Ω, BTL
  - 1×65W, 1% THD+N, 24V, 4Ω, PBTL
  - 2×42W, 1% THD+N, 24V, 6Ω, BTL
  - 1×84W, 1% THD+N, 24V, 3Ω, PBTL
- **Excellent Audio Performance**
  - THD+N ≤ 0.02% at 1W, 1kHz, 4Ω, PVDD = 24V
  - Higher Order Modulator Enable Better THD+N for full audio band
  - Idle switching A-weighted noise ≤ 63 uV_{RMS}
- **Efficient Class-D Operation**
  - >90% efficient Class-D operation eliminates need for heat sink
  - Low Idle Current: <24mA, PVDD=12V, LC Filter=10uH+0.68uF
  - Patented Modulation Schemes to Minimize inductor ripple Current for all output power level
  - Class-H Control improves efficiency for full output power range
- **Low EMI Technology**
  - Spread Spectrum Option
  - 180° PWM Phase Shift
- **Gain Management**
  - 20dB, 26dB, 30dB, 34dB fixed gain setting
  - Mute Operation to stop PWM switching
  - Programmable Power Limit
- **Analog Protections**
  - Short-Circuit protection with Auto-recovery option
  - Under-Voltage detection
  - Over-Voltage detection
  - Output DC detection for speaker protection
  - Over temperature protection with auto recovery

2. Applications

- Bluetooth/Wireless Speakers
- Soundbars
- Docks, Monitors
- Home Theaters
- LCD TV/PC

3. General Description

The ACM3128A is a stereo/mono, Class D audio amplifier delivers up to 2×42W into 6Ω stereo mode and 1×84W into a 3Ω load in mono mode while offering up to 92% efficiency. In order to minimize power dissipation, a new patented modulation scheme - Dynamic PWM been used to minimize inductor loss for full output power range.

The ACM3128A operates from a single +4.5V to +26.4V supply, driving the load in BTL or PBTL configuration.

The ACM3128A offers a spread-spectrum modulation mode that reduces EMI noise and provide 2 switching frequency option (384kHz, 480kHz).

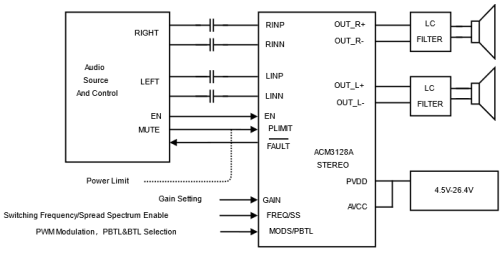
Feature include fully differential inputs, comprehensive pop-and click suppression, and four selectable-gain settings (20dB,26dB,30dB and 34dB). A pin adjustable power limit function and speaker DC protection protect speaker without damage. Short-circuit protection, Over-temperature protection and Over/Under Voltage protection prevent the device from being damaged during a fault condition.

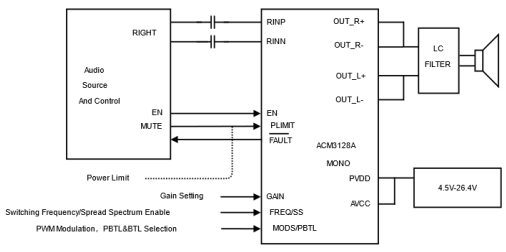
ACM3128A supports Class-H control which can extent battery life time in case the system power supply is 'Battery + Boost Convertor'.

4. Device Information

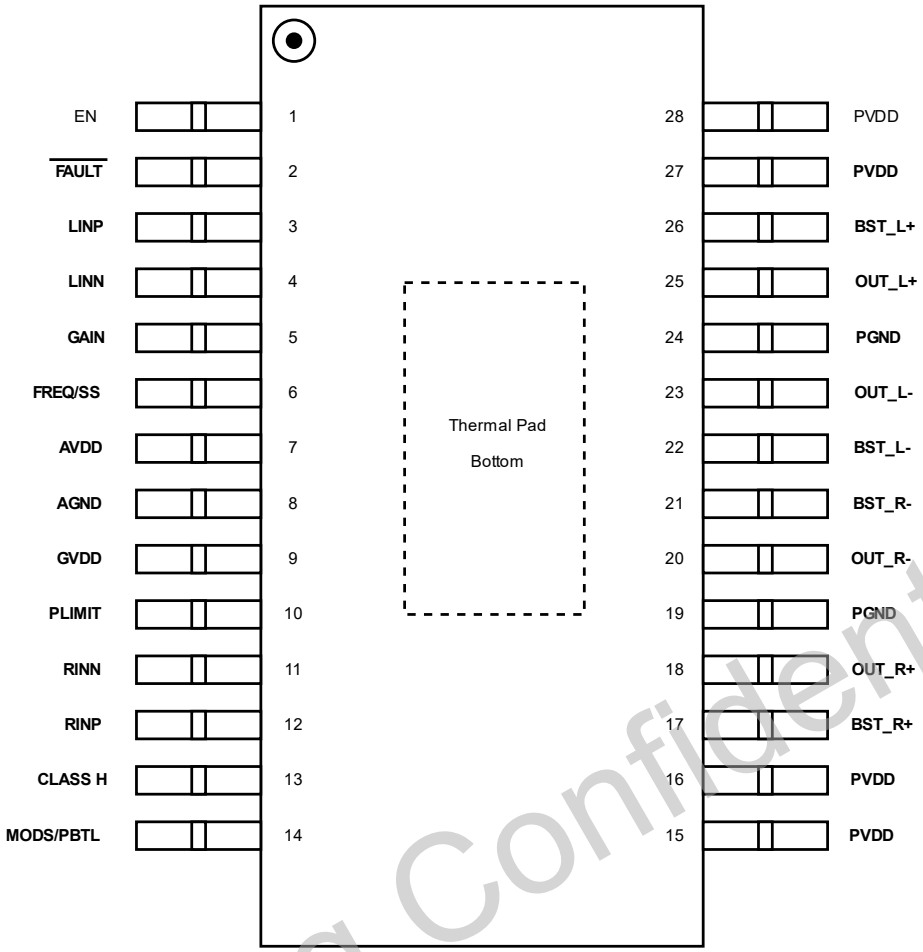
Part number	Package	Body size
ACM3128A	TSSOP 28	9.7 *mm* × 4.4 *m*m

- **Simplified Application Circuit**





5. Pin Configuration and Function Descriptions



Pin No.	Name	Type	Description
1	EN	AIN	Enable Logic input for amplifier (LOW=Output Hi-Z, HIGH=Output Enabled). TTL logic levels with compliance to AVCC
2	$\overline{\text{FAULT}}$	DO	Fault reporting including Over-temperature, DC Detection, Over-Current Protection. Open Drain $\overline{\text{FAULT}}$ = High, normal operation $\overline{\text{FAULT}}$ = Low, fault condition
3	LINP	AIN	Positive audio input for left channel
4	LINN	AIN	Negative audio input for left channel
5	GAIN	AIN	Gain Selection via Pull-down resistor
6	FREQ/SS	AIN	Switching Frequency Selection and Spread Spectrum Enable/Disable
7	AVCC	PWR	Analog Supply
8	AGND	G	Ground
9	GVDD	PO	5V regulated output, also used as supply for PLIMIT function
10	PLIMIT	AIN	Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V(PLIMIT)<0.5V to Mute amplifier (set amplifier to Hi-Z state, power stage stops switching). Give 0.6V<V(PLIMIT)<3V to set the power limit level. Give V(PLIMIT)>4.2V to bypass the power limit function.
11	RINN	AIN	Negative audio input for right channel
12	RINP	AIN	Positive audio input for right channel
13	CLASS H	AO	Class-H control signal
14	MODS/PBTL	AIN	PWM Modulation Selection and BTL/PBTL Selection
15	PVDD	PWR	Power Supply
16	PVDD	PWR	Power Supply
17	BST_R+	BST	Boot strap for positive right channel output, connect to 470nF X5R or better ceramic cap to OUT_R+
18	OUT_R+	PO	Positive right channel output

19	PGND	G	Ground
20	OUT_R-	PO	Negative right channel output
21	BST_R-	BST	Boot strap for negative right channel output, connect to 470nF X5R or better ceramic cap to OUT_R-
22	BST_L-	BST	Boot strap for negative left channel output, connect to 470nF X5R or better ceramic cap to OUT_L-
23	OUT_L-	PO	Negative left channel output
24	PGND	G	Ground
25	OUT_L+	PO	Positive left channel output
26	BST_L+	BST	Boot strap for positive left channel output, connect to 470nF X5R or better ceramic cap to OUT_L-
27	PVDD	PWR	Power Supply
28	PVDD	PWR	Power Supply

6. Device Family Comparison

Device Name	PVDD Range （V）
ACM3108	4.5V-14.5V
ACM3128A	4.5V-26.4V

7. Specifications

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
PVDD, AVCC	Supply Voltage	-0.3	30	V
Input Voltage, V_I	LINP, LINN, RINN, RINP	-0.3	6.3	V
	PLIMIT, MODS/PBTL, FREQ/SS	-0.3	GVDD+0.3	V
	$\overline{\text{FAULT}}$, EN	-0.3	PVDD+0.3	V
T_A	Ambient operating temperature	-40	85	℃
T_J	Operating junction temperature	-40	160	℃
T_{stg}	Storage temperature	-40	125	℃

(1) Stressed beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicted under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{(SUPLLY)}$	Power supply inputs	PVDD, AVCC	4.5		26.4	V
V_{IH}	High-level input voltage	EN	2			V
V_{IL}	Low-level input voltage	EN			0.8	
V_{OL}	Low-level output voltage	$\overline{\text{FAULT}}$, $R_{PULL-UP}$=100kΩ, PVDD=12V			0.8	V

SYMBOL	PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
I_{IH}	High-level input current	EN			50	μA
I_{IL}	Low-level input current	EN			5	μA
R_L(BTL)	Minimum load Impedance	(Output LC filter=10uH+0.68uF)	3.2	4		
R_L(PBTL)			1.6	2		
T_J	Junction Operating Temperature		-40		160	℃
T_A	Ambient Operating Temperature		-40		85	℃

7.4 Thermal Information

		ACM3128A, TSSOP 28 PINS JEDEC STANDARD 4-LAYER PCB	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	28	℃/W
θ_{JT}	Junction-to-case (top) thermal resistance	22	℃/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	℃/W

7.5 Electrical Characteristics

PVDD=12V, Fin=1kHz, Load=4Ω, Bootstrap Capacitor=0.47μF, free-are room temperature 25℃, LC filter=10uH+0.68uF, Fsw=384kHz, BD Mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Electrical Characteristics						
$\|V_{OS}\|$	Class-D output offset voltage (measured differentially)	V_I=0V, BTL Mode		0.5	2	mV
		V_I=0V, PBTL Mode		0.5	3	mV
I_{CC}	Quiescent supply current	EN≥2V, LC filter=10μH+0.68μF, 2× BTL, Dynamic PWM Modulation		24		mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	EN≤0.8V, PVDD=12V		20		μA
$R_{DS(ON)}$	Drain-source on-state resistance, High side NMOS	PVDD=12V, I_{OUT} = 500mA, T_J = 25		75		mΩ
	Drain-source on-state resistance, Low side NMOS			75		mΩ
G	Gain	Pull Down Resistor = 47kΩ		20		dB
		Pull Down Resistor≥120kΩ or Open		26		dB
		Pull Down Resistor≤4.7kΩ or Short		30		dB
		Pull Down Resistor = 15kΩ		34		dB
t_{ON}	Turn-on-time	EN≥2V		10		ms
t_{OFF}	Turn-off-time	EN≤0.8V		5.7		μs
GVDD	Gate drive supply	I_{GVDD} < 200 uA		5		V
AC Electrical Characteristics, Stereo Output						
PSRR	Power supply ripple rejection	200mV_{PP} ripple at 1kHz, Gain=20dB, Input AC coupled to GND		-70		dB
$P_{O(SPK)}$	Continuous output power (4Ω Load)	THD+N = 10%, f = 1kHz, PVDD = 18V		42		W
		THD+N = 1%, f = 1kHz, PVDD = 18V		33		W
		THD+N = 10%, f = 1kHz, PVDD = 20V		50		W
		THD+N = 1%, f = 1kHz, PVDD = 20V		40		W
	Continuous output power (6Ω Load)	THD+N = 10%, f = 1kHz, PVDD = 18V		31		W
		THD+N = 1%, f = 1kHz, PVDD = 18V		24		W
		THD+N = 10%, f = 1kHz, PVDD = 24V		54		W
		THD+N = 1%, f = 1kHz, PVDD = 24V		42		W
V_n	Output integrated noise, 20Hz to 22kHz, A-weighted filter	Gain = 20dB		63		μVrms
		Gain = 26dB		75		μVrms
F_{SW}	Switching frequency of the	Spread Spectrum Disable		384		kHz

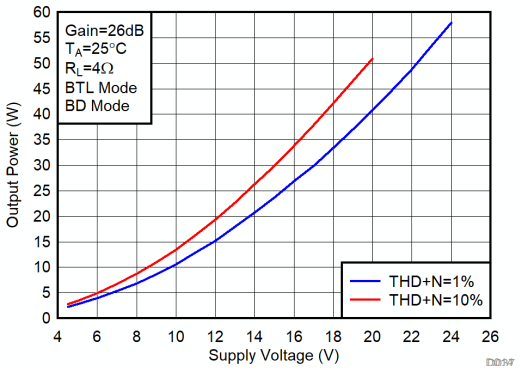
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	speaker amplifier			480		kHz
		Spread spectrum Enable	345	384	423	kHz
			432	480	528	kHz
X-talk(1)	Crosstalk	V_o=2Vrms, Gain=26dB, f=1kHz, based on ACM3128AEVM		90		dB
AC Electrical Characteristics, Mono Output						
PSRR	Power supply ripple rejection	200mV_{PP} ripple at 1kHz, Gain=20dB, Input AC coupled to GND		-70		dB
$P_{O(SPK)}$	Continuous output power (3Ω Load)	THD+N = 10%, f = 1kHz, PVDD = 24V		103		W
		THD+N = 1%, f = 1kHz, PVDD = 24V		84		W
V_n	Output integrated noise, 20Hz to 22kHz, A-weighted filter	Gain = 20dB		63		μVrms
		Gain = 26dB		75		μVrms
F_{SW}	Switching frequency of the speaker amplifier	Spread Spectrum Disable		384		kHz
				480		kHz
		Spread spectrum Enable	345	384	423	kHz
			432	480	528	kHz
PROTECTION						
OCE_{THRES}	Over-Current Error Threshold	Speaker Output Current (Post LC filter), Speaker current, PVDD=15V	7.5	8		A
$UVE_{THRES(PVDD)}$	PVDD under voltage error threshold			4.1		V
$0VE_{THRES(PVDD)}$	PVDD over voltage error threshold			29.2		V
DCE_{THRES}	Output DC Error protection threshold	Class D Amplifier's output DC voltage cross speaker load to trigger Output DC Fault protection		2.5		V
T_{DCDET}	Output DC Detect time	Class D Amplifier's output remain at or above DCE_{THRES}		700		ms
OTE_{THRES}	Over temperature error threshold			160		℃
$OTE_{Hysteresis}$	Over temperature error hysteresis			30		℃

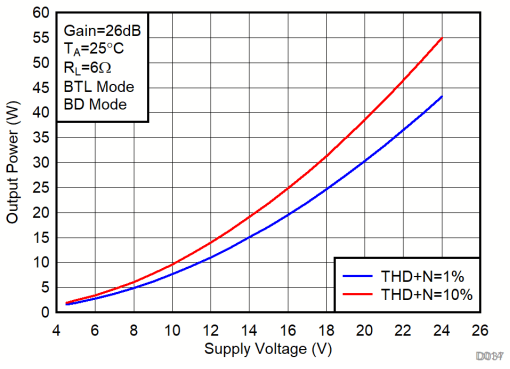
1) Crosstalk high depends on output layout (L channel and R channel routing distance), Inductor type.

8. *Typical Characteristics*

8.1 Bridge Tied Load (BTL) Configuration Curves with BD Mode

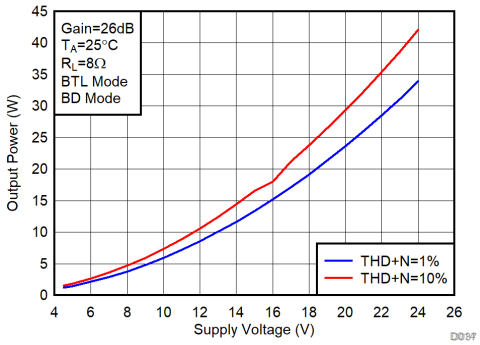
Free-air room temperature 25℃ (unless otherwise noted.) Measurements were made using ACM3128EVM board and Audio Precision System APX5xx Series with Analog Analyzer filter set to 20-kHz Low Pass filter. Device PWM Modulator mode set to BD mode with 384kHz Fsw, LC filter=10μH+0.68μF.





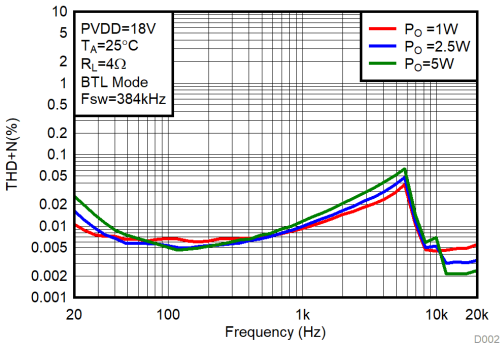
(Load=4Ω, Fsw=384kHz, BD Modulation)

Figure 1 Max Output Power vs PVDD



(Load=6Ω, Fsw=384kHz, BD Modulation)

Figure 2 Max Output Power vs PVDD

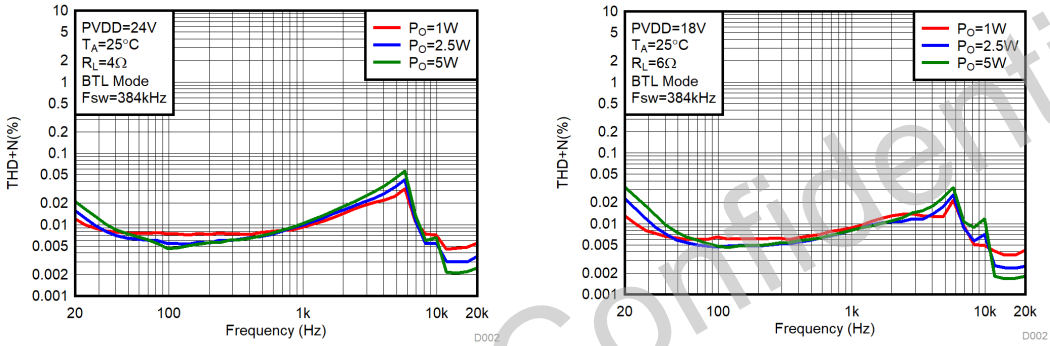


(Load=8Ω, Fsw=384kHz, BD Modulation)

Figure 3 Max Output Power vs PVDD

(Load=4Ω, Fsw=384kHz,BD Modulation, PVDD=18V)

Figure 4 THD+N vs Frequency

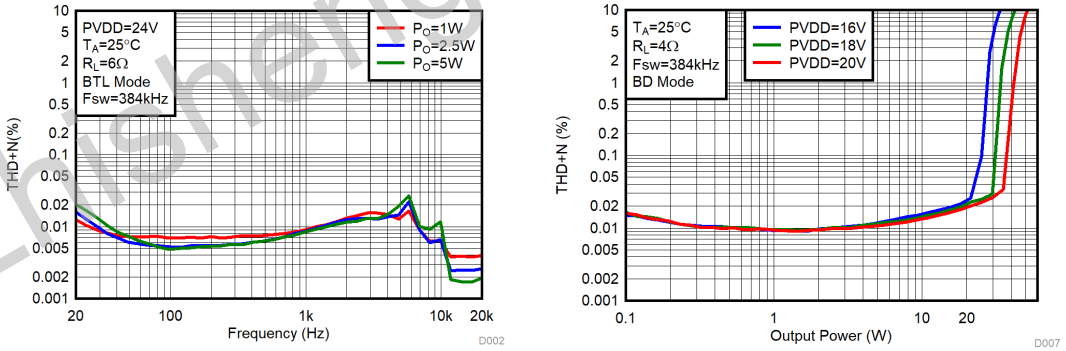


(Load=4Ω, Fsw=384kHz, BD Modulation, PVDD=24V)

Figure 5 THD+N vs Frequency

(Load=6Ω, Fsw=384kHz, BD Modulation, PVDD=18V)

Figure 6 THD+N vs Frequency

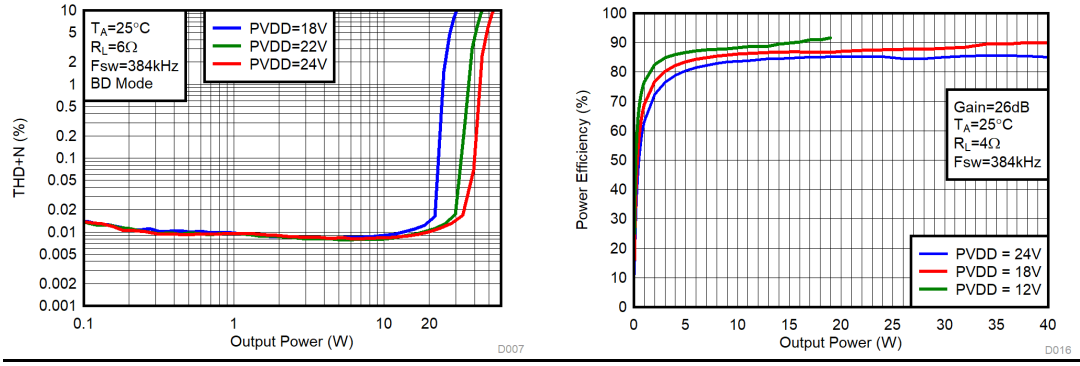


(Load=6Ω, Fsw=384kHz, BD Modulation, PVDD=24V)

Figure 7 THD+N vs Frequency

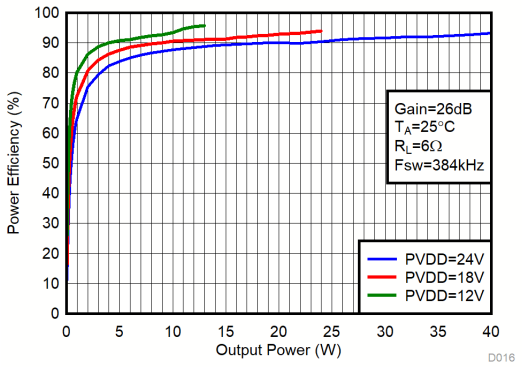
(Load=4Ω, Fin=1kHz, BD Modulation, PVDD=16V/18V/22V)

Figure 8 THD+N vs Output Power



(Load=6Ω, Fin=1kHz, BD Modulation)

Figure 9 THD+N vs Output Power

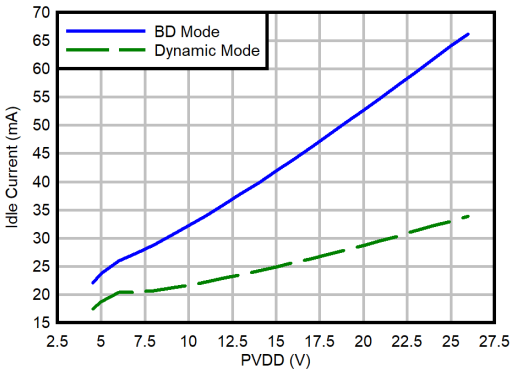


(Load=6Ω, Fsw=384kHz, Dynamic PWM Mode)

Figure 11 Efficiency

(Load=4Ω, Fsw=384kHz, Dynamic PWM Mode)

Figure 10 Efficiency

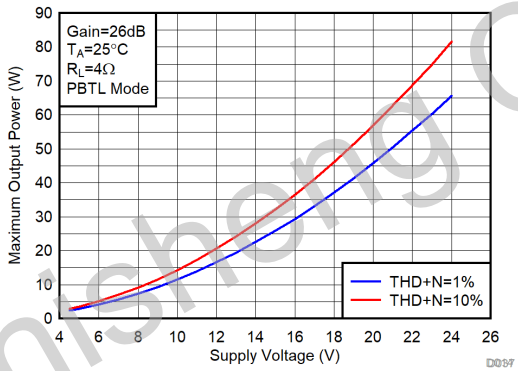


(Fsw=384kHz, Dynamic PWM Mode vs BD Mode)

Figure 12 Idle Current vs PVDD

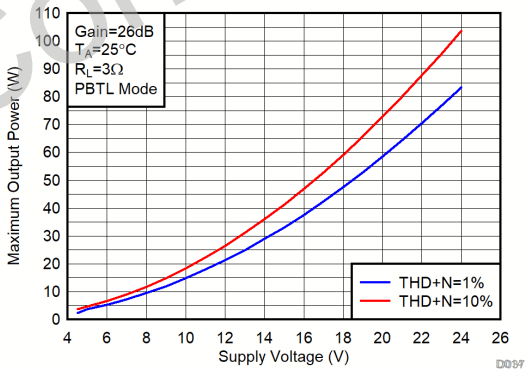
8.2 Bridge Tied Load (PBTL) Configuration Curves with BD Mode

Free-air room temperature 25℃ (unless otherwise noted.) Measurements were made using ACM3128EVM board and Audio Precision System APX5xx Series with Analog Analyzer filter set to 20-kHz Low Pass filter. Device PWM Modulator mode set to BD mode with 384kHz Fsw, LC filter=10μH+0.68μF.



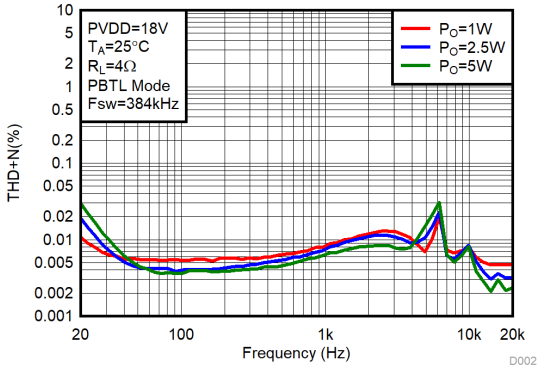
(Load=4Ω, Fsw=384kHz, BD Modulation)

Figure 9 Max Output Power vs PVDD



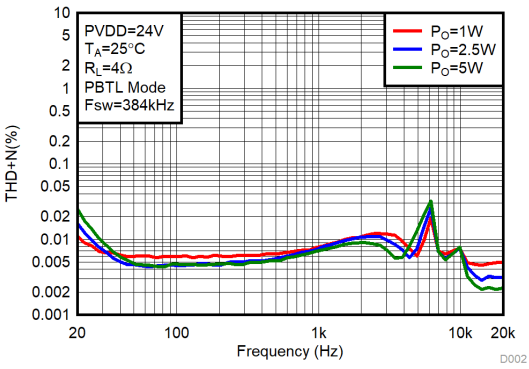
(Load=3Ω,Fsw = 384kHz, BD Modulation)

Figure 10 Max Output Power vs PVDD



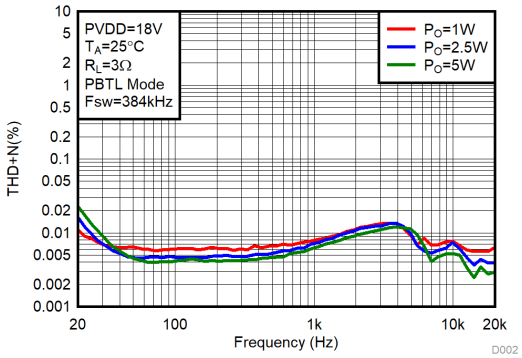
(Load=4Ω, Fsw=384kHz,BD Modulation)

Figure 11 THD+N vs Frequency



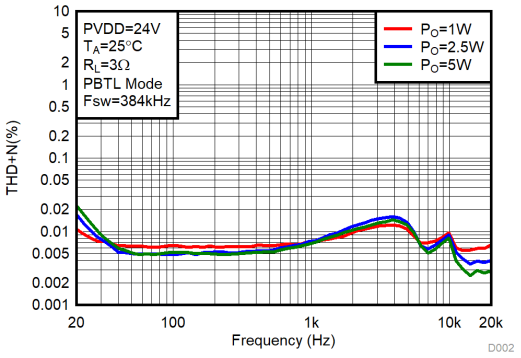
(Load=4Ω, Fsw=384kHz,BD Modulation)

Figure 12 THD+N vs Frequency



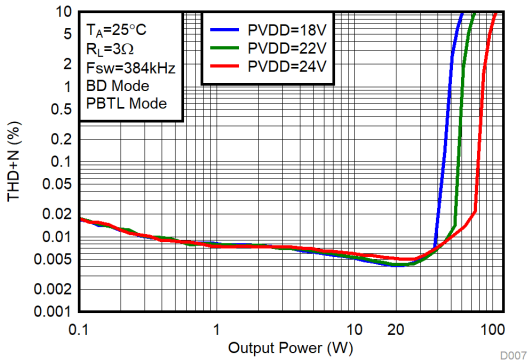
(Load=3Ω, Fsw=384kHz,BD Modulation)

Figure 11 THD+N vs Frequency



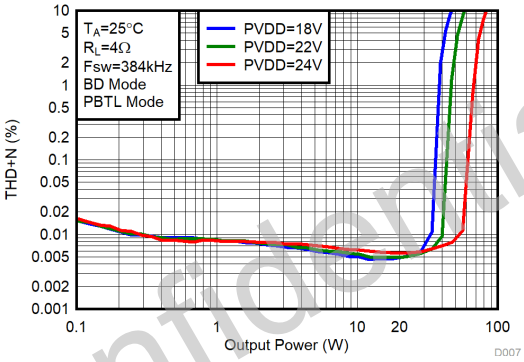
(Load=3Ω, Fsw=384kHz,BD Modulation)

Figure 12 THD+N vs Frequency



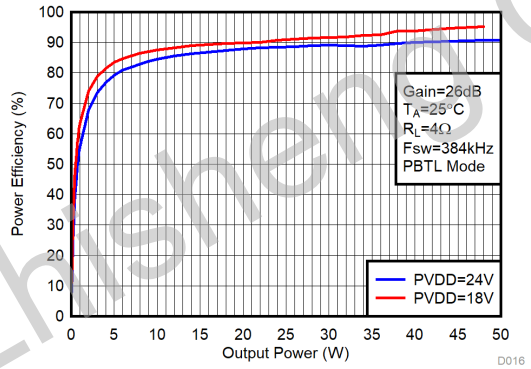
(Load=3Ω, Fsw=384kHz, BD Modulation)

Figure 13 THD+N vs Output Power



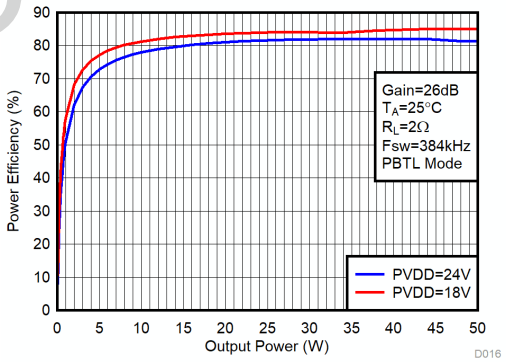
(Load=4Ω, Fsw=384kHz, BD Modulation)

Figure 14 THD+N vs Output Power



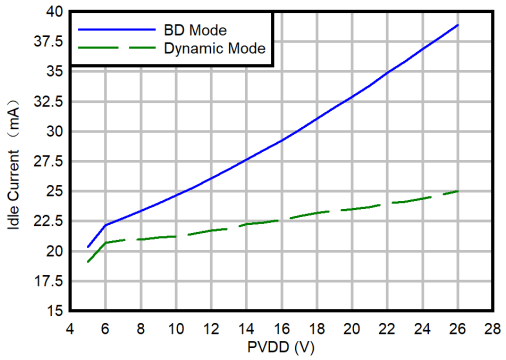
(Load=4Ω, Dynamic PWM Modulation)

Figure 15 Efficiency vs Output Power



(Load=2Ω, Dynamic PWM Modulation)

Figure 16 Efficiency vs Output Power



(Dynamic PWM vs BD, Fsw=384kHz)

Figure 17 Idle Current vs PVDD

9. Detailed Description

9.1 Overview

The ACM3128A device is a highly efficient Class D audio amplifier with extreme low idle power dissipation. It can support as low as 24-mA idle loss current using standard LC filter configurations. It is integrated with 75-mΩ MOSFET that allows output currents up to 8A. The high efficiency allows the amplifier to provide an excellent audio performance without the requirement for a bulky heat sink.

9.2 Functional Block Diagram

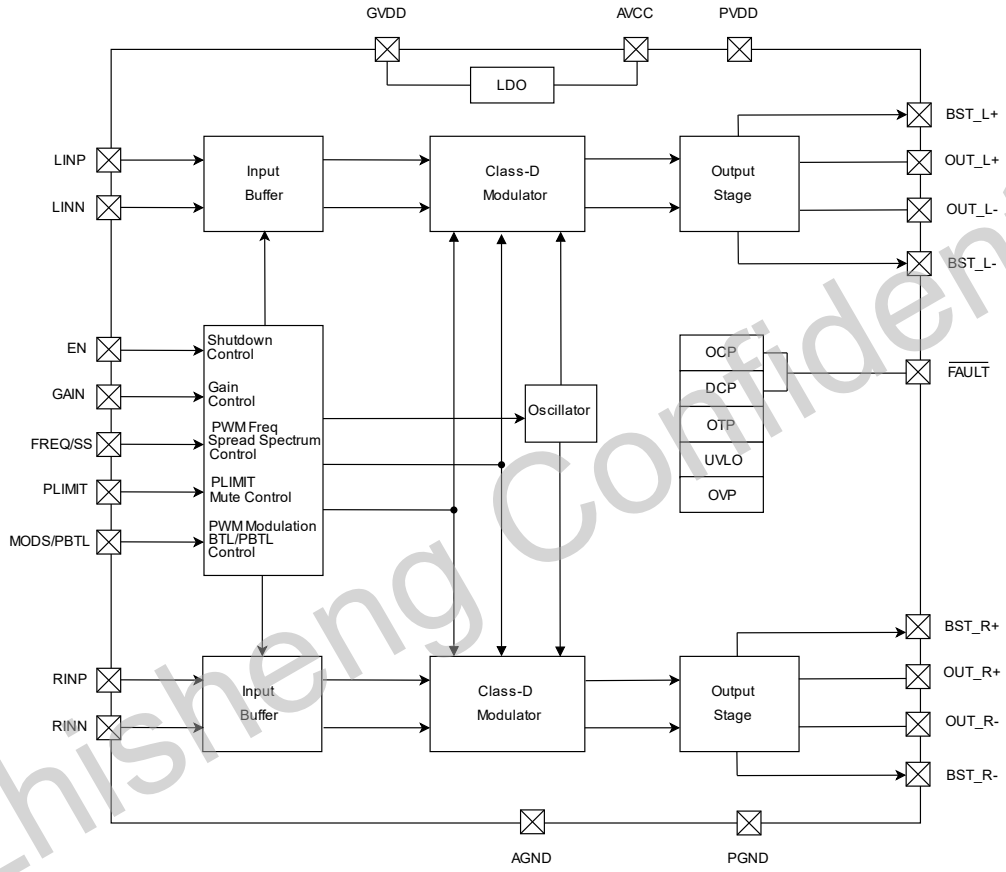


Figure 29 Function Block Diagram

9.3 Feature Description

9.3.1 Gain Setting

The gain of the ACM3128A is set by the pull down resistor connect to GAIN control pin. The gain setting is latched during power-up and cannot be changed while device is powered. Table 1 lists the recommended resistor values and gain.

Table 1. Gain Setting

GAIN	R1 (to GND)	Input Impedance
20dB	47kΩ	30kΩ
26dB	120kΩ or Open	15kΩ

30dB	4.7kΩ or Short	9.48kΩ
34dB	15kΩ	5.987kΩ

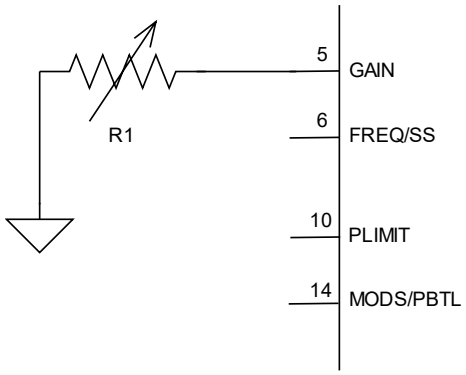


Figure 30 Gain Setting

9.3.2 Switching Frequency Selection and Spread Spectrum Selection

The ACM3128A provides 2 switching frequency option, 384kHz and 480kHz which best balance the audio performance and power dissipation. Spread spectrum is supported by ACM3128A to minimize EMI noise.

Table 2. Switching Frequency Selection and Spread Spectrum Setting

R2 (to GND)	Switching Frequency (kHz)	Spread Spectrum
120kΩ or Open	384kHz	Disable
47kΩ	480kHz	Disable
15kΩ	480kHz	Enable
4.7kΩ or Short	384kHz	Enable

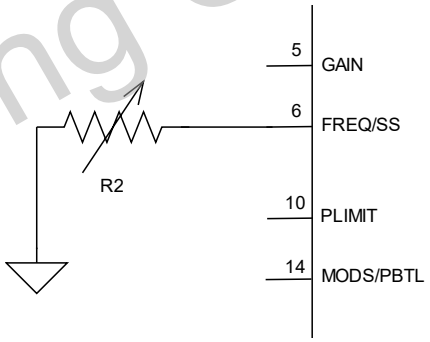


Figure 31 Switching Frequency Selection and Spread Spectrum Setting

9.3.3 Modulation Scheme Selection and BTL/PBTL Selection

The ACM3128A provides 2 PWM Modulation Scheme, BD Modulation and Dynamic PWM Modulation. With Dynamic PWM Modulation, the amplifier's output common mode voltage keeps tracking with audio signal to minimize inductor ripple current. Compare with BD modulation, Dynamic PWM Modulation decrease power dissipation more than 40% and improve efficiency more than 5% under <1W output power.

Table 3. Modulation Scheme Selection and BTL/PBTL Selection

R3 (to GND)	PWM Modulation Scheme	BTL/PBTL
120kΩ or Open	BD	BTL
47kΩ	BD	PBTL
15kΩ	Dynamic PWM	PBTL

4.7kΩ or Short	Dynamic PWM	BTL

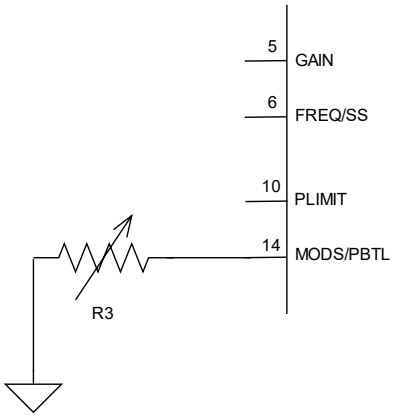


Figure 32 Modulation Scheme and BTL/PBTL Selection

9.3.4 Power Limit

The voltage at PLIMIT pin can be used to limit the amplifier output. V_{PLIMIT} (at the PLIMIT pin) is set by a resistor divider from GVDD to ground. V_{PLIMIT} sets a limit on the output peak-to-peak voltage. As Figure 34 shows, V_{PLIMIT} just limit the peak-to-peak voltage, but can't not been used to control the clipping depth. PLIMIT is adjustable from 0.6V to 3.5V. The output peak voltage been limited within ~9×V_{PLIMIT}. Set V_{PLIMIT}<0.5V, turn off output driver to mute device. Set V_{PLIMIT}>4.2V, Disable power limit function.

Table 4. Device behavior vs V_{PLIMIT}

V_{PLIMIT}	Device behavior	Description
<0.5V	Mute	Turn off output driver to mute device
0.6V~3.5V	Power Limit	Set V_{PLIMIT} limits output peak voltage.
>4.2V	Disable Power Limit	Disable Power Limit

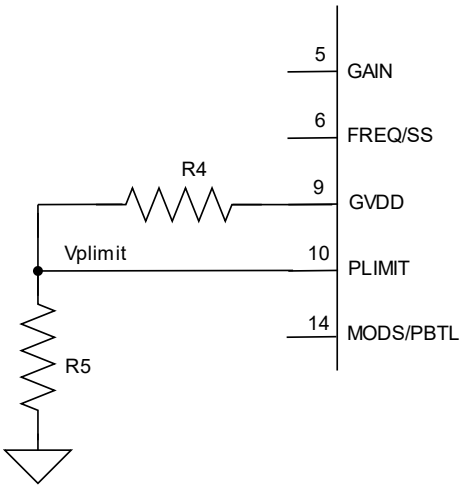


Figure 33 Power Limit Setting

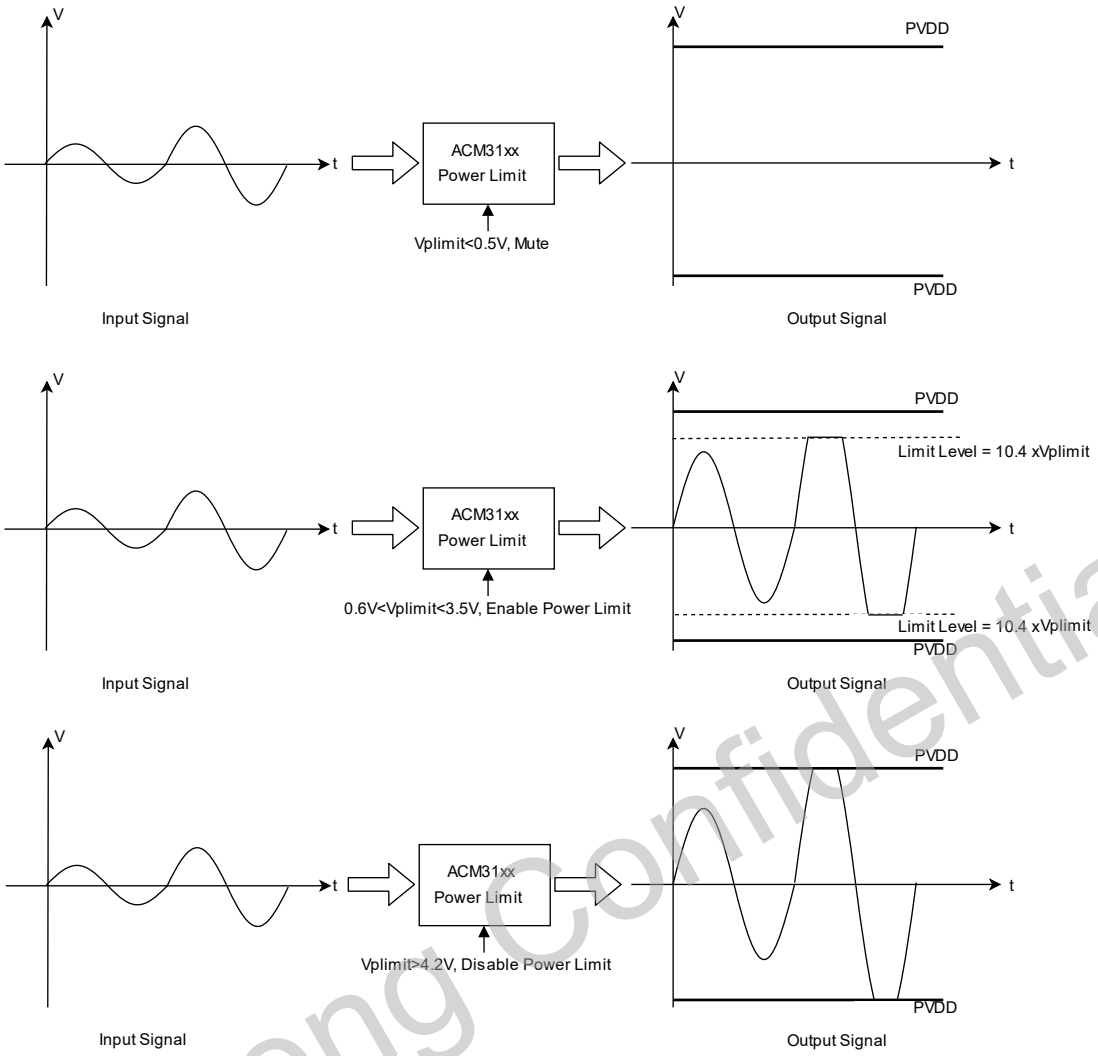


Figure 34 Power Limit Example

9.3.5 Shutdown (EN) control

Pulling EN pin low will let ACM3128A operate in low-current state for power conservation. The ACM3128A outputs will enter mute once EN pin is pulled low, and regulator will also disable to save power. If let EN pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

9.3.6 DC detection

ACM3128A has dc detection circuit to protect the speakers from large DC currents or AC current less than 2Hz which might be occurred as input capacitor defect or inputs short on printed circuit board. A DC Detect Fault is issued when the output differential voltage of either channel exceeds DC protection threshold level (2.5V Typical) for more than 700ms at the same polarity. The amplifier outputs area switched to a high impedance state when the DC Detection fault latch is engaged. The latch can be cleared by cycling the EN pin through the low state.

Connecting the $\overline{\text{FAULT}}$ and EN pins allows the $\overline{\text{FAULT}}$ pin function to automatically drive the EN pin low which clears the DC Detection protection latch.

9.3.7 Short-Circuit Protection and Automatic Recovery Feature

The ACM3128A has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the EN pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the EN pin. Connecting the $\overline{\text{FAULT}}$ and EN pins allows the $\overline{\text{FAULT}}$ pin function to automatically drive the EN pin low which clears the short-circuit protection latch.

9.3.8 Thermal Protection

Thermal protection on the ACM3128A prevents damage to the device when the internal die temperature exceeds 160℃. This trip point has a +/-10℃ tolerance from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ pin.

9.3.9 Over Voltage Protection

Once the PVDD votlage exceed the $OVE_{THRES(PVDD)}$ (29.2V Typical), device will set the output driver from Play mode to Hi-Z mode. Once PVDD drop below 28.7V (Typical), device will come back to Play mode.

9.3.10 Under Voltage Protection

Once the PVDD votlage drop below the $UVE_{THRES(PVDD)}$ (4.1V Typical), device will set the output driver from Play mode to Hi-Z mode. Once PVDD rise above 4.4V (Typical), device will come back to Play mode.

9.3.11 Class-H Control Operation

ACM31xx Class-H Control provides a new scheme to increase efficiency and reduce power dissipation for battery supply system. ACM31xx internal Class H block monitors the amplifier output audio signal and provides V_{CTRL} through hardware Pin 13 (CLASS-H) to feedback network of external DC-DC Boost Convertor, adjust Boost Convertor's V_{OUT} accordingly. As ACM31xx use the external Booster Convertor's V_{OUT} as the power supply, so ACM31xx's Power supply dynamic tracking with output audio signal, shown in Figure 35.

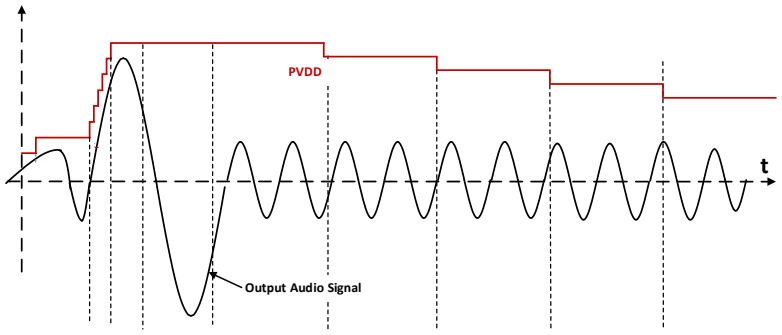
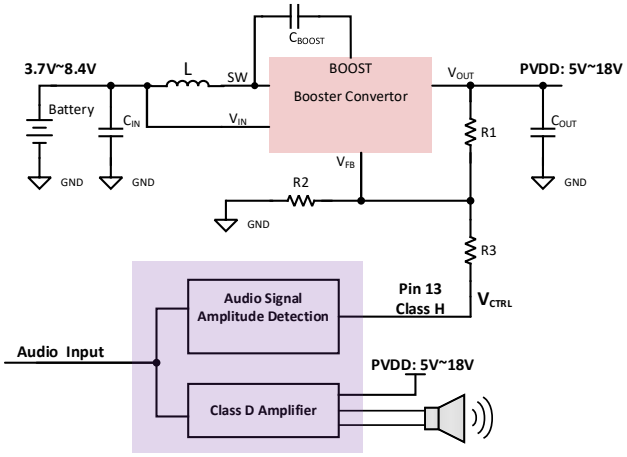


Figure 35 Class H Operation Signal

To use ACM31xx's Class H control function, customer only need to calculate R1 and R3 (show in Figure 36) based on $\mathbf{V_{FB}}$, **R2,** $\mathbf{V_{CTRL}}$, $\mathbf{V_{OUTL}}$ and $\mathbf{V_{OUTH}}$.



$$\frac{V_{OUT}-V_{FB}}{R1} = \frac{V_{FB}}{R2} + \frac{V_{FB}-V_{CTRL}}{R3}$$

$$V_{OUT} = \left(\frac{R1}{R2} + 1 + \frac{R1}{R3}\right) \quad V_{FB} - \frac{R1}{R3} V_{CTRL}$$

Figure 36 Class H Operation Diagram

The design procedure shown as following:

Step1: V_{FB} depends on DC-DC Boost Convertor, typical is 0.6V or 1V or 1.2V, get this data from Boost convertor's datasheet; **V_{CTRL}**=3.5V; **R2** depends DC-DC Booster Convertor's recommendation (check the reference design schematic from Booster Convertor's vendor), **V_{OUTL}** represents Boost Convertor's minimal output voltage, **V_{OUTH}** represents Boost Convertor's maxim output voltage.

Step2: Follow below formula to calculate **R1** and **R3**.

$$R3 = \left(\frac{V_{OUTH}}{V_{FB}} - \frac{V_{OUTH} - V_{OUTL}}{V_{CTRL}} - 1\right) \times R2 \times \frac{V_{CTRL}}{V_{OUTH} - V_{OUTL}}$$

$$R1 = \left(\frac{V_{OUTH} - V_{OUTL}}{V_{CTRL}}\right) \times R3$$

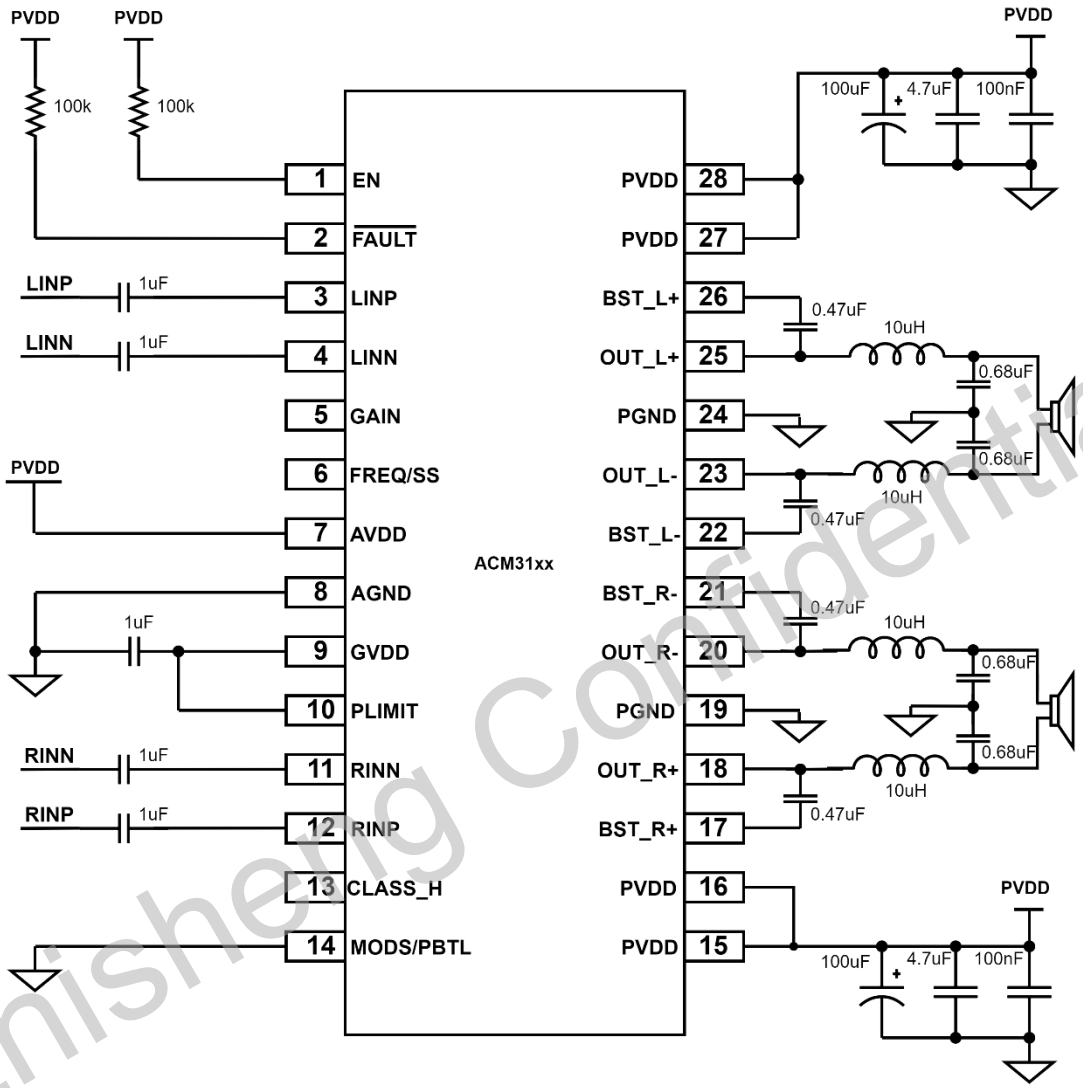
Example setting of R1/R3 and V_{OUT} of Boost, user can refer to calculator tool provided by ACME or caclulate mannually based on the formula in **Step2**.

Table 5. R1 and R3 Calculation Example

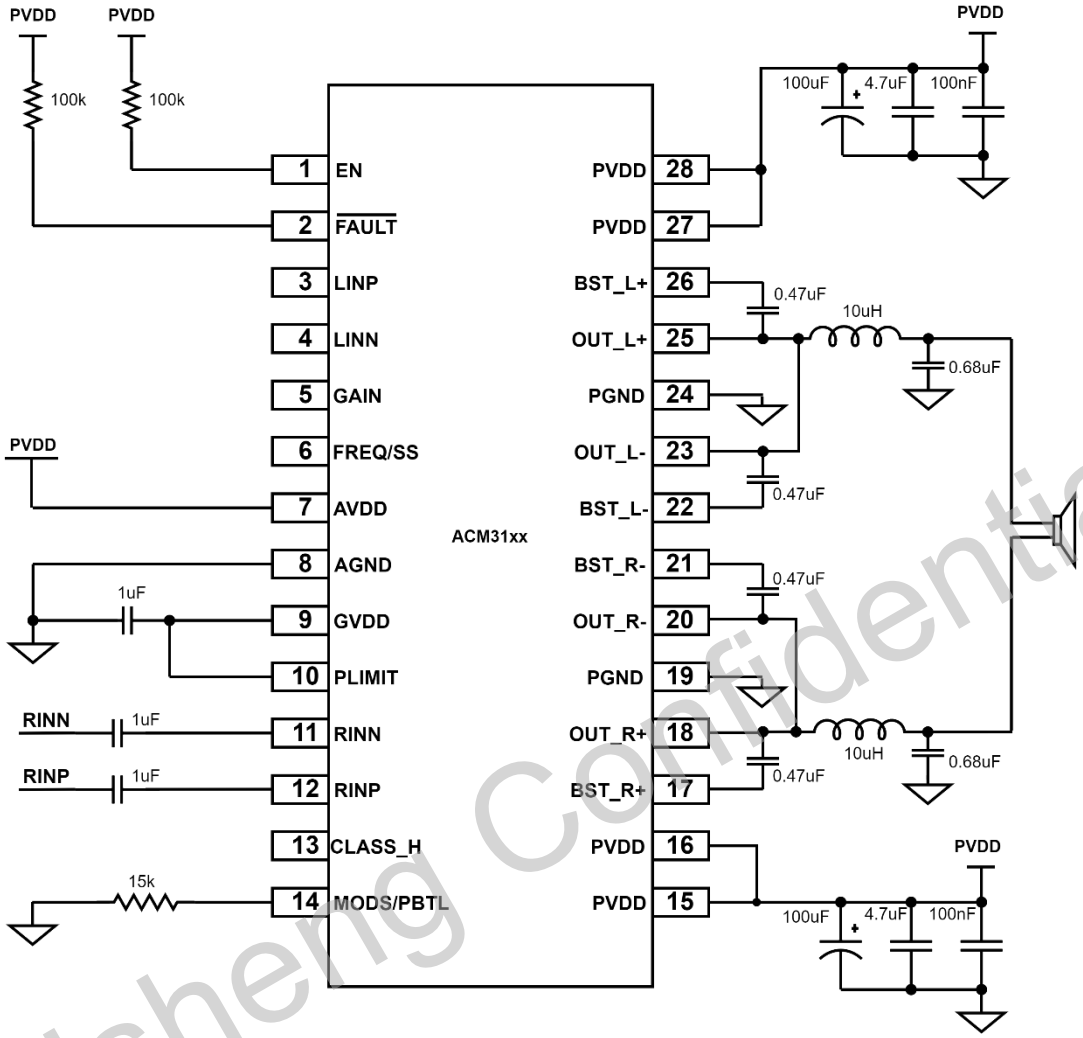
User Input				Calculator Output	
V_{OUTL} (V)	**V_{OUTH}** (V)	**R2** (kΩ)	**V_{FB}** (V)	**R1** (kΩ)	**R3** (kΩ)
5.437179487	11.85384615	13	0.6	220	120
8.231868132	15.73186813	13	0.6	300	140
4.965656566	10.05656566	27	1.2	160	110
7.85	11.93333333	27	1.2	210	180

9.4 Application Information

9.4.1 Application Circuit Example Of Stereo

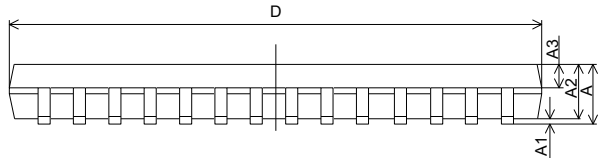


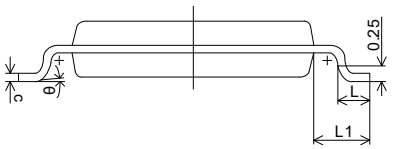
9.4.2 Application Circuit Example Of Mono

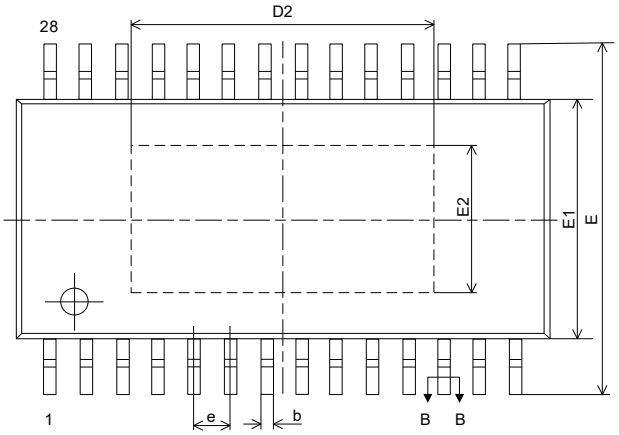


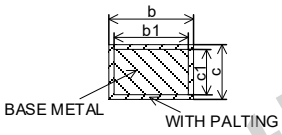
10. Package Dimensions

Orderable Device	Package Type	MPQ	MOQ	Eco Plan	MSL Level	Device Marking
ACM3128A	TSSOP28 Tape and Reel	3000	3000	RoHS Compliant Lead-Free Finish	MSL3	ACM3128A









SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	_	_	1.20
A1	0.05	_	0.15
A2	0.80	_	1.00
A3	0.39	0.44	0.49
b	0.20	_	0.29
b1	0.19	0.22	0.25
c	0.13	_	0.18
c1	0.12	0.13	0.15
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	_	8°

L/F 载体尺寸 (mil)	D2	E2
150*110	3.66REF	2.65REF
232*118	5.50REF	2.70REF