

## ACM8625M 2×26W 立体声、数字输入 D 类音频功放

### 内置 DSP 音效处理算法+CLASS H 动态升压控制技术

#### 1. 特征

- 灵活电源配置
  - 供电电压范围 PVDD: 4.5V to 26.4V
  - DVDD 和 I/O: 3.3V 或 1.8V
- 输出功率
  - 2×26W, 立体声输出 (8Ω, 22V, THD+N = 1%)
  - 2×21W, 立体声输出 (4Ω, 15V, THD+N = 1%)
  - 2X30W (散热片), 立体声输出 (4Ω, 18V, THD+N = 1%)
- 出色的音频性能
  - THD+N ≤ 0.04% at 1W, 1kHz, PVDD = 12V
  - SNR 信噪比 114 dB (加权)
  - 超低底噪 ≤ 32  $\mu V_{RMS}$  (A 加权)
  - 超低静态电流: 18 mA
  - 效率: 90% (8Ω load at 12V)
  - 防止掉电 POP
- 数字音频接口
  - I<sup>2</sup>C 可选 4 个器件通信地址
  - I<sup>2</sup>S, 左、右边对齐, TDM 音频格式
  - 3 线数字音频输入
  - 采样 32kHz, 44.1kHz/48kHz, 88.2kHz/96kHz, 176.4kHz/192kHz
  - SDOUT 数字音频输出支持回声消除
- 集成音效算法
  - 数字/模拟增益调整
  - 小音量低音增强
  - 左右通道独立具备 2×15 个 BQs, 另外加 2×5 个 post BQs 加强音效调节
  - 防爆音的压缩器前后调节音量, 动态维护音频处理中的动态范围
  - 3 段 DRC, 提前能量预测结合后端均衡器, 实现平滑的多段音效控制, 提高音乐清晰度
- 保护机制
  - FAULT 状态输出
  - OCP 过流保护、OTP 过热保护
  - UVLO 过压欠压保护
  - 数字音频时钟检查

#### 2. 应用

- 便携式音箱: 蓝牙音响、拉杆音响
- 智能音响, 智能设备
- 家庭音频: 电视、家庭影院
- Soundbar, 条形音响, 桌面音响
- 笔记本电脑、台式机

#### 3. 概述

ACM8625M 一款高度集成、高效率的双通道数字输入功放。供电电压范围在 4.5V-26.4V, 数字接口电源支持 3.3V 或 1.8V。在 8 欧负载下, 输出功率可以到 2×26W, PBTL 模式下单通道可以输出 1×52W @1% THD+N。

ACM8625M 采用新型 PWM 脉宽调制架构, 根据信号大小动态调整脉宽, 在保证音频性能前提下, 降低静态功耗, 提高效率, 另外防止 POP 音的产生。

CLASS H 动态升压控制技术, 针对电池升压产品, 根据音乐信号大小, 动态调整升压, 降低升压芯片和功放的热量功耗, 极大程度的延长播放时长。

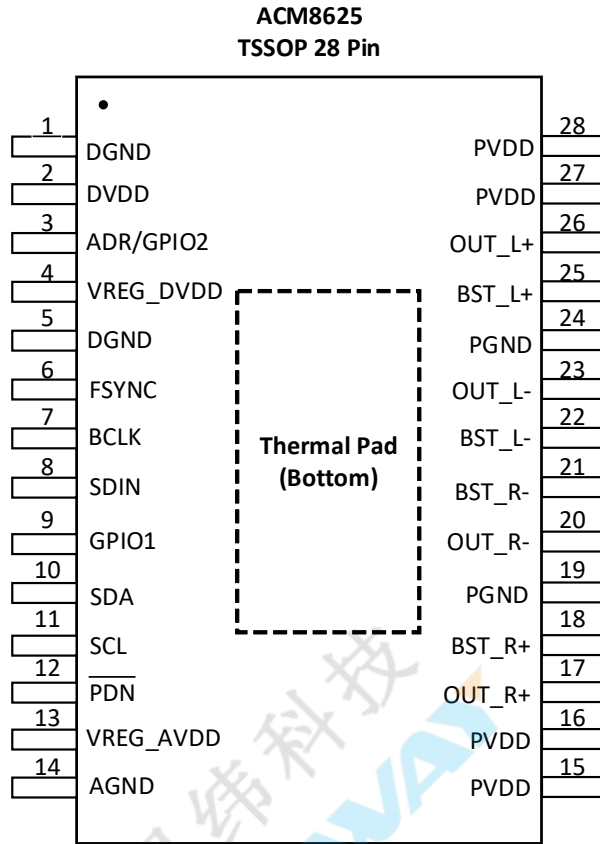
扩频技术的应用可以大幅降低 EMI 辐射, 在功率和喇叭线长一定的范围内, 可以用磁珠替代电感方案, 从而优化成本和电路面积。

ACM8625M 高度集成了多种音效算法。内部模块可以独立控制, 左右通道也可以独立控制。内部集成数字、模拟增益调节, 信号混合模块, 15 个 EQ 和 5 个 post EQ, 可编程特定频段信号动态增强, 3 段提前能量预测 DRC 外加 1 段 AGL 等多个独立模块, 可实现多种音效。例如小信号低音增强, 高低音补偿等功能可以通过这些模块实现。

#### 4. 芯片信息

| 料号       | 封装       | 尺寸              | Pcs/盘 |
|----------|----------|-----------------|-------|
| ACM8625M | TSSOP 28 | 9.7 mm × 4.4 mm | 3000  |

5. 管脚定义



| Pin No. | 管脚名称             | 类型   | 描述   |
|---------|------------------|------|--|
| 1       | DGND             | PWR  | 数字地  |
| 2       | DVDD             | PWR  | 数字电源输入: 3.3V 或 1.8V.   |
| 3       | ADR/GPIO2        | DIO  | I <sup>2</sup> C 地址选择 /<br>GPIO2: FAULT / WARNING / SDOUT... |
| 4       | VREG_DVDD        | AOUT | 1.8V 数字调节器输出.  |
| 5       | DGND             | PWR  | 数字地  |
| 6       | FSYNC            | DIN  | TDM 信号帧同步 (或 I <sup>2</sup> S 左右通道选择) 时钟                     |
| 7       | BCLK             | DIN  | TDM/I <sup>2</sup> S 的位选择时钟                                  |
| 8       | SDIN             | DIN  | 串行数据输入   |
| 9       | GPIO1            | DIO  | GPIO1: FAULT / WARNING / SDOUT...                            |
| 10      | SDA              | DIO  | I <sup>2</sup> C 串行数据.                                       |
| 11      | SCL              | DIN  | I <sup>2</sup> C clock.                                      |
| 12      | $\overline{PDN}$ | DIN  | 关机, 低有效.   |
| 13      | VREG_AVDD        | AOUT | 5.0V 模拟调节器输出.  |
| 14      | AGND             | PWR  | 模拟地  |
| 15      | PVDD             | PWR  | 输入电源   |
| 16      | PVDD             | PWR  | 输入电源   |
| 17      | OUT_R+           | AOUT | 右通道输出正极  |

## ACM8625M

|    |        |      |              |
|----|--------|------|--------------|
| 18 | BST_R+ | AIN  | 右通道输出正极的自举电容 |
| 19 | PGND   | PWR  | 电源功率地        |
| 20 | OUT_R- | AOUT | 右通道输出负极      |
| 21 | BST_R- | AIN  | 右通道输出负极的自举电容 |
| 22 | BST_L- | AIN  | 左通道输出负极的自举电容 |
| 23 | OUT_L- | AOUT | 左通道输出负极      |
| 24 | PGND   | PWR  | 电源功率地        |
| 25 | BST_L+ | AIN  | 左通道输出正极的自举电容 |
| 26 | OUT_L+ | AOUT | 左通道输出正极      |
| 27 | PVDD   | PWR  | 输入供电电源       |
| 28 | PVDD   | PWR  | 输入供电电源       |

### 6. 系列比较

| 料号       | $R_{dson}$ | 供电电源 PVDD    | 输出功率                            |
|----------|------------|--------------|---------------------------------|
| ACM8615  | 135 mΩ     | 4.5V ~ 21V   | 单通道 1×21W (8Ω, 20V, THD+N = 1%) |
| ACM8625M | 135 mΩ     | 4.5V ~ 26.4V | 立体声 2×26W (8Ω, 22V, THD+N = 1%) |

## 7. 规格参数

### 7.1 绝对最大值

| 符号             | 描述      | MIN  | MAX            | UNIT |
|----------------|---------|------|----------------|------|
| DVDD           | 数字电源    | -0.3 | 3.9            | V    |
| PVDD           | 输入电源    | -0.3 | 30             | V    |
| $V_{I(DIGIN)}$ | 数字输入参考脚 | -0.5 | $V_{DVDD}+0.5$ | V    |
| $V_{I(OUTXX)}$ | 输出脚电压   | -0.3 | 32             | V    |
| $T_A$          | 环境工作温度  | -25  | 85             | °C   |
| $T_{stg}$      | 存储问题    | -40  | 125            | °C   |

- 超出以上绝对最大值范围会导致器件损坏。以上仅仅是绝对最大值范围，不是应用范围。这个范围并不意味着器件能在这个条件下工作，超出绝对最大值范围会影响器件的可靠性。
- DVDD 数字输入参考脚包含: ADR/GPIO2, GPIO3, FSYNC, BCLK, SDIN, GPIO1, SDA, SCL, PDN.

### 7.2 ESD 特性

|             |                         |   | VALUE | UNIT |
|-------------|-------------------------|---|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | 人体模式(HBM), per ANSI/ESDA/ JEDEC JS-001            | +2000 | V    |
|             |                         | 组件充电模式 (CDM), per JEDEC specification JESD22-C101 | +500  |      |

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 推荐工作条件

Over operating free-air temperature range (unless otherwise noted)

|                 |             |                               | MIN          | NOM | MAX          | UNIT |
|-----------------|-------------|-------------------------------|--------------|-----|--------------|------|
| $V_{(SUPPLY)}$  | 输入电源        | 数字电源 DVDD                     | 1.62         |     | 3.63         | V    |
|                 |             | 供电电源 PVDD                     | 4.5          |     | 26.4         |      |
|                 | 推荐的 PVDD 范围 | 双通道, 喇叭负载=4Ω (+/-20% 余量)      | 4.5          |     | 19.2         | V    |
|                 |             | 双通道, 喇叭负载=6Ω (+/-20% 余量)      | 4.5          |     | 26.4         |      |
|                 |             | 双通道, 喇叭负载=8Ω (+/-20% 余量)      | 4.5          |     | 26.4         |      |
|                 |             | PBTL 单通道, 喇叭负载=2Ω (+/-20% 余量) | 4.5          |     | 19.2         |      |
|                 |             | PBTL 单通道, 喇叭负载=3Ω (+/-20% 余量) | 4.5          |     | 26.4         |      |
|                 |             | PBTL 单通道, 喇叭负载=4Ω (+/-20% 余量) | 4.5          |     | 26.4         |      |
| $V_{IH(DIGIN)}$ | DVDD 参考高电平  |                               | 0.9×<br>DVDD |     | DVDD         | V    |
| $V_{IL(DIGIN)}$ | DVDD 参考低电平  |                               |              |     | 0.1×<br>DVDD |      |

|                  |         | MIN | NOM | MAX | UNIT |
|------------------|---------|-----|-----|-----|------|
| L <sub>OUT</sub> | 输出最小电感量 | 1   |     |     | μH   |
| T <sub>J</sub>   | 结工作温度   | -40 |     | 150 | °C   |
| T <sub>A</sub>   | 环境工作温度  | -40 |     | 85  | °C   |

## 7.4 热性能信息

|                 |              | ACM8625M<br>TSSOP 28 PINS<br>JEDEC STANDARD<br>4-LAYER PCB | UNIT |
|-----------------|--------------|--|------|
| θ <sub>JA</sub> | 结到环境温度热阻     | 28   | °C/W |
| θ <sub>JT</sub> | 结到顶部热阻       | 22   | °C/W |
| ψ <sub>JT</sub> | 结到 TOP 的参数热阻 | 1.2  | °C/W |

## 7.5 电气特性

室温 25°C, BD 模式, LC filter=4.7uH+0.68uF, Fsw=480kHz, (unless otherwise noted)

| 参数                         | 测试条件                     | MI<br>N  | TYP      | MA<br>X | 单位                        |
|----------------------------|--------------------------|--|----------|---------|---------------------------|
| <b>数字 I/O</b>              |                          |  |          |         |                           |
| I <sub>IH</sub>            | 输入逻辑高电流范围                |  |          | 10      | μA                        |
| I <sub>IL</sub>            | 输入逻辑低电流范围                |  |          | -10     | μA                        |
| V <sub>IH(Digin)</sub>     | 输入逻辑高电平范围                | 70<br>%  |          |         | V <sub>DVDD</sub>         |
| V <sub>IL(Digin)</sub>     | 输入逻辑低电平范围                |  |          | 30%     | V <sub>DVDD</sub>         |
| V <sub>OH(Digin)</sub>     | 输出逻辑高电平范围                | I <sub>OH</sub> = 2mA  | 80<br>%  |         | V <sub>DVDD</sub>         |
| V <sub>OL(Digin)</sub>     | 输出逻辑低电平范围                | I <sub>OH</sub> = -2mA   |          | 20%     | V <sub>DVDD</sub>         |
| <b>I<sup>2</sup>C 控制端口</b> |                          |  |          |         |                           |
| C <sub>L(I2C)</sub>        | I <sup>2</sup> C 容许的负载电容 |  |          | 400     | pF                        |
| F <sub>SCL(fast)</sub>     | 支持 SCL 高频率               | No wait states, fast mode  |          | 400     | kHz                       |
| F <sub>SCL(slow)</sub>     | 支持 SCL 低频率               | No wait states, slow mode  |          | 100     | kHz                       |
| <b>串行音频端口</b>              |                          |  |          |         |                           |
| t <sub>DLY</sub>           | 需要 FSYNC 到 BCLK 的上升沿延迟   |  | 5        |         | ns                        |
| D <sub>SCLK</sub>          | 允许的 SCLK 占空比             |  | 40<br>%  | 60%     |                           |
| f <sub>S</sub>             | 输入采样率                    |  | 32       | 192     | kHz                       |
| F <sub>BCLK</sub>          | BCLK 频率                  |  | 32       | 64      | f <sub>S</sub>            |
| <b>功放工作模式和直流参数</b>         |                          |  |          |         |                           |
| t <sub>OFF</sub>           | 关机时间                     |  |          | 10      | ms                        |
| A <sub>V(SPK_AMP)</sub>    | 可编程增益                    | 输入 (1FS)条件下, 峰值电压的值  | 4.9<br>5 | 29.5    | V <sub>peak</sub> /F<br>S |
| ΔA <sub>V(SPK_AMP)</sub>   | 增益误差                     | Gain=29.5V <sub>p</sub> /FS  |          | 0.5     | dB                        |
| F <sub>SW</sub>            | 放大器开关频率                  |  |          | 384     | kHz                       |
|                            |                          |  |          | 260     | kHz                       |
|                            |                          |  |          | 480     | kHz                       |
|                            |                          |  |          | 576     | kHz                       |
|                            |                          |  |          | 768     | kHz                       |
| R <sub>DS(ON)</sub>        | 输出端 MOSFETs 内阻           | FET + Metallization. V <sub>PVDD</sub> =24V, I <sub>(OUT)</sub> =500mA, T <sub>J</sub> =25°C |          | 135     | mΩ                        |
| <b>保护参数</b>                |                          |  |          |         |                           |

# ACM8625M

| 参数                              |  | 测试条件   | MI<br>N | TYP  | MA<br>X | 单位    |
|---------------------------------|--|--|---------|------|---------|-------|
| OCE <sub>THRES</sub>            | 过流点阈值  | 喇叭输出电流 PVDD=24V (100Hz Burst on, 500 cycles interval), 输出 LC =4.7uF+0.68uF, Fsw=480kHz | 6       | 6.5  |         | A     |
| UVE <sub>THRES(PVD<br/>D)</sub> | PVDD 欠压保护阈值  |  |         | 4    |         | V     |
| OVE <sub>THRES(PVD<br/>D)</sub> | PVDD 过压保护阈值  |  |         | 28   |         | V     |
| DCE <sub>THRES</sub>            | 输出直流检测   | 输出端检测阈值  |         | 1.9  |         | V     |
| T <sub>DCDET</sub>              | 输出直流检测时间   | 触发保护时间   |         | 570  |         | ms    |
| OTE <sub>THRES</sub>            | 过温保护   |  |         | 160  |         | °C    |
| OTE <sub>Hysteresis</sub>       | 过温保护迟滞   |  |         | 10   |         | °C    |
| OTW <sub>THRES</sub>            | 过温警告温度   |  |         | 135  |         | °C    |
| <b>音频性能 (双通道输出)</b>             |  |  |         |      |         |       |
| V <sub>OS</sub>                 | 放大器输出偏移电压  | 0 信号输入, 可编程增益 29.5Vp/FS, V <sub>PVDD</sub> =12V  | -5      |      | 5       | mV    |
| P <sub>O(SPK)</sub>             | 输出功率 (每通道)   | V <sub>PVDD</sub> =12V, R <sub>SPK</sub> =4Ω, f=1kHz, THD+N=10%                        |         | 14.6 |         | W     |
|                                 |  | V <sub>PVDD</sub> =12V, R <sub>SPK</sub> =4Ω, f=1kHz, THD+N=1%                         |         | 12.2 |         | W     |
|                                 |  | V <sub>PVDD</sub> =18V, R <sub>SPK</sub> =6Ω, f=1kHz, THD+N=10%                        |         | 27.2 |         | W     |
|                                 |  | V <sub>PVDD</sub> =18V, R <sub>SPK</sub> =6Ω, f=1kHz, THD+N=1%                         |         | 22.2 |         | W     |
|                                 |  | V <sub>PVDD</sub> =24V, R <sub>SPK</sub> =8Ω, f=1kHz, THD+N=10%                        |         | 37.6 |         | W     |
|                                 |  | V <sub>PVDD</sub> =24V, R <sub>SPK</sub> =8Ω, f=1kHz, THD+N=1%                         |         | 30.7 |         | W     |
| THD+N <sub>SPK</sub>            | 谐波和噪音 (P <sub>O</sub> =1W, f=1kHz, R <sub>SPK</sub> =6Ω) | V <sub>PVDD</sub> =12V   |         | 0.01 |         | %     |
|                                 |  | V <sub>PVDD</sub> =18V   |         | 0.01 |         | %     |
|                                 |  | V <sub>PVDD</sub> =24V   |         | 0.01 |         | %     |
| ICN <sub>(SPK)</sub>            | 底噪 (A 加权, AES17)   | V <sub>PVDD</sub> =12V, LC filter=10uH+0.47uF, Load=6Ω                                 |         | 30.5 |         | μVrms |
|                                 |  | V <sub>PVDD</sub> =18V, LC filter=10uH+0.47uF, Load=6Ω                                 |         | 30.6 |         | μVrms |
| DR                              | 动态范围   | 加权, -60dBFS method. V <sub>PVDD</sub> =24V, Analog Gain=29.5Vp/FS                      |         | 111  |         | dB    |
| SNR                             | 信噪比  | 加权, 1% THD+N 输出水平, V <sub>PVDD</sub> =24V  |         | 114  |         | dB    |
| PSRR                            | 电源纹波抑制比  | Injected Noise=1kHz, 1Vrms, V <sub>PVDD</sub> =12V, 输入信号 0                             |         | 72   |         | dB    |
| X-talk <sub>SPK</sub>           | 串扰   | f=1kHz, V <sub>PVDD</sub> =24V, Load=8Ω  |         | 90   |         | dB    |
| <b>音频性能 (单通道 PBTl)</b>          |  |  |         |      |         |       |
| V <sub>OS</sub>                 | 放大器输出偏移电压  | 0 信号输入, 可编程增益 29.5Vp/FS, V <sub>PVDD</sub> =12V  | -5      |      | 5       | mV    |
| P <sub>O(SPK)</sub>             | 输出功率   | V <sub>PVDD</sub> =24V, R <sub>SPK</sub> =4Ω, f=1kHz, THD+N=1%                         |         | 62   |         | W     |
|                                 |  | V <sub>PVDD</sub> =24V, R <sub>SPK</sub> =4Ω, f=1kHz, THD+N=10%                        |         | 76   |         | W     |
|                                 |  | V <sub>PVDD</sub> =18V, R <sub>SPK</sub> =3Ω, f=1kHz, THD+N=1%                         |         | 35.5 |         | W     |

# ACM8625M

| 参数                   | 测试条件  | MIN | TYP  | MAX | 单位 |
|----------------------|---|-----|------|-----|----|
|                      | $V_{PVDD}=18V, R_{SPK}=3\Omega, f=1kHz, THD+N=10\%$                             |     | 44   |     | W  |
| THD+N <sub>SPK</sub> | 谐波和噪音 ( $P_O=1W, f=1kHz$ )  |     | 0.04 |     | %  |
|                      | $V_{PVDD}=24V, LC\ filter, R_{SPK}=4\Omega$                                     |     | 0.04 |     | %  |
| DR                   | 加权, 1% THD+N 输出水平, $V_{PVDD}=24V, R_{SPK}=4\Omega$                              |     | 115  |     | dB |
| SNR                  | A-Weighted, reference to 1% THD+N Output Level, $V_{PVDD}=24V, R_{SPK}=4\Omega$ |     | 117  |     | dB |
| PSRR                 | Injected Noise=1kHz, 1Vrms, $V_{PVDD}=12V$ , 输入信号 0                             |     | 72   |     | dB |

## 7.6 时序要求

|                                  |   | MIN         | NOM | MAX  | UNIT    |
|----------------------------------|---|-------------|-----|------|---------|
| 串行音频端口计时从模式                      |   |             |     |      |         |
| $f_{BCLK}$                       | BCLK 频率   | 1.024       |     |      | MHz     |
| $f_{BCLK}$                       | BCLK 周期   | 40          |     |      | ns      |
| $f_{BCLKL}$                      | BCLK 脉冲宽度, 低  | 16          |     |      | ns      |
| $f_{BCLKH}$                      | BCLK 脉冲宽度, 高  | 16          |     |      | ns      |
| $t_{BF}$                         | BCLK 到 FSYNC 上升沿  | 8           |     |      | ns      |
| $t_{FB}$                         | FSYNC 边沿到 BCLK 上升沿  | 8           |     |      | ns      |
| $t_{SU}$                         | 数据设置时间, 在 BCLK 上升沿前   | 8           |     |      | ns      |
| $t_{DH}$                         | Data 保持时间, 在 BCLK 上升沿后  | 8           |     |      | ns      |
| $t_{DFB}$                        | Data 延迟时间从 BCLK 下降沿   |             |     | 15   | ns      |
| I <sup>2</sup> C Bus 总线时序        |   |             |     |      |         |
| $f_{SCL}$                        | SCL 时钟频率  |             |     | 100  | kHz     |
| $t_{BUF}$                        | Bus 空闲时间从停止和启动时间  | 4.7         |     |      | $\mu$ s |
| $t_{LOW}$                        | 时钟的低周期  | 4.7         |     |      | $\mu$ s |
| $t_{HI}$                         | SCL clock 的高周期  | 4           |     |      | $\mu$ s |
| $t_{RS-SU}$                      | START 条件的设置时间 (重复)  | 4.7         |     |      | $\mu$ s |
| $t_{S-HD}$                       | START 条件的保持时间 (重复)  | 4           |     |      | $\mu$ s |
| $t_{D-SU}$                       | 数据设置时间  | 250         |     |      | ns      |
| $t_{D-HD}$                       | 数据保持时间  | 0           |     | 3450 | ns      |
| $t_{SCL-R}$                      | SCL 信号的上升时间   | $20+0.1C_B$ |     | 1000 | ns      |
| $t_{SCL-R1}$                     | Rise time of SCL signal after a repeated START condition and after an acknowledge bit | $20+0.1C_B$ |     | 1000 | ns      |
| $t_{SCL-F}$                      | Fall time of SCL signal   | $20+0.1C_B$ |     | 1000 | ns      |
| $t_{SDA-R}$                      | Rise time of SDA signal   | $20+0.1C_B$ |     | 1000 | ns      |
| $t_{SDA-F}$                      | Fall time of SDA signal   | $20+0.1C_B$ |     | 1000 | ns      |
| $t_{P-SU}$                       | Setup time for STOP condition   | 4           |     |      | $\mu$ s |
| $C_B$                            | Capacitive load for each bus line   |             |     | 400  | pf      |
| I <sup>2</sup> C Bus Timing-Fast |   |             |     |      |         |

# ACM8625M

|              |   | MIN         | NOM | MAX | UNIT    |
|--------------|---|-------------|-----|-----|---------|
| $f_{SCL}$    | SCL clock frequency   |             |     | 400 | kHz     |
| $t_{BUF}$    | Bus free time between a STOP and START condition                                      | 1.3         |     |     | $\mu$ s |
| $t_{LOW}$    | Low period of the SCL clock   | 1.3         |     |     | $\mu$ s |
| $t_{HI}$     | High period of the SCL clock  | 600         |     |     | ns      |
| $t_{RS-SU}$  | Setup time for (repeated) START condition   | 600         |     |     | ns      |
| $t_{RS-HD}$  | Hold time for (repeated) START condition  | 600         |     |     | ns      |
| $t_{D-SU}$   | Data setup time   | 100         |     |     | ns      |
| $t_{D-HD}$   | Data hold time  | 0           |     | 900 | ns      |
| $t_{SCL-R}$  | Rise time of SCL signal   | $20+0.1C_B$ |     | 300 | ns      |
| $t_{SCL-R1}$ | Rise time of SCL signal after a repeated START condition and after an acknowledge bit | $20+0.1C_B$ |     | 300 | ns      |
| $t_{SCL-F}$  | Fall time of SCL signal   | $20+0.1C_B$ |     | 300 | ns      |
| $t_{SDA-R}$  | Rise time of SDA signal   | $20+0.1C_B$ |     | 300 | ns      |
| $t_{SDA-F}$  | Fall time of SDA signal   | $20+0.1C_B$ |     | 300 | ns      |
| $t_{P-SU}$   | Setup time for STOP condition   | 600         |     |     | ns      |
| $t_{SP}$     | Pulse width of spike suppressed   |             |     | 50  | ns      |
| $C_B$        | Capacitive load for each bus line   |             |     | 400 | pf      |

## 7.7 时序参数要求信息

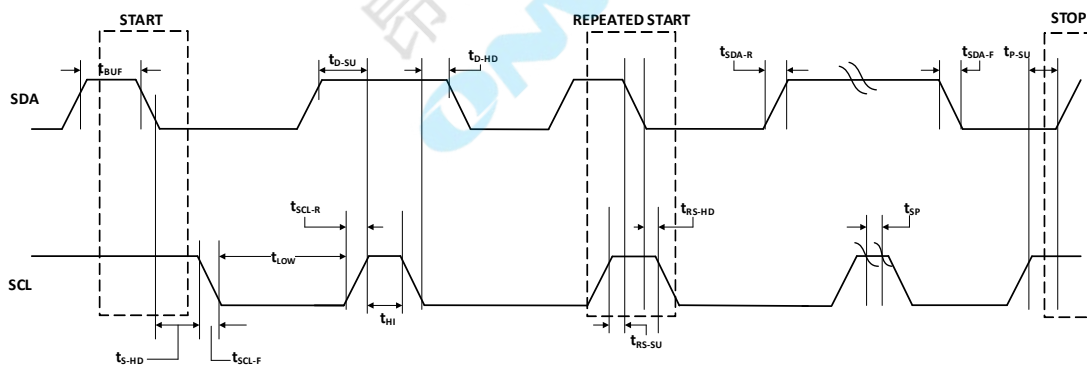


Figure 1 I<sup>2</sup>C Communication Port Timing Diagram



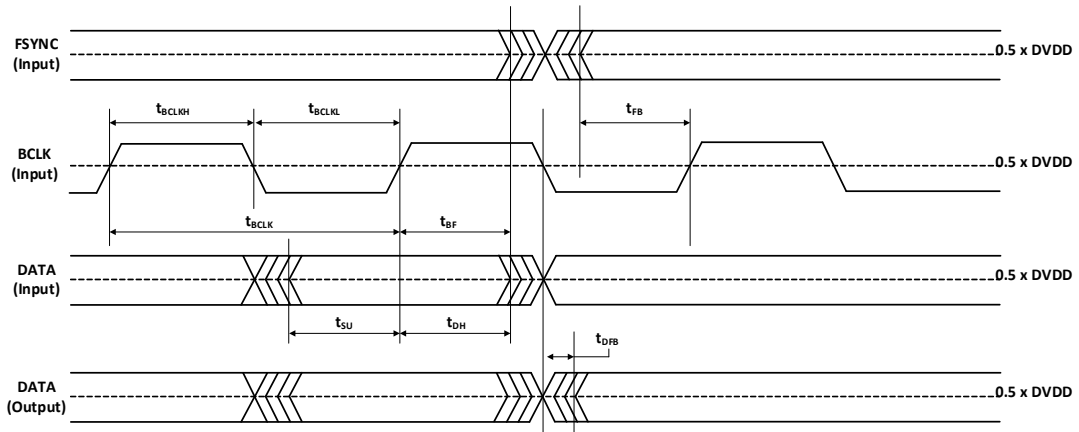


Figure 2 Serial Audio Port Timing in Slave Mode

## 8. 静态功耗

### 8.1 DVDD 电流

室温 25°C, 48kHz 采样频率.

Table 1 DVDD Current

| DVDD (V) | Device Mode             | Current Consumption (mA) | Setting Register Location       |
|----------|-------------------------|--------------------------|---------------------------------|
| 3.3      | Play Mode (DSP Enable)  | 30.65                    | Register 0x04                   |
|          | Play Mode (DSP Bypass)  | 13.066                   | Register 0x04 and Register 0x05 |
|          | Driver-off (DSP Enable) | 30.375                   | Register 0x04                   |
|          | Driver-off (DSP Bypass) | 12.798                   | Register 0x04                   |
|          | Analog-off              | 0.933                    | Register 0x04                   |
|          | Digital-off             | 0.848                    | Register 0x04                   |
|          | PDN=0                   | 0.007                    | Pin 12 pulled to low            |
| 1.8      | Play Mode (DSP Enable)  | 27.68                    | Register 0x04                   |
|          | Play Mode (DSP Bypass)  | 13                       | Register 0x04 and Register 0x05 |
|          | Driver-off (DSP Enable) | 27.47                    | Register 0x04                   |
|          | Driver-off (DSP Bypass) | 12.7                     | Register 0x04                   |
|          | Analog-off              | 0.688                    | Register 0x04                   |
|          | Digital-off             | 0.604                    | Register 0x04                   |
|          | PDN=0                   | 0.0019                   | Pin 12 pulled to low            |

### 8.2 PVDD 电流

室温 25°C, 48kHz 采样频率, LC Filter=10uH+0.68uF.

Table 2 PVDD Current

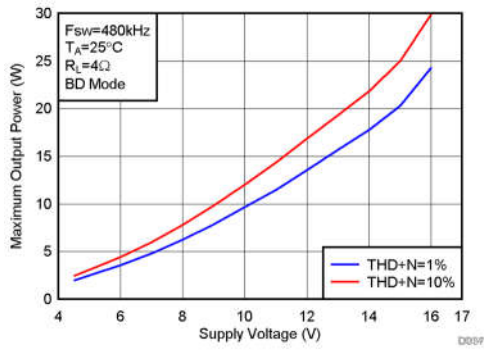
| PVDD | Device Mode | Current | Setting Register Location |
|------|-------------|---------|---------------------------|
|------|-------------|---------|---------------------------|

| (V)  |                           | Consumption (mA) |                      |
|------|---------------------------|------------------|----------------------|
| 7.4  | Play                      | 19.176           | Register 0x04        |
|      | Driver-off                | 9.593            |                      |
|      | Analog-off                | 5.897            |                      |
|      | Digital-off               | 0.0924           |                      |
|      | $\overline{\text{PDN}}=0$ | 0.0062           | Pin 12 pulled to low |
| 12   | Play                      | 24.996           | Register 0x04        |
|      | Driver-off                | 9.623            |                      |
|      | Analog-off                | 5.943            |                      |
|      | Digital-off               | 0.0934           |                      |
|      | $\overline{\text{PDN}}=0$ | 0.0069           | Pin 12 pulled to low |
| 16   | Play                      | 31.063           | Register 0x04        |
|      | Driver-off                | 9.67             |                      |
|      | Analog-off                | 5.998            |                      |
|      | Digital-off               | 0.0938           |                      |
|      | $\overline{\text{PDN}}=0$ | 0.0075           | Pin 12 pulled to low |
| 18.5 | Play                      | 35.103           | Register 0x04        |
|      | Driver-off                | 9.705            |                      |
|      | Analog-off                | 6.035            |                      |
|      | Digital-off               | 0.0944           |                      |
|      | $\overline{\text{PDN}}=0$ | 0.0082           | Pin 12 pulled to low |
| 24   | Play                      | 44.861           | Register 0x04        |
|      | Driver-off                | 9.787            |                      |
|      | Analog-off                | 6.112            |                      |
|      | Digital-off               | 0.098            |                      |
|      | $\overline{\text{PDN}}=0$ | 0.009            | Pin 12 pulled to low |

## 9. 典型特性曲线

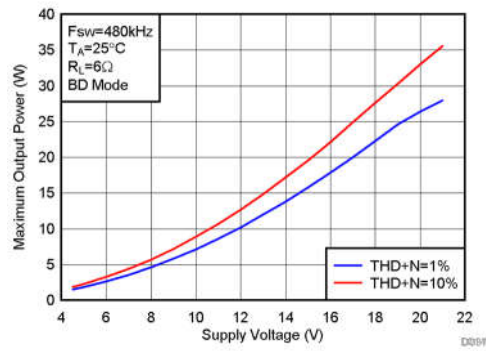
### 9.1 双通道桥式输出(BTL)曲线 BD 模式

室温 25°C. 测量基于 ACM8625MEVM 评估板和 Audio Precision System 2722 (内部使用 20-kHz brick-wall filter). PWM 调制方式采用 BD mode, Class D 的环路带宽设置为 180kHz, 开关频率设置为 480kHz.



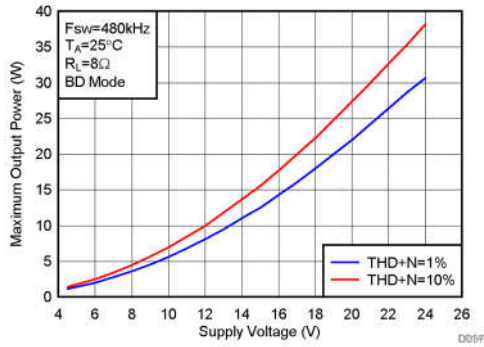
(Load=4Ω, Fsw=480kHz, BD Mode)

Figure 3 Output Power vs PVDD



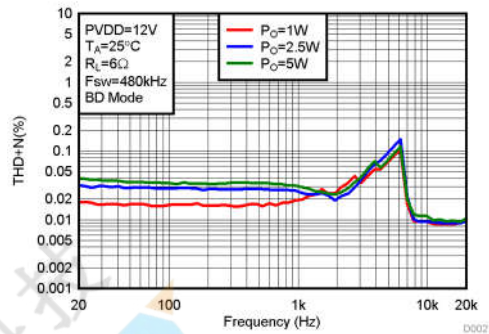
(Load=6Ω, Fsw=480kHz, BD Mode)

Figure 4 Output Power vs PVDD



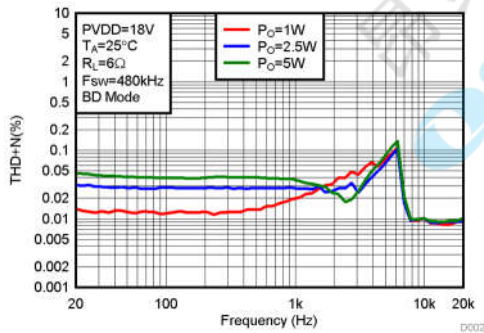
(Load=8Ω, Fsw=480kHz, BD Mode)

Figure 5 Output Power vs PVDD



(PVDD=12V, Load=6Ω, Fsw=480kHz)

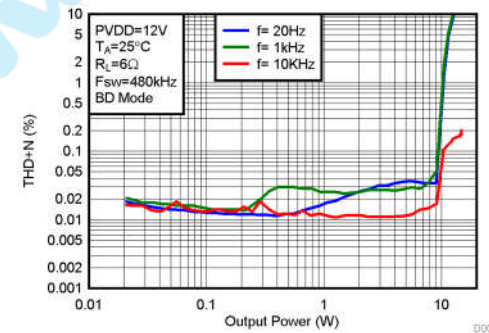
Figure 6 THD+N vs Frequency



(PVDD=18V, Load=6Ω, Fsw=480kHz)

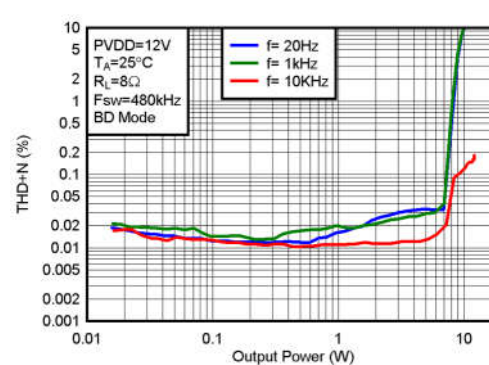
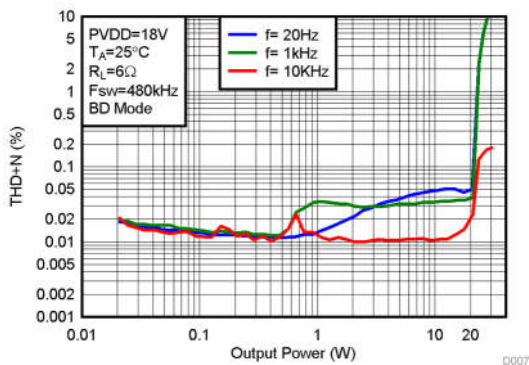
Fsw=480kHz)

Figure 7 THD+N vs Frequency



(PVDD=12V, Load=6Ω,

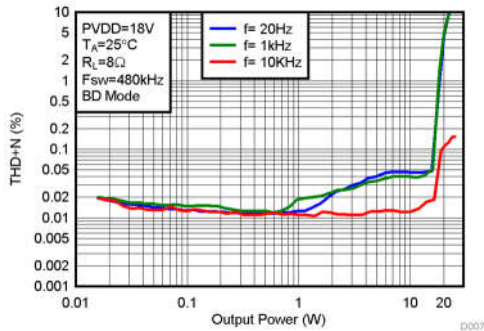
Figure 8 THD+N vs Output Power



(PVDD=18V, Load=6Ω, Fsw=480kHz)

Figure 9 THD+N vs Output Power

Power



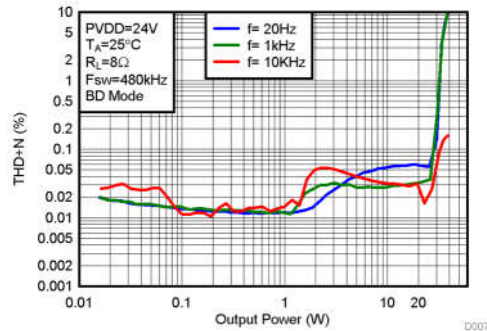
(PVDD=18V, Load=8Ω, Fsw=480kHz)

Figure 11 THD+N vs Output Power

Power

(PVDD=12V, Load=8Ω, Fsw=480kHz)

Figure 10 THD+N vs Output Power

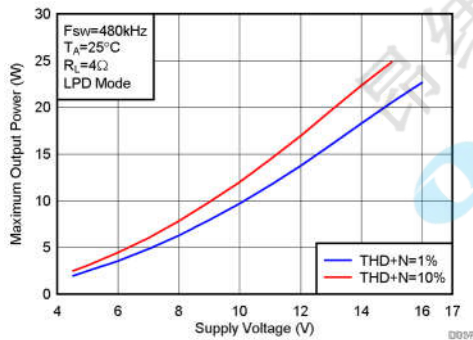


(PVDD=24V, Load=8Ω, Fsw=480kHz)

Figure 12 THD+N vs Output Power

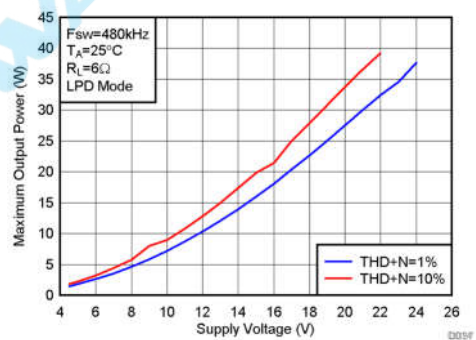
## 9.2 双通道桥式输出 (BTL) 曲线 LPD 模式

室温 25°C. 测量基于 ACM8625MEVM 评估板和 Audio Precision System 2722 (内部使用 20-kHz brick-wall filter). PWM 调制方式采用低功耗模式 (LPD mode), Class D 的环路带宽设置为 105kHz, 开关频率设置为 480kHz.



(Load=4Ω, Fsw=480kHz, LPD Mode)

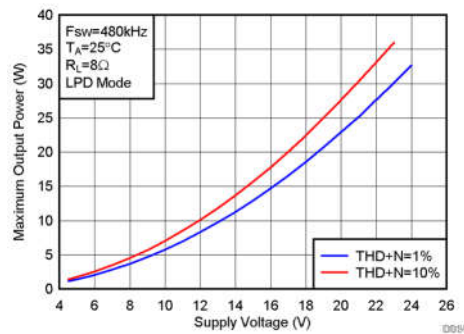
Figure 13 Output Power vs PVDD



(Load=6Ω, Fsw=480kHz, LPD Mode)

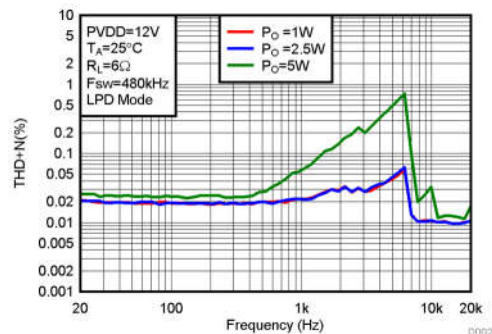
Figure 14 Output Power vs PVDD

PVDD



(Load=8Ω, Fsw=480kHz, LPD Mode)

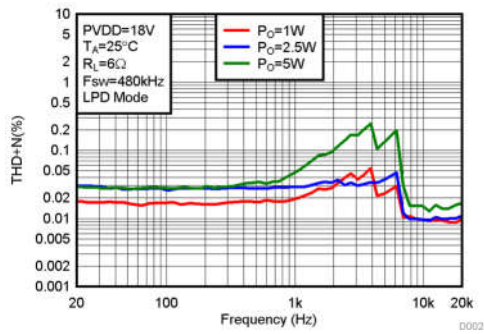
Figure 15 Output Power vs PVDD



(PVDD=12V, Load=6Ω, Fsw=480kHz)

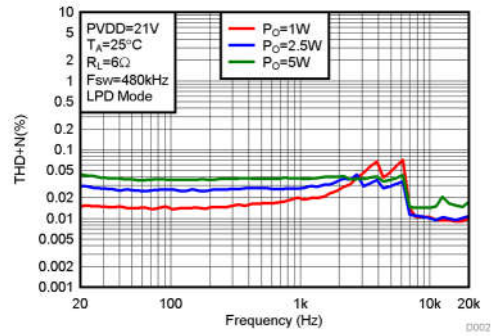
Figure 16 THD+N vs Frequency

Frequency



(PVDD=18V, Load=6Ω, Fsw=480kHz)

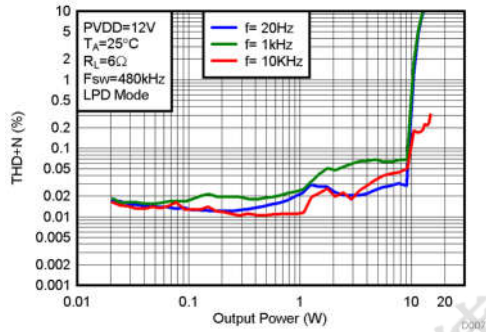
Figure 17 THD+N vs Frequency



(PVDD=21V, Load=6Ω, Fsw=480kHz)

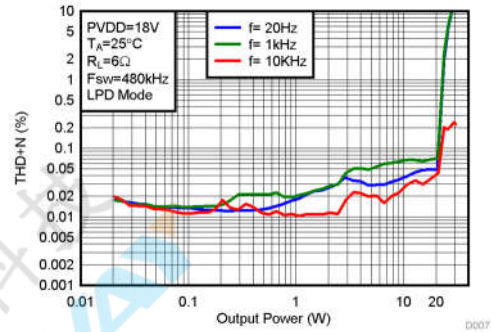
Figure 18 THD+N vs

Frequency



(PVDD=12V, Load=6Ω, Fsw=480kHz)

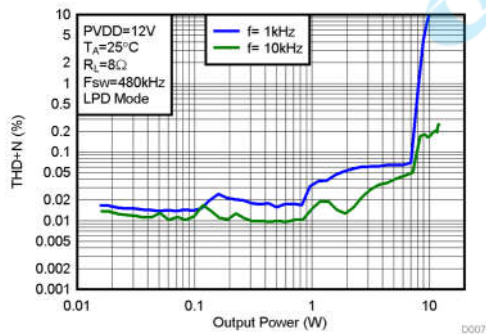
Figure 19 THD+N vs Output Power



(PVDD=18V, Load=8Ω, Fsw=480kHz)

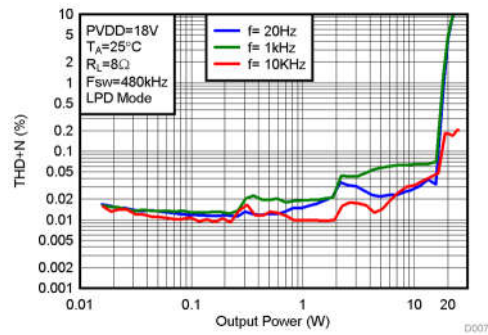
Figure 20 THD+N vs Output

Power



(PVDD=12V, Load=8Ω, Fsw=480kHz)

Figure 21 THD+N vs Output Power

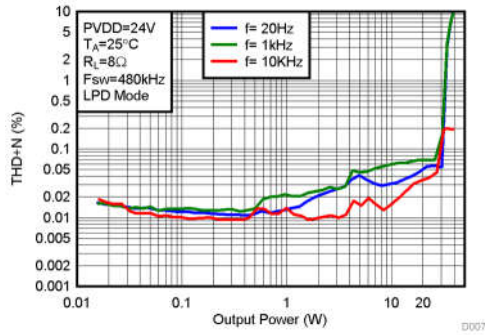


(PVDD=18V, Load=8Ω, Fsw=480kHz)

Figure 22 THD+N vs Output

Power

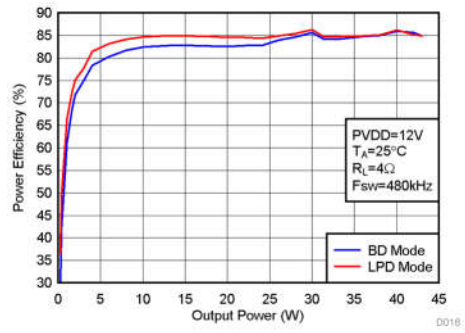




(PVDD=24V, Load=8Ω, Fsw=480kHz)

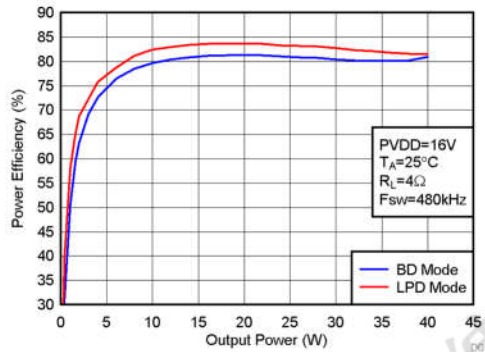
Figure 23 THD+N vs Output Power

Output Power



(PVDD=12V, Load=4Ω,

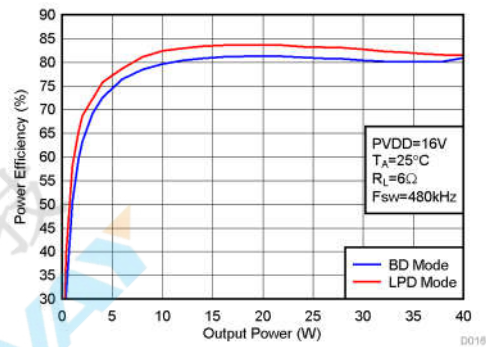
Figure 24 Efficiency vs



(PVDD=16V, Load=4Ω, Fsw=480kHz)

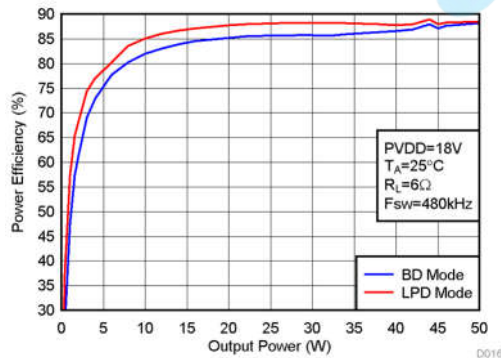
Figure 25 Efficiency vs Output Power

Output Power



(PVDD=16V, Load=6Ω,

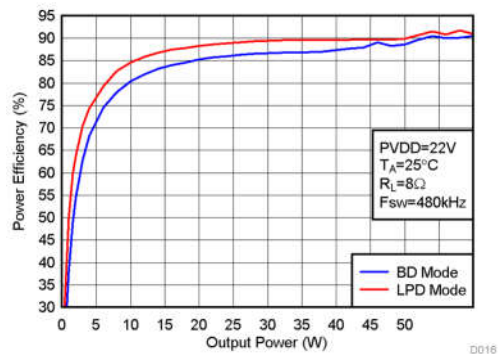
Figure 26 Efficiency vs



(PVDD=18V, Load=6Ω, Fsw=480kHz)

Figure 27 Efficiency vs Output Power

Output Power



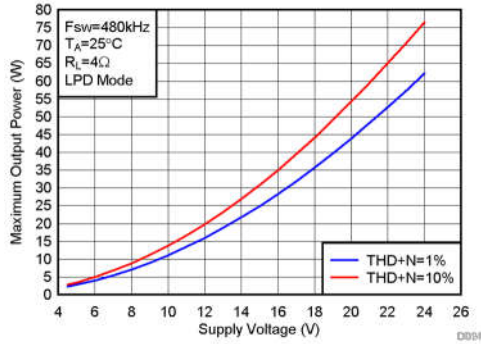
(PVDD=22V, Load=8Ω,

Figure 28 Efficiency vs

### 9.3 单通道并行桥式输出 (PBTL) 曲线 LPD 模式

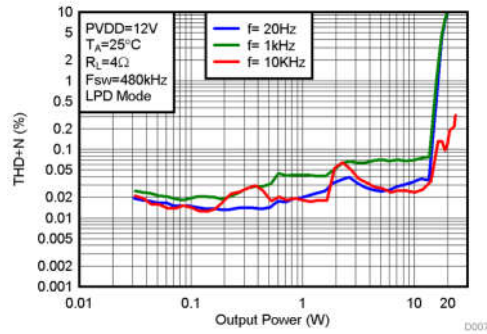
室温 25°C. 测量基于 ACM8625MEVM 评估版和 Audio Precision System 2722 (内部使用 20-kHz brick-wall filter). PWM 调制方式采用低功耗模式 (LPD mode), Class D 的环路带宽设置为 105kHz,

开关频率设置为 480kHz.



(Load=4Ω, Fsw=480kHz, LPD Mode)

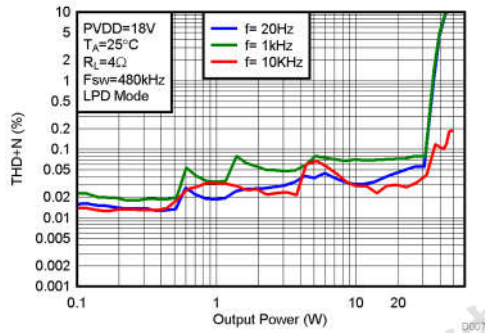
Figure 29 Output Power vs PVDD



(Load=4Ω, Fsw=480kHz, LPD Mode)

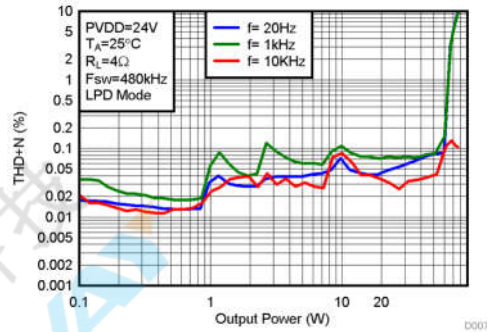
Figure 30 THD+N vs Output

Power



(Load=4Ω, Fsw=480kHz, LPD Mode)

Figure 31 THD+N vs Output Power



(Load=4Ω, Fsw=480kHz, LPD Mode)

Figure 32 THD+N vs Output

Mode)

Power

## 10. 细节描述

### 10.1 总述

ACM8625M 架构上包含 4 个主要模块，集成模块保障了音频质量、更加灵活和易用。4 个模块如下：

- 一个双通道 DAC
- 一个音效调节器
- 一个灵活的闭环功放
- 一个 I<sup>2</sup>C 控制和通信模块

芯片需要两个电源工作，一个是 DVDD，主要是给低功耗的数字电路供电。另外一个电源是功率电源 PVDD，主要是给功放提供功率电源。内部还会产生两个 LDO，一路是 PVDD 降压到 5V 给 VREG\_AVDD 供电，还有一路是降压到 1.8V 给 VREG\_DVDD 供电。

## 10.2 功能模块

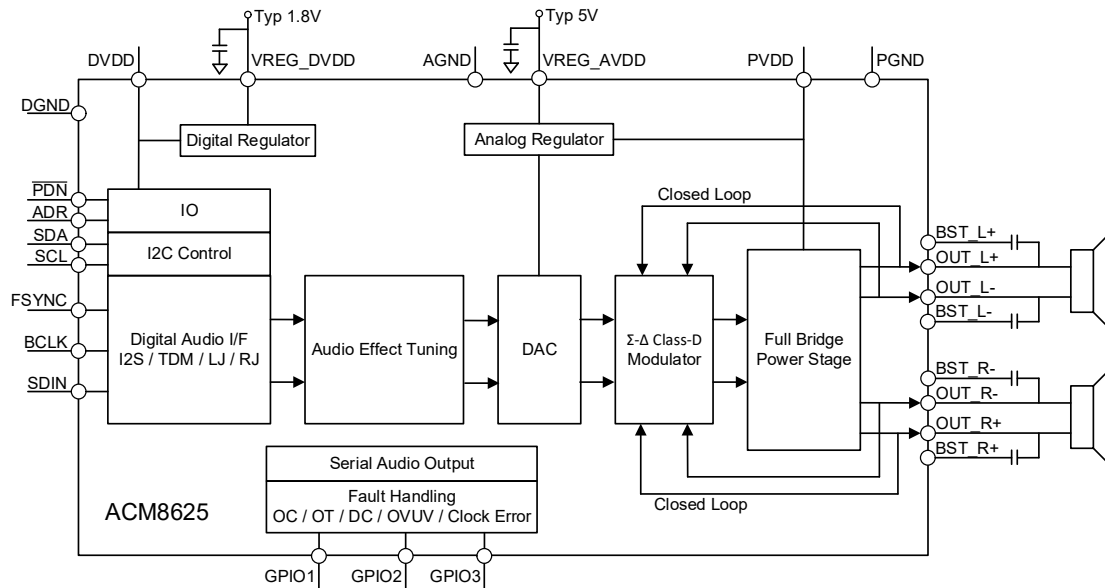


Figure 13 功能模块图

## 10.3 时钟

### 9.3.1 主时钟 Main Clocks

ACM8625M 的时钟系统比较丰富，且简单易用。

串行音频接口典型的有三个接口：

- BCLK
- FSYNC/LRCLK (Left/Right Word Clock and Frame Sync)
- SDIN (输入数据)

芯片内部的 PLL 采用 BCLK 作为参考时钟，根据内部数字音频处理和 DAC 的要求，会基于参考时钟产生更高频的时钟。ACM8625M 集成音频采样率的检测电路，能够自动获得采样率。支持音频信号采用率 32kHz, 44.1kHz-48kHz, 88.2kHz-96kHz, 176.4-192kHz 采样率的检测能够自动调整内部 SRC 满足内部音频信号处理和 DAC 的时钟要求。

### 9.3.2 串行音频端口 – 时钟频率

串行音频端口是三线端口，分别是 FSYNC/LRCLK, BCLK 和 SDIN. BCLK 是位时钟，是同步信号（也叫 SCK, SCL），用于把 SDIN 上的数据写入串行移位寄存器。ACM8625M 的数据写入是在 BCLK 的上升沿时写入的。FSYNC/LRCLK 是左右声道选择信号，或者在 TDM 模式时作为帧同步信号。

Table 1. 数据格式，位深和时钟频率

| 格式                     | 数据位         | MAXIMUM LRCLK/FS FREQUENCY (kHz) | BCLK RATE (Fs) |
|------------------------|-------------|----------------------------------|----------------|
| I <sup>2</sup> S/LJ/RJ | 32,24,20,16 | 32 to 192                        | 64,32          |
| TDM                    | 32,24,20,16 | 32                               | 128            |



|  |         |             |
|--|---------|-------------|
|  | 44.1/48 | 128,256,512 |
|  | 96      | 128,256     |
|  | 192     | 128         |

When clock halt, non-supported BCLK to FSYNC/LRCLK ratio is detected, the device reports clock error in Register 0x18 in Page0.

### 9.3.3 时钟停摆-自动恢复

当没有信号输入时，一些主处理器会停止 I<sup>2</sup>S 时钟。当时钟停止时，芯片会把所有输出通道（输出功率管）设置为高阻状态，并输出时钟错误报告，错误报告在寄存器 0x18。当时钟恢复，芯片会自动返回原来的状态，输出通道（输出功率管）重新打开。

### 9.3.4 采样率动态变化

ACM8625M 支持 FSYNC/LRCLK 动态更改。例如 FSYNC/LRCLK 从 32kHz 改为 48kHz 或者 96kHz 时，在变更新采样率之前，主程序需要把 FSYNC/LRCLK 停止 10ms 以上。

### 9.3.5 音频数据端口 -数据格式和位深

该芯片支持行业标准音频数据格式，包括标准 I<sup>2</sup>S,左对齐,右对齐和 TDM/DSP 数据. 数据格式的选择在 Page0 页的寄存器 0x07 里面. 如果 TDM/DSP 模式下 FSYNC/LRCLK 的高宽度小于 BCLK 的 8 个周期,则寄存器 Page0/0x07 D[5:4] 应设置为 01. 所有格式都必须是 2 进制的补码, MSB-first 音频数据, 32 位的音频数据都可以. 在 Table1 中列出了所有支持的数据格式, 字节长度和采样率. 在图 14 到图 18 列出了格式的细节要求. 字节长度可以通过寄存器 Page0/0x07 D[1:0]选择. 数据移位可以通过寄存器 Page0/0x08 选择.

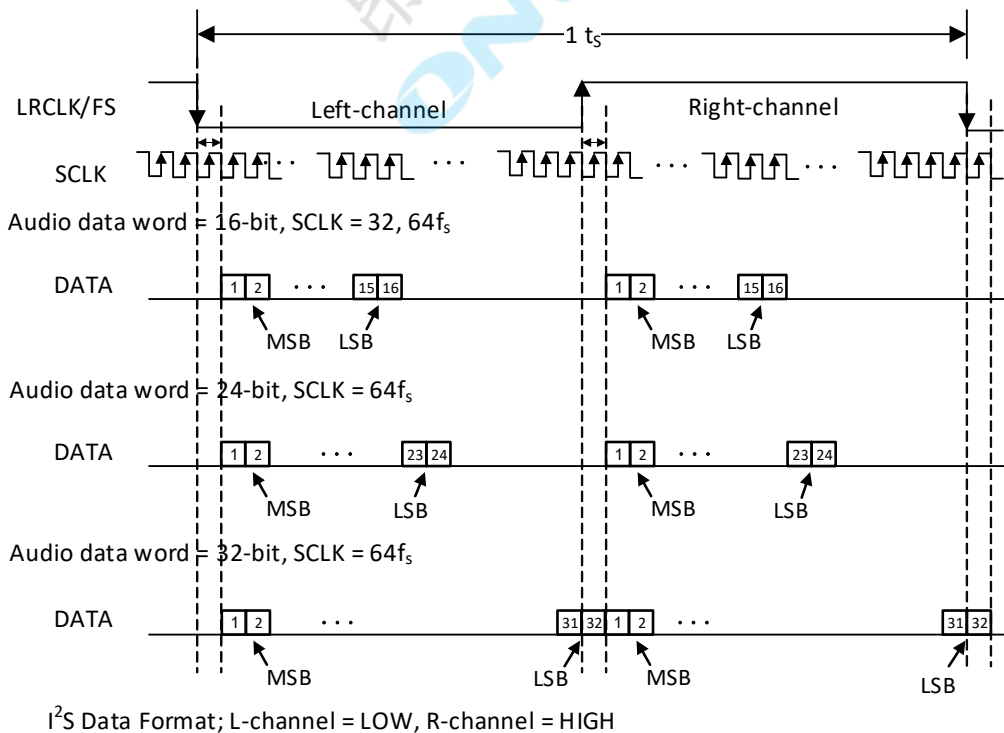


Figure 14 I<sup>2</sup>S Audio Data Format

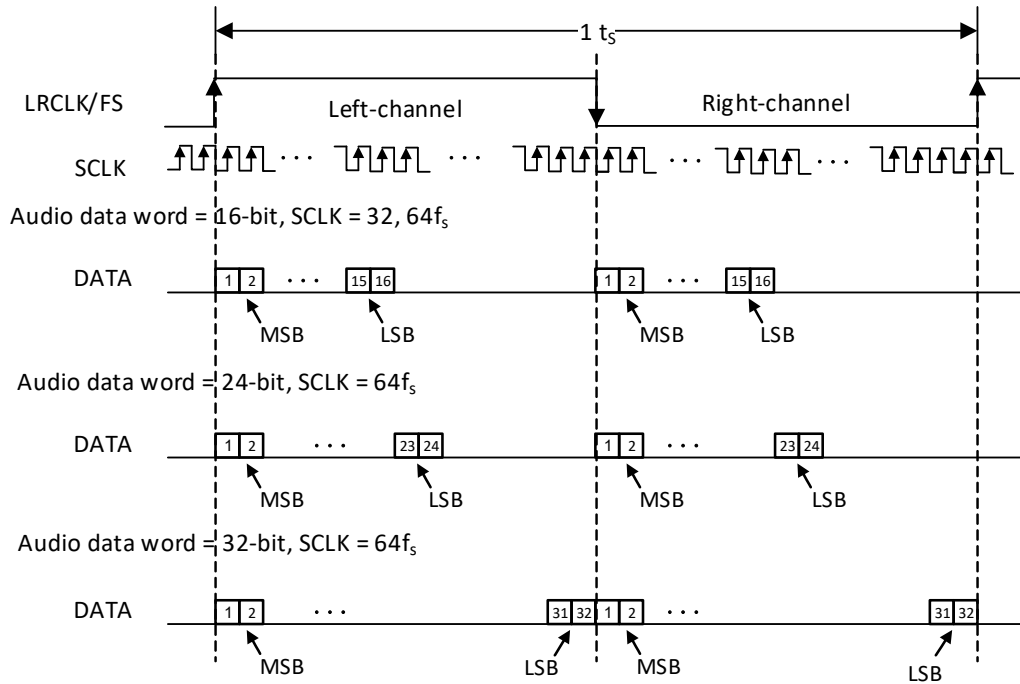


Figure 15 Left-Justified Audio Data Format

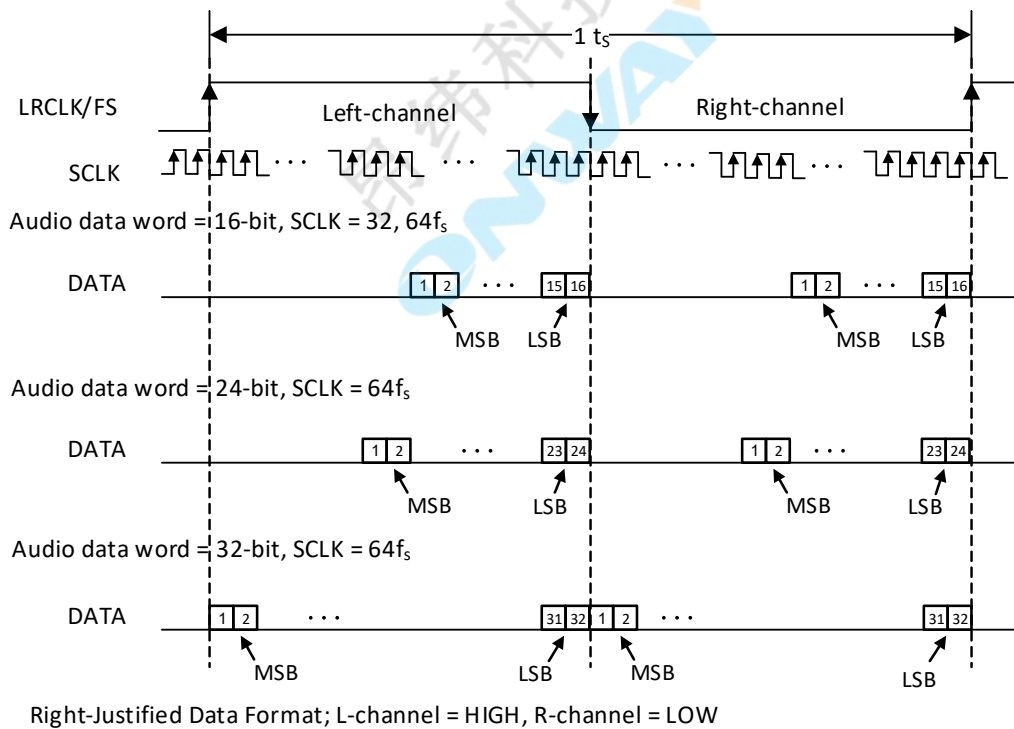
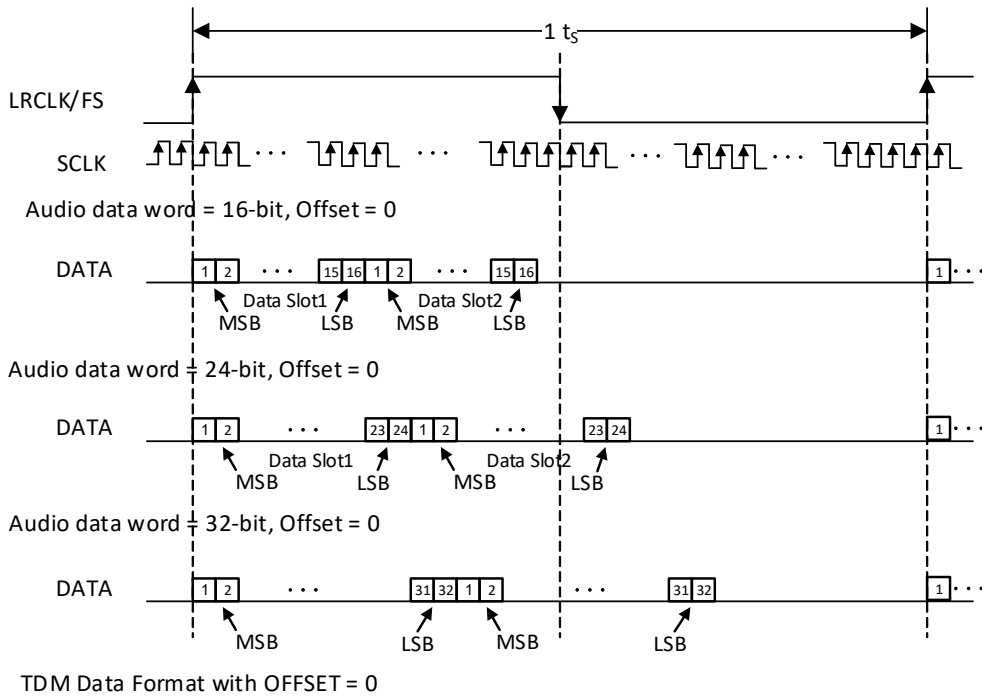
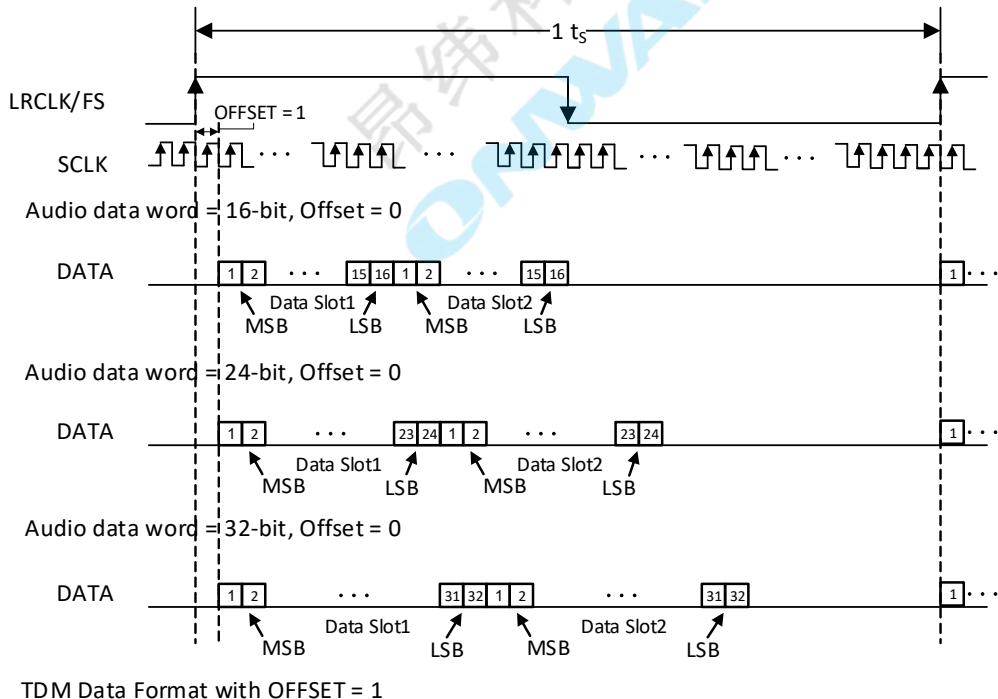


Figure 16 Right-Justified Audio Data Format



In TDM Modes, Duty Cycle of LRCLK/FS should be  $1 \times$  SCLK at minimum. Rising edge is considered frame start

Figure 17 TDM 1 Audio Data Format



In TDM Modes, Duty Cycle of LRCLK/FS should be  $1 \times$  SCLK at minimum. Rising edge is considered frame start

Figure 18 TDM 2 Audio Data Format

## 10.4 电源选择

为了系统设计方便，ACM8625M 除了功率电源 PVDD(4.5V~26.4V) 之外，还需要一个 3.3V 或 1.8V。芯片还有两

组内部的 LDO 给 gate drive 电路和内部电路供电，对应的外部管脚需要一组旁路电容。两组 LDO 不建议给其他器件使用，否则会降低内部 LDO 的性能影响输出音频质量。另外，需要浮动电源的，例如高栅极驱动器，都需要几个外部电容做自举电容用。为了良好的电气特性和声学特性，输出端的 PWM 信号采用完全相同但是相互独立的半桥模式。因此每个输出有单独的自举管脚(BST\_x)。特别需要注意的是，所有的去耦电容都要尽可能的靠近对应的管脚摆放。

## 10.5 增益设置

如下图所示，ACM8625M 的路径包括数字输入，数字路径，数字转 PWM，gate driver 驱动，功放级，还有从输出反馈环路。增益分成两个部分，一个是数字增益，一个是后端的模拟增益。

注意下表中的是模拟增益是 DAC 音量，而不是开发工具 GUI 上 DSP 中的音量。音量调整一般建议调整 GUI 上的数字音量。

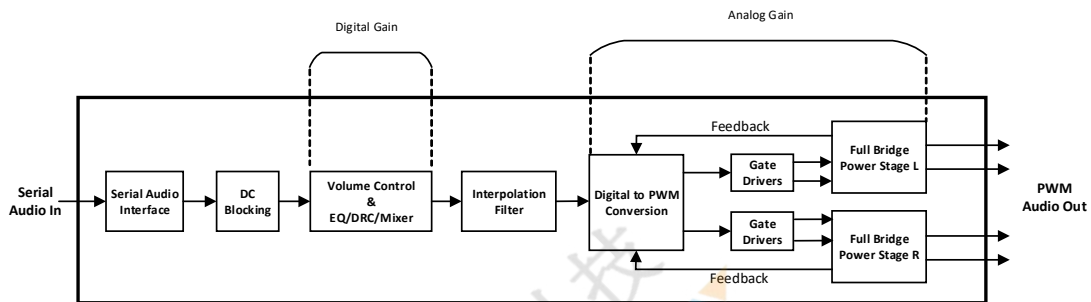


Figure 19 Gain Structure

数字增益部分包含音量控制器和 EQ/DRC/Mixer。音量控制器默认设置是 0dB，EQ/DRC/Mixer 默认是 bypass。功放的模拟增益设置是用输出幅度衡量 A 额 rms)。  $V_{AMP} = \text{Input} + \text{数字增益} + \text{模拟增益}$  dBV

其中:

- $V_{AMP}$  是功放的输出幅度，单位是 dBV<sub>RMS</sub>
- 输入是数字输入相对于 0dBFS 的振幅，单位是 dB
- 数字增益是数字音量控制设置，从 -110dB 到 24dB。
- 模拟增益设置从 26.38dB, 25.88dB, 25.38dB 到 10.88dB，每个 0.5dB 一个档位

Table 2 增益在 dBV<sub>RMS</sub> 和 V<sub>PEAK</sub>对应关系如下表

Table 2 Amplifier Gain Settings

| 模拟增益<br>(Register 0x02h in Page0) | 全幅输出               |                   |
|-----------------------------------|--------------------|-------------------|
|                                   | dBV <sub>RMS</sub> | V <sub>PEAK</sub> |
| 00000                             | 26.38              | 29.5              |
| 00001                             | 25.88              | 27.84             |
| 00010                             | 25.38              | 26.3              |
| 00011                             | 24.88              | 24.8              |
| ...                               | ...                | ...               |
| 01110                             | 19.38              | 13.17             |
| 01111                             | 18.88              | 12.44             |
| 10000                             | 18.38              | 11.74             |
| ...                               | ...                | ...               |
| 11111                             | 10.88              | 4.95              |

## 10.6 保护机制

ACM8625M 的保护机制有温度保护，短路保护，欠压保护，过压保护，直流输出保护，时钟错误侦测等保护电路。一旦发生错误，错误日志输出在寄存器 0x17h-0x19h(Page0)。这些错误通过正确设置寄存器 0x0Ah 和 0x0Ch(Page0)，把 GPIO0/1 脚拉到 DGND。通过改写寄存器 0x01h (Page0) 中的 bit7，从 0 改为 1，从而清空这些错误日志。

1. 过温保护。内部结温超过 160°C 时芯片就会关掉，当回落到 150°C 时才会恢复。温度浮动会有 10% 的误差范围。通过改写寄存器 0x11h 的 Bit2，从 0 到 1，使得过温保护自动恢复。
2. 短路保护。当输出端短路，或者输出端短路到 GND/PVDD 时，短路保护电路会启动电路保护。对于 24V 的正常应用，流经功率管电流应该不大于 6.5A。否则，短路保护电路将会把 FAULT 脚 (GPIO 脚) 拉到 DGND，关掉输出。
3. PVDD 过压保护。供电电压超过 28V，ACM8625M 就会关闭功放输出端。当回落到 27.5V 时，才会恢复正常工作。
4. PVDD 欠压保护。PVDD 低于 4V，芯片关闭输出，回升到 4.3V 时恢复正常工作。
5. 喇叭直流检测保护。输出检测到直流电压超过 1.9V 超过 570ms，芯片启动直流保护，关掉输出端。这种错误移除后，通过改写寄存器 0x01h 中的 Bit7，从 0 改到 1，清除错误。或者芯片保持输出阶段在高阻状态。
6. 时钟错误检测。检测到时钟停止，不支持 BCLK 到 FSYNC/LRCLK 被检测，芯片在寄存器 0x18 输出错误报告。错误移除时，器件恢复正常模式。

## 10.7 CLASS H 动态升压控制

ACM86XX 系列 H 类控制为电池供电系统提供了一种提高效率、降低功耗的新方案。ACM86xx 内部 H 类模块监控数字音频信号，并向外部 DC-DC Boost converter 反馈网络提供控制信号，相应地调整 Boost converter 的 VOUT。由于 ACM86xx 使用外部 Booster converter 的 VOUT 作为电源，所以 ACM86xx 的电源动态跟踪并输出音频信号，如图 29 所示。

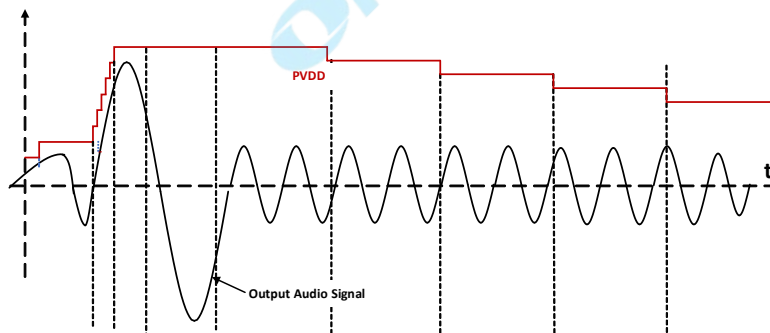
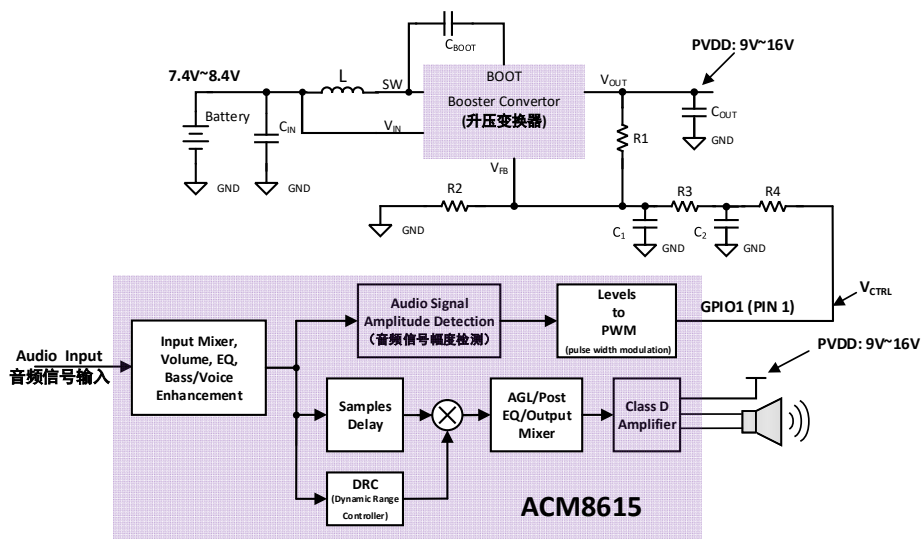


图 29 CLASS H 信号控制

ACM86xx 采用内部的音频信号幅值检测模块进行音频信号幅值检测。通常，ACM86xx 支持 16 级 H 类控制。例如，如果 PVDD 范围是 9V- 16v，PVDD 跟踪输出音频信号的值如下：{9V, 9.466V, 9.933V, 10.399V, 10.866V, 11.333V, 11.799V, 12.266V, 12.732V, 13.199V, 14.132V, 14.599V, 15.065V, 15.532V, 15.999V}。

ACME 音频调音软件根据详细的系统应用需求(PVDD min/max 值、升压转换器 VFB 值、PVDD 值、R2)生成相应的寄存器配置和外部 BOM，如图 30 所示。



$$\frac{V_{OUT}-V_{FB}}{R1} = \frac{V_{FB}}{R2} + \frac{V_{FB}-V_{CTRL}}{R3+R4}$$

图 30. CLASS H 控制模块图

## 10.8 扩频技术

ACM8625M 采用扩频技术降低 EMI 干扰。通过寄存器 0x0Eh 进行配置，默认是关闭的。虽然各种情形不能一概而论，但在功率和喇叭线长一定的情况下，可以用扩频技术节省电感（磁珠电容取代电感电容电路）。

ACM8628M 支持扩频技术，扩频技术能有效降低 EMI 噪音辐射。

打开扩频的寄存器是 0x0Eh，Page 0，默认是关闭的。

打开展频的顺序如下（适用于 384kHz/480kHz/576kHz 开关频率）：

1. Step1, Write content 0x00 to Register address 0x00.
2. Step2, Write content 0x01 to Register address 0x0E.
3. Step3, Write content 0x01 to Register address 0x00.
4. Step4, Write content 0x02 to Register address 0x1A.
5. Step5, Write content 0x00 to Register address 0x00.

## 10.9 I<sup>2</sup>C 设备地址

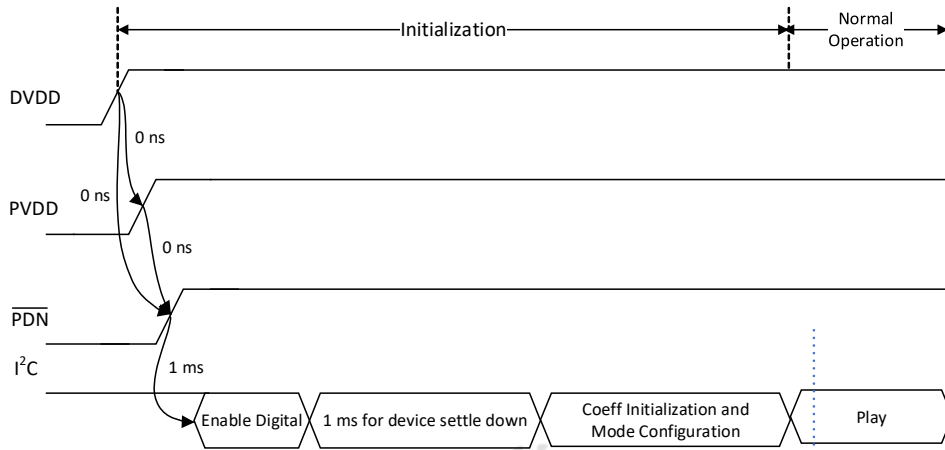
ACM8625M 的 I<sup>2</sup>C 地址有 7 个 bits。前 5 个 bits(MSBs)预设定为 01011 (0x5x)。后面两个 bits 是设备选择位，用户可以通过下表 3 中的 ADR 脚自定义。

Table 3 I<sup>2</sup>C 设备地址配置

| ADR PIN Configuration | MSBs |   |   |   |   | User Define |   | LSB | Device Write Address |
|-----------------------|------|---|---|---|---|-------------|---|-----|----------------------|
| 4.7kΩ to DVDD         | 0    | 1 | 0 | 1 | 1 | 0           | 0 | R/W | 0x58                 |
| 15kΩ to DVDD          | 0    | 1 | 0 | 1 | 1 | 0           | 1 | R/W | 0x5a                 |
| 47kΩ to DVDD          | 0    | 1 | 0 | 1 | 1 | 1           | 0 | R/W | 0x5c                 |
| 120k to DVDD          | 0    | 1 | 0 | 1 | 1 | 1           | 1 | R/W | 0x5e                 |

## 启动序列

1. 配置 ADR/GPIO2 脚, 给 I<sup>2</sup>C 配置正确的器件地址。
2. 提供电源 (I<sup>2</sup>C 通信需要电源 DVDD).
3. 所有电源 (PVDD 和 DVDD) 稳定后, 把 PDN 脚拉高。
4. 根据用户需求通过 I<sup>2</sup>C 控制口配置地址, 配置前确保 PDN 脚已经拉高。
5. 芯片进入正常操作模式。



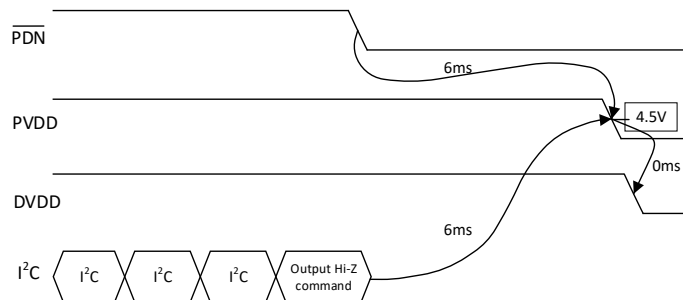
Notes:

- 1) 0ns means no sequence requirement
- 2) I<sup>2</sup>C communication and internal Digital processing work in DVDD domain, no PVDD required

Figure 20 启动时序

## 10.10 关机时序

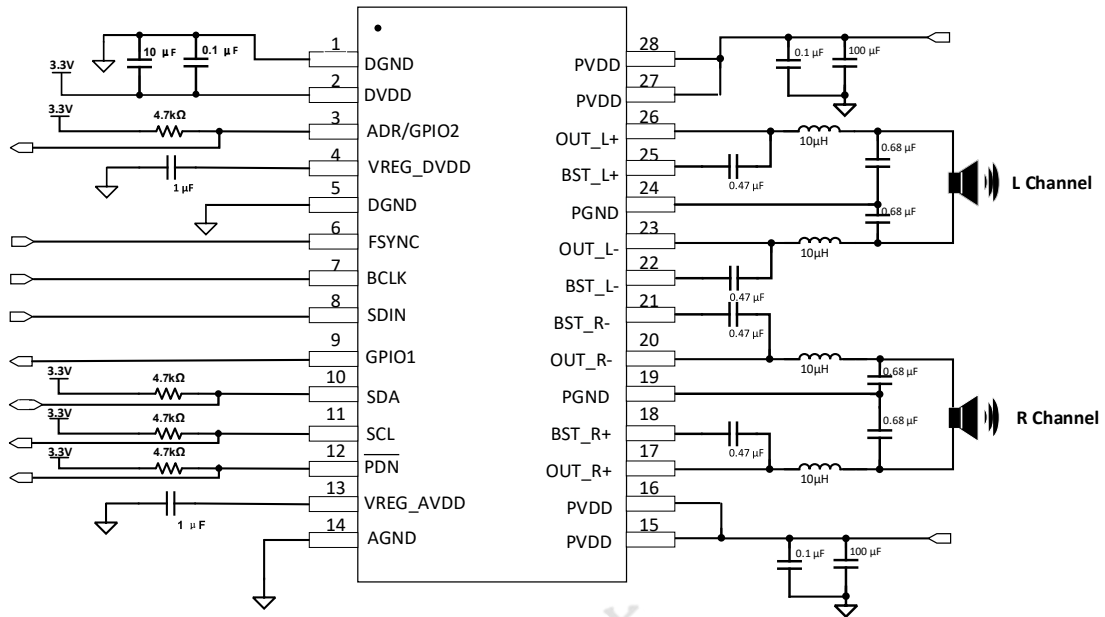
1. 从正常模式开始。
2. 通过修改寄存器 0x04h 或者拉低 PDN 脚让芯片进入数字关机状态。
3. 等待至少 6ms (时间取决于 FSYNC 频率, 数字音量和下降沿时间)。
4. 关闭电源。
5. 芯片进入完全关机状态。



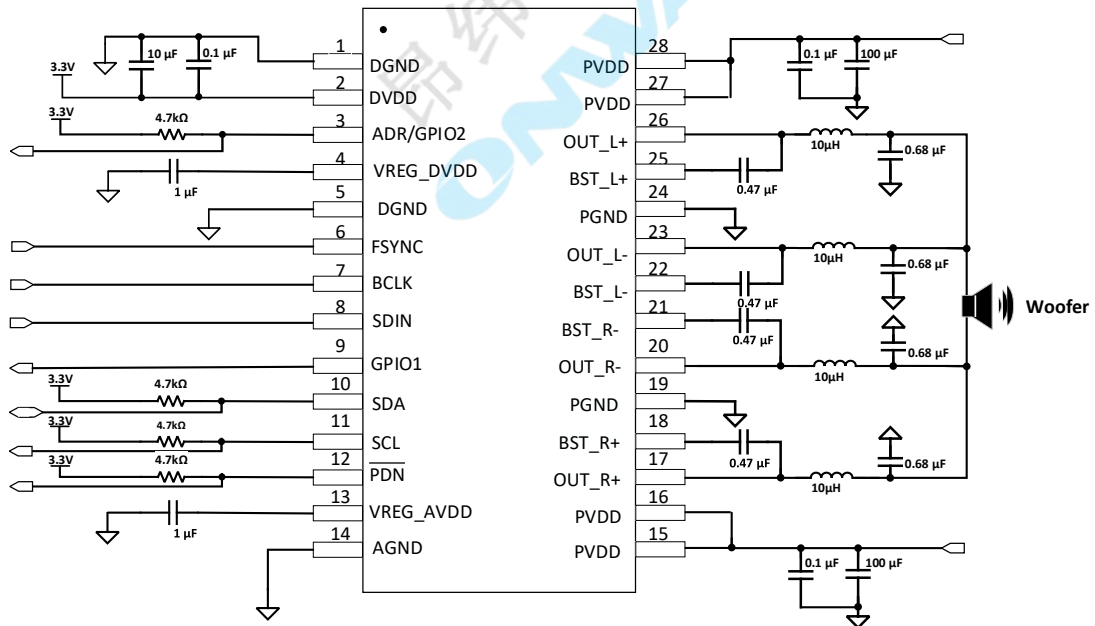
- Before PVDD/DVDD power down, Class D Output driver needs to be disabled by  $\overline{\text{PDN}}$  or by I<sup>2</sup>C.
- At least 6ms delay needed based on LRCLK (Fs) = 48kHz, Digital volume ramp down update every sample period, decreased by 0.5dB for each update, digital volume = 24dB.

Figure 21 关机时序

### 11. 立体声典型应用图



### 12. PBTl 单通道典型应用





## 13. 寄存器查询

### 13.1 Control Registers on Page0

| Offset | Acronym             | Register Name  | Reset Value |
|--------|---------------------|--|-------------|
| 0x01   | AMP_CTRL1           | F <sub>sw</sub> PWM switching frequency, Fault clear, PBTL/BTL | 0x00        |
| 0x02   | AMP_CTRL2           | Analog gain  | 0x00        |
| 0x03   | AMP_CTRL3           | Loop bandwidth, 2 PWM channels phase control                   | 0x00        |
| 0x04   | STATE_CTRL          | Reset, Separate channel Hi-Z / Mute, State Control             | 0x00        |
| 0x05   | PROCESSING_CTRL1    | AGL, DRB, Hybrid, Post EQ, Sub-CH bypass control               | 0x12        |
| 0x06   | PROCESSING_CTRL2    | Processing flow selection and low power mode selection         | 0xF0        |
| 0x07   | I2S_DATA_FORMAT1    | I2S data format, length, FSYNC                                 | 0x02        |
| 0x08   | I2S_DATA_FORMAT2    | I2S Shift bits   | 0x00        |
| 0x09   | I2S_DATA_FORMAT3    | Reserved   | 0x05        |
| 0x0A   | GPIO2_CTRL          | SDOUT (GPIO2) enable and function selection                    | 0x29        |
| 0x0B   | GPIO1_CTRL          | ADR (GPIO1) enable and function selection                      | 0x2B        |
| 0x0C   | GPIO1_FAULT_SEL     | Clipping, OTW, OTSD, Clock Fault, PVDD UV/OV, DC, OC selection | 0xFF        |
| 0x0D   | GPIO2_FAULT_SEL     | Clipping, OTW, OTSD, Clock Fault, PVDD UV/OV, DC, OC selection | 0xFF        |
| 0x0E   | SS_CTRL             | Spread spectrum setting  | 0x00        |
| 0x0F   | VOLUME_CTRL_L       | Volume control for left channel                                | 0xD0        |
| 0x10   | VOLUME_CTRL_R       | Volume control for right channel                               | 0xD0        |
| 0x11   | MSIC_CTRL           | Fault latch selection, OTSD auto-recovery enable               | 0x03        |
| 0x12   | I2S_CLK_FORMAT_RPT1 | BCLK ratio (MSB), Sample rate detect                           | 0x00        |
| 0x13   | I2S_CLK_FORMAT_RPT2 | BCLK ratio (LSB)   | 0x00        |
| 0x15   | DIEID_RPT           | DIE ID   | 0x00        |
| 0x16   | STATE_RPT           | State report   | 0x00        |
| 0x17   | FAULT_RPT1          | OTSD, PVDD OV/UV, DC, OC                                       | 0x00        |
| 0x18   | FAULT_RPT2          | Clock fault, EQs write error                                   | 0x00        |
| 0x19   | FAULT_RPT3          | Clipping, OTW  | 0x00        |
| 0x7E   | XOR_CHECKSUM        | XOR Checksum   | 0x00        |
| 0x7F   | CRC_CHECKSUM        | CRC Checksum   | 0x00        |

#### 12.1.1 Register 1 AMP\_CTRL1 (Offset=1h) [Reset=0x00]

| 7         | 6        | 5 | 4 | 3       | 2 | 1 | 0    |
|-----------|----------|---|---|---------|---|---|------|
| FAULT_CLR | RESERVED |   |   | FSW_SWL |   |   | PBTL |
| R/W       | R        |   |   | R/W     |   |   | R/W  |

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 7   | FAULT_CLR | R/W  | 0     | Once write this bit to 1, device will clear analog fault, this bit is auto-clear |
| 6-4 | RESERVED  | R    | 000   | These bits are reserved  |
| 3-1 | FSW_SEL   | R/W  | 000   | 000: 384kHz<br>001: 260kHz<br>010: 480kHz<br>011: 576kHz<br>100: 768kHz          |
| 0   | PBTL      | R/W  | 0     | 0: BTL Mode<br>1: PBTL Mode, PBTL can be set when device is in digital off state |

## 12.1.2 Register 2 AMP\_CTRL2 (Offset=2h) [Reset=0x00]

| 7        | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
|----------|---|---|---|----------|---|---|---|
| RESERVED |   |   |   | ANA_GAIN |   |   |   |
| R        |   |   |   | R/W      |   |   |   |

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 7-5 | RESERVED | R    | 000   | These bits are reserved  |
| 4-0 | ANA_GAIN | R/W  | 00000 | Analog Gain Control, with 0.5dB per step. These bits control the analog gain.<br>00000: 0dB (29.5Vp/FS)<br>00001: -0.5dB<br>00010: -1dB<br>...<br>11111: -15.5dB |

## 12.1.3 Register 3 AMP\_CTRL3 (Offset=3h) [Reset=0x00]

| 7        | 6 | 5            | 4        | 3 | 2       | 1 | 0 |
|----------|---|--------------|----------|---|---------|---|---|
| RESERVED |   | CH_PHASE_CTL | RESERVED |   | BW_CTRL |   |   |
| R        |   | R/W          | R        |   | R/W     |   |   |

| Bit | Field         | Type | Reset | Description                 |
|-----|---------------|------|-------|-----------------------------|
| 7-6 | RESERVED      | R    | 00    | These bits are reserved     |
| 5   | CH_PHASE_CTRL | R/W  | 0     | 0: out phase<br>1: in phase |
| 2-0 | BW_CTRL       | R/W  | 000   | 000: 75kHz                  |

## ACM8625M

|  |  |  |  |  |
|--|--|--|--|--|
|  |  |  |  | 001: 90kHz<br>010: 105kHz<br>011: 125kHz<br>100: 155kHz<br>101: 180kHz<br>110: 220kHz<br>111: 265kHz |
|--|--|--|--|--|

### 12.1.4 Register 4 STATE\_CTRL (Offset=4h) [Reset=0x00]

| 7       | 6        | 5        | 4        | 3      | 2      | 1          | 0 |
|---------|----------|----------|----------|--------|--------|------------|---|
| RST_REG | REST_MOD | CH_L_HIZ | CH_R_HIZ | MUTE_L | MUTE_R | CTRL_STATE |   |
| R/W     | R/W      | R/W      | R/W      | R/W    | R/W    | R/W        |   |

| Bit | Field      | Type | Reset | Description   |
|-----|------------|------|-------|---|
| 7   | RST_REG    | R/W  | 0     | Register Reset<br>0: Normal<br>1: Reset Register  |
| 6   | RST_MOD    | R/W  | 0     | Signal path Reset<br>0: Normal<br>1: Reset Signal path  |
| 5   | CH_L_HIZ   | R/W  | 0     | Force Channel L' s output driver into Hi-Z state<br>0: Normal State<br>1: Change L channel' s output driver into Hi-Z state |
| 4   | CH_R_HIZ   | R/W  | 0     | Force Channel R' s output driver into Hi-Z state<br>0: Normal State<br>1: Change R channel' s output driver into Hi-Z state |
| 3   | MUTE_L     | R/W  | 0     | MUTE L Channel<br>0: Normal<br>1: Mute L Channel  |
| 2   | MUTE_R     | R/W  | 0     | MUTE R Channel<br>0: Normal<br>1: Mute R Channel  |
| 1-0 | CTRL_STATE | R/W  | 00    | 00: Digital Off<br>01: Analog off<br>10: Driver Off (Hiz)<br>11: Play   |

### 12.1.5 Register 5 PROCESSING\_CTRL1 (Offset=5h) [Reset=0x12]

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|---|---|---|---|---|---|---|---|

## ACM8625M

|        |        |          |            |          |           |               |
|--------|--------|----------|------------|----------|-----------|---------------|
| AGL_BP | DRB_BP | RESERVED | POST_EQ_BP | RESERVED | SUB_CH_BP | PROCESSING_BP |
| R/W    | R/W    | R        | R/W        | R        | R/W       | R/W           |

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7   | AGL_BP        | R/W  | 0     | 0: Enable AGL<br>1: Bypass AGL                                       |
| 6   | DRB_BP        | R/W  | 0     | 0: Enable DRB<br>1: Bypass DRB                                       |
| 5-4 | RESERVED      | R    | 0     | This bit is reserved   |
| 3   | POST_EQ_BP    | R/W  | 0     | 0: Enable Post-EQ<br>1: Bypass Post-EQ                               |
| 2   | RESERVED      | R    | 0     | This bit is reserved   |
| 1   | SUB_CH_BP     | R/W  | 1     | 0: Enable Sub Channel Processing<br>1: Bypass Sub Channel Processing |
| 0   | PROCESSING_BP | R/W  | 0     | 0: Enable audio effect tuning<br>1: Bypass all audio effect tuning   |

### 12.1.6 Register 6 PROCESSING\_CTRL2 (Offset=6h) [Reset=0xF0]

|          |   |   |                 |             |   |            |   |
|----------|---|---|-----------------|-------------|---|------------|---|
| 7        | 6 | 5 | 4               | 3           | 2 | 1          | 0 |
| RESERVED |   |   | POWER_SAVE_DOWN | PLL_CLK_DIV |   | REAL_96KHZ |   |
| R        |   |   | R/W             | R/W         |   | R/W        |   |

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7-4 | RESERVED        | R    | 1111  | These bits are reserved  |
| 3   | POWER_SAVE_DOWN | R/W  | 0     | 0: when have clock fault, device will not shut down analog and digital, only shut down driver<br>1: when have clock fault, device will shut down analog and digital and driver |
| 2-1 | PLL_CLK_DIV     | R/W  | 0     | 00: high PLL frequency<br>01: middle PLL frequency<br>10: low PLL frequency<br>11: low PLL frequency   |
| 0   | REAL_96KHZ      | R/W  | 0     | 0: 48kHz internal processing<br>1: 96kHz internal processing   |

### 12.1.7 Register 7 I2S\_DATA\_FORMAT1 (Offset=7h) [Reset=0x02]

|           |        |                  |   |                 |   |                 |   |
|-----------|--------|------------------|---|-----------------|---|-----------------|---|
| 7         | 6      | 5                | 4 | 3               | 2 | 1               | 0 |
| 44K_INPUT | 44K_EN | I2S_DATA_FORMAT1 |   | I2S_FSYNC_PULSE |   | I2S_WORD_LENGTH |   |
| R/W       | R/W    | R/W              |   | R/W             |   | R/W             |   |

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7   | 44K_INPUT       | R/W  | 0     | 0: 48K/96K/192K input<br>1: 44.1K/88.2K/176.4K input   |
| 6   | 44K_EN          | R/W  | 0     | 0: disable 44k input<br>1: enable 44k input  |
| 5-4 | I2S_DATA_FORMAT | R/W  | 00    | 00: I2S<br>01: TDM/DSP<br>10: RTJ<br>11: LTJ   |
| 3-2 | I2S_FSYNC_PULSE | R/W  | 00    | 01: FSYNC pulse <8 BCLK. If the high width of LRCLK/FSYNC in TDM/DSP mode is less than 8 cycles of BCLK, these two bits need set to 01.<br>Others: These bits are reserved   |
| 1-0 | I2S_WORD_LENGTH | R/W  | 10    | I2S Word length. These bits control both input and output audio interface sample word lengths for DAC operation.<br>00: 16 bits<br>01: 20 bits<br>10: 24 bits<br>11: 32 bits |

## 12.1.8 Register 8 I2S\_DATA\_FORMAT2 (Offset=8h) [Reset=0x00]

| 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|---|---|---|---|---|---|---|
| I2S_LEFT_BITS_SHIFT |   |   |   |   |   |   |   |
| R/W                 |   |   |   |   |   |   |   |

| Bit | Field              | Type | Reset    | Description   |
|-----|--------------------|------|----------|---|
| 7-0 | I2S_LEFT_BIT_SHIFT | R/W  | 00000000 | Control the offset of Left Channel audio data in the audio frame for both input and output. The offset is defined as the number of BCLK from the starting (MSB) of audio frame to the starting of the desired audio sample.<br>00000000: offset = 0 BCLK (no offset)<br>00000001: offset = 1 BCLK<br>.....<br>11111111: offset = 256 BCLK |

**12.1.9 Register 9 I2S\_DATA\_FORMAT3 (Offset=9h) [Reset=0x00]**

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

RESERVED

R

| Bit | Field    | Type | Reset    | Description              |
|-----|----------|------|----------|--------------------------|
| 7-0 | RESERVED | R    | 00000000 | These bits are reserved. |

昂纬科技  
ONWAY

## 12.1.10 Register 10 GPIO1\_CTRL (Offset=0Ah) [Reset=0x29]

| 7        | 6 | 5        | 4              | 3 | 2 | 1 | 0 |
|----------|---|----------|----------------|---|---|---|---|
| RESERVED |   | GPIO1_OE | GPIO1_FUNC_SEL |   |   |   |   |
| R        |   | R/W      | R/W            |   |   |   |   |

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 7-6 | RESERVED       | R    | 00    | These bits are reserved  |
| 5   | GPIO1_OE       | R/W  | 1     | 0: GPIO1 is input<br>1: GPIO1 is output  |
| 4-0 | GPIO1_FUNC_SEL | R/W  | 01001 | DEFAULT is SDOOUT<br>0000: off(low)<br>0001: digital off<br>0010: analog off<br>0011: driver off<br>0100: mute right<br>0101: mute left<br>0110: clock invalid flag (clock error or clock missing)<br>0111: pll lock flag<br>1000: GPIO1 as WARNZ output<br>1001: serial audio interface data output (SDOUT)<br>1011: GPIO1 as FAULTZ output<br>1100: resetz |

## 12.1.11 Register 11 GPIO2\_CTRL (Offset=0Bh) [Reset=0x2B]

| 7        | 6 | 5        | 4              | 3 | 2 | 1 | 0 |
|----------|---|----------|----------------|---|---|---|---|
| RESERVED |   | GPIO2_OE | GPIO1_FUNC_SEL |   |   |   |   |
| R        |   | R/W      | R/W            |   |   |   |   |

| Bit | Field          | Type | Reset | Description   |
|-----|----------------|------|-------|---|
| 7-6 | RESERVED       | R    | 00    | These bits are reserved   |
| 5   | GPIO2_OE       | R/W  | 1     | 0: GPIO2 is input<br>1: GPIO2 is output   |
| 4-0 | GPIO2_FUNC_SEL | R/W  | 01011 | DEFAULT is FAULT pin<br>0000: off(low)<br>0001: digital off<br>0010: analog off<br>0011: driver off<br>0100: mute right<br>0101: mute left<br>0110: clock invalid flag (clock error or clock missing) |

## ACM8625M

| Bit | Field | Type | Reset | Description  |
|-----|-------|------|-------|--|
|     |       |      |       | 0111: pll lock flag<br>1000: gpio1 as WARNZ output<br>1001: serial audio interface data output (SDOUT)<br>1011: GPIO2 as FAULTZ output<br>1100: resetz |

### 12.1.12 Register 12 GPIO1\_FAULT\_SEL (Offset=0Ch) [Reset=0xFF]

| 7    | 6   | 5    | 4         | 3       | 2       | 1   | 0   |
|------|-----|------|-----------|---------|---------|-----|-----|
| CLIP | OTW | OTSD | CLK_FAULT | PVDD_UV | PVDD_OV | DC  | OC  |
| R/W  | R/W | R/W  | R/W       | R/W     | R/W     | R/W | R/W |

| Bit | Field     | Type | Reset | Description        |
|-----|-----------|------|-------|--------------------|
| 7   | CLIP      | R/W  | 1     | 0: Mask; 1: Report |
| 6   | OTW       | R/W  | 1     | 0: Mask; 1: Report |
| 5   | OTSD      | R/W  | 1     | 0: Mask; 1: Report |
| 4   | CLK_FAULT | R/W  | 1     | 0: Mask; 1: Report |
| 3   | PVDD_UV   | R/W  | 1     | 0: Mask; 1: Report |
| 2   | PVDD_OV   | R/W  | 1     | 0: Mask; 1: Report |
| 1   | DC        | R/W  | 1     | 0: Mask; 1: Report |
| 0   | OC        | R/W  | 1     | 0: Mask; 1: Report |

### 12.1.13 Register 13 GPIO2\_FAULT\_SEL (Offset=0Dh) [Reset=0xFF]

| 7    | 6   | 5    | 4         | 3       | 2       | 1   | 0   |
|------|-----|------|-----------|---------|---------|-----|-----|
| CLIP | OTW | OTSD | CLK_FAULT | PVDD_UV | PVDD_OV | DC  | OC  |
| R/W  | R/W | R/W  | R/W       | R/W     | R/W     | R/W | R/W |

| Bit | Field     | Type | Reset | Description        |
|-----|-----------|------|-------|--------------------|
| 7   | CLIP      | R/W  | 1     | 0: Mask; 1: Report |
| 6   | OTW       | R/W  | 1     | 0: Mask; 1: Report |
| 5   | OTSD      | R/W  | 1     | 0: Mask; 1: Report |
| 4   | CLK_FAULT | R/W  | 1     | 0: Mask; 1: Report |
| 3   | PVDD_UV   | R/W  | 1     | 0: Mask; 1: Report |
| 2   | PVDD_OV   | R/W  | 1     | 0: Mask; 1: Report |
| 1   | DC        | R/W  | 1     | 0: Mask; 1: Report |
| 0   | OC        | R/W  | 1     | 0: Mask; 1: Report |



## 12.1.14 Register 14 SS\_CTRL (Offset=0Eh) [Reset=0x00]

|          |   |   |   |   |   |        |        |
|----------|---|---|---|---|---|--------|--------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1      | 0      |
| RESERVED |   |   |   |   |   | RDM_EN | TRI_EN |
| R        |   |   |   |   |   | R/W    | R/W    |

| Bit | Field    | Type | Reset | Description                                     |
|-----|----------|------|-------|---|
| 7-2 | RESERVED | R    | 00000 | These bits are reserved                         |
| 1   | RDM_EN   | R/W  | 0     | 0: Random SS disable<br>1: Random SS enable     |
| 0   | TRI_EN   | R/W  | 0     | 0: Triangle SS disable<br>1: Triangle SS enable |

## 12.1.15 Register 15 VOLUME\_CTRL\_L (Offset=0Fh) [Reset=0xD0]

|       |   |   |   |   |   |   |   |
|-------|---|---|---|---|---|---|---|
| 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOL_L |   |   |   |   |   |   |   |
| R/W   |   |   |   |   |   |   |   |

| Bit | Field | Type | Reset    | Description  |
|-----|-------|------|----------|--|
| 7-0 | VOL_L | R/W  | 11010000 | Volume control for left channel.<br>00000000: -104dB<br>....<br>11010000: 0dB<br>11010001: 0.5dB<br>....<br>11111111: 24dB |

## 12.1.16 Register 16 VOLUME\_CTRL\_R (Offset=10h) [Reset=0xD0]

|       |   |   |   |   |   |   |   |
|-------|---|---|---|---|---|---|---|
| 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOL_R |   |   |   |   |   |   |   |
| R/W   |   |   |   |   |   |   |   |

| Bit | Field | Type | Reset    | Description  |
|-----|-------|------|----------|--|
| 7-0 | VOL_R | R/W  | 11010000 | Volume control for left channel.<br>00000000: -104dB<br>....<br>11010000: 0dB<br>11010001: 0.5dB<br>.... |

## ACM8625M

| Bit | Field | Type | Reset | Description    |
|-----|-------|------|-------|----------------|
|     |       |      |       | 11111111: 24dB |

昂纬科技  
ONWAY

## 12.1.17 Register 17 MISC\_CTRL (Offset=11h) [Reset=0x03]

| 7        | 6 | 5 | 4 | 3 | 2             | 1                 | 0                 |
|----------|---|---|---|---|---------------|-------------------|-------------------|
| RESERVED |   |   |   |   | OTSD_AUTO_REC | GPIO2_FAULT_LATCH | GPIO1_FAULT_LATCH |
| R        |   |   |   |   | R/W           | R/W               | R/W               |

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 7-3 | RESERVED          | R    | 0000  |  |
| 2   | OTSD_AUTO_REC     | R/W  | 0     | 0: OT auto-recovery disable<br>1: OT auto-recovery enable          |
| 1   | GPIO2_FAULT_LATCH | R/W  | 1     | 0: GPIO2 report fault not latched<br>1: GPIO2 report fault latched |
| 0   | GPIO1_FAULT_LATCH | R/W  | 1     | 0: GPIO1 report fault not latched<br>1: GPIO1 report fault latched |

## 12.1.18 Register 18 I2S\_CLK\_FORMAT\_RPT1 (Offset=12h)

[Reset=0x00]

| 7        | 6 | 5               | 4 | 3      | 2 | 1 | 0 |
|----------|---|-----------------|---|--------|---|---|---|
| RESERVED |   | BCLK_RATIO_HIGH |   | FS_DET |   |   |   |
| R        |   | R               |   | R      |   |   |   |

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7-6 | RESERVED        | R    | 00    | These bits are reserved  |
| 5-4 | BCLK_RATIO_HIGH | R    | 00    | These bits indicate the BCLK ratio, the number of BCLK in one audio frame. BCLK=32FS-512FS MSB Bit [9-8].  |
| 3-0 | FS_DET          | R    | 0000  | These bits indicate the currently detected audio sample rate.<br>0110: 32KHZ<br>1000: 44.1KHZ<br>1001: 48KHZ<br>1010: 88.2KHZ<br>1011: 96KHZ<br>1100: 176.4KHZ<br>1101: 192KHZ |

**12.1.19 Register 19 I2S\_CLK\_FORMAT\_RPT2 (Offset=13h)**

**[Reset=0x00]**

|            |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BCLK_RATIO |   |   |   |   |   |   |   |
| R          |   |   |   |   |   |   |   |

| Bit | Field      | Type | Reset    | Description  |
|-----|------------|------|----------|--|
| 7-0 | BCLK_RATIO | R    | 00000000 | These bits indicate the BCLK ratio, the number of BCLK in one audio frame.<br>00000000:<br>00000001:<br>...<br>11111111: |

**12.1.20 Register 20 DIEID\_RPT (Offset=15h) [Reset=0x00]**

|           |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIEID_RPT |   |   |   |   |   |   |   |
| R         |   |   |   |   |   |   |   |

| Bit | Field  | Type | Reset    | Description |
|-----|--------|------|----------|-------------|
| 7-0 | DIE_ID | R    | 00000000 | DIE ID      |

**12.1.21 Register 21 STATE\_RPT (Offset=16h) [Reset=0x00]**

|          |   |   |   |   |   |           |   |
|----------|---|---|---|---|---|-----------|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1         | 0 |
| RESERVED |   |   |   |   |   | STATE_RPT |   |
| R        |   |   |   |   |   | R         |   |

| Bit | Field     | Type | Reset  | Description   |
|-----|-----------|------|--------|---|
| 7-2 | RESERVED  | R    | 000000 | These bits are reserved   |
| 1-0 | STATE_RPT | R    | 00     | 00: Digital Off<br>01: Analog Off<br>10: Driver Off (Hiz)<br>11: Play |

## 12.1.22 Register 22 FAULT\_RPT1(Offset=17h) [Reset=0x00]

| 7        | 6    | 5       | 4       | 3      | 2      | 1      | 0      |
|----------|------|---------|---------|--------|--------|--------|--------|
| RESERVED | OTSD | PVDD_OV | PVDD_UV | CH2_DC | CH1_DC | CH2_OC | CH1_OC |
| R        | R    | R       | R       | R      | R      | R      | R      |

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 7   | RESERVED | R    | 0     | This bit is reserved                                   |
| 6   | OTSD     | R    | 0     | 0: Normal<br>1: Over temperature shutdown fault report |
| 5   | PVDD_OV  | R    | 0     | 0: Normal<br>1: PVDD over-voltage fault report         |
| 4   | PVDD_UV  | R    | 0     | 0: Normal<br>1: PVDD under-voltage fault report        |
| 3   | CH2_DC   | R    | 0     | 0: Normal<br>1: CH2 speaker DC fault report            |
| 2   | CH1_DC   | R    | 0     | 0: Normal<br>1: CH1 speaker DC fault report            |
| 1   | CH2_OC   | R    | 0     | 0: Normal<br>1: CH2 over-current fault report          |
| 0   | CH1_OC   | R    | 0     | 0: Normal<br>1: CH1 over-current fault report          |

## 12.1.23 Register 23 FAULT\_RPT2(Offset=18h) [Reset=0x00]

| 7        | 6 | 5 | 4 | 3 | 2         | 1        | 0 |
|----------|---|---|---|---|-----------|----------|---|
| RESERVED |   |   |   |   | CLK_FAULT | RESERVED |   |
| R        |   |   |   |   | R         | R        |   |

| Bit | Field     | Type | Reset | Description                        |
|-----|-----------|------|-------|------------------------------------|
| 7-3 | RESERVED  | R    | 00000 | This bit is reserved               |
| 2   | CLK_FAULT | R    | 0     | 0: Normal<br>1: Clock fault report |
| 1-0 | RESERVED  | R    | 0     | This bit is reserved               |

## 12.1.24 Register 24 FAULT\_RPT3(Offset=19h) [Reset=0x00]

|          |   |   |   |   |          |          |     |
|----------|---|---|---|---|----------|----------|-----|
| 7        | 6 | 5 | 4 | 3 | 2        | 1        | 0   |
| RESERVED |   |   |   |   | CH2_CLIP | CH1_CLIP | OTW |
| R        |   |   |   |   | R        | R        | R   |

| Bit | Field    | Type | Reset | Description                              |
|-----|----------|------|-------|--|
| 7-3 | RESERVED | R    | 00000 | This bit is reserved                     |
| 2   | CH2_CLIP | R    | 0     | 0: Normal<br>1: Channel 2 clipping       |
| 1   | CH1_CLIP | R    | 0     | 0: Normal<br>1: Channel 1 clipping       |
| 0   | OTW      | R    | 0     | 0: Normal<br>1: Over temperature warning |

## 12.1.25 Register 25 XOR\_CHECKSUM(Offset=7Eh) [Reset=0x00]

|              |   |   |   |   |   |   |   |
|--------------|---|---|---|---|---|---|---|
| 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XOR_CHECKSUM |   |   |   |   |   |   |   |
| R            |   |   |   |   |   |   |   |

| Bit | Field        | Type | Reset | Description         |
|-----|--------------|------|-------|---------------------|
| 7-0 | XOR_CHECKSUM | R    | 0     | XOR checksum result |

## 12.1.26 Register 26 CRC\_CHECKSUM(Offset=7Fh) [Reset=0x00]

|              |   |   |   |   |   |   |   |
|--------------|---|---|---|---|---|---|---|
| 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC_CHECKSUM |   |   |   |   |   |   |   |
| R            |   |   |   |   |   |   |   |

| Bit | Field        | Type | Reset | Description         |
|-----|--------------|------|-------|---------------------|
| 7-0 | CRC_CHECKSUM | R    | 0     | CRC checksum result |

14. 封装尺寸

