ACM8628M 2×41W 立体声 | 1×82W 单通道 数字输入功放

内置 DSP 多种音频处理效果

1. 特征

- 灵活电压配置
  - PVDD: 4.5V 到 26.4V
  - DVDD 和 I/O: 3.3V 或者 1.8V
- 输出功率
  - 2×41W, 立体声 (6Ω, 24V, THD+N = 1%)
  - 2×33W, 立体声 (4Ω, 18V, THD+N = 1%)
  - 1×82W, 单通道 (3Ω, 24V, THD+N = 1%)
- 出色的音频性能
  - THD+N ≤ 0.03% ： 1W, 1kHz, PVDD = 12V
  - SNR 信噪比 114 dB (加权)
  - 底噪 ≤ 37 uV_{RMS}
  - 28 mA 低静态电流 @ PVDD=12V
  - 91.7% 的效率, 6Ω 负载 ,PVDD=20V,2×28W
- 数字音频接口
  - I^2C 可选 4 个器件通信地址
  - I^2S, 左、右边对齐, TDM 音频格式
  - 3-线数字音频输入
  - 采样 32kHz, 44.1kHz/48kHz, 88.2kHz/96kHz
  - SDOUT 数字音频输出支持回声消除 – AEC 或 1.1 / 2.1 子通道信号通路
- 高阶音效算法
  - 多种方式支持数字/模拟增益调整
  - 小音量下低音增强算法
  - 输入信号混合到左或右通道
  - 左右通道独立的 2×15 个 BQs 和 2×5 post BQs 支持频响灵活调整
  - 爆音的压缩器前后调节音量，动态维护音频处理中的动态范围
  - 3 段 DRC，提前能量预测结合后端均衡器，实现平滑的多段音效控制，提高音乐清晰度
- 保护机制
  - FAULT 状态输出
  - OCP 过流保护
  - OTP 过热保护
  - UVLO 过压和欠压保护
  - 数字音频时钟检查

2. 应用

- 便携音箱: 蓝牙音箱，语音助手音箱
- 家庭音频: 电视，声霸，盒子，家庭影院
- 笔记本、台式机
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3. 概述

ACM8628M 一款高度集成、高效率的双通道数字输入功放。供电电压范围在 4.5V-26.4V,数字接口电源支持 3.3V 或 1.8V。在 8 欧负载下，输出功率可以到 2×41W，PBTL 模式下单通道可以输出 1×82W @1% THD+N.

ACM868M 采用新型 PWM 脉宽调制架构，根据信号大小动态调整脉宽，在保证音频性能前提下，降低静态功耗，提高效率，另外防止 POP 音的产生。

扩频技术的应用可以大幅降低 EMI 辐射，在功率和喇叭线长一定的范围内，可以用磁珠替代电感方案，从而优化成本和电路面积。

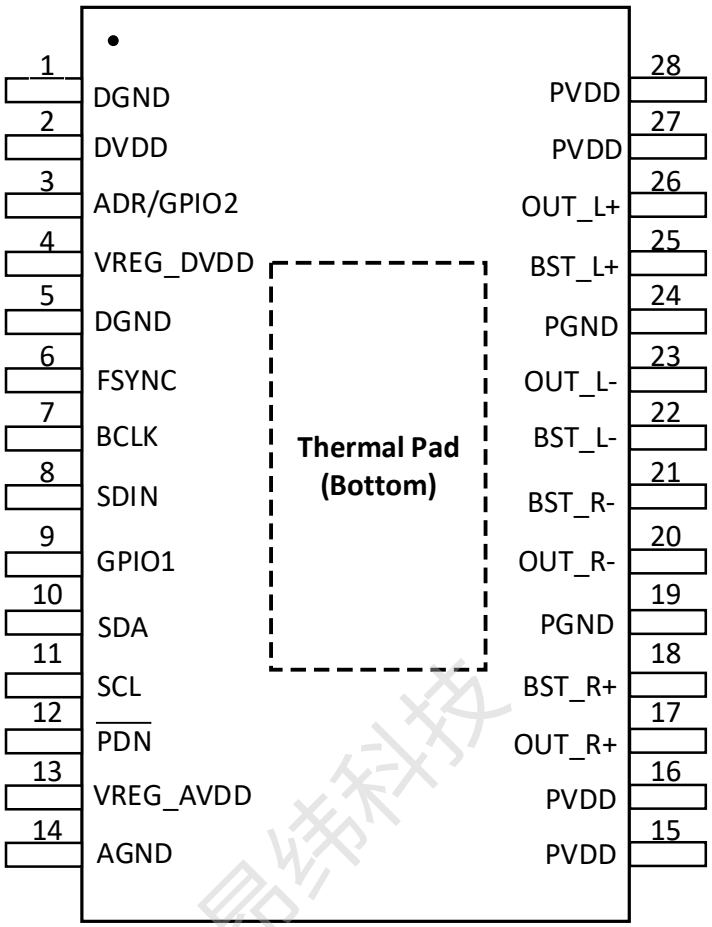
ACM8628M 高度集成了多种音效算法。内部模块可以独立控制，左右通道也可以独立控制。内部集成数字、模拟增益调节，信号混合模块，15 个 EQ 和 5 个 post EQ，可编程特定频段信号动态增强，3 段提前能量预测 DRC 外加 1 段 AGL 等多个独立模块，可实现多种音效。例如小信号低音增强，高低音补偿等功能可以通过这些模块实现.

4. 器件信息

料号	封装	尺寸	包装
ACM8628M	TSSOP 28	9.7 mm × 4.4 mm	3K/盘

5. 管脚配置和功能说明

ACM8628M
TSSOP 28 Pin



Pin No.	管脚名称	类型	描述
1	DGND	PWR	数字地
2	DVDD	PWR	数字电源输入: 3.3V 或 1.8V.
3	ADR/GPIO2	DIO	I^2C 地址选择 / GPIO2: FAULT / WARNING / SDOUT…
4	VREG_DVDD	AOUT	1.8V 数字调节器输出.
5	DGND	PWR	数字地
6	FSYNC	DIN	TDM 信号帧同步（或 I²S 左右通道选择）时钟
7	BLCK	DIN	TDM/I²S 的位选择时钟
8	SDIN	DIN	串行数据输入
9	GPIO1	DIO	GPIO1: FAULT / WARNING / SDOUT…
10	SDA	DIO	I^2C 串行数据.
11	SCL	DIN	I^2C clock.
12	$\overline{PDN}$	DIN	关机，低有效.
13	VREG_AVDD	AOUT	5.0V 模拟调节器输出.
14	AGND	PWR	模拟地
15	PVDD	PWR	输入电源

16	PVDD	PWR	输入电源
17	OUT_R+	AOUT	右通道输出正极
18	BST_R+	AIN	右通道输出正极的自举电容
19	PGND	PWR	电源功率地
20	OUT_R-	AOUT	右通道输出负极
21	BST_R-	AIN	右通道输出负极的自举电容
22	BST_L-	AIN	左通道输出负极的自举电容
23	OUT_L-	AOUT	左通道输出负极
24	PGND	PWR	电源功率地
25	BST_L+	AIN	左通道输出正极的自举电容
26	OUT_L+	AOUT	左通道输出正极
27	PVDD	PWR	输入供电电源
28	PVDD	PWR	输入供电电源

6. 器件系列比较

器件名称	R_{dson}	PVDD	输出功率
ACM8615M	135 mΩ	4.5V ~ 21V	单通道 1×21W (8Ω, 20V, THD+N = 1%)
ACM8625M	135 mΩ	4.5V ~ 26.4V	立体声 2×26W (8Ω, 22V, THD+N = 1%)
ACM8628M	90 mΩ	4.5V ~ 26.4V	立体声 2×41W (6Ω, 24V, THD+N = 1%)

7. 规格参数

7.1 绝对最大值

符号	描述	MIN	MAX	UNIT
DVDD	数字电源	-0.3	3.9	V
PVDD	输入电源	-0.3	30	V
$V_{I(Digin)}$	数字输入参考脚	-0.5	V_{DVDD}+0.5	V
$V_{I(OUTxx)}$	输出脚电压	-0.3	32	V
T_A	环境工作温度	-25	85	℃
T_{stg}	存储问题	-40	125	℃

(1) 超出以上绝对最大值范围会导致器件损坏。以上仅仅是绝对最大值范围，不是应用范围。这个范围不意味着器件能在这个条件下工作， 超出绝对最大值范围会影响器件的可靠性。

(2) VDD 数字输入参考脚包含: ADR/GPIO2, GPIO3, FSYNC, BCLK, SDIN, GPIO1, SDA, SCL, PDN.

7.2 ESD 特性

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001	±2000	V
		Charged-device model (CDM),per JEDEC specification JESD22-C101	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(SUPLLY)}$	输入电源	DVDD	1.62		3.63	V
		PVDD	4.5		26.4	
	推荐的 PVDD 范围	双通道，喇叭负载=4Ω (+/-20% 余量)	4.5		20.8	V
		双通道，喇叭负载=6Ω (+/-20% 余量)	4.5		26.4	
		双通道，喇叭负载=8Ω (+/-20% 余量)	4.5		26.4	
		PBTL 单通道，喇叭负载=2Ω (+/-20% 余量)	4.5		21	
		PBTL 单通道，喇叭负载=3Ω (+/-20% 余量)	4.5		26.4	
		PBTL 单通道，喇叭负载=4Ω (+/-20% 余量)	4.5		26.4	
$V_{IH(DIGIN)}$	DVDD 参考高电平		0.9×DVDD		DVDD	V
$V_{IL(DIGIN)}$	DVDD 参考低电平				0.1×DVDD	
L_{OUT}	输出最小电感量		1			μH
T_J	结工作温度		-40		150	℃
T_A	环境工作温度		-40		85	℃

7.4 Thermal Information

	ACM8628M	UNIT

		TSSOP 28 PINS JEDEC STANDARD 4-LAYER PCB	
θ_{JA}	结到环境温度热阻	28	℃/W
θ_{JT}	结到顶部热阻	22	℃/W
ψ_{JT}	结到 TOP 的参数热阻	1.2	℃/W

7.5 电气特性

室温 25° C, LPD mode, LC filter=10uH+0.68uF, Fsw=480kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL I/O						
|IIH|	输入逻辑高电流范围	$V_{IN(Digin)}=V_{DVDD}$			10	μA
|IIL|	输入逻辑低电流范围	$V_{IN(Digin)}$=0 V			-10	μA
$V_{IH(Digin)}$	输入逻辑高电平范围		70%			V_{DVDD}
$V_{IL(Digin)}$	输入逻辑低电平范围				30%	V_{DVDD}
$V_{OH(Digin)}$	输出逻辑高电平范围	I_{OH} = 2mA	80%			V_{DVDD}
$V_{OL(Digin)}$	输出逻辑低电平范围	I_{OH} = -2mA			20%	V_{DVDD}
I²C CONTROL PORT						
$C_{L(I2C)}$	I²C 容许的负载电容				400	pF
$F_{SCL(fast)}$	支持 SCL 高频率	No wait states, fast mode			400	kHz
$F_{SCL(slow)}$	支持 SCL 低频率	No wait states, fast mode			100	kHz
SERIAL AUDIO PORT						
t_{DLY}	需要 FSYNC 到 BCLK 的上升沿延迟		5			ns
D_{SCLK}	允许的 SCLK 占空比		40%		60%	
f_S	输入采样率		32		192	kHz
F_{BCLK}	BCLK 频率		32		64	f_S
AMPLIFIER OPERATING MODE AND DC PARAMETERS						
t_{OFF}	关机时间				10	ms
$A_{V(SPK\_AMP)}$	可编程增益	输入 (1FS)条件下，峰值电压的值	4.95		29.5	V_{peak}/FS
$\Delta A_{V(SPK\_AMP)}$	增益误差	Gain=29.5V_P/FS		0.5		dB
F_{SW}	放大器开关频率			384		kHz
				260		kHz
				480		kHz
				576		kHz
				768		kHz
$R_{DS(ON)}$	输出端 MOSFETs 内阻	FET + Metallization. V_{PVDD}=24V, $I_{(OUT)}$=500mA, T_J=25℃		90		mΩ
PROTECTION						
OCE_{THRES}	过流点阀值	喇叭输出电流 PVDD=24V (100Hz Burst on, 500 cycles interval)，输出 LC =4.7uF+0.68uF, Fsw=480kHz	6.5	7.5		A
$UVE_{THRES(PVDD)}$	PVDD 欠压保护阈值			4		V
$0VE_{THRES(PVDD)}$	PVDD 过压保护阈值			28.2		V
DCE_{THRES}	输出直流检测	输出端检测阈值		1.9		V
T_{DCDET}	输出直流检测时间	触发保护时间		570		ms
OTE_{THRES}	过温保护			160		℃
$OTE_{Hysteresis}$	过温保护迟滞			10		℃
OTW_{THRES}	过温警告温度			130		℃
AUDIO PERFORMANCE (STEREO BTL)						
|V_{OS}|	放大器输出偏移电压	0 信号输入，可编程增益 29.5Vp/FS, V_{PVDD}=12V	-10		10	mV

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{O(SPK)}$	输出功率 (每个通道 I) (LPD 模式, Fsw=480kHz)	V_{PVDD}=18V,R_{SPK}=6Ω,f=1kHz,THD+N=10%		30.72		W
		V_{PVDD}=18V,R_{SPK}=6Ω,f=1kHz,THD+N=1%		24.6		W
		V_{PVDD}=18V,R_{SPK}=4Ω,f=1kHz,THD+N=10%		42.41		W
		V_{PVDD}=18V,R_{SPK}=4Ω,f=1kHz,THD+N=1%		33.5		W
		V_{PVDD}=24V,R_{SPK}=6Ω,f=1kHz,THD+N=10%		52		W
		V_{PVDD}=24V,R_{SPK}=6Ω,f=1kHz,THD+N=1%		41		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O=1W,f=1kHz,R_{SPK}=6Ω, LPD Mode, Fsw=480kHz)	V_{PVDD}=18V		0.022		%
		V_{PVDD}=24V		0.021		%
$ICN_{(SPK)}$	底噪 (A-Weighted, AES17)	PVDD=18V, LC filter=10uH+0.68uF, Load=6Ω, LPD Mode		37.1		μVrms
		V_{PVDD}=18V, LC filter=10uH+0.68uF, Load=6Ω, BD Mode		38.2		μVrms
DR	动态范围	A-Weighted, -60dBFS method. V_{PVDD}=24V, Analog Gain=29.5Vp/FS		111		dB
SNR	信噪比	A-Weighted, reference to 1% THD+N Output Level, V_{PVDD}=24V		114		dB
PSRR	电源纹波抑制比	Injected Noise=1kHz, 1Vrms, V_{PVDD}=18V, input audio signal=digital zero		72		dB
$X\text{-}talk_{SPK}$	串扰	f=1kHz, V_{PVDD}=24V, Load=6Ω		90		dB
AUDIO PERFORMANCE (MONO PBTL)						
$\lvert V_{OS}\rvert$	放大器输出偏移电压	Measure differentially with zero input data, programmable gain configured with 29.5Vp/FS, V_{PVDD}=24V	-10		10	mV
$P_{O(SPK)}$	输出功率	V_{PVDD}=24V,R_{SPK}=3Ω,f=1kHz,THD+N=1%		82		W
		V_{PVDD}=24V,R_{SPK}=3Ω,f=1kHz,THD+N=10%		105		W
		V_{PVDD}=24V,R_{SPK}=4Ω,f=1kHz,THD+N=1%		67.57		W
		V_{PVDD}=24V,R_{SPK}=4Ω,f=1kHz,THD+N=10%		83		W
$THD+N_{SPK}$	谐波和噪音(P_O=1W, f=1kHz)	V_{PVDD}=24V, LC filter, R_{SPK}=3Ω, LPD Mode		0.027		%
DR	动态范围	A-Weighted, -60dBFS method, V_{PVDD}=24V, R_{SPK}=3Ω		115		dB
SNR	信噪比	A-Weighted, reference to 1% THD+N Output Level, V_{PVDD}=24V, R_{SPK}=3Ω		117		dB
$ICN_{(SPK)}$	底噪	VPVDD=24V, LC filter=10uH+0.68uF, Load=4Ω, BD Mode		37		μVrms
PSRR	电源纹波抑制比	V_{PVDD}=18V, LC filter=10uH+0.68uF, Load=3Ω, BD Mode		72		dB

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Serial Audio Port Timing-Slave Mode					
f_{BCLK}	BCLK 频率	1.024			MHz
t_{BCLK}	BCLK 周期	40			ns
t_{BCLKL}	BCLK 脉冲宽度，低	16			ns
t_{BCLKH}	BCLK 脉冲宽度，高	16			ns
t_{BF}	BCLK 到 FSYNC 上升沿	8			ns
t_{FB}	FSYNC 边沿到 BCLK 上升沿	8			ns
t_{SU}	数据设置时间，在 BCLK 上升沿前	8			ns
t_{DH}	Data 保持时间，在 BCLK 上升沿后	8			ns

		MIN	NOM	MAX	UNIT
t_{DFB}	Data 延迟时间从 BCLK 下降沿			22	ns
I^2C Bus Timing-Standard					
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7			μs
t_{LOW}	Low period of the SCL clock	4.7			μs
t_{HI}	High period of the SCL clock	4			μs
t_{RS-SU}	Setup time for (repeated) START condition	4.7			μs
t_{S-HD}	Hold time for (repeated) START condition	4			μs
t_{D-SU}	Data setup time	250			ns
t_{D-HD}	Data hold time	0		3450	ns
t_{SCL-R}	Rise time of SCL signal	$20+0.1C_B$		1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20+0.1C_B$		1000	ns
t_{SCL-F}	Fall time of SCL signal	$20+0.1C_B$		1000	ns
t_{SDA-R}	Rise time of SDA signal	$20+0.1C_B$		1000	ns
t_{SDA-F}	Fall time of SDA signal	$20+0.1C_B$		1000	ns
t_{P-SU}	Setup time for STOP condition	4			μs
C_B	Capacitive load for each bus line			400	pf
I^2C Bus Timing-Fast					
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			μs
t_{LOW}	Low period of the SCL clock	1.3			μs
t_{HI}	High period of the SCL clock	600			ns
t_{RS-SU}	Setup time for (repeated) START condition	600			ns
t_{RS-HD}	Hold time for (repeated) START condition	600			ns
t_{D-SU}	Data setup time	100			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20+0.1C_B$		300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20+0.1C_B$		300	ns
t_{SCL-F}	Fall time of SCL signal	$20+0.1C_B$		300	ns
t_{SDA-R}	Rise time of SDA signal	$20+0.1C_B$		300	ns
t_{SDA-F}	Fall time of SDA signal	$20+0.1C_B$		300	ns
t_{P-SU}	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns
C_B	Capacitive load for each bus line			400	pf

7.7 时序参数要求信息

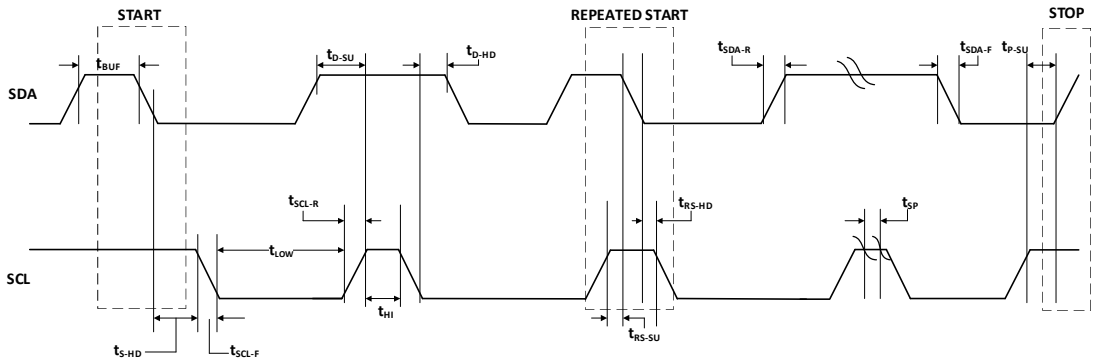


Figure 1 I²C Communication Port Timing Diagram

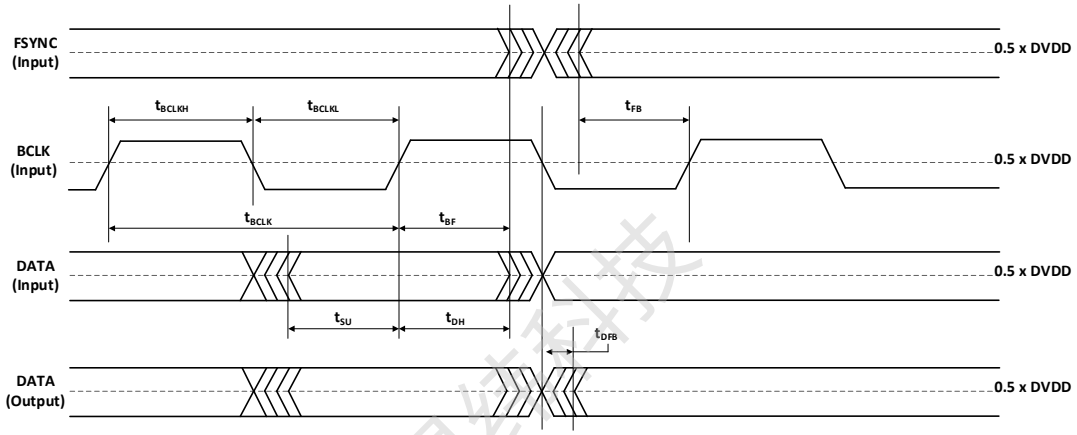


Figure 2 Serial Audio Port Timing in Slave Mode

8. 静态功耗

8.1 DVDD 电流

Fs=48kHz，室温 25° C.

Table 1 DVDD Current

DVDD (V)	Device Mode	Current Consumption (mA)	Setting Register Location
3.3	Play Mode (DSP Enable)	30.65	Register 0x04
	Play Mode (DSP Bypass)	13.066	Register 0x04 and Register 0x05
	Driver-off (DSP Enable)	30.375	Register 0x04
	Driver-off (DSP Bypass)	12.798	Register 0x04
	Analog-off	0.933	Register 0x04
	Digital-off	0.848	Register 0x04
	$\overline{PDN}$=0	0.007	Pin 12 pulled to low
1.8	Play Mode (DSP Enable)	27.68	Register 0x04
	Play Mode (DSP Bypass)	13	Register 0x04 and Register 0x05
	Driver-off (DSP Enable)	27.47	Register 0x04
	Driver-off (DSP Bypass)	12.7	Register 0x04
	Analog-off	0.688	Register 0x04
	Digital-off	0.604	Register 0x04
	$\overline{PDN}$=0	0.0019	Pin 12 pulled to low

8.2 PVDD 电流

Fs=48kHz，室温 25° C. LC Filter=10uH+0.68uF，Fsw=480khz， LPD Mode.

Table 2 PVDD Current

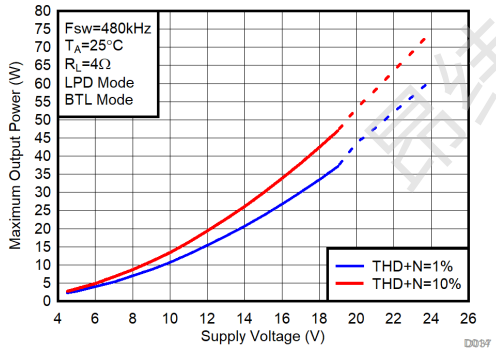
PVDD (V)	Device Mode	Current Consumption (mA)	Setting Register Location
7.4	Play	22	Register 0x04
	Driver-off	9.593	
	Analog-off	5.897	
	Digital-off	0.0924	
	PDN=0	0.0062	Pin 12 pulled to low
12	Play	27.7	Register 0x04
	Driver-off	9.623	
	Analog-off	5.943	
	Digital-off	0.0934	
	PDN=0	0.0069	Pin 12 pulled to low
16	Play	33.26	Register 0x04
	Driver-off	9.67	
	Analog-off	5.998	

	Digital-off	0.0938	
	PDN=0	0.0075	Pin 12 pulled to low
18.5	Play	37	Register 0x04
	Driver-off	9.705	
	Analog-off	6.035	
	Digital-off	0.0944	
	PDN=0	0.0082	Pin 12 pulled to low
24	Play	46	Register 0x04
	Driver-off	9.787	
	Analog-off	6.112	
	Digital-off	0.098	
	PDN=0	0.009	Pin 12 pulled to low

9. 典型特性曲线

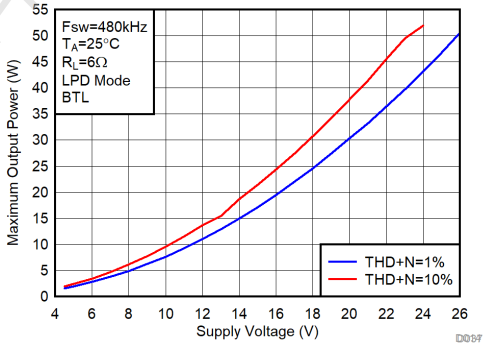
9.1 LPD 模式下 Bridge Tied Load (BTL) 特性曲线

室温 25℃（除非特殊说明）。测试基于 ACM8628M EVM 板子，设备 Audio Precision System 2722 和 20KHz brickwall 滤波器。芯片 PWM 模式设定为 LPD (低功耗模式)， D 类功放带宽 105kHz 到 480kHz。



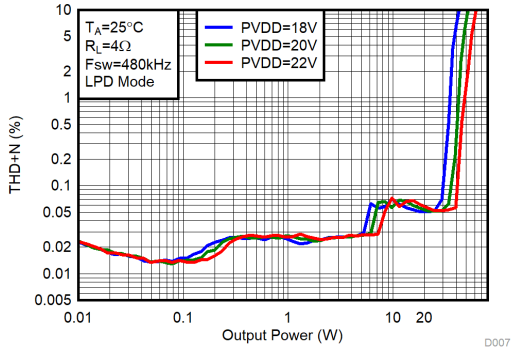
(Load=4Ω, Fsw=480kHz, LPD Mode)

Figure 3 Output Power vs PVDD



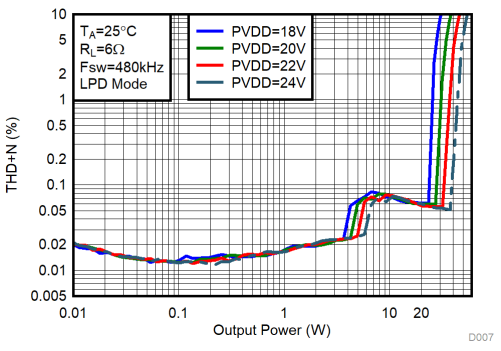
(Load=6Ω, Fsw=480kHz, LPD Mode)

Figure 4 Output Power vs PVDD



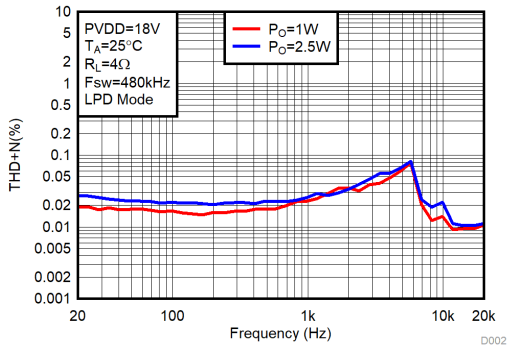
(Load=4Ω, Fsw=480kHz, LPD Mode)

Figure 5 THD+N vs Output Power



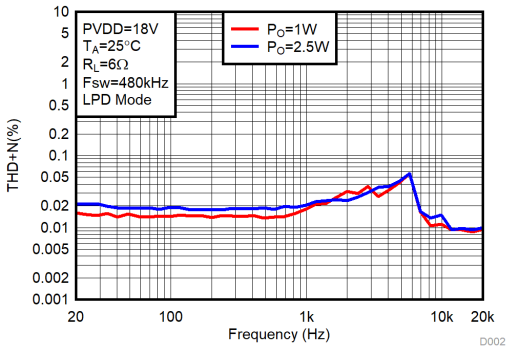
(Load=6Ω, Fsw=480kHz, LPD Mode)

Figure 6 THD+N vs Frequency



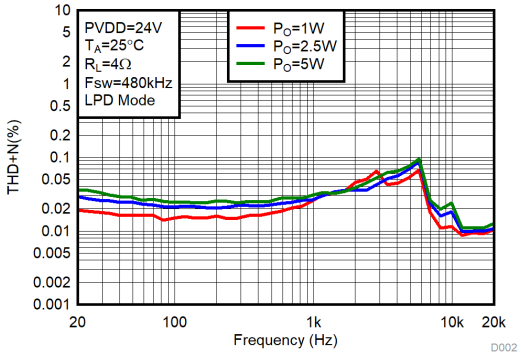
(PVDD=18V, Load=4Ω, Fsw=480kHz)

Figure 7 THD+N vs Frequency



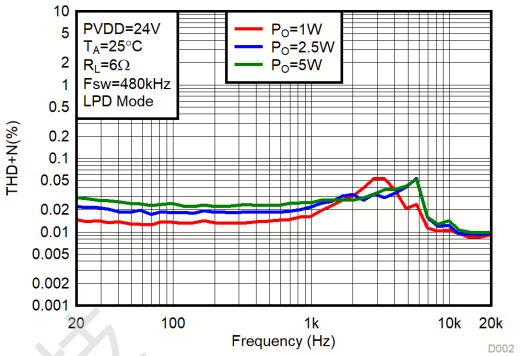
(PVDD=18V, Load=6Ω, Fsw=480kHz)

Figure 8 THD+N vs Frequency



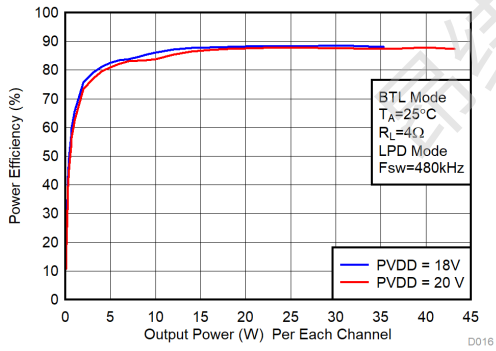
(PVDD=24V, Load=4Ω, Fsw=480kHz)

Figure 9 THD+N vs Frequency



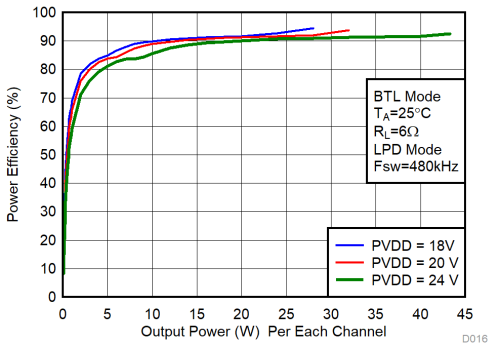
(PVDD=24V, Load=6Ω, Fsw=480kHz)

Figure 10 THD+N vs Frequency



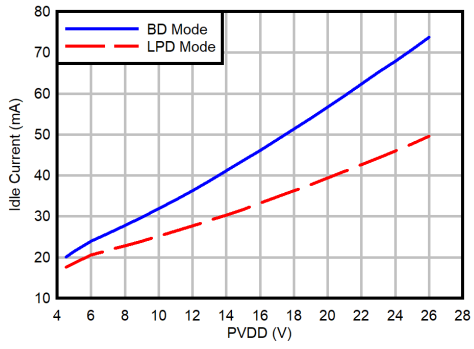
(Load=4Ω, Fsw=480kHz, LPD Mode)

Figure 11 Efficiency vs Output Power



(Load=6Ω, Fsw=480kHz, LPD Mode)

Figure 12 Efficiency vs Output Power

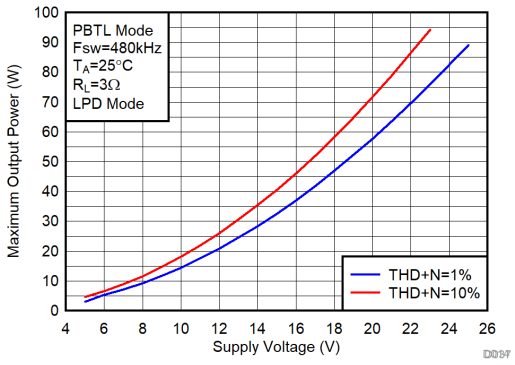


(Fsw=480kHz, LC Filter=10uH+0.68uF)

Figure 13 Idle Current vs PVDD

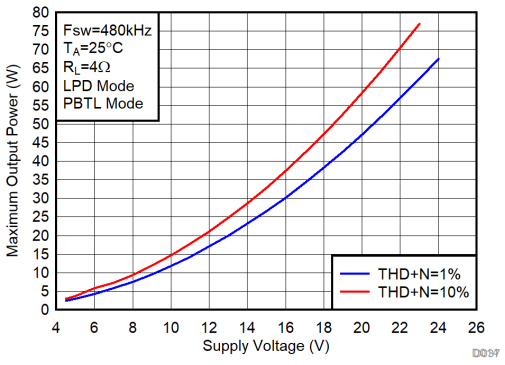
9.2 Parallel Bridge Tied Load (PBTL 模式) 特性曲线 低功耗模式

室温 25℃ (除非特殊说明) 。测试基于 ACM8628M EVM 板子，设备 Audio Precision System 2722 和 20KHz brickwall 滤波器。芯片 PWM 模式设定为 LPD (低功耗模式) ， D 类功放带宽 105kHz 到 480kHz。



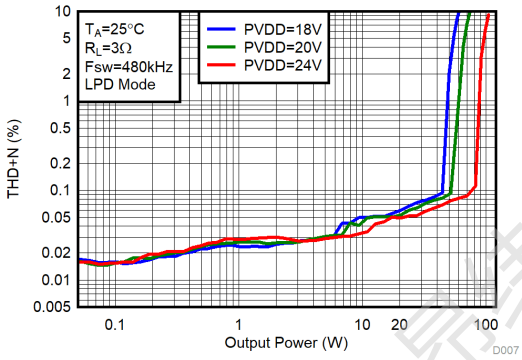
(Load=3Ω, Fsw=480kHz, LPD Mode)

Figure 14 Output Power vs PVDD



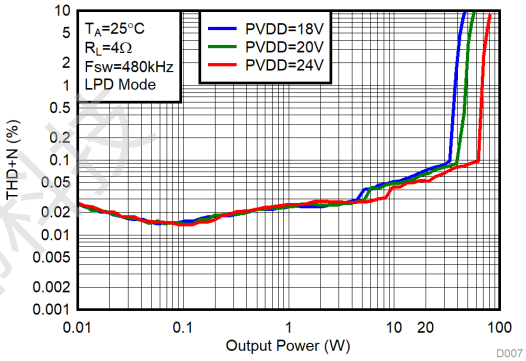
(Load=4Ω, Fsw=480kHz, LPD Mode)

Figure 15 Output Power vs PVDD



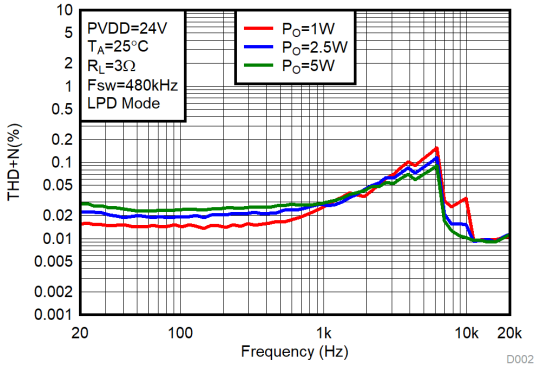
(Load=3Ω, Fsw=480kHz, LPD Mode)

Figure 16 THD+N vs Output Power



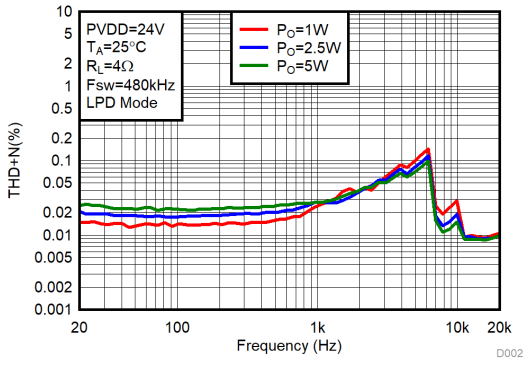
(Load=4Ω, Fsw=480kHz, LPD Mode)

Figure 17 THD+N vs Output Power



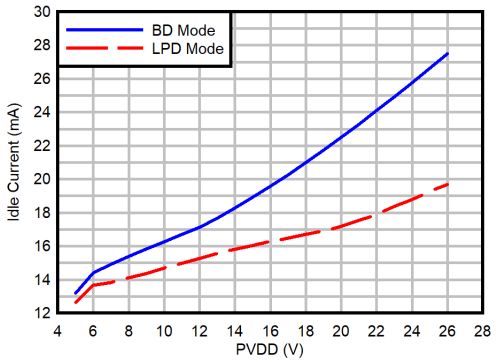
(Load=3Ω, Fsw=480kHz, LPD Mode)

Figure 18 THD+N vs Frequency



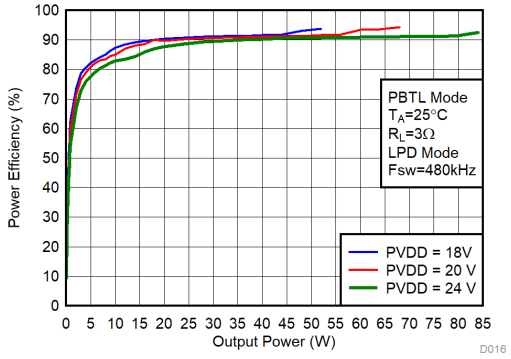
(Load=4Ω, Fsw=480kHz, LPD Mode)

Figure 19 THD+N vs Frequency



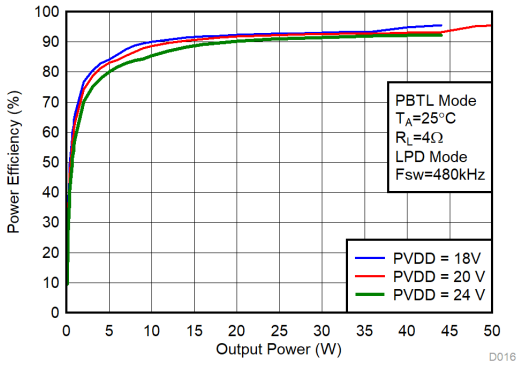
(Fsw=480kHz, LC Filter=10uH+0.68uF)

Figure 20 Idle Current vs PVDD



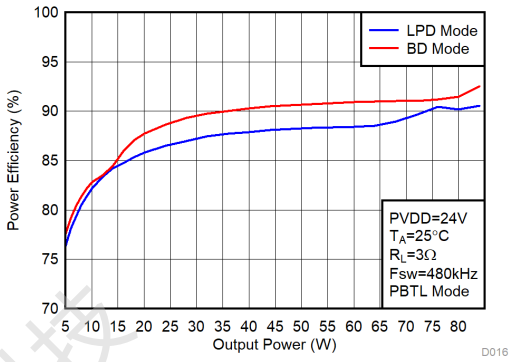
(Load=3Ω, Fsw=480kHz, LPD Mode)

Figure 21 Efficiency vs Output Power



(Load=4Ω, Fsw=480kHz, LPD Mode)

Figure 22 Efficiency vs Output Power



(Load=3Ω, Fsw=480kHz, BD vs LPD)

Figure 23 Efficiency vs Output Power

10. 细节描述

10.1 细节描述

ACM8628M 架构上包含 4 个主要模块，集成模块保障了音频质量、更加灵活和易用。4 个模块如下：

- 一个双通道 DAC
- 一个音效调节器
- 一个灵活的闭环功放
- 一个 I²C 控制和通信模块

芯片需要两个电源工作，一个是 DVDD，主要是给低功耗的数字电路供电。另外一个电源是功率电源 PVDD，主要是给功放提供功率电源。内部还会产生两个 LDO，一路是 PVDD 降压到 5V 给 VREG_AVDD 供电，还有一路是降压到 1.8V 给 VREG_DVDD 供电。

10.2 功能框图

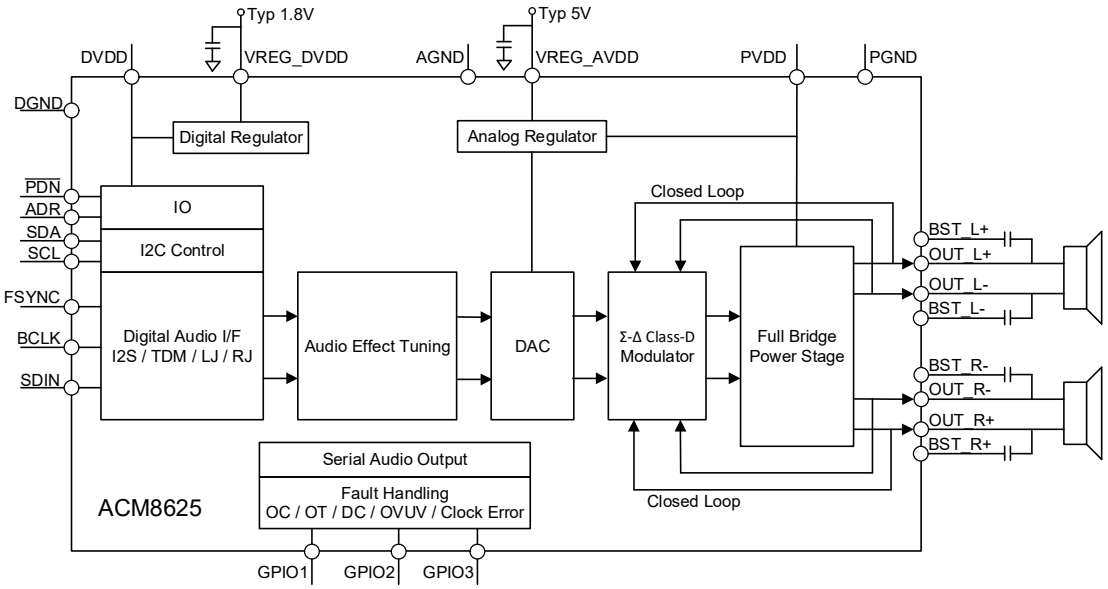


Figure 24 Function Block Diagram

10.3 时钟

9.3.1 主时钟

ACM8628M 的时钟系统比较丰富，且简单易用.

串行音频接口典型的有三个接口:

- BCLK
- FSYNC/LRCLK (Left/Right Word Clock and Frame Sync)
- SDIN (输入数据)

芯片内部的 PLL 采用 BCLK 作为参考时钟，根据内部数字音频处理和 DAC 的要求，会基于参考时钟产生更高频的时钟。

ACM8628M 集成音频采样率的检测电路，能够自动获得采样率。支持音频信号采用率 32kHz, 44.1kHz-48kHz, 88.2kHz-96kHz 采样率的检测能够自动调整内部 SRC 满足内部音频信号处理和 DAC 的时钟要求。

9.3.2 串行音频端口 – 时钟频率

串行音频端口是三线端口，分别是 FSYNC/LRCLK, BCLK 和 SDIN. BCLK 是位时钟，是同步信号（也叫 SCK,SCL），用于把 SDIN 上的数据写入串行移位寄存器。ACM8628M 的数据写入是在 BCLK 的上升沿时写入的。FSYNC/LRCLK 是左右声道选择信号，或者在 TDM 模式时作为帧同步信号.

Table 3. 数据格式，位深和时钟频率

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	BCLK RATE (Fs)

I²S/LJ/RJ	32,24,20,16	32 to 96	64,32
TDM	32,24,20,16	32	128
		44.1/48	128,256,512
		96	128,256

When clock halt, non-supported BCLK to FSYNC/LRCLK ratio is detected, the device reports clock error in Register 0x18 in Page0.

9.3.3 钟停摆-自动恢复

当没有信号输入时，一些主处理器会停止 I²S 时钟。当时钟停止时，芯片会把所有输出通道（输出功率管）设置为高阻状态，并输出时钟错误报告，错误报告在寄存器 0x18。当时钟恢复，芯片会自动返回原来的状态，输出通道（输出功率管）重新打开。

9.3.4 采样率动态变化

ACM8628M 支持 FSYNC/LRCLK 动态更改。例如 FSYNC/LRCLK 从 32kHz 改为 48kHz 或者 96kHz 时，在变更新采样率之前，主程序需要把 FSYNC/LRCLK 停止 10ms 以上。

9.3.5 音频数据端口 –数据格式和位深

芯片支持行业标准音频数据格式，包括标准 I²S,左对齐，右对齐和 TDM/DSP 数据. 数据格式的选择在 Page0 页的寄存器 0x07 里面. 如果 TDM/DSP 模式下 FSYNC/LRCLK 的高宽度小于 BCLK 的 8 个周期，则寄存器 Page0/0x07 D[5:4]应设置为 01。所有格式都必须是 2 进制的补码，MSB-first 音频数据，32 位的音频数据都可以。在 Table1 中列出了所有支持的数据格式，字节长度和采样率。在图 14 到图 18 列出了格式的细节要求。 字节长度可以通过寄存器 Page0/0x07 D[1:0]选择。数据移位可以通过寄存器 Page0/0x08 选择.

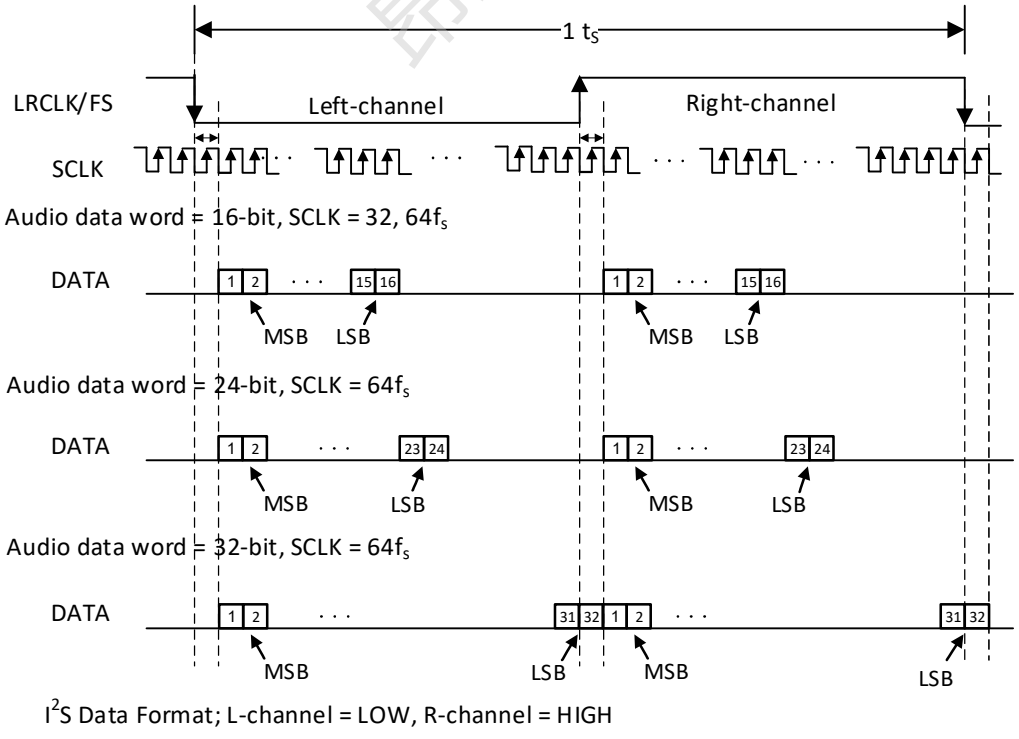


Figure 25 I²S Audio Data Format

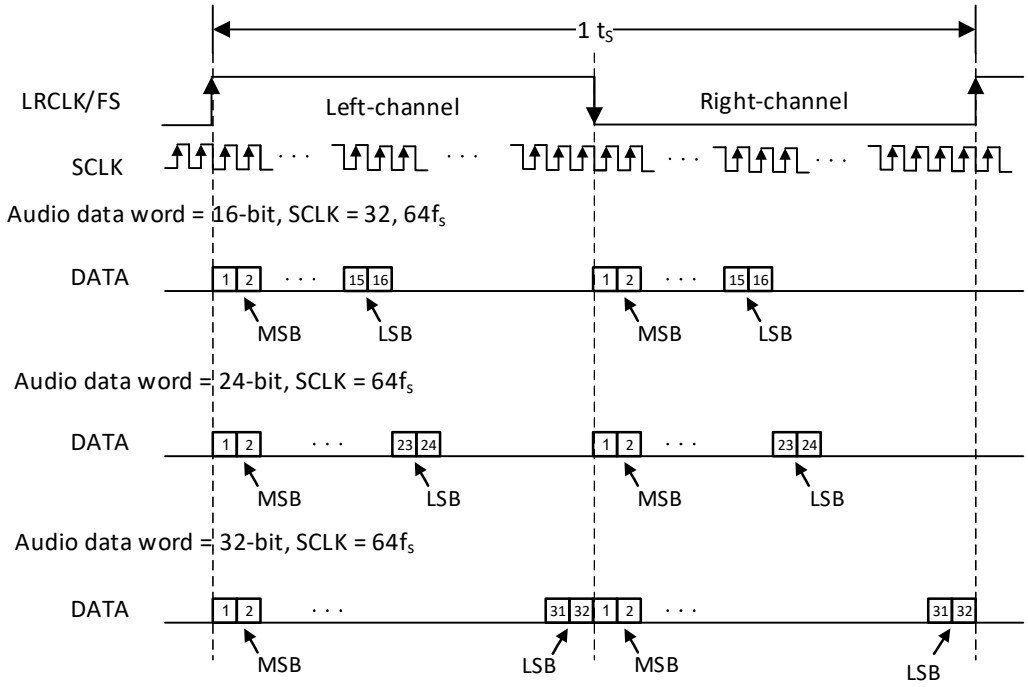
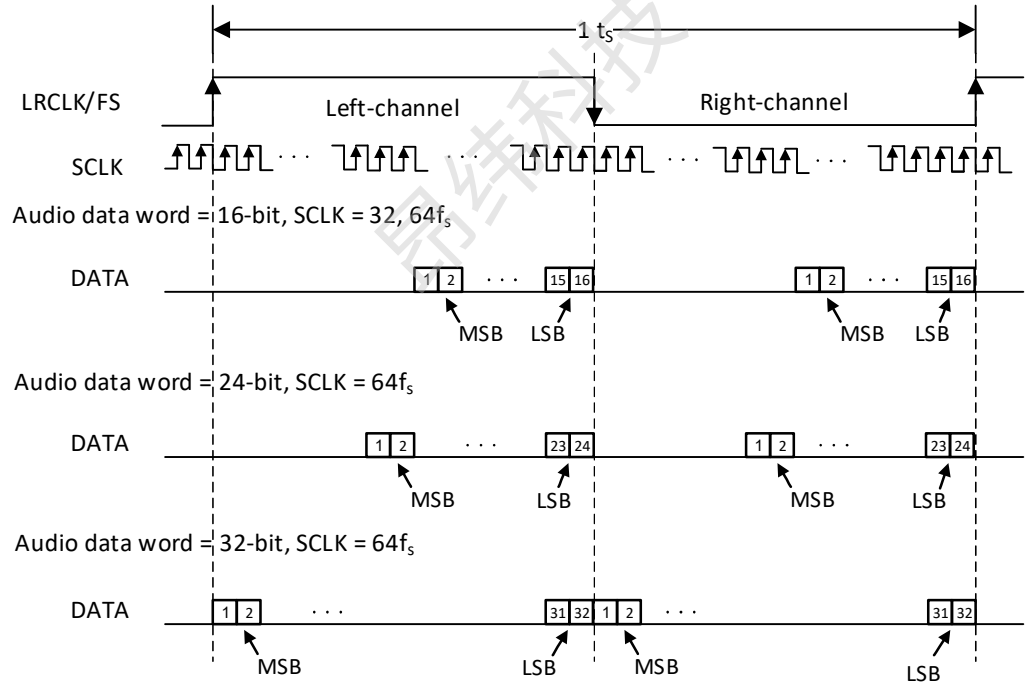
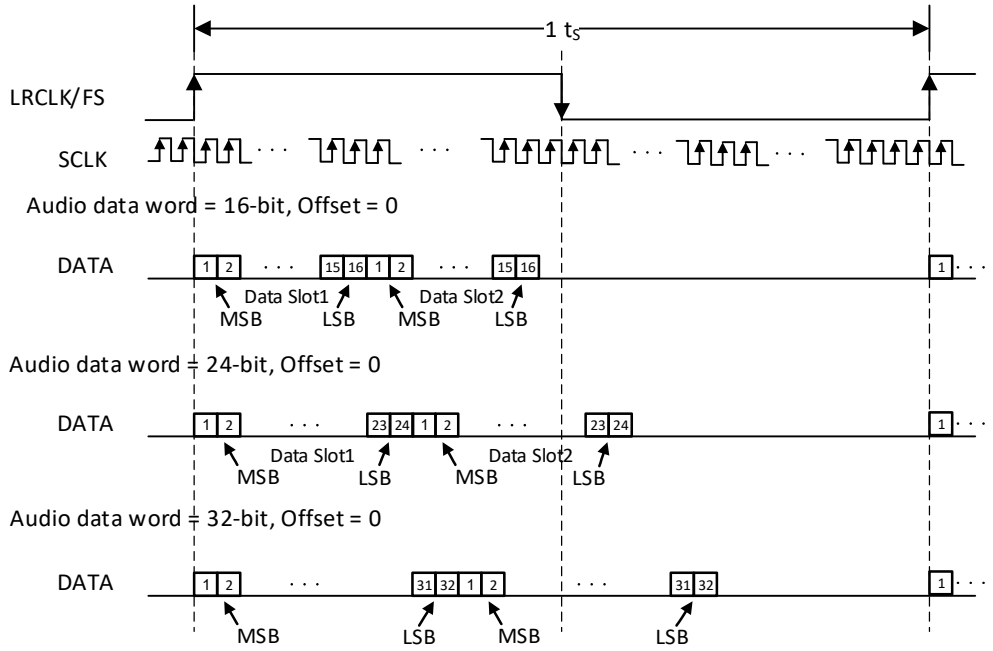


Figure 26 Left-Justified Audio Data Format



Right-Justified Data Format; L-channel = HIGH, R-channel = LOW

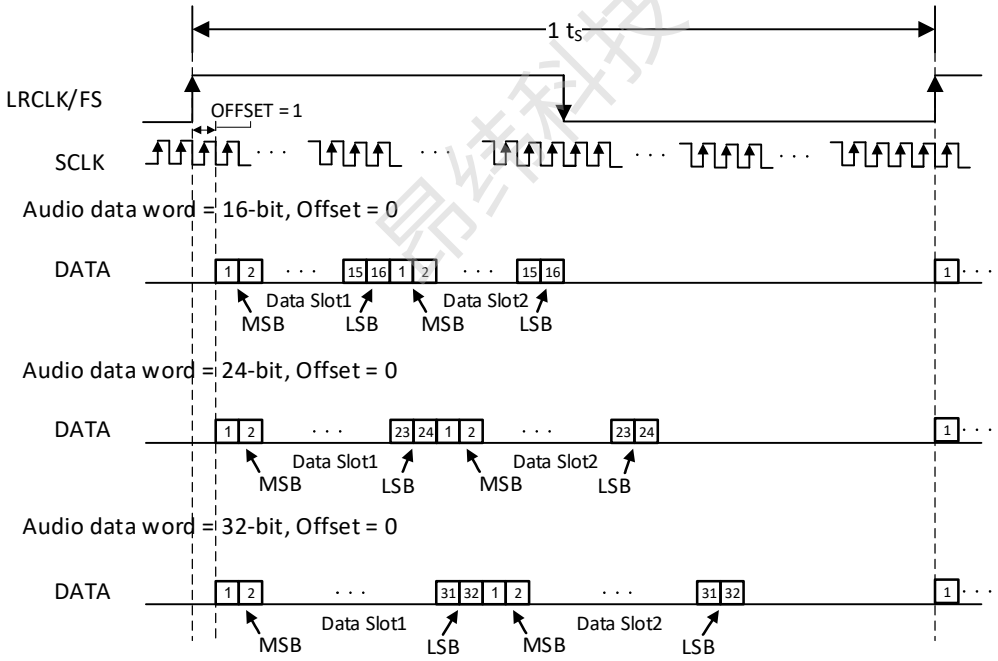
Figure 27 Right-Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCLK/FS should be 1× SCLK at minimum. Rising edge is considered frame start

Figure 28 TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCLK/FS should be 1× SCLK at minimum. Rising edge is considered frame start

Figure 29 TDM 2 Audio Data Format

10.4 电源供电

为了系统设计方便，ACM8628M 除了功率电源 PVDD(4.5V~26.4V) 之外，还需要一个 3.3V 或 1.8V 。 芯片还有两组内部的 LDO 给 gate drive 电路和内部电路供电，对应的外部管脚需要一组旁路电容。两组 LDO 不

建议给其他器件使用，否则会降低内部 LDO 的性能影响输出音频质量。另外，需要浮动电源的，例如高栅极驱动器，都需要几个外部电容做自举电容用。为了良好的电气特性和声学特性，输出端的 PWM 信号采用完全相同但是相互独立的半桥模式。因此每个输出有单独的自举管脚(BST_x)。特别需要注意的是，所有的去耦电容都要尽可能的靠近对应的管脚摆放.

10.5 增益设置

下图所示，ACM8628M 的路径包括数字输入，数字路径，数字转 PWM，gate driver 驱动，功放级，还有从输出反馈环路。增益分成两个部分，一个是数字增益，一个是后端的模拟增益。
注意下表中的是模拟增益是 DAC 音量，而不是开发工具 GUI 上 DSP 中的音量。音量调整一般建议调整 GUI 上的数字音量。

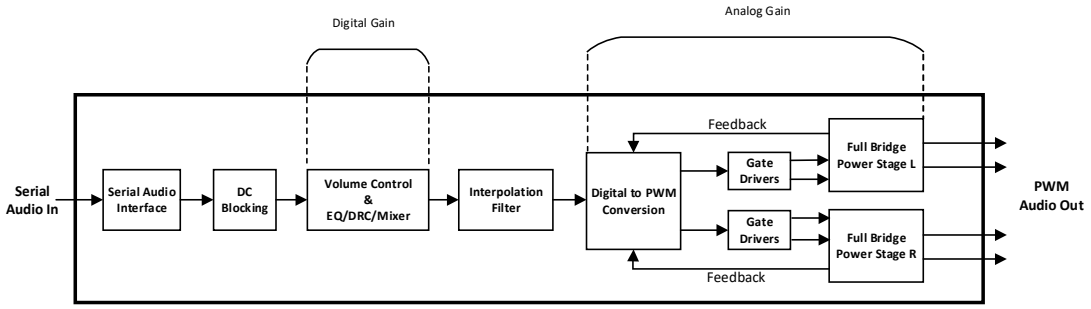


Figure 30 Gain Structure

数字增益部分包含音量控制器和 EQ/DRC/Mixer. 音量控制器默认设置是 0dB ， EQ/DRC/Mixer 默认是 bypass. 功放的模拟增益设置是用输出幅度衡量 A 额 rms) 。V_{AMP}=Input +数字增益 + 模拟增益 dBV
其中:

- V_{AMP} 是功放的输出幅度，单位是 dBV_{RMS}
- 输入是数字输入相对于 0dBFS 的振幅，单位是 dB
- 数字增益是数字音量控制设置，从 -110dB 到 24dB.
- 模拟增益设置从 26.38dB, 25.88dB, 25.38dB 到 10.88dB，每个 0.5dB 一个挡位

Table 4 Amplifier Gain Settings

模拟增益	全幅输出	
(Register 0x02h in Page0)	dBV_{RMS}	V_{PEAK}
00000	26.38	29.5
00001	25.88	27.84
00010	25.38	26.3
00011	24.88	24.8
…	…	…
01110	19.38	13.17
01111	18.88	12.44
10000	18.38	11.74
…	…	…
11111	10.88	4.95

10.6 保护机制

ACM8628M 的保护机制有温度保护，短路保护，欠压保护，过压保护，直流输出保护，时钟错误侦测等保

护电路。一旦发生错误，错误日志输出在寄存器 0x17h-0x19h（Page0）。这些错误通过正确设置寄存器 0x0Ah 和 0x0Ch（Page0），把 GPIO0/1 脚拉到 DGND。通过改写寄存器 0x01h（Page0）中的 bit7，从 0 改为 1，从而清空这些错误日志。

1. 过温保护.。内部结温超过 160°C 时芯片就会关掉，当回落到 150°C 时才会恢复。 温度浮动会有 10%的误差范围。通过改写寄存器 0x11h 的 Bit2，从 0 到 1，使得过温保护自动恢复。
2. 短路保护。当输出端短路，或者输出端短路到 GND/PVDD 时，短路保护电路会启动电路保护。对于 24V 的正常应用，流经功率管电流应该不大于 6.5A。否则，短路保护电路将会把 FAULT 脚 (GPIO 脚) 拉到 DGND，关掉输出。
3. PVDD 过压保护。 供电电压超过 28V，ACM8628M 就会关闭功放输出端。当回落到 27.5V 时，才会恢复正常工作。
4. PVDD 欠压保护。 PVDD 低于 4V，芯片关闭输出，回升到 4.3V 时恢复正常工作。
5. 喇叭直流检测保护。输出检测到直流电压超过 1.9V 超过 570ms，芯片启动直流保护，关掉输出端。这种错误移除后，通过改写寄存器 0x01h 中的 Bit7，从 0 改到 1，清除错误。或者芯片保持输出阶段在高阻状态。

时钟错误检测。检测到时钟停止，不支持 BCLK 到 FSYNC/LRCLK 被检测，芯片在寄存器 0x18 输出错误报告。错误移除时，器件恢复正常模式.

10.7 扩频技术

ACM8628M 支持扩频技术，扩频技术能有效降低 EMI 噪音辐射。

打开扩频的寄存器是 0x0Eh ， Page 0，默认是关闭的.

打开展频的顺序如下 (适用于 384kHz/480kHz/576kHz 开关频率):

1. Step1, Write content 0x00 to Register address 0x00.
2. Step2, Write content 0x01 to Register address 0x0E.
3. Step3, Write content 0x01 to Register address 0x00.
4. Step4, Write content 0x02 to Register address 0x1A.
5. Step5, Write content 0x00 to Register address 0x00.

10.8 I²C 设备地址

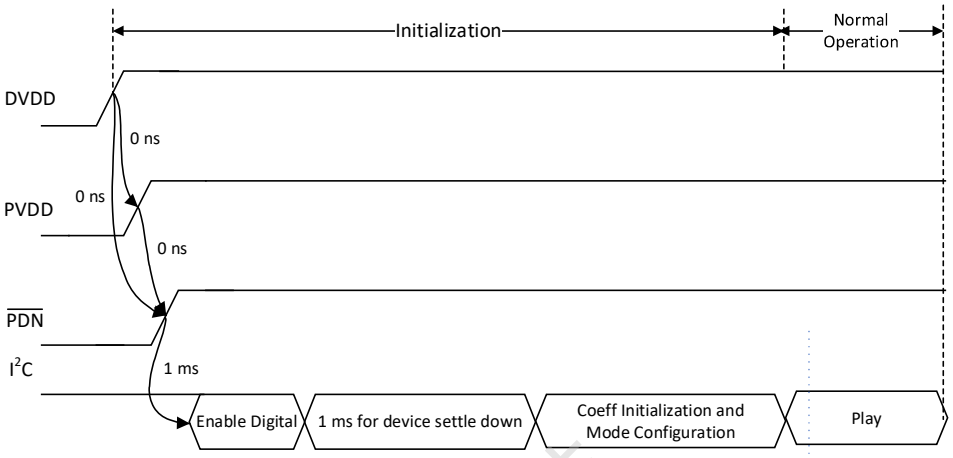
ACM8628 的 I2C 地址有 7 个 bits。前 5 个 bits(MSBs)预设定为 00101 (0x2x)。后面两个 bits 是设备选择位，用户可以通过下表 3 中的 ADR 脚自定义。

Table 5 I²C Device Address Configuration

ADR PIN Configuration	MSBs					User Define		LSB	Device Write Address
4.7kΩ to DVDD	0	0	1	0	1	0	0	R/W	0x28
15kΩ to DVDD	0	0	1	0	1	0	1	R/W	0x2a
47kΩ to DVDD	0	0	1	0	1	1	0	R/W	0x2c
120kΩ to DVDD	0	0	1	0	1	1	1	R/W	0x2e

10.9 启动序列

1. 配置 ADR/GPIO2 脚，给 I²C 配置正确的器件地址。s.
2. 提供电源 (I²C 通信需要电源 DVDD).
3. 当所有电源稳定后，在 I²C 通信前，把 PDN 拉高至少 1ms 。
4. 通过 I²C 控制口配置芯片（确保 PDN 在 I²C 通信前已经拉高）。
5. 芯片进入正常工作模式。

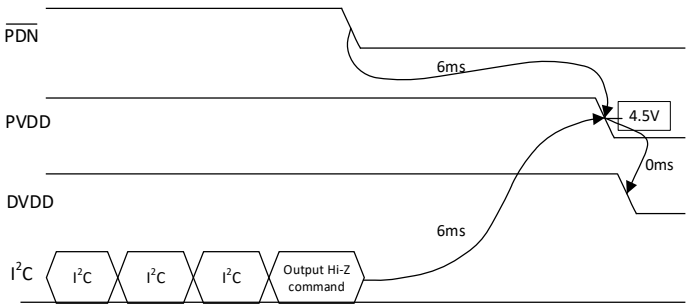


Notes:
1) 0ns means no sequence requirement
2) I²C communication and internal Digital processing work in DVDD domain, no PVDD required

Figure 31 Start-up Sequence

10.10 关机时序

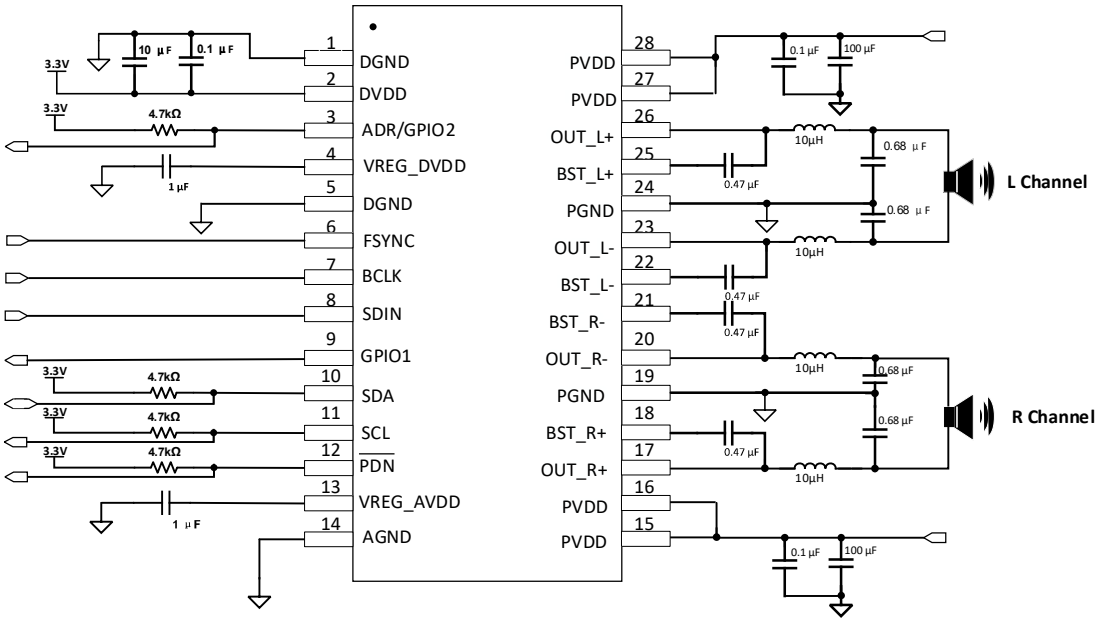
1. 从正常模式开始。
2. 通过修改寄存器 0x04h 或者拉低 PDN 脚让芯片进入数字关机状态.
3. 等待至少 6ms (时间取决于 FSYNC 频率,数字音量和下降沿时间)。
4. 关闭电源.
5. 芯片进入完全关机状态.



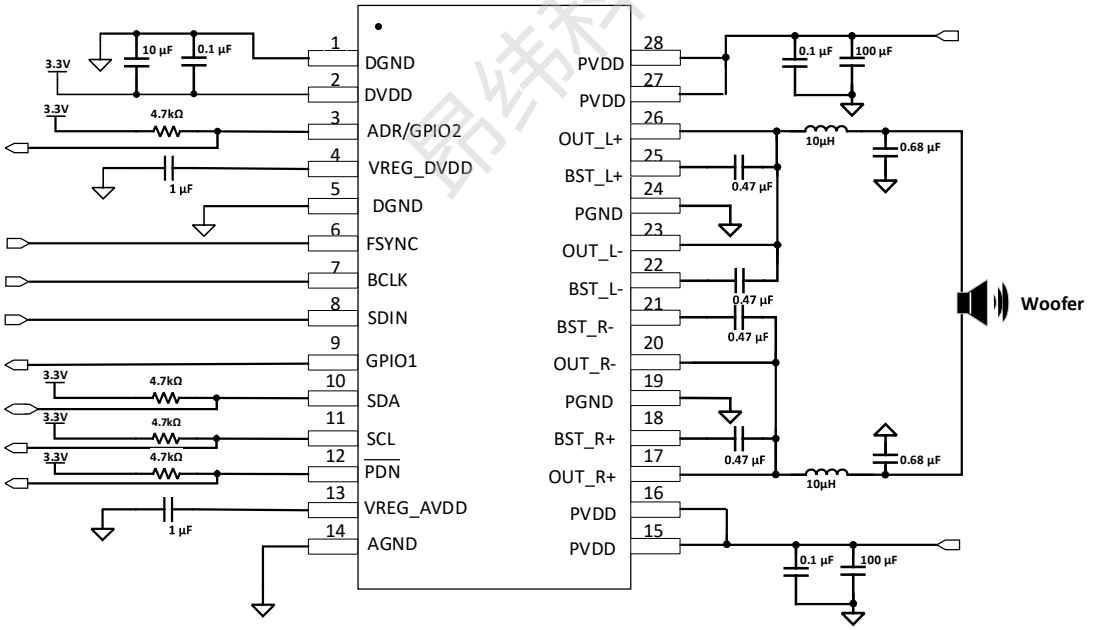
- Before PVDD/DVDD power down, Class D Output driver needs to be disabled by PDN or by I²C.
- At least 6ms delay needed based on LRCLK (Fs) = 48kHz,Digital volume ramp down update every sample period, decreased by 0.5dB for each update, digital volume =24dB.

Figure 32 Shutdown Sequence

11. 立体声典型应用



12. 单通道典型应用



13. Register Maps

13.1 Control Registers on Page0

Offset	Acronym	Register Name	Reset Value
0x01	AMP_CTRL1	F_{SW} PWM switching frequency, Fault clear, PBTL/BTL	0x00
0x02	AMP_CTRL2	Analog gain	0x00
0x03	AMP_CTRL3	Loop bandwidth, 2 PWM channels phase control	0x00
0x04	STATE_CTRL	Reset, Separate channel Hi-Z / Mute, State Control	0x00
0x05	PROCESSING_CTRL1	AGL, DRB, Hybrid, Post EQ, Sub-CH bypass control	0x12
0x06	PROCESSING_CTRL2	Processing flow selection and low power mode selection	0xF0
0x07	I2S_DATA_FORMAT1	I2S data format, length, FSYNC	0x02
0x08	I2S_DATA_FORMAT2	I2S Shift bits	0x00
0x09	I2S_DATA_FORMAT3	Reserved	0x05
0x0A	GPIO2_CTRL	SDOUT (GPIO2) enable and function selection	0x29
0x0B	GPIO1_CTRL	ADR (GPIO1) enable and function selection	0x2B
0x0C	GPIO1_FAULT_SEL	Clipping, OTW, OTSD, Clock Fault, PVDD UV/OV, DC, OC selection	0xFF
0x0D	GPIO2_FAULT_SEL	Clipping, OTW, OTSD, Clock Fault, PVDD UV/OV, DC, OC selection	0xFF
0x0E	SS_CTRL	Spread spectrum setting	0x00
0x0F	VOLUME_CTRL_L	Volume control for left channel	0xD0
0x10	VOLUME_CTRL_R	Volume control for right channel	0xD0
0x11	MSIC_CTRL	Fault latch selection, OTSD auto-recovery enable	0x03
0x12	I2S_CLK_FORMAT_RPT1	BCLK ratio (MSB), Sample rate detect	0x00
0x13	I2S_CLK_FORMAT_RPT2	BCLK ratio (LSB)	0x00
0x15	DIEID_RPT	DIE ID	0x00
0x16	STATE_RPT	State report	0x00
0x17	FAULT_RPT1	OTSD, PVDD OV/UV, DC, OC	0x00
0x18	FAULT_RPT2	Clock fault, EQs write error	0x00
0x19	FAULT_RPT3	Clipping, OTW	0x00
0x7E	XOR_CHECKSUM	XOR Checksum	0x00
0x7F	CRC_CHECKSUM	CRC Checksum	0x00

12.1.1 Register 1 AMP_CTRL1 (Offset=1h) [Reset=0x00]

7	6	5	4	3	2	1	0
FAULT_CLR	RESERVED			FSW_SWL			PBTL
R/W	R			R/W			R/W

Bit	Field	Type	Reset	Description
7	FAULT_CLR	R/W	0	Once write this bit to 1, device will clear analog fault, this bit is auto-clear

6-4	RESERVED	R	000	These bits are reserved
3-1	FSW_SEL	R/W	000	000: 384kHz 001: 260kHz 010: 480kHz 011: 576kHz 100: 768kHz
0	PBTL	R/W	0	0: BTL Mode 1: PBTL Mode, PBTL can be set when device is in digital off state

12.1.2 Register 2 AMP_CTRL2 (Offset=2h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED			ANA_GAIN				
R			R/W				

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	000	These bits are reserved
4-0	ANA_GAIN	R/W	00000	Analog Gain Control, with 0.5dB per step. These bits control the analog gain. 00000: 0dB (29.5Vp/FS) 00001: -0.5dB 00010: -1dB … 11111: -15.5dB

12.1.3 Register 3 AMP_CTRL3 (Offset=3h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED		CH_PHASE_CTL	RESERVED		BW_CTRL		
R		R/W	R		R/W		

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5	CH_PHASE_CTRL	R/W	0	0: out phase 1: in phase
2-0	BW_CTRL	R/W	000	000: 75kHz 001: 90kHz 010: 105kHz 011: 125kHz 100: 155kHz 101: 180kHz 110: 220kHz 111: 265kHz

12.1.4 Register 4 STATE_CTRL (Offset=4h) [Reset=0x00]

7	6	5	4	3	2	1	0
RST_REG	REST_MOD	CH_L_HIZ	CH_R_HIZ	MUTE_L	MUTE_R	CTRL_STATE	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit	Field	Type	Reset	Description
7	RST_REG	R/W	0	Register Reset 0: Normal 1: Reset Register
6	RST_MOD	R/W	0	Signal path Reset 0: Normal 1: Reset Signal path
5	CH_L_HIZ	R/W	0	Force Channel L's output driver into Hi-Z state 0: Normal State 1: Change L channel's output driver into Hi-Z state
4	CH_R_HIZ	R/W	0	Force Channel R's output driver into Hi-Z state 0: Normal State 1: Change R channel's output driver into Hi-Z state
3	MUTE_L	R/W	0	MUTE L Channel 0: Normal 1: Mute L Channel
2	MUTE_R	R/W	0	MUTE R Channel 0: Normal 1: Mute R Channel
1-0	CTRL_STATE	R/W	00	00: Digital Off 01: Analog off 10: Driver Off (Hiz) 11: Play

12.1.5 Register 5 PROCESSING_CTRL1 (Offset=5h) [Reset=0x12]

7	6	5	4	3	2	1	0
AGL_BP	DRB_BP	RESERVED		POST_EQ_BP	RESERVED	SUB_CH_BP	PROCESSING_BP
R/W	R/W	R		R/W	R	R/W	R/W

Bit	Field	Type	Reset	Description
7	AGL_BP	R/W	0	0: Enable AGL 1: Bypass AGL
6	DRB_BP	R/W	0	0: Enable DRB 1: Bypass DRB
5-4	RESERVED	R	0	This bit is reserved

Bit	Field	Type	Reset	Description
3	POST_EQ_BP	R/W	0	0: Enable Post-EQ 1: Bypass Post-EQ
2	RESREVED	R	0	This bit is reserved
1	SUB_CH_BP	R/W	1	0: Enable Sub Channel Processing 1: Bypass Sub Channel Processing
0	PROCESSING_BP	R/W	0	0: Enable audio effect tuning 1: Bypass all audio effect tuning

12.1.6 Register 6 PROCESSING_CTRL2 (Offset=6h) [Reset=0xF0]

7	6	5	4	3	2	1	0
RESERVED				POWER_SAVE_DOWN	PLL_CLK_DIV		REAL_96KHZ
R				R/W	R/W		R/W

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	1111	These bits are reserved
3	POWER_SAVE_DOWN	R/W	0	0: when have clock fault, device will not shut down analog and digital, only shut down driver 1: when have clock fault, device will shut down analog and digital and driver
2-1	PLL_CLK_DIV	R/W	0	00: high PLL frequency 01: middle PLL frequency 10: low PLL frequency 11: low PLL frequency
0	REAL_96KHZ	R/W	0	0: 48kHz internal processing 1: 96kHz internal processing

12.1.7 Register 7 I2S_DATA_FORMAT1 (Offset=7h) [Reset=0x02]

7	6	5	4	3	2	1	0
44K_INPUT	44K_EN	I2S_DATA_FORMATI		I2S_FSYNC_PULSE		I2S_WORD_LENGTH	
R/W	R/W	R/W		R/W		R/W	

Bit	Field	Type	Reset	Description
7	44K_INPUT	R/W	0	0: 48K/96K/192K input 1: 44.1K/88.2K/176.4K input
6	44K_EN	R/W	0	0: disable 44k input 1: enable 44k input
5-4	I2S_DATA_FORMAT	R/W	00	00: I2S 01: TDM/DSP 10: RTJ 11: LTJ

Bit	Field	Type	Reset	Description
3-2	I2S_FSYNC_PULSE	R/W	00	01: FSYNC pulse <8 BCLK. If the high width of LRCLK/FSYNC in TDM/DSP mode is less than 8 cycles of BCLK, these two bits need set to 01. Others: These bits are reserved
1-0	I2S_WORD_LENGTH	R/W	10	I2S Word length. These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

12.1.8 Register 8 I2S_DATA_FORMAT2 (Offset=8h) [Reset=0x00]

7	6	5	4	3	2	1	0
I2S_LEFT_BITS_SHIFT							
R/W							

Bit	Field	Type	Reset	Description
7-0	I2S_LEFT_BIT_SHIFT	R/W	00000000	Control the offset of Left Channel audio data in the audio frame for both input and output. The offset is defined as the number of BLCK from the starting (MSB) of audio frame to the starting of the desired audio sample. 00000000: offset = 0 BCLK (no offset) 00000001: offset = 1 BCLK …….. 11111111: offset = 256 BCLK

12.1.9 Register 9 I2S_DATA_FORMAT3 (Offset=9h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED							
R							

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	00000000	These bits are reseved.

12.1.10 Register 10 GPIO1_CTRL (Offset=0Ah) [Reset=0x29]

7	6	5	4	3	2	1	0
RESERVED		GPIO1_OE	GPIO1_FUNC_SEL				
R		R/W	R/W				

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5	GPIO1_OE	R/W	1	0: GPIO1 is input 1: GPIO1 is output
4-0	GPIO1_FUNC_SEL	R/W	01001	DEFAULT is SDOUT 0000: off(low) 0001: digital off 0010: analog off 0011: driver off 0100: mute right 0101: mute left 0110: clock invalid flag(clock error or clock missing) 0111: pll lock flag 1000: GPIO1 as WARNZ output 1001: serial audio interface data output(SDOUT) 1011: GPIO1 as FAULTZ output 1100: resetz

12.1.11 Register 11 GPIO2_CTRL (Offset=0Bh) [Reset=0x2B]

7	6	5	4	3	2	1	0
RESERVED		GPIO2_OE	GPIO1_FUNC_SEL				
R		R/W	R/W				

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5	GPIO2_OE	R/W	1	0: GPIO2 is input 1: GPIO2 is output
4-0	GPIO2_FUNC_SEL	R/W	01011	DEFAULT is FAULT pin 0000: off(low) 0001: digital off 0010: analog off 0011: driver off 0100: mute right 0101: mute left 0110: clock invalid flag(clock error or clock missing) 0111: pll lock flag

Bit	Field	Type	Reset	Description
				1000: gpio1 as WARNZ output 1001: serial audio interface data output(SDOUT) 1011: GPIO2 as FAULTZ output 1100: resetz

12.1.12 Register 12 GPIO1_FAULT_SEL (Offset=0Ch) [Reset=0xFF]

7	6	5	4	3	2	1	0
CLIP	OTW	OTSD	CLK_FAULT	PVDD_UV	PVDD_OV	DC	OC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	CLIP	R/W	1	0: Mask; 1: Report
6	OTW	R/W	1	0: Mask; 1: Report
5	OTSD	R/W	1	0: Mask; 1: Report
4	CLK_FAULT	R/W	1	0: Mask; 1: Report
3	PVDD_UV	R/W	1	0: Mask; 1: Report
2	PVDD_OV	R/W	1	0: Mask; 1: Report
1	DC	R/W	1	0: Mask; 1: Report
0	OC	R/W	1	0: Mask; 1: Report

12.1.13 Register 13 GPIO2_FAULT_SEL (Offset=0Dh) [Reset=0xFF]

7	6	5	4	3	2	1	0
CLIP	OTW	OTSD	CLK_FAULT	PVDD_UV	PVDD_OV	DC	OC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	CLIP	R/W	1	0: Mask; 1: Report
6	OTW	R/W	1	0: Mask; 1: Report
5	OTSD	R/W	1	0: Mask; 1: Report
4	CLK_FAULT	R/W	1	0: Mask; 1: Report
3	PVDD_UV	R/W	1	0: Mask; 1: Report
2	PVDD_OV	R/W	1	0: Mask; 1: Report
1	DC	R/W	1	0: Mask; 1: Report
0	OC	R/W	1	0: Mask; 1: Report

12.1.14 Register 14 SS_CTRL (Offset=0Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED						RDM_EN	TRI_EN
R						R/W	R/W

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	00000	These bits are reserved
1	RDM_EN	R/W	0	0: Random SS disable 1: Random SS enable
0	TRI_EN	R/W	0	0: Triangle SS disable 1: Triangle SS enable

12.1.15 Register 15 VOLUME_CTRL_L (Offset=0Fh) [Reset=0xD0]

7	6	5	4	3	2	1	0
VOL_L							
R/W							

Bit	Field	Type	Reset	Description
7-0	VOL_L	R/W	11010000	Volume control for left channel. 00000000: -104dB .... 11010000: 0dB 11010001: 0.5dB 11111111: 24dB

12.1.16 Register 16 VOLUME_CTRL_R (Offset=10h) [Reset=0xD0]

7	6	5	4	3	2	1	0
VOL_R							
R/W							

Bit	Field	Type	Reset	Description
7-0	VOL_R	R/W	11010000	Volume control for left channel. 00000000: -104dB .... 11010000: 0dB 11010001: 0.5dB 11111111: 24dB

12.1.17 Register 17 MISC_CTRL (Offset=11h) [Reset=0xA3]

7	6	5	4	3	2	1	0
RESERVED					OTSD_AUTO_REC	GPIO2_FAULT_LATCH	GPIO1_FAULT_LATCH
R					R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	10	These bits are reserved
5		R/W	1	0: Disable CBC 1: Enable CBC
2	OTSD_AUTO_REC	R/W	0	0: OT auto-recovery disable 1: OT auto-recovery enable
1	GPIO2_FAULT_LATCH	R/W	1	0: GPIO2 report fault not latched 1: GPIO2 report fault latched
0	GPIO1_FAULT_LATCH	R/W	1	0: GPIO1 report fault not latched 1: GPIO1 report fault latched

12.1.18 Register 18 I2S_CLK_FORMAT_RPT1 (Offset=12h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED		BCLK_RATIO_HIGH		FS_DET			
R		R		R			

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5-4	BCLK_RATIO_HIGH	R	00	These bits indicate the BCLK ratio, the number of BCLK in one audio frame. BCLK=32FS-512FS MSB Bit [9-8].
3-0	FS_DET	R	0000	These bits indicate the currently detected audio sample rate. 0110: 32KHZ 1000: 44.1KHZ 1001: 48KHZ 1010: 88.2KHZ 1011: 96KHZ 1100: 176.4KHZ 1101: 192KHZ

12.1.19 Register 19 I2S_CLK_FORMAT_RPT2 (Offset=13h) [Reset=0x00]

7	6	5	4	3	2	1	0
BCLK_RATIO							
R							

Bit	Field	Type	Reset	Description
7-0	BCLK_RATIO	R	00000000	These bits indicate the BCLK ratio, the number of BCLK in one audio frame. 00000000: 00000001: … 11111111:

12.1.20 Register 20 DIEID_RPT (Offset=15h) [Reset=0x00]

7	6	5	4	3	2	1	0
DIEID_RPT							
R							

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	00000000	DIE ID

12.1.21 Register 21 STATE_RPT (Offset=16h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED						STATE_RPT	
R						*R*	

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	These bits are reserved
1-0	STATE_RPT	R	00	00: Digital Off 01: Analog Off 10: Driver Off (Hiz) 11: Play

12.1.22 Register 22 FAULT_RPT1(Offset=17h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED	OTSD	PVDD_OV	PVDD_UV	CH2_DC	CH1_DC	CH2_OC	CH1_OC
R	R	R	R	R	R	R	R

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	This bit is reserved
6	OTSD	R	0	0: Normal 1: Over temperature shutdown fault report
5	PVDD_OV	R	0	0: Normal 1: PVDD over-voltage fault report
4	PVDD_UV	R	0	0: Normal 1: PVDD under-voltage fault report
3	CH2_DC	R	0	0: Normal 1: CH2 speaker DC fault report
2	CH1_DC	R	0	0: Normal 1: CH1 speaker DC fault report
1	CH2_OC	R	0	0: Normal 1: CH2 over-current fault report
0	CH1_OC	R	0	0: Normal 1: CH1 over-current fault report

12.1.23 Register 23 FAULT_RPT2(Offset=18h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED					CLK_FAULT	RESERVED	
R					R	R	

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000	This bit is reserved
2	CLK_FAULT	R	0	0: Normal 1: Clock fault report
1-0	RESERVED	R	0	This bit is reserved

12.1.24 Register 24 FAULT_RPT3(Offset=19h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED					CH2_CLIP	CH1_CLIP	OTW
R					R	R	R

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000	This bit is reserved
2	CH2_CLIP	R	0	0: Normal 1: Channel 2 clipping
1	CH1_CLIP	R	0	0: Normal 1: Channel 1 clipping
0	OTW	R	0	0: Normal 1: Over temperature warning

12.1.25 Register 25 XOR_CHECKSUM(Offset=7Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
XOR_CHECKSUM							
R							

Bit	Field	Type	Reset	Description
7-0	XOR_CHECKSUM	R	0	XOR checksum result

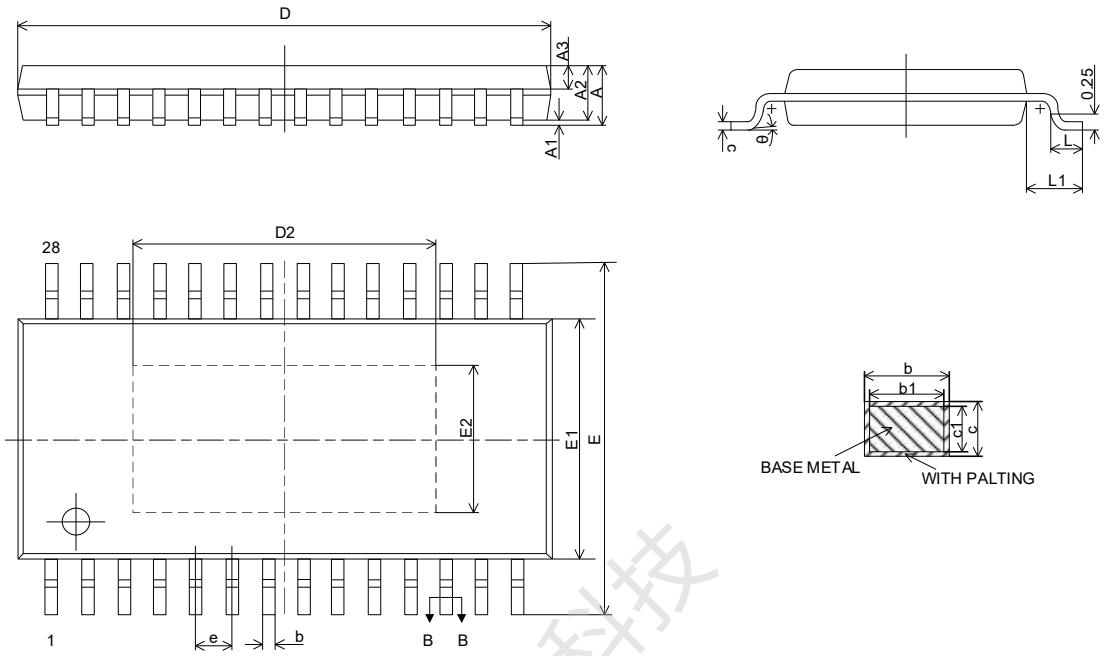
12.1.26 Register 26 CRC_CHECKSUM(Offset=7Fh) [Reset=0x00]

7	6	5	4	3	2	1	0
CRC_CHECKSUM							
R							

Bit	Field	Type	Reset	Description
7-0	CRC_CHECKSUM	R	0	CRC checksum result

14. Package Dimensions

Orderable Device	Package Type	MPQ	MOQ	Eco Plan	MSL Level	Device Marking
ACM8628M	TSSOP28 Tape and Reel	3000	3000	RoHS Compliant Lead-Free Finish	MSL3	ACM8628M



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	_	_	1.20
A1	0.05	_	0.15
A2	0.80	_	1.00
A3	0.39	0.44	0.49
b	0.20	_	0.29
b1	0.19	0.22	0.25
c	0.13	_	0.18
c1	0.12	0.13	0.15
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	_	8°

L/F 载体尺寸 (mil)	D2	E2
232*118	5.50REF	2.70REF