ACPL-M46T

Automotive Intelligent Power Module
with R²Coupler™ Isolation and Small Outline, 5 Lead Package

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

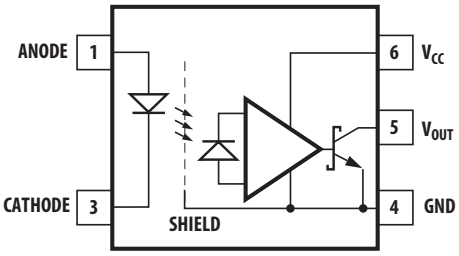
Description

The ACPL-M46T consists of a AlGaAs optically coupled to an integrated high gain photodetector. Minimized propagation delay difference between devices make these optocouplers excellent solutions for improving automotive inverter efficiency through reduced switching dead time.

Specification and performance plots are given for typical IPM applications.

Avago R²Coupler isolation products provide the reinforced insulation and reliability needed for critical in automotive and high temperature industrial applications.

Schematic Diagram



Truth Table

LED	V_O
ON	L
OFF	H

The connection of a 0.1 µF bypass capacitor between pins 4 and 6 is recommended.

Features

- Performance specified for common IPM applications over automotive temperature range: -40°C to 125°C
- Fast maximum propagation delays
  - t_{PHL} & t_{PLH} = 550 ns
- Minimized Pulse Width Distortion (PWD = 370 ns)
- Very high Common Mode Rejection (CMR): 15 kV/µs at V_{CM} = 1500 V
- CTR > 44% at I_F = 10 mA
- Qualified to AEC-Q100 Test Guidelines
- Safety approval
  - UL recognized per UL1577 (file no. E55361) 4000 V_{rms} for 1 minute
  - IEC/EN/DIN EN 60747-5-2 Approved
  - CSA Approved

Applications

- Automotive IPM isolation for battery management system and motor control
- Isolated IGBT/MOSFET gate drive
- AC and brushless dc motor drives
- Industrial inverters for power supplies and motor controls

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

Part Number	Option (RoHS) Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
ACPL-M46T	-000E	SO-5	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-M46T-500E t o or der pr oduct of SO -5 Sur face M ount pack age in Tape and Reel pack aging with RoHS compliant.

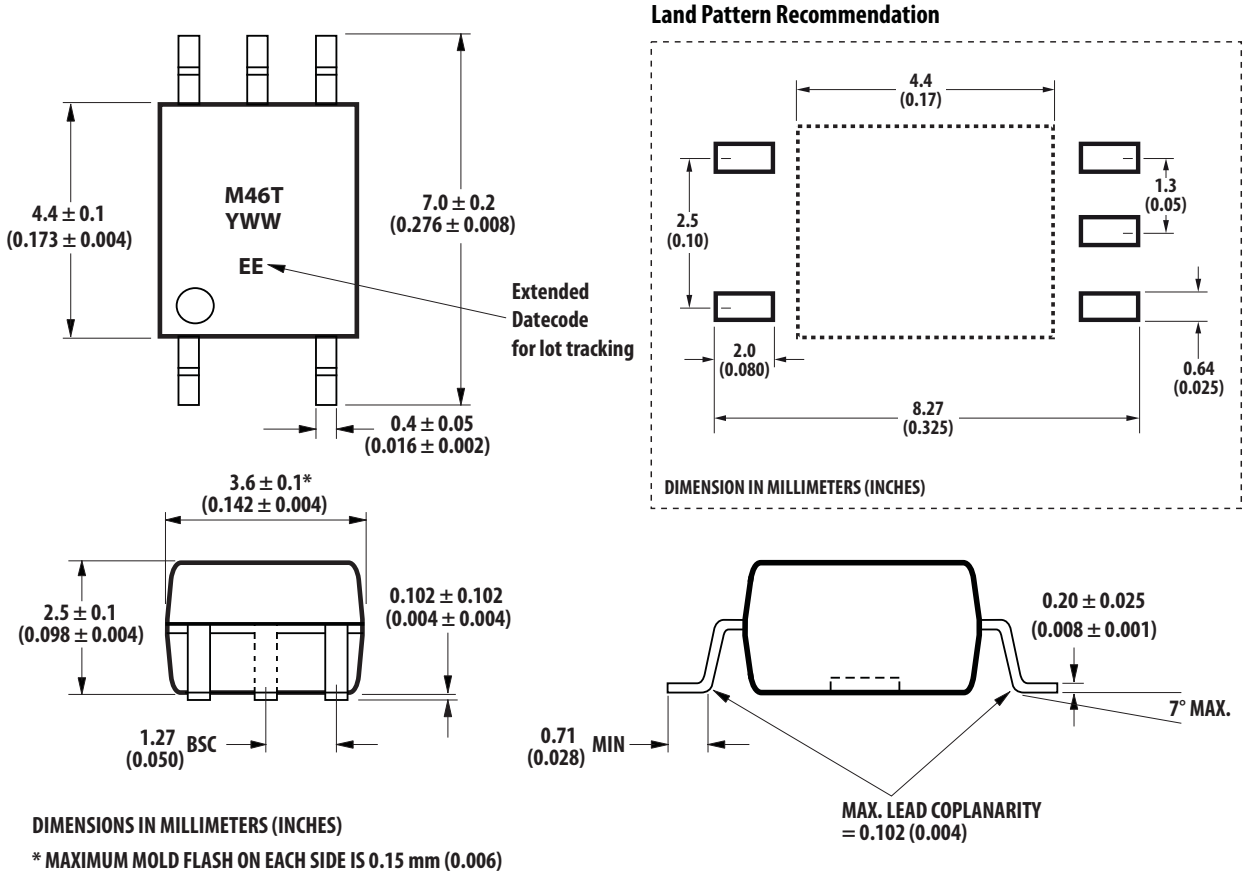
Example 2:

ACPL-M46T-000E to order product of SO-5 Surface Mount package in tube packaging with RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawing

ACPL-M46T-000E Small Outline SO-5 Package (JEDEC MO-155)



DIMENSIONS IN MILLIMETERS (INCHES)

* MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 mm (0.006)

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Note: Non-halide flux should be used

Regulatory Information

The ACPL-M46T is approved by the following organizations:

UL

Approved under UL 1577, component recognition program up to V_{ISO} = 4000 V_{RMS}

CSA

Approved under CSA Component Acceptance Notice #5.

IEC/EN/DIN EN 60747-5-2

Approved under:
IEC 60747-5-2:2007
EN 60747-5-2:2001 + A1
DIN EN 60747-5-2 (VDE 0884 Teil 2)

IEC/EN/DIN EN 60747-5-2 Insulation Characteristics*

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 Vrms		I – III	
for rated mains voltage ≤ 600 V_{rms}		I – II	
Climatic Classification		55/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1063	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	>109	W

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	≥5	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	≥5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (ComparativeTracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	150	°C
Operating Temperature	T_A	-40	125	°C
Average Input Current	$I_{F(avg)}$		20	mA
Peak Input Current (50% duty cycle, <1 ms pulse width)	$I_{F(peak)}$		40	mA
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(tran)}$		1.0	A
Reverse Input Voltage (Pin 3-1)	V_R		5	Volts
Average Output Current (Pin 5)	$I_{O(avg)}$		15	mA
Output Voltage (Pin 5-4)	V_O	-0.5	30	Volts
Supply Voltage (Pin 6-4)	V_{CC}	-0.5	30	Volts
Output Power Dissipation	P_O		100	mW
Total Power Dissipation	P_T		130	mW
Infrared and Vapor Phase Reflow Temperature	See Reflow Thermal Profile below.			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	30	Volts
Output Voltage	V_O	0	30	Volts
Input Current (ON)	$I_{F(on)}$	10	20	mA
Input Voltage (OFF)	$V_{F(off)}$	-5	0.8	V
Operating Temperature	T_A	-40	125	°C

Electrical Specifications

Over recommended operating conditions unless otherwise specified:
T_A = -40°C to +125°C, V_{CC} = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	44	90		%	I_F = 10 mA, V_O = 0.6 V		1
Low Level Output Current	I_{OL} 4.4		9.0		mA	I_F = 10 mA, V_O = 0.6 V	2,3	
Low Level Output Voltage	V_{OL}		0.3	0.6	V	I_O = 2.4 mA		
Input Threshold Current	I_{TH}		1.5	5.0	mA	V_O = 0.8 V, I_O = 0.75 mA	2	4
High Level Output Current	I_{OH}		5	50	µA	V_F = 0.8 V	4	
High Level Supply Current	I_{CCH}		0.6	1.3	mA	V_F = 0.8 V, V_O = Open		4
Low Level Supply Current	I_{CCL}		0.6	1.3	mA	I_F = 10 mA, V_O = Open		4
Input Forward Voltage	V_F 1.45		1.5	1.75	V	T_A = 25°C , I_F = 10 mA	5	
		1.25	1.5	1.85	V	I_F = 10 mA		
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.5		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R 5				V	I_R = 10 µA		
Input Capacitance	C_{IN}		90		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Voltage	V_{ISO} 4000				V_{RMS}	RH < 50%, t = 1 min, T_A = 25°C		2, 3
Resistance (Input - Output)	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 Vdc	6	
Capacitance (Input - Output)	C_{I-O}		0.6		pF	f = 1 MHz	6	

*All typical values at 25°C, V_{CC} = 15 V.

Switching Specifications (R_L= 20 kΩ)

Over recommended operating conditions unless otherwise specified:
T_A = -40°C to +125°C, V_{CC} = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Low Output Level	t_{PHL}	30	200	550	ns	C_L = 100 pF	$I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8 V, V_{CC} = 15.0 V, V_{THLH} = 2.0 V, V_{THHL} = 1.5 V	6, 8-12	4, 5
		100			ns	C_L = 10 pF			
Propagation Delay Time to High Output Level	t_{PLH}	270	400	550	ns	C_L = 100 pF			
		130				C_L = 10 pF			
Pulse Width Distortion	PWD		200	450	ns	C_L = 100 pF			9
Propagation Delay Difference Between Any 2 Parts	t_{PLH}-t_{PHL}	-150	50	200	450	ns			6
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15		30		kV/µs	I_F = 0 mA, V_O > 11.0 V	V_{CC} = 15.0 V, C_L = 100 pF, V_{CM} = 1500 V_{P-P}, T_A = 25°C	7	7
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15		30		kV/µs	I_F = 10 mA, V_O < 1.0 V			8

*All typical values at 25°C, V_{CC} = 15 V.

Notes:
1. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current (I_O) to the forward LED input current (I_F) times 100.
2. Device considered a two-terminal device: Pins 1 and 3 shorted together and Pins 4, 5 and 6 shorted together.
3. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4800 V_{RMS} for 1 second.
4. Pulse: f = 20 kHz, Duty Cycle = 10%.
5. Use of a 0.1 µF bypass capacitor connected between pins 4 and 6 can improve performance by filtering power supply line noise.
6. The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)
7. Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 11.0 V).
8. Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 1.0 V).
9. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.

LED Drive Circuit Considerations For Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 14. The ACPL-M46T improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and the optocoupler output pin and output ground as shown in Figure 15. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 13), can achieve 15 kV/µs CMR while minimizing component complexity. Note that a CMOS gate is recommended in Figure 13 to keep the LED off when the gate is in the high state.

Another cause of CMR failure for a shielded optocoupler is direct coupling to the optocoupler output pins through C_{LEDO1} in Figure 15. Many factors influence the effect and magnitude of the direct coupling including: the position of the LED current setting resistor and the value of the capacitor at the optocoupler output (C_L).

Techniques to keep the LED in the proper state and minimize the effect of the direct coupling are discussed in the next two sections.

CMR with the LED on (CMRL)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. The recommended minimum LED current of 10 mA provides adequate margin over the maximum I_{TH} of 4.0 mA (see Figure 2) to achieve 15 kV/µs CMR.

The placement of the LED current setting resistor effects the ability of the drive circuit to keep the LED on during transients and interacts with the direct coupling to the optocoupler output. For example, the LED resistor in Figure 16 is connected to the anode. Figure 17 shows the AC equivalent circuit for Figure 16 during common mode transients. During a $+dV_{CM}/dt$ in Figure 17, the current available at the LED anode (Itotal) is limited by the series resistor. The LED current (I_F) is reduced from its DC value by an amount equal to the current that flows through C_{LEDP} and C_{LEDO1}. The situation is made worse because the current through C_{LEDO1} has the effect of trying to pull the output high (toward a CMR failure) at the same time the LED current is being reduced. For this reason, the recommended LED drive circuit (Figure 13) places the current setting resistor in series with the LED cathode. Figure 18 is the AC equivalent circuit for Figure 13 during common mode transients. In this case, the LED current is not reduced during a $+dV_{CM}/dt$ transient because the current flowing through the package capacitance is supplied by the power supply. During a dV_{CM}/dt transient, however, the LED current is reduced by the amount of current flowing through CLEDN. But, better CMR performance is achieved since the current flowing in C_{LEDO1} during a negative transient acts to keep the output low.

CMR with the LED Off (CMRH)

A high CMR LED drive circuit must keep the LED off ($V_F \le V_{F(OFF)}$) during common mode transients. For example, during a $+dV_{CM}/dt$ transient in Figure 18, the current flowing through C_{LEDN} is supplied by the parallel combination of the LED and series resistor. As long as the voltage developed across the resistor is less than $V_{F(OFF)}$ the LED will remain off and no common mode failure will occur. Even if the LED momentarily turns on, the 100 pF capacitor from pins 5-4 will keep the output from dipping below the threshold. The recommended LED drive circuit (Figure 13) provides about 10 V of margin between the lowest optocoupler output voltage and a 3 V IPM threshold during a 15kV/µs transient with V_{CM} = 1500 V. Additional margin can be obtained by adding a diode in parallel with the resistor, as shown by the dashed line connection in Figure 18, to clamp the voltage across the LED below $V_{F(OFF)}$.

Since the open collector drive circuit, shown in Figure 19, cannot keep the LED off during a $+dV_{CM}/dt$ transient, it is not desirable for applications requiring ultra high CMRH performance. Figure 20 is the AC equivalent circuit for Figure 19 during common mode transients. Essentially all the current flowing through CLEDN during a $+dV_{CM}/dt$ transient must be supplied by the LED. CMRH failures can occur at dv/dt rates where the current through the LED and CLEDN exceeds the input threshold. Figure 21 is an alternative drive circuit which does achieve ultra high CMR performance by shunting the LED in the off state.

IPM Dead Time and Propagation Delay Specifications

The ACPL-M46T includes a Propagation Delay Difference specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 22) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time the designer must consider the propagation delay characteristics of the optocoupler as well as the characteristics of the IPM IGBT gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the IPM IGBT gate drive circuit can be analyzed in the same way) it is important to know the minimum and maximum turn-on (t_{PHL}) and turn-off (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range.

The limiting case of zero dead time occurs when the input to Q1 turns off at the same time that the input to Q2 turns on. This case determines the minimum delay between LED1 turn-off and LED turn-on, which is related to the worst case optocoupler propagation delay waveforms, as shown in Figure 23. A minimum dead time of zero is achieved in Figure 23 when the signal to turn on LED is delayed by ($t_{PLH\ max}$ - $t_{PHL\ min}$) from the LED1 turn off. Note that the propagation delays used to calculate PDD are taken at equal temperatures since the optocouplers under consideration are typically mounted in close proximity to each other. (Specifically, $t_{PLH\ max}$ and $t_{PHL\ min}$ in the previous equation are not the same as the $t_{PLH\ max}$ and $t_{PHL\ min}$, over the full operating temperature range, specified in the data sheet.) This delay is the maximum value for the propagation delay difference specification which is specified at 370 ns for the ACPL-M46T over an operating temperature range of -40°C to 125°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time occurs in the highly unlikely case where one optocoupler with the fastest t_{PLH} and another with the slowest t_{PHL} are in the same inverter leg. The maximum dead time in this case becomes the sum of the spread in the t_{PLH} and t_{PHL} propagation delays as shown in Figure 24. The maximum dead time is also equivalent to the difference between the maximum and minimum propagation delay difference specifications. The maximum dead time (due to the optocouplers) for the ACPL-M46T is 520 ns (= 370 ns - (-150 ns)) over an operating temperature range of -40°C to 125°C.

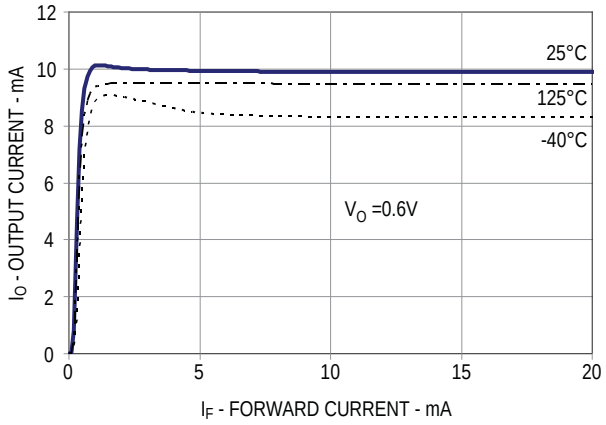


Figure 2. Typical Transfer Characteristics.

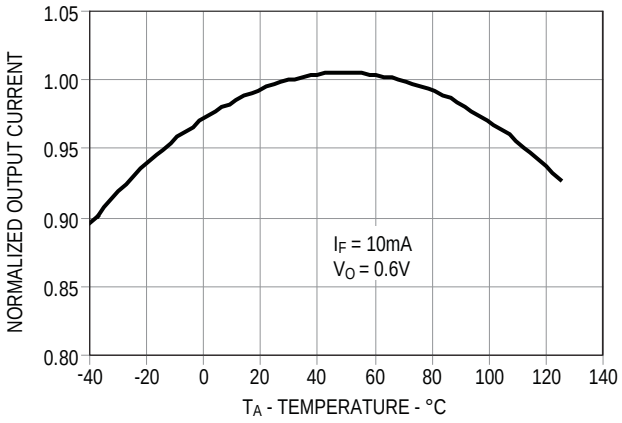


Figure 3. Normalized Output Current vs. Temperature.

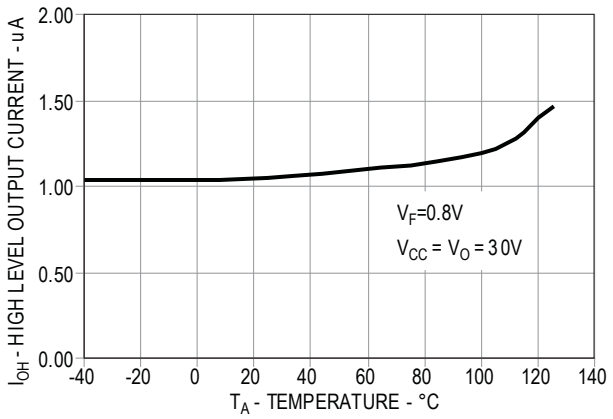


Figure 4. High Level Output Current vs. Temperature.

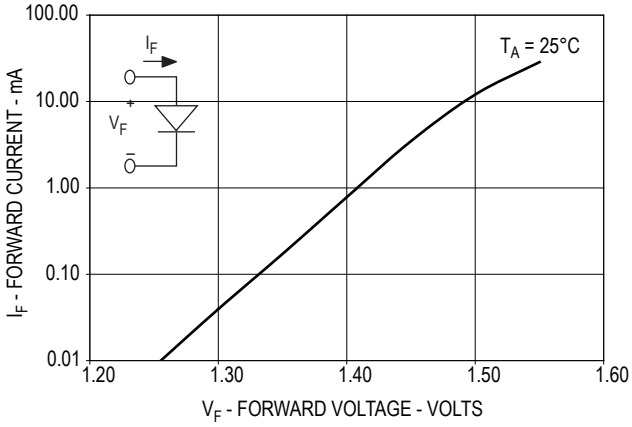
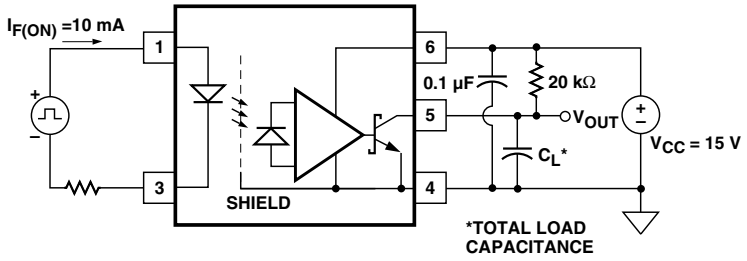


Figure 5. Input Current vs. Forward Voltage.



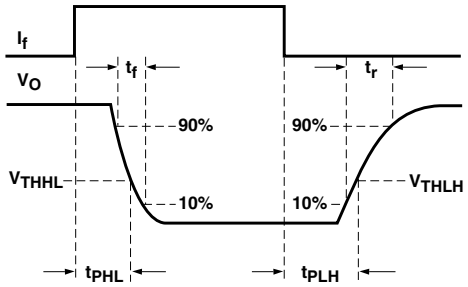
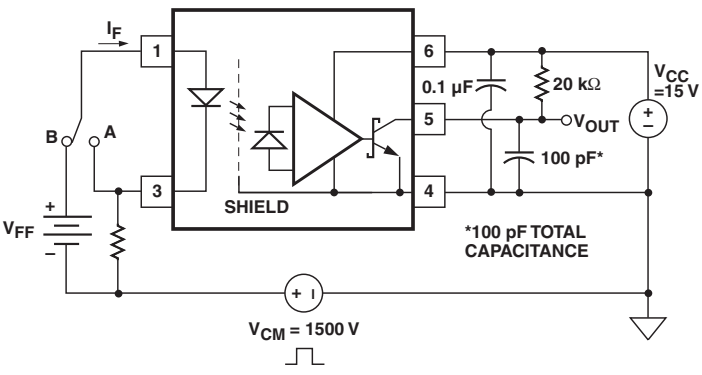
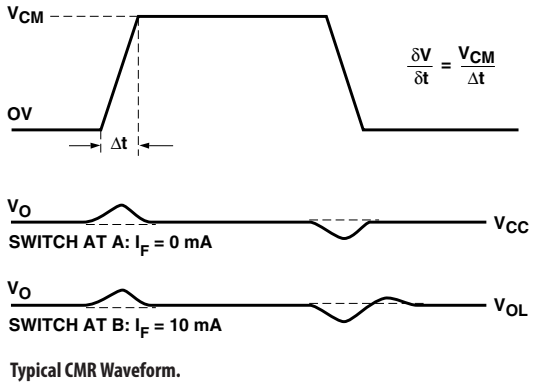


Figure 6. Propagation Delay Test Circuit.





Typical CMR Waveform.

Figure 7. CMR Test Circuit.

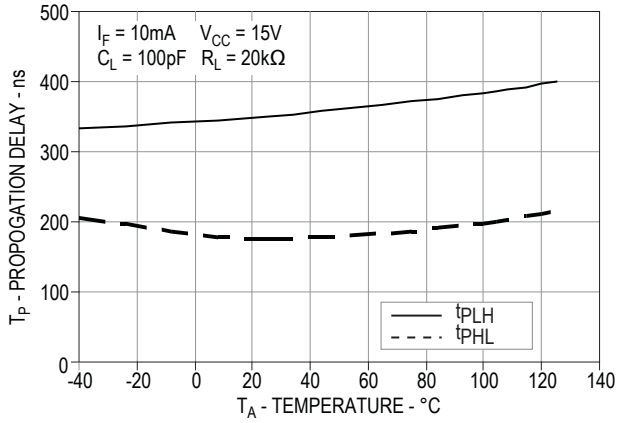


Figure 8. Propagation Delay with External 20 kΩ RL vs. Temperature.

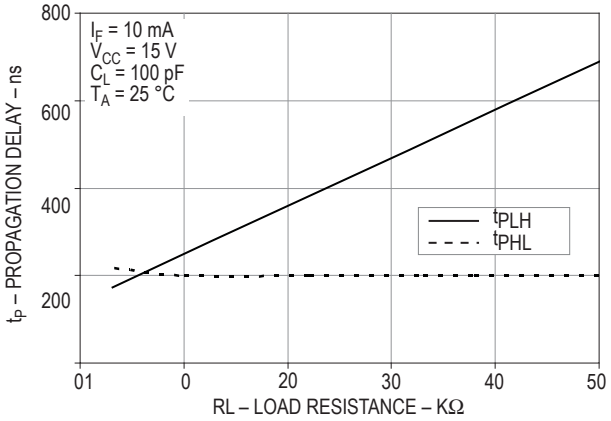


Figure 9. Propagation Delay vs. Load Resistance.

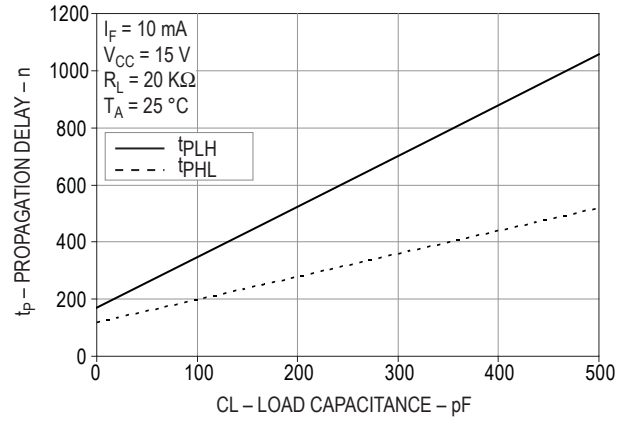


Figure 10. Propagation Delay vs. Load Capacitance.

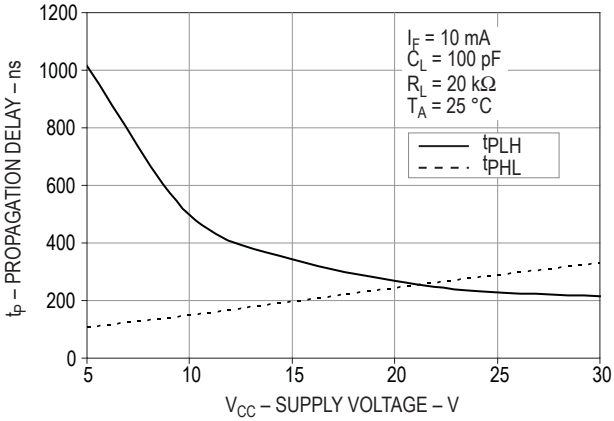


Figure 11. Propagation Delay vs. Supply Voltage.

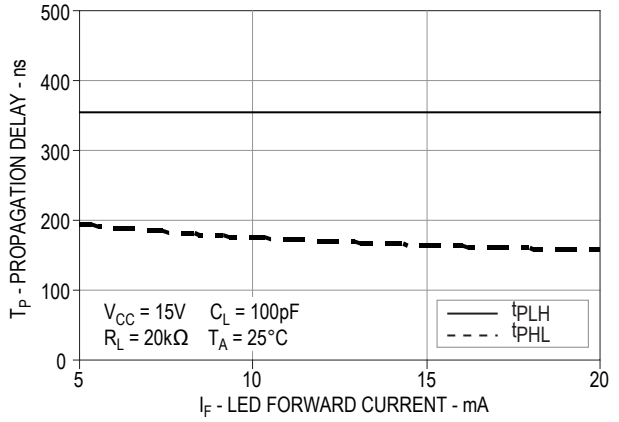


Figure 12. Propagation Delay vs. Input Current.

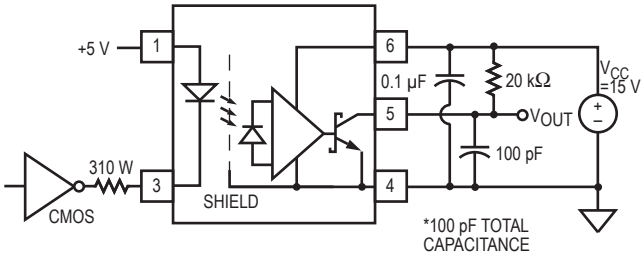


Figure 13. Recommended LED Drive Circuit.

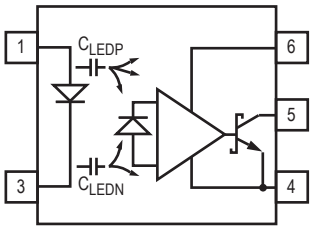


Figure 14. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

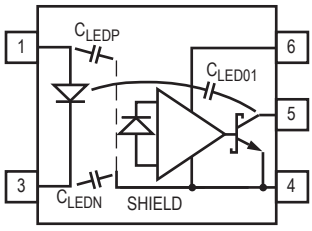


Figure 15. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

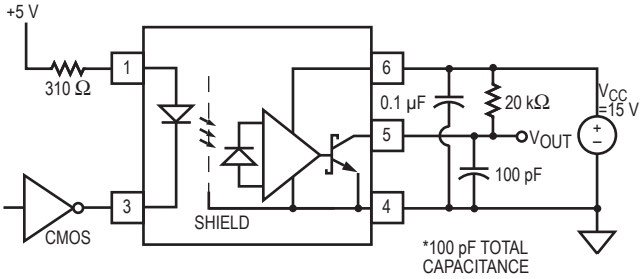


Figure 16. LED Drive Circuit with Resistor Connected to LED Anode (Not Recommended).

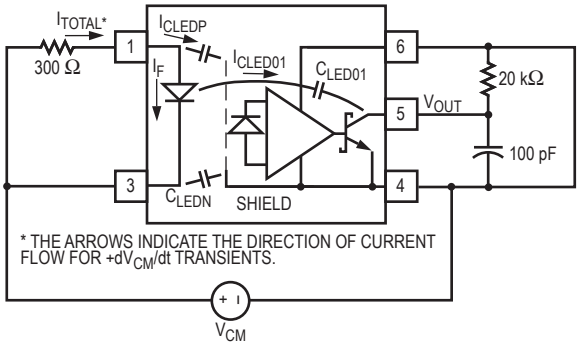


Figure 17. AC Equivalent Circuit for Figure 16 during Common Mode Transients.

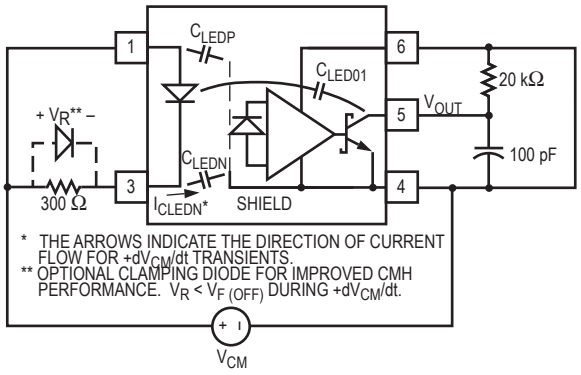


Figure 18. AC Equivalent Circuit for Figure 13 during Common Mode Transients.

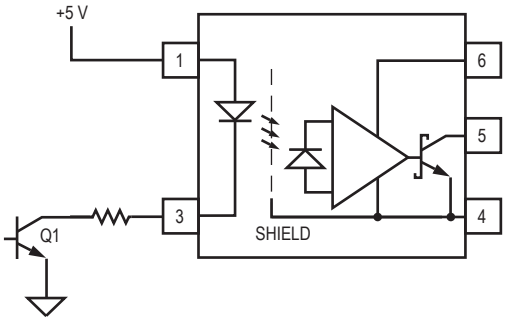


Figure 19. Not Recommended Open Collector LED Drive Circuit.

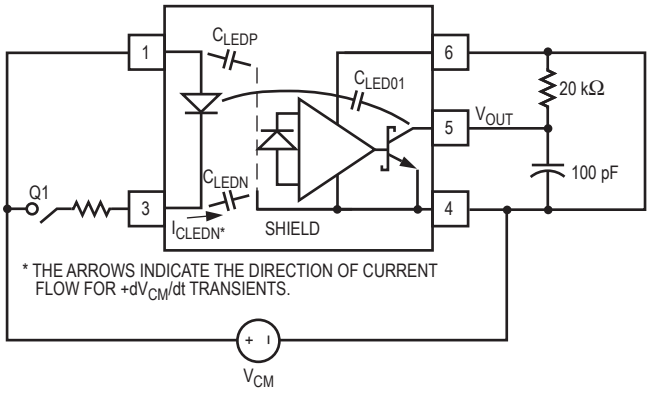


Figure 20. AC Equivalent Circuit for Figure 19 during Common Mode Transients.

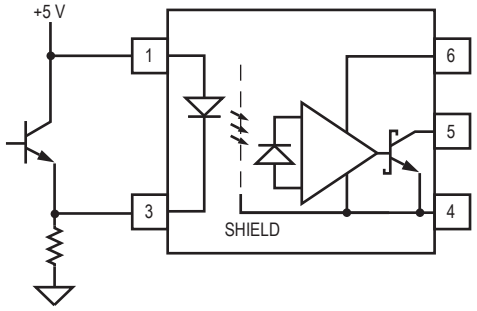


Figure 21. Recommended LED Drive Circuit for Ultra High CMR.

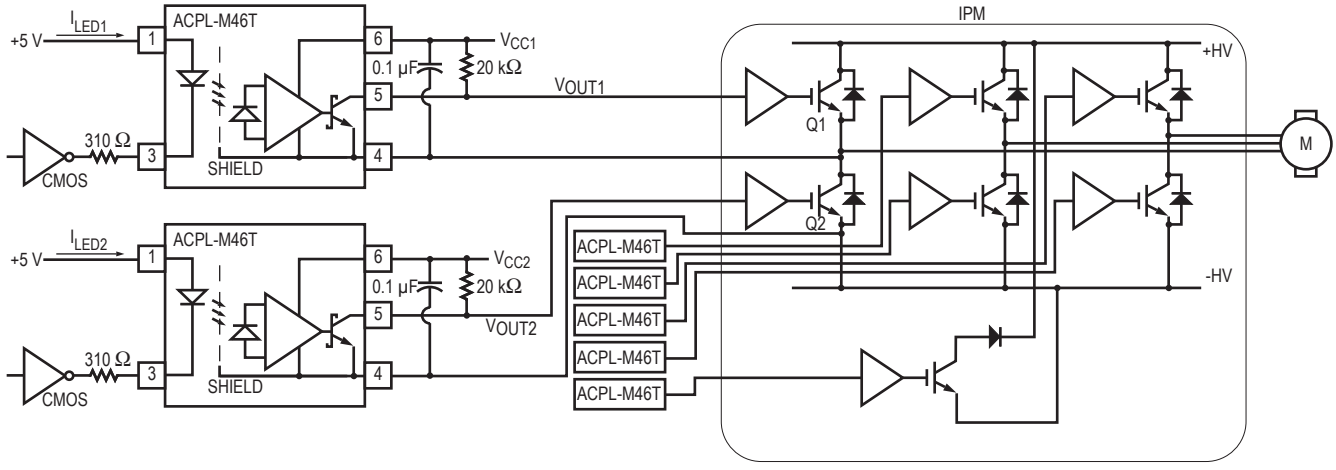
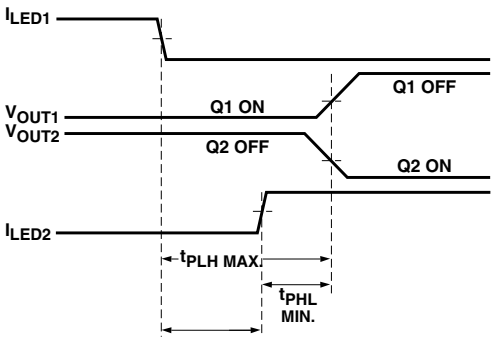


Figure 22. Typical Application Circuit.

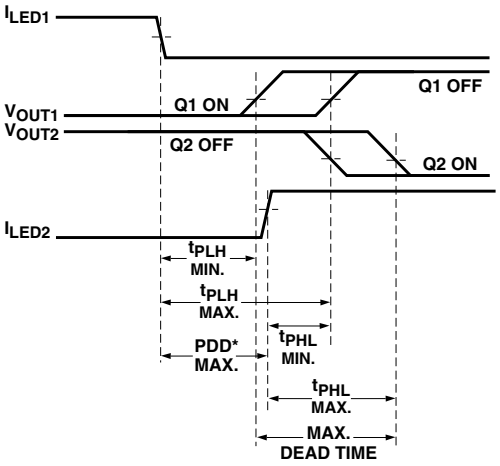


PDD* MAX. =
$(t_{PLH}-t_{PHL})$ MAX. = t_{PLH} MAX. - t_{PHL} MIN.

*PDD = PROPAGATION DELAY DIFFERENCE

NOTE: THE PROPAGATION DELAYS USED TO CALCULATE PDD ARE TAKEN AT EQUAL TEMPERATURES.

Figure 23. Minimum LED Skew for Zero Dead Time.



MAXIMUM DEAD TIME (DUE TO OPTOCOUPLER)
= $(t_{PLH\ MAX.} - t_{PLH\ MIN.}) + (t_{PHL\ MAX.} - t_{PHL\ MIN.})$
= $(t_{PLH\ MAX.} - t_{PHL\ MIN.}) - (t_{PLH\ MIN.} - t_{PHL\ MAX.})$
= PDD* MAX. - PDD* MIN.

*PDD = PROPAGATION DELAY DIFFERENCE

NOTE: THE PROPAGATION DELAYS USED TO CALCULATE THE MAXIMUM DEAD TIME ARE TAKEN AT EQUAL TEMPERATURES.

Figure 24. Waveforms for Deadtime Calculation.

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