ACPM-5251

4x5 UMTS Band I & Band V Dual-Band Power Amplifier Module with Integrated Coupler

Data Sheet

Description

The ACPM-5251 is the dual-band power amplifier module with integrated directional coupler designed for UMTS Band 1 and Band 5 uplink transmission in the mobile handsets, data cards or dongles supporting WCDMA and/or HSPA. This product has been designed, tested and characterized to the stringent spectral linearity and other requirements of the 3GPP standards including the HSDPA, HSUPA and HSPA+ UL transmission while keeping the key emphasis on the excellent PAE over the entire power range, i.e. the exceptional average power consumption and talk-time.

The ACPM-5251 contains all of the input and output matching networks, Vcc decoupling/bypass capacitors, RF input & output DC blocking capacitors as well as the daisy-chained directional coupler integrated into the module substrate PCB, all in a single 14-pad surface-mount leadless package with 4x5 mm from factor and 1mm thickness.

The integrated directional coupler has a single coupled-out port and is daisy-chained between the both bands with internally 50Ω-terminated isolation port. It also has excellent coupler directivity in both bands allowing small coupled out power variation or delivered power variation caused by the load mismatch from the antenna. The coupler directivity, i.e. the power variation into the mismatched load is critical to the TRP performance of the mobile phones in the real operation as well as the spec. compliance test.

The ACPM-5251 features CoolPAM-5 circuit technology which supports 3 power/gain modes – active bypass (low power), mid power, and high power modes. CoolPAM is the stage bypass technology that enables very lower power consumption especially in the low and mid output power ranges. The active bypass technology added in the CoolPAM-5 further enhances the PAE at low output power range together with the exceptionally low quiescent current. It dramatically saves the average power consumption extending the talk time of the phones and battery life of the other mobile data devices even much longer.

The ACPM-5251 has integrated on-chip Vref and on-module bias switch as the one of the key features of the CoolPAM-5, so the external Vref is not required eliminating the external LDO regulators and switches from the circuit boards of the mobile devices. It also makes the PA fully digital-controllable by the Ven pin that simply turns the PA on and off from the digital control logic inputs

Features

- UMTS Band 1 and Band 5 dual-band PA
- Integrated directional coupler (daisy-chained between both bands with single coupled out port and internally terminated isolation port)
- High directivity (small coupled power or delivered power variation into mismatched load)
- 3-mode power/gain control (active bypass, mid power, and high power modes)
- Excellent PAE in low and mid power ranges.
- 3.5mA quiescent current in active bypass (low-power) mode
- Excellent average power consumption and talk-time
- Spectral linearity supporting HSDPA, HSUPA, and HSPA+
- Internally matched 50Ω RF input & output ports
- Internal RF input & output DC blocking capacitors
- Internal Vcc bypass capacitors
- Internal Vref eliminating external LDO regulators and switches
- 1.8V CMOS compatible control logics (VH=1.35V~3.1V)
- 4 x 5 x 1mm 14-pad leadless surface-mount package
- Lead-free, RoHS compliant, Halogen-free, Sb-free, Green

Applications

- UMTS Band 1 and Band 5 Uplink Transmission in WCDMA / HSDPA / HSUPA / HSPA+ handsets, data cards and dongles

Ordering Information

Part Number	Number of Devices	Container
ACPM-5251-TR1	1000	7"Tape/Reel
ACPM-5251-BLK	100	Bulk

Description (Cont.)

from the baseband chipsets. All of the digital control input pins such as the Ven, Vmode and Vbp are fully CMOS compatible down to the 1.8V logic and all they needs just several uA of current drawn per pin to be driven.

The CoolPAM series of power amplifiers are manufactured on an advanced InGaP HBT technology offering excellent performance, temperature stability, ruggedness, and reliability.

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Absolute Maximum Ratings

– Stresses in excess of the absolute ratings may cause permanent damage. Exposure to absolute ratings for extended periods of time may adversely affect reliability. Functional operation is not implied under these conditions.

Description	Condition	Min	Nominal	Max	Unit	Associated Pins
DC Supply Voltage (Vcc)	RF Off, All Modes, Z_S=Z_L=50Ω	–	–	+6.0	V	Vcc1, Vcc2
	RF On, All Modes, Z_S=Z_L=50Ω	–	–	+4.5	V	Vcc1, Vcc2
Enable Control Voltage (Ven_LB, Ven_HB)		–	–	+3.3	V	Ven_LB, Ven_HB
Mode Control Voltage (Vmode)		–	–	+3.3	V	Vmode
Bypass Control Voltage (Vbp)		–	–	+3.3	V	Vbp
RF Input Power (Pin)	HPM, Z_S=Z_L=50Ω MPM, Z_S=Z_L=50Ω BPM, Z_S=Z_L=50Ω	– – –	– – –	+10 +6 +6	dBm dBm dBm	RFin_LB, RFin_HB
Revere RF Power injected into RF Output Port (Por)	B5, PDM, GMSK 25% Duty Cycle B1, PDM, GMSK 25% Duty Cycle	– –	– –	+31 +29	dBm dBm	RFout_LB RFout_HB
Storage Temperature (Tstg)		-55	–	+125	°C	

Recommended Operating Condition

Description		Min	Nominal	Max	Unit
DC Supply Voltage (Vcc)		3.2	3.4	4.2	V
Enable Control Voltage (Ven_LB, Ven_HB)	V_{LOW} V_{HIGH}	0 1.35	0 1.8	0.5 3.1	V V
Enable Control Current (Ien_LB, Ien_HB)		–	–	0.1	mA
Mode & Bypass Control Voltage (Vmode, Vbp)	V_{LOW} V_{HIGH}	0 1.35	0 1.8	0.5 3.1	V V
Mode & Bypass Control Current (Imode, Ibp)		–	–	0.1	mA
Operating Frequency (fc)	Band 5 Band 1	824 1920	– –	849 1980	MHz MHz
Case Temperature (Tc)		-20	+25	+85	°C

Operating Logic Table

Selected Band & Power Mode	Vcc1 / Vcc2	Ven_LB	Ven_HB	Vmode	Vbp
LB (B5) HPM (High-Power Mode)	On	High	Low	Low	X
LB (B5) MPM (Mid-Power Mode)	On	High	Low	High	Low
LB (B5) BPM (Bypass Power Mode)	On	High	Low	High	High
HB (B1) HPM (High-Power Mode)	On	Low	High	Low	X
HB (B1) MPM (Mid-Power Mode)	On	Low	High	High	Low
HB (B1) BPM (Bypass Power Mode)	On	Low	High	High	High
PDM (Power Down Mode)	On	Low	Low	X	X

* BPM (Bypass Modes) = Active Bypass Mode / Low Power Mode

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Electrical Characteristics

– Conditions: Vcc=3.4V, Ta=25°C, $Z_{SOURCE} = Z_{LOAD} = 50\Omega$
– Signal Configuration : 3GPP UL RMC 12.2kbps (WCDMA R'99) unless specified otherwise

Band 5

Characteristics	Condition	Min	Typ	Max	Unit
Operating Frequency Range		824	–	849	MHz
Max. Linear Output Power	HPM, WCDMA (CM=0 / MPR=-1dB) HPM, HSDPA MPR=0dB HPM, HSUPA MPR=0dB	27.5 26.5 26.0	– – –	– – –	dBm
	MPM, WCDMA (CM=0 / MPR=-1dB) MPM, HSPA MPR=0dB	18.0 17.0	– –	– –	dBm
	BPM, WCDMA (CM=0 / MPR=-1dB) BPM, HSPA MPR=0dB	12.0 11.0	– –	– –	dBm
Gain	HPM, Pout=27.5dBm	24	27.8	31	dB
	MPM, Pout=18.0dBm	14	17.8	22	dB
	BPM, Pout=12.0dBm	8	12.6	16	dB
PAE	HPM, Pout=27.5dBm	34.8	39.0	–	%
	MPM, Pout=18.0dBm	18.3	23.1	–	%
	BPM, Pout=12.0dBm	9.8	13.8		%
Total Supply Current	HPM, Pout=27.5dBm	350	425	475	mA
	MPM, Pout=18.0dBm	50	79	100	mA
	BPM, Pout=12.0dBm	20	32	45	mA
Quiescent Current	HPM	70	100	130	mA
	MPM	10	19	30	mA
	BPM	2	3.4	5	mA
Enable Control Current	HPM, Ven_LB=1.8V	–	10	50	µA
	MPM, Ven_LB=1.8V	–	10	50	µA
	BPM, Ven_LB=1.8V	–	10	50	µA
Mode Control Current	MPM, Vmode=1.8V	–	10	50	µA
	BPM, Vmode=1.8V	–	10	50	µA
Bypass Control Current	BPM, Vbp=1.8V	–	10	50	µA
Total Current in Power Down Mode	Ven_LB=Ven_HB=0V, Vmode=Vbp=0V	–	1	5	µA
Adjacent Channel Leakage Ratio +/-5MHz Offset	– – –	– – –	-42 – –	-36 -36 -36	dBc
+/-5MHz Offset	– –	– –	-45 –	-36 -36	dBc
+/-5MHz Offset	– –	– –	-46 –	-36 -36	dBc
Adjacent Channel Leakage Ratio +/-10MHz Offset	– – –	– – –	-56 – –	-46 -46 -46	dBc
+/-10MHz Offset	– –	– –	-62 –	-46 -46	dBc
+/-10MHz Offset	– –	– –	-61 –	-46 -46	dBc
Harmonic Suppression 2nd 3rd	– –	– –	-38 -63	-30 -40	dBc
EVM	Pout ≤ Max.Pout – MPR Pout ≤ Max.Pout – MPR – 3dB	– –		5 4	% rms
Input VSWR		–	2:1	2.5:1	–

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Band 5 (Continue)

Characteristics		Condition	Min	Typ	Max	Unit
Rx Band Noise		HPM, Pout=27.5dBm, Vcc=4.2V	–	-135	-132	dBm/Hz
GPS Band Noise		HPM, Pout=27.5dBm, Vcc=4.2V	–	-155	-140	dBm/Hz
ISM Band Noise		HPM, Pout=27.5dBm, Vcc=4.2V	–	-157	-143	dBm/Hz
Phase Discontinuity		MPM↔HPM, at Pout=18dBm	Typ-30	8	Typ+30	deg
		BPM↔MPM, at Pout=12dBm	Typ-30	22	Typ+30	deg
Turn-On/Off Time	DC Turn-On (RF Off)	Ven transition to final I_{CQ} ±10%	–	–	20	µs
	DC Turn-Off (RF Off)	Ven transition to I_{CQ} ≤ 0.1mA	–	–	20	
	RF Turn-On	RFin On to final Pout ±1dB	–	–	6	
	RF Turn-Off	RFin Off to initial Pout – 30dB	–	–	6	
Mode Switching Time	PDM↔BPM / MPM / HPM	Ven transition to final RF Pout ±1dB	–	3.5	10	µs
	BPM↔MPM	Vbp transition to final RF Pout ±1dB	–	3.5	10	
	MPM↔HPM	Vmode transition to final RF Pout ±1dB	–	3.5	10	
	BPM↔HPM	Vbp/Vmode transition to final RF Pout ±1dB	–	3.5	10	
Coupling Factor		Pcpl – Pout, RFout & Couple Z_{LOAD} = 50Ω	–	-20	–	dB
Delivered Power Variation by Load Mismatch with Constant Coupled Power		Load VSWR = 2.5:1 All Phase, Constant Pcpl	–	±0.3	±1.0	dB
Stability (Spurious Output)		In-Band Load VSWR ≤ 5:1 All Phase, Pout≤27.5dBm & Pin≤6dBm	–	–	-60	dBc
Ruggedness (No Damage or Degradation)		Pout≤27.5dBm & Pin≤10dBm, All Phase	–	–	10:1	VSWR

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Band 1

Characteristics		Condition	Min	Typ	Max	Unit
Operating Frequency Range			1920	–	1980	MHz
Max. Linear Output Power		HPM, WCDMA (CM=0 / MPR=-1dB) HPM, HSDPA MPR=0dB HPM, HSUPA MPR=0dB	27.5 26.5 26.0	– – –	– – –	dB
		MPM, WCDMA (CM=0 / MPR=-1dB) MPM, HSPA MPR=0dB	18.0 17.0	– –	– –	dB
		BPM, WCDMA (CM=0 / MPR=-1dB) BPM, HSPA MPR=0dB	12.0 11.0	– –	– –	dB
Gain		HPM, Pout=27.5dBm	24	27.5	31	dB
		MPM, Pout=18.0dBm	15	19.5	24	dB
		BPM, Pout=12.0dBm	8	11.7	16	dB
PAE		HPM, Pout=27.5dBm	34.0	38.4	–	%
		MPM, Pout=18.0dBm	18.3	24.5	–	%
		BPM, Pout=12.0dBm	8.7	11.7	–	%
Total Supply Current		HPM, Pout=27.5dBm	360	430	485	mA
		MPM, Pout=18.0dBm	50	75	100	mA
		BPM, Pout=12.0dBm	20	37	50	mA
Quiescent Current		HPM	85	115	145	mA
		MPM	15	22	30	mA
		BPM	2	3.5	5	mA
Enable Control Current		HPM, Ven_HB=1.8V	–	10	50	µA
		MPM, Ven_HB=1.8V	–	10	50	µA
		BPM, Ven_HB=1.8V	–	10	50	µA
Mode Control Current		MPM, Vmode=1.8V	–	10	50	µA
		BPM, Vmode=1.8V	–	10	50	µA
Bypass Control Current		BPM, Vbp=1.8V	–	10	50	µA
Total Current in Power Down Mode		Ven_LB=Ven_HB=0V, Vmode=Vbp=0V	–	1	5	µA
Adjacent Channel Leakage Ratio	+/-5MHz Offset	HPM, WCDMA R'99, Pout=27.5dBm HPM, HSDPA MPR=0dB, Pout=26.5dBm HPM, HSUPA MPR=0dB, Pout=26.0dBm	– – –	-43 – –	-36 -36 -36	dBc
	+/-5MHz Offset	MPM, WCDMA R'99, Pout=18.0dBm MPM, HSPA MPR=0dB, Pout=17.0dBm	– –	-42 –	-36 -36	dBc
	+/-5MHz Offset	BPM, WCDMA R'99, Pout=12.0dBm BPM, HSPA MPR=0dB, Pout=11.0dBm	– –	-39 –	-36 -36	dBc
Adjacent Channel Leakage Ratio	+/-10MHz Offset	HPM, WCDMA R'99, Pout=27.5dBm HPM, HSDPA MPR=0dB, Pout=26.5dBm HPM, HSUPA MPR=0dB, Pout=26.0dBm	– – –	-55 – –	-46 -46 -46	dBc
	+/-10MHz Offset	MPM, WCDMA R'99, Pout=18.0dBm MPM, HSPA MPR=0dB, Pout=17.0dBm	– –	-63 –	-46 -46	dBc
	+/-10MHz Offset	BPM, WCDMA R'99, Pout=12.0dBm BPM, HSPA MPR=0dB, Pout=11.0dBm	– –	-58 –	-46 -46	dBc
Harmonic Suppression	2nd 3rd	HPM, Pout=27.5dBm, Meas.BW=1MHz	– –	-44 -64	-30 -40	dBc
EVM		Pout ≤ Max.Pout – MPR Pout ≤ Max.Pout – MPR – 3dB	– –		5 4	% rms
Input VSWR			–	2.2:1	2.5:1	

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Band 1 (Continue)

Characteristics		Condition	Min	Typ	Max	Unit
Rx Band Noise		HPM, Pout=27.5dBm, Vcc=4.2V	–	-137	-134	dBm/Hz
GPS Band Noise		HPM, Pout=27.5dBm, Vcc=4.2V	–	-141	-136	dBm/Hz
ISM Band Noise		HPM, Pout=27.5dBm, Vcc=4.2V	–	-145	-142	dBm/Hz
Phase Discontinuity		MPM↔HPM, at Pout=18dBm	Typ-30	15	Typ+30	deg
		BPM↔MPM, at Pout=12dBm	Typ-30	3	Typ-30	deg
Turn-On/Off Time	DC Turn-On (RF Off) DC Turn-Off (RF Off) RF Turn-On RF Turn-Off	Ven transition to final I_{CQ} ±10% Ven transition to I_{CQ} ≤ 0.1mA RFin On to final Pout ±1dB RFin Off to initial Pout – 30dB	– – – –	– – – –	10 10 6 6	µs
Mode Switching Time	PDM↔BPM / MPM / HPM BPM↔MPM MPM↔HPM BPM↔HPM	Ven transition to final RF Pout ±1dB Vbp transition to final RF Pout ±1dB Vmode transition to final RF Pout ±1dB Vbp/Vmode transition to final RF Pout ±1dB	– – – –	3.5 3.5 3.5 3.5	10 10 10 10	µs
Coupling Factor		Pcpl – Pout, RFout & Couple Z_{LOAD} = 50Ω	–	-20	–	dB
Delivered Power Variation by Load Mismatch with Constant Coupled Power		Load VSWR = 2.5:1 All Phase, Constant Pcpl	–	±0.5	±1.0	dB
Stability (Spurious Output)		In-Band Load VSWR ≤ 5:1 All Phase, Pout≤27.5dBm & Pin≤6dBm	– –	– –	-60	dBc
Ruggedness (No Damage or Degradation)		Pout≤27.5dBm & Pin≤10dBm, All Phase	–	–	10:1	VSWR

HSDPA MPR=0dB Signal Configuration used:

3GPP TS 34.121-1
Annex C (normative): Measurement channels
C.10.1 UL reference measurement channel for HSDPA tests
Table C.10.1.4: β values for transmitter characteristics tests with HS-DPCCH → Sub-test 2 (CM=1.0, MPR=0.0)

HSUPA MPR=0dB Signal Configuration used:

3GPP TS 34.121-1
Annex C (normative): Measurement channels
C.11.1 UL reference measurement channel for E-DCH tests
Table C.11.1.3: β values for transmitter characteristics tests with HS-DPCCH and E-DCH → Sub-test 1 (CM=1.0, MPR=0.0)

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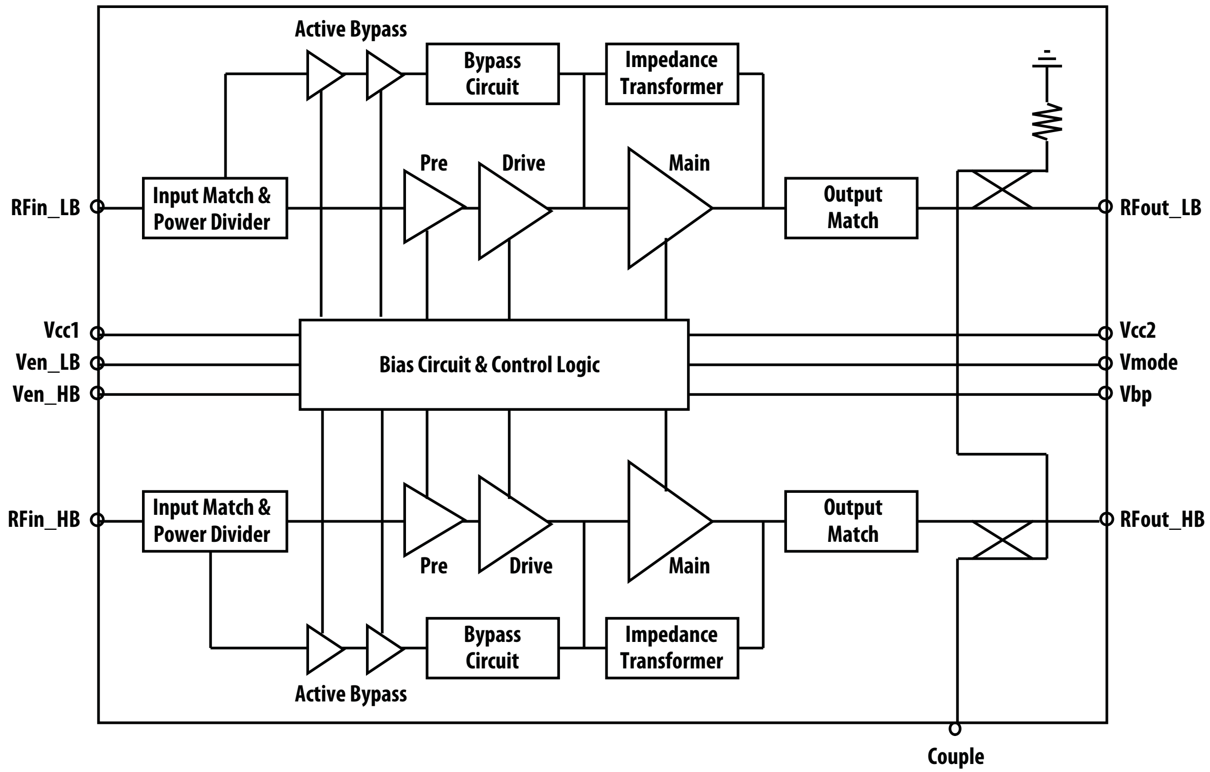
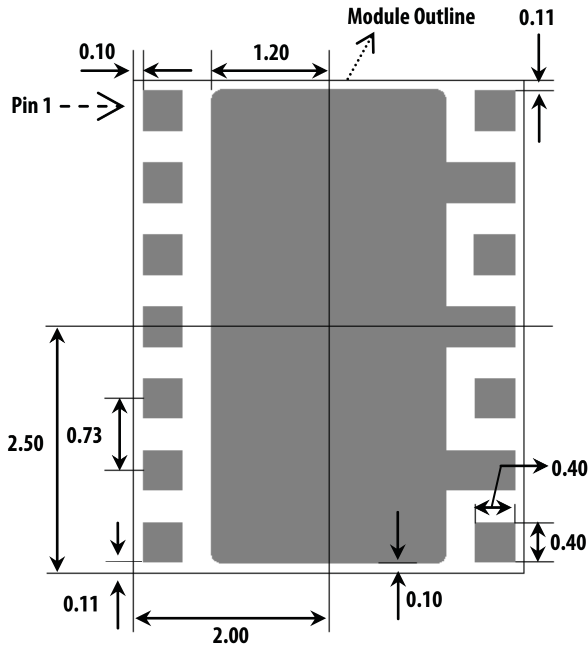
Functional Block Diagram



Footprint



X-Ray Top View through Package

All dimensions are in mm

PIN DESCRIPTIONS

Pin #	Name	Description
1	RFIn_LB	LB (B5) RF Input
2	Vmode	Mode Control
3	Vbp	Bypass Control
4	Vcc1	Supply Voltage 1
5	Ven_LB	LB (B5) PA Enable
6	Ven_HB	HB (B1) PA Enable
7	RFIn_HB	HB (B1) RF Input
8	Couple	Coupled Out
9	Gnd	Ground
10	RFOut_HB	HB (B1) RF Ouptut
11	Gnd	Ground
12	Vcc2	Supply Voltage 2
13	Gnd	Ground
14	RFOut_LB	LB (B5) RF Output

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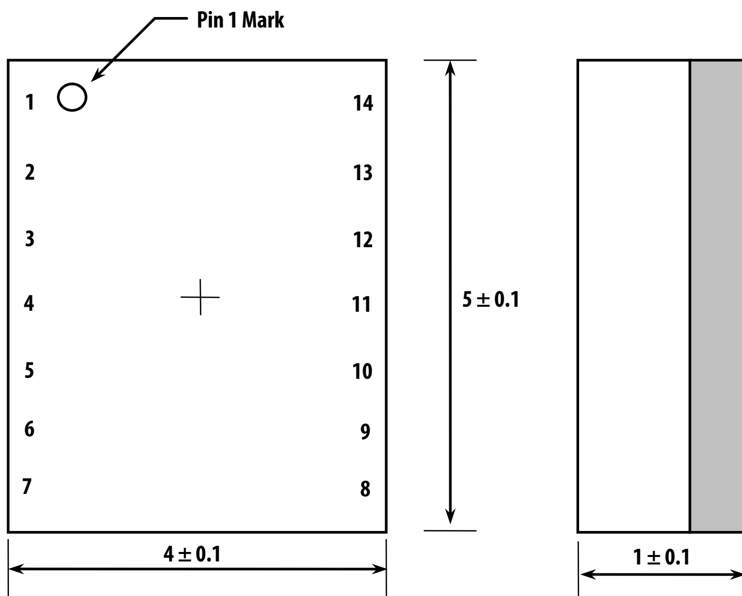
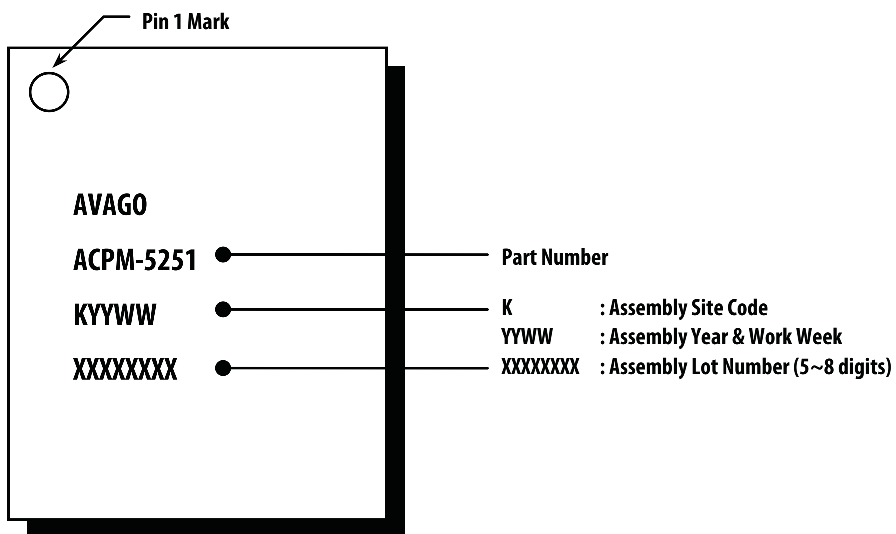
Package Dimensions



Marking Specification



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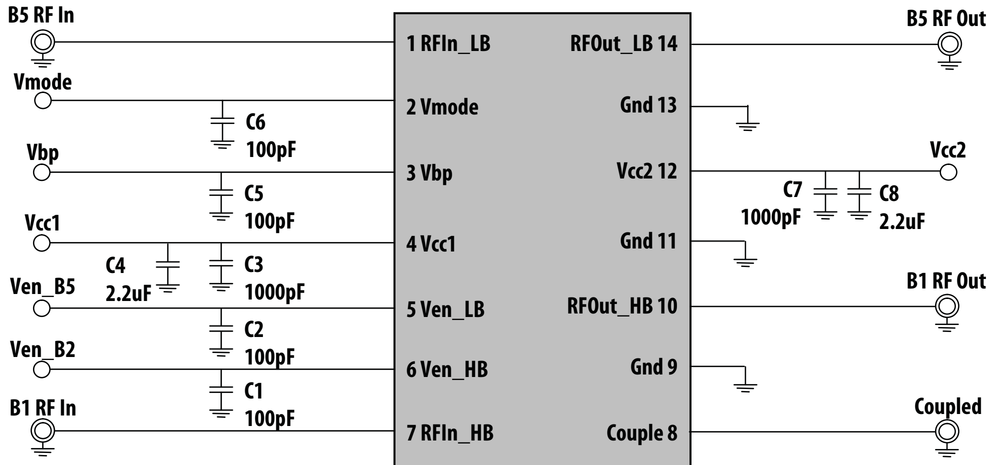
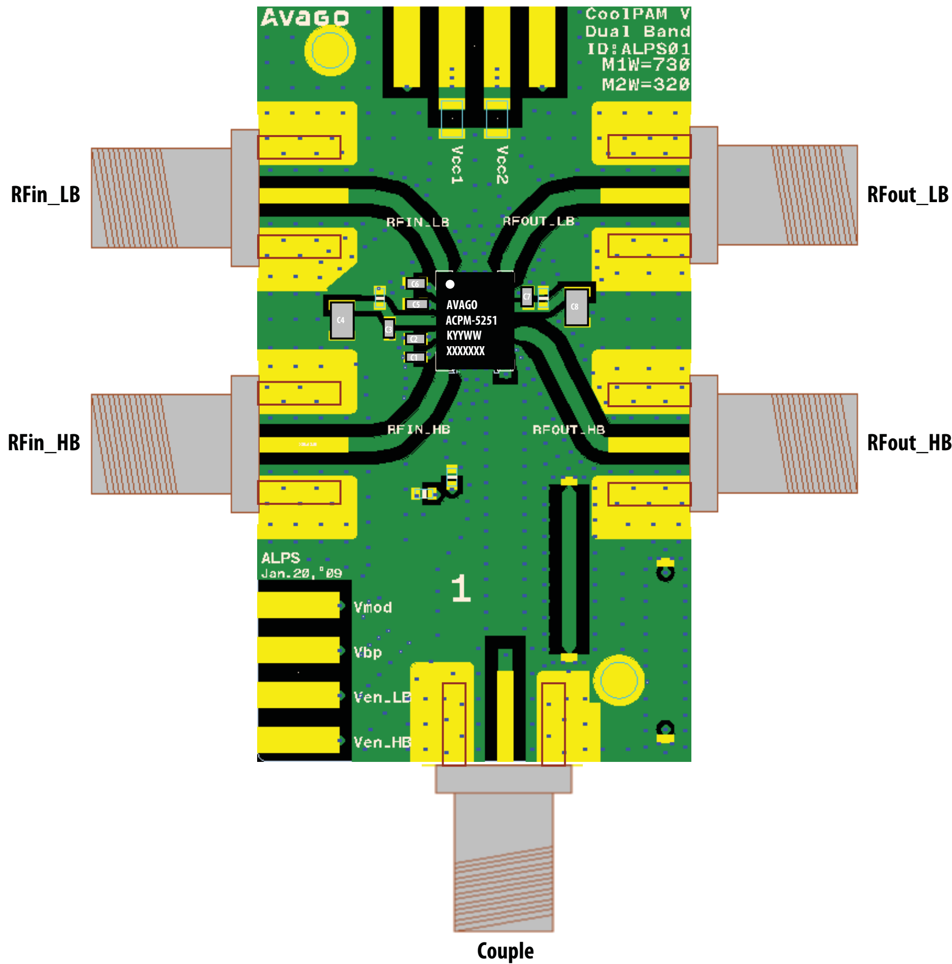
Evaluation Board Schematic



Evaluation Board Description



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Application on mobile phone board

The figure 1 shows an application example in mobile. C5 and C6 should be placed close to pin4 and pin11. Bypass cap C1, C2, C3 and C4 should be also placed nearby from pin2, pin3, pin5 and pin6, respectively. The length of post-PA transmission line should be minimized to reduce line loss.

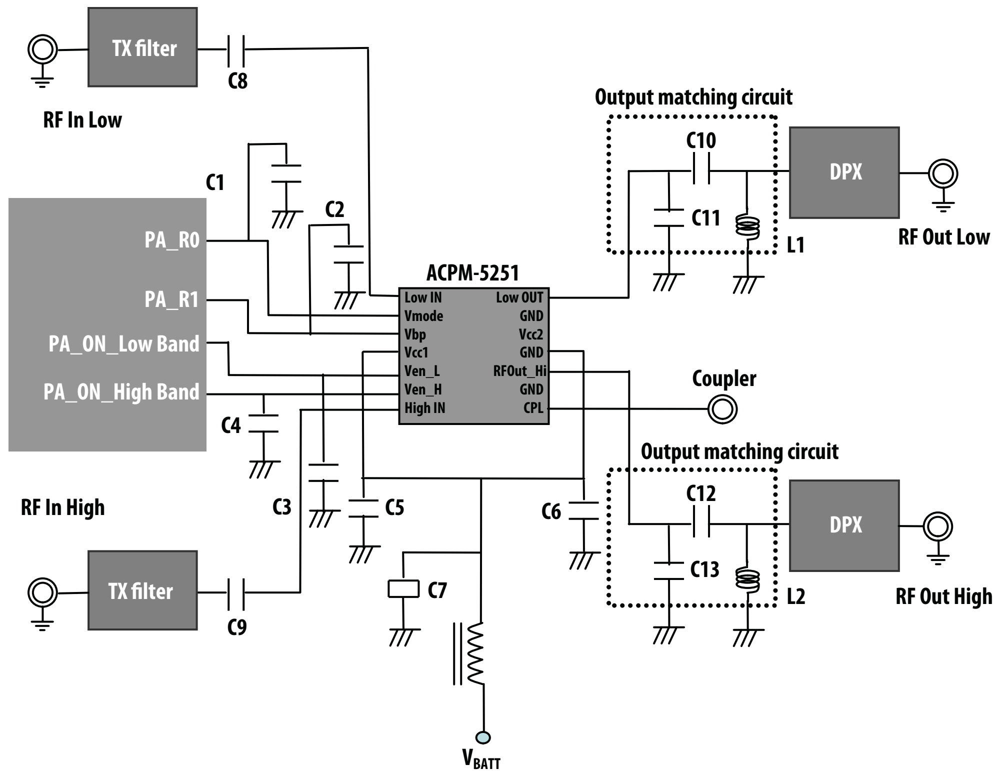

Figure 1. Peripheral Circuits

Recommended Values (L, C)

C1	100pF	C6	1000pF	C11	DNI*
C2	100pF	C7	2.2uF	C12	100pF
C3	100pF	C8	100pF	C13	DNI*
C4	100pF	C9	100pF	L1	DNI*
C5	1000pF	C10	100pF	L2	DNI*

Notes:

1. C1, C2, C3 and C4 should be placed close to each pin to reduce noise coming from the BB chipset as well as crossing between other power lines.
2. C5 and C6 are used for decoupling high frequency noise and C7 is for decoupling low frequency noise. They may affect Rx band noise, GPS band noise and spurious characteristics. For better performance, C5 and C6 should be used both Vcc1 and Vcc2 pins.

* Recommended Values are changeable by phone Board impedance.

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PCB layout and part placement on phone board

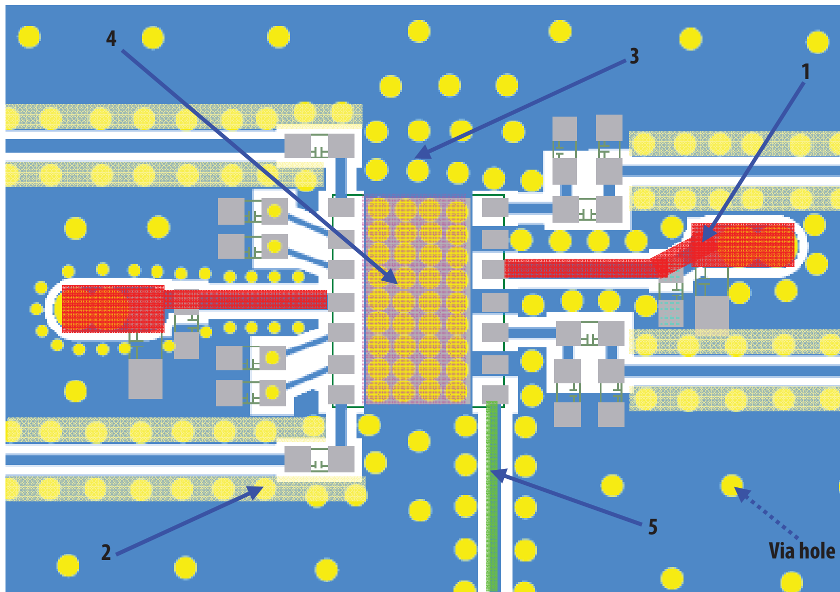

Figure 2. PCB guideline on phone board

Notes:

1. To prevent voltage drop, make the bias lines as wide as possible (Red line).
2. Use many via holes to fence off PA RF input and output traces for better isolation. Output signal of the PA should be isolated from input signal and the receive signal. Output signal should not be fed into PA input. (Yellow line)
3. Use via holes to connect outer ground planes to internal ground planes. They help heat spread out more easily and accordingly the board temperature can be lowered. They also help to improve RF stability.
4. PA which has a ground slug requires many via holes which go through all the layers (Pink square).
5. CPL_out line and RFout line are recommended to be at the different layer for better CPL_out/RF_out isolation (Green line).

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Matching network and loadpull data

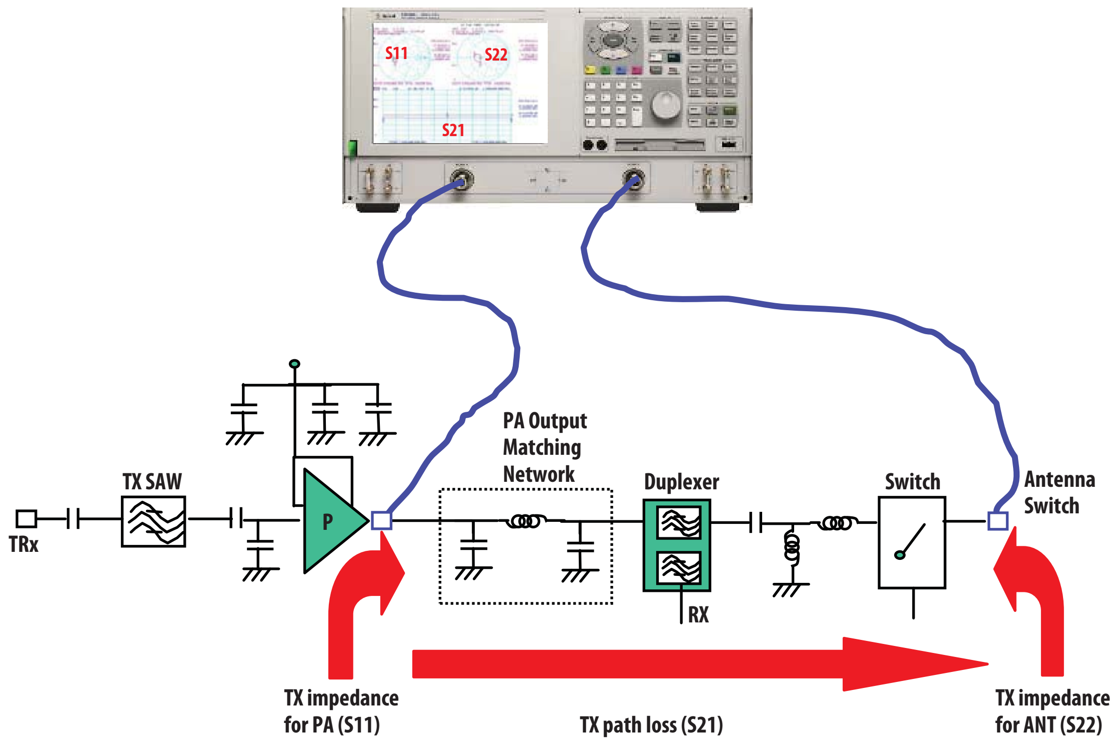

Figure 3. PA matching setup on the phone board

Vcc3.4v, Ven=2.6v, Vmode,Vbp=0, WCDMA(Rel99)

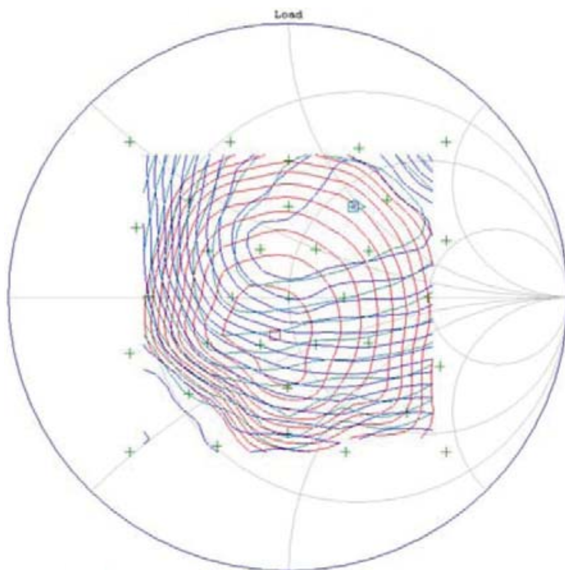

Figure 4. ACPM-5251 B1 loadpull data

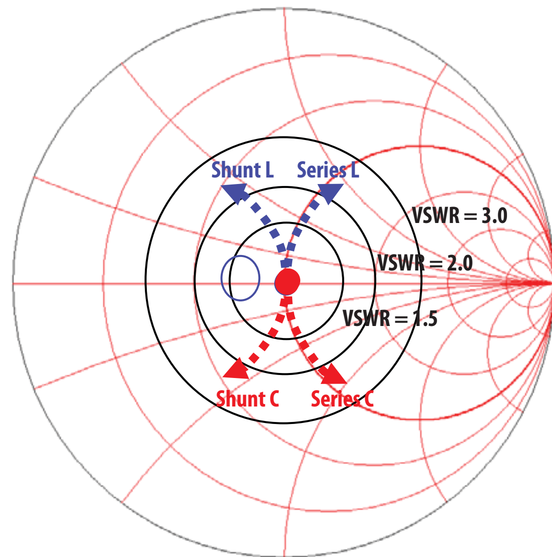

Figure 5. Matching network and PA optimized area

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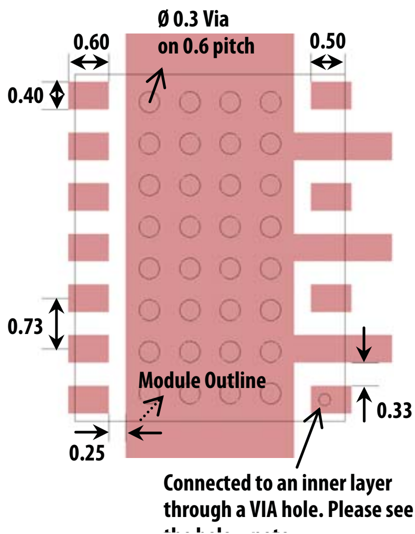
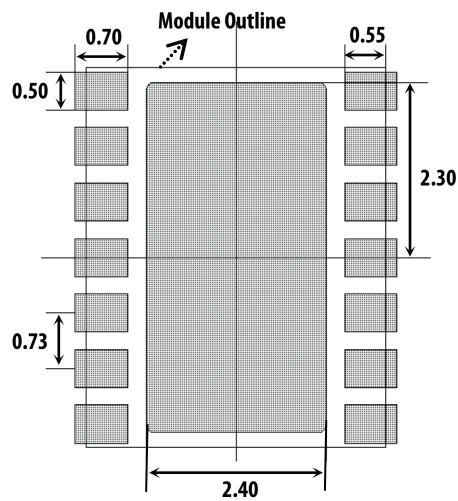
Metallization

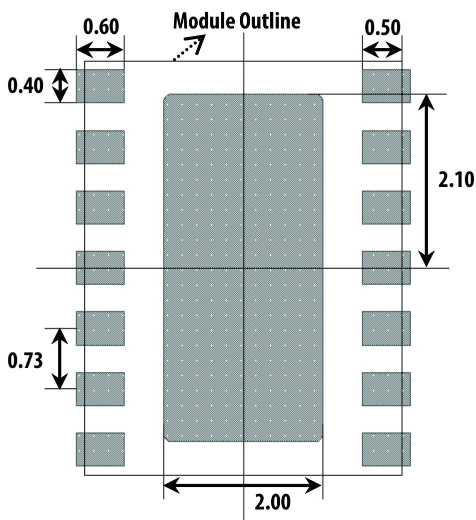


Note: High isolation between a CPL line and a RFout_HB line is required to avoid unwanted power coupling from high band RF output line to coupler line.

Solder Mask Opening



Solder Paste Stencil Aperture



PCB Design Guidelines

The recommended PCB land pattern is shown in figures on the left side. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

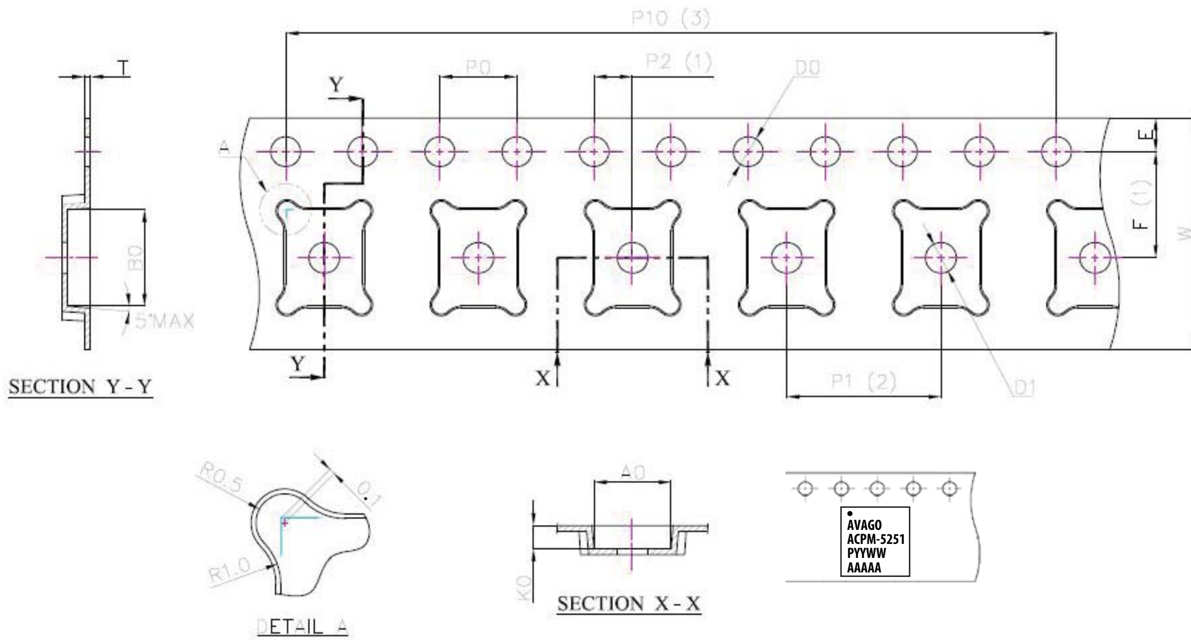
Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.

The recommended stencil layout is shown here. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100mm(4mils) or 0.127mm(5mils) thick stainless steel which is capable of producing the required fine stencil outline.

Free Datasheet http://www.datasheet4u.com/

Tape and Reel Information



Dimension List

Annote	Millimeter
A0	4.40±0.10
B0	5.30±0.10
K0	1.20±0.10
D0	1.55±0.05
D1	1.60±0.10
P0	4.00±0.10
P1	8.00±0.10

Annote	Millimeter
P2	2.00±0.05
P10	40.00±0.20
E	1.75±0.10
F	5.50±0.05
W	12.00±0.30
T	0.30±0.05

Tape and Reel Format – 4 mm x 5 mm

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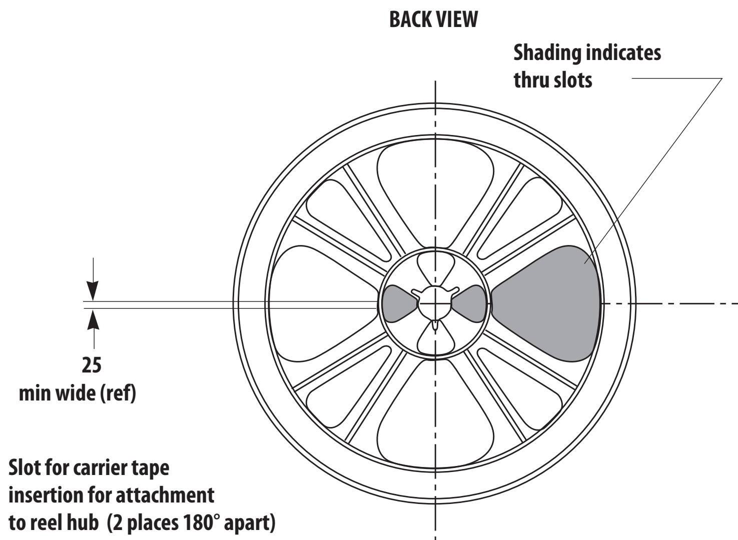
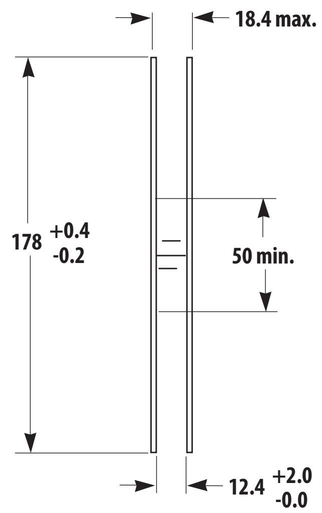
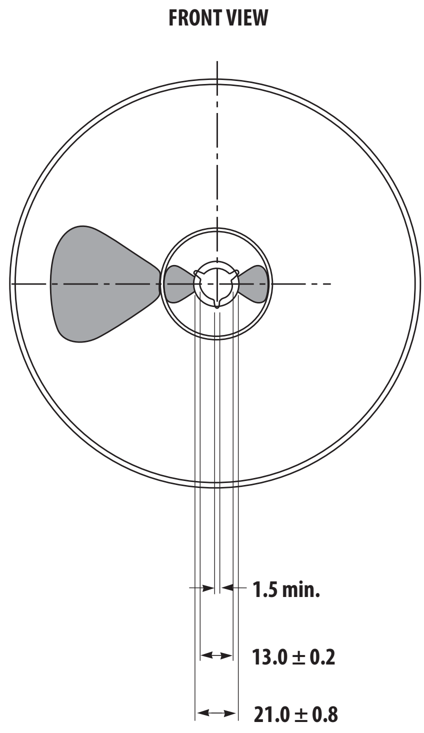
Reel Drawing







NOTES:

1. Reel shall be labeled with the following information (as a minimum).
   a. manufacturers name or symbol
   b. Avago Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance (c of c) shall be issued and accompany each shipment of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm)

Plastic Reel Format (all dimensions are in millimeters)

Free Datasheet http://www.datasheet4u.com/

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature.

Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

ACPM-5252 is MSL3. Thus, according to the J-STD-033 p.10, the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked. MSL classification reflow temperature for the ACPM-5252 is targeted at 260°C +0/-5°C. Figure and table on next page show typical SMT profile for maximum temperature of 260 +0/-5°C.

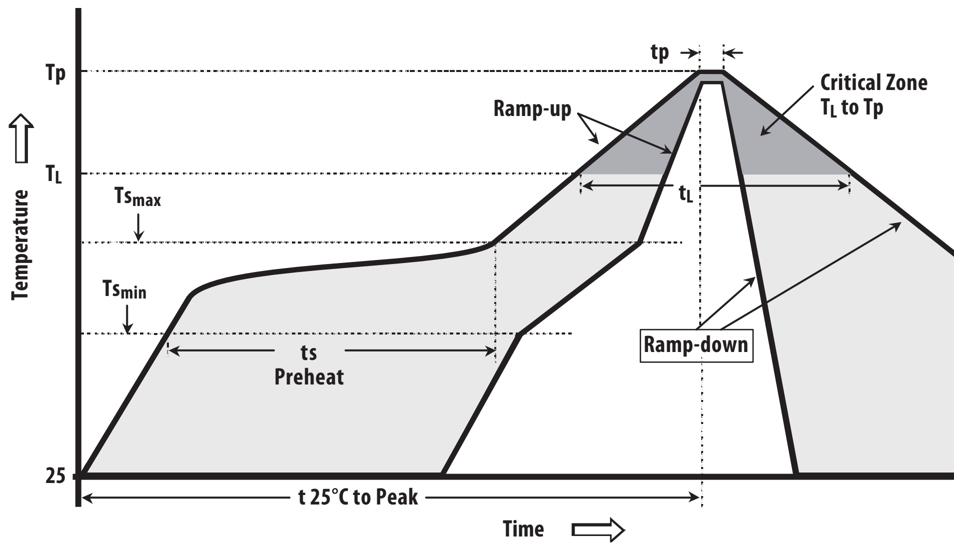
Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient =< 30°C/60% RH or as stated
1	Unlimited at =< 30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note :
1. The MSL Level is marked on the MSL Label on each shipping bag.

Free Datasheet http://www.datasheet4u.com/

Reflow Profile Recommendations



Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5°C

Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (TL to TP)	3°C/sec max	3°C/sec max
Preheat – Temperature Min (Tsmin) – Temperature Max (Tsmax) – Time (min to max) (ts)	 100°C 150°C 60-120 sec	 150°C 200°C 60-120 sec
Tsmax to TL – Ramp-up Rate		 3°C/sec max
Time maintained above: – Temperature (TL) – Time (TL)	 183°C 60-150 sec	 217°C 60-150 sec
Peak temperature (Tp)	240 +0/-5°C	260 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 sec	20-40 sec
Ramp-down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.

Free Datasheet http://www.datasheet4u.com/

Storage Condition

Packages described in this document must be stored in sealed moisture barrier, antistatic bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p.6.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours with factory conditions <30°C and 60% RH as listed in the Table 5-1 on the J-STD-020D p.6.

Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above has not been satisfied. The baking conditions are listed in the Table 4-1 on the J-STD-033 p.8.

CAUTION

Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/ reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 andIPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in table of Moisture Classification Level and Floor Life. This approach, however, does not work if the factory humidity or temperature is greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device.

Table on following page lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperature, 20°C, 25°C, and 30°C.

This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating this table:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121exp (-0.35eV/kT) mm2/s (this used smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity = 1.320exp (-0.35eV/kT) mm2/s (this used largest known Diffusivity @ 30°C).

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Recommended Equivalent Total Floor Life (days) @ 20°C, 25°C & 30°C, 35°C

For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified) Maximum Percent Relative Humidity

Maximum Percent Relative Humidity												
Package Type and Body Thickness	**Moisture Sensitivity Level**	**5%**	**10%**	**20%**	**30%**	**40%**	**50%**	**60%**	**70%**	**80%**	**90%**	
Body Thickness ≥3.1 mm Including PQFPs >84 pin, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞	∞	94	44	32	26	16	7	5	4	35°C
		∞	∞	124	60	41	33	28	10	7	6	30°C
		∞	∞	167	78	53	42	36	14	10	8	25°C
		∞	∞	231	103	69	57	47	19	13	10	20°C
	Level 3	∞	∞	8	7	6	6	6	4	3	3	35°C
		∞	∞	10	9	8	7	7	5	4	4	30°C
		∞	∞	13	11	10	9	9	7	6	5	25°C
		∞	∞	17	14	13	12	12	10	8	7	20°C
	Level 4	∞	3	3	3	2	2	2	2	1	1	35°C
		∞	5	4	4	4	3	3	3	2	2	30°C
		∞	6	5	5	5	5	4	3	3	3	25°C
		∞	8	7	7	7	7	6	5	4	4	20°C
	Level 5	∞	2	2	2	2	1	1	1	1	1	35°C
		∞	4	3	3	2	2	2	2	1	1	30°C
		∞	5	5	4	4	3	3	2	2	2	25°C
		∞	7	7	6	5	5	4	3	3	3	20°C
	Level 5a	∞	1	1	1	1	1	1	1	1	1	35°C
		∞	2	1	1	1	1	1	1	1	1	30°C
		∞	3	2	2	2	2	2	1	1	1	25°C
		∞	5	4	3	3	3	2	2	2	2	20°C
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pin SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞	∞	∞	∞	58	30	22	3	2	1	35°C
		∞	∞	∞	∞	86	39	28	4	3	2	30°C
		∞	∞	∞	∞	148	51	37	6	4	3	25°C
		∞	∞	∞	∞	∞	69	49	8	5	4	20°C
	Level 3	∞	∞	12	9	7	6	5	2	2	1	35°C
		∞	∞	19	12	9	8	7	3	2	2	30°C
		∞	∞	25	15	12	10	9	5	3	3	25°C
		∞	∞	32	19	15	13	12	7	5	4	20°C
	Level 4	∞	5	4	3	3	2	2	1	1	1	35°C
		∞	7	5	4	4	3	3	2	2	1	30°C
		∞	9	7	5	5	4	4	3	2	2	25°C
		∞	11	9	7	6	6	5	4	3	3	20°C
	Level 5	∞	3	2	2	2	2	1	1	1	1	35°C
		∞	4	3	3	2	2	2	1	1	1	30°C
		∞	5	4	3	3	3	3	2	1	1	25°C
		∞	6	5	5	4	4	4	3	3	2	20°C
	Level 5a	∞	1	1	1	1	1	1	1	0.5	0.5	35°C
		∞	2	1	1	1	1	1	1	0.5	0.5	30°C
		∞	2	2	2	2	2	2	1	1	1	25°C
		∞	3	2	2	2	2	2	2	2	1	20°C
Body Thickness <2.1 mm including SOICs <18 pin All TQFPs, TSOPs or All BGAs <1 mm body thickness	Level 2a	∞	∞	∞	∞	∞	∞	17	1	0.5	0.5	35°C
		∞	∞	∞	∞	∞	∞	28	1	1	1	30°C
		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°C
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°C
	Level 3	∞	∞	∞	∞	∞	8	5	1	0.5	0.5	35°C
		∞	∞	∞	∞	∞	11	7	1	1	1	30°C
		∞	∞	∞	∞	∞	14	10	2	1	1	25°C
		∞	∞	∞	∞	∞	20	13	2	2	1	20°C
	Level 4	∞	∞	∞	7	4	3	2	1	0.5	0.5	35°C
		∞	∞	∞	9	5	4	3	1	1	1	30°C
		∞	∞	∞	12	7	5	4	2	1	1	25°C
		∞	∞	∞	17	9	7	6	2	2	1	20°C
	Level 5	∞	∞	7	3	2	2	1	1	0.5	0.5	35°C
		∞	∞	13	5	3	2	2	1	1	1	30°C
		∞	∞	18	6	4	3	3	2	1	1	25°C
		∞	∞	26	8	6	5	4	2	2	1	20°C
	Level 5a	∞	7	2	1	1	1	1	1	0.5	0.5	35°C
		∞	10	3	2	1	1	1	1	1	0.5	30°C
		∞	13	5	3	2	2	2	1	1	1	25°C
		∞	18	6	4	3	2	2	2	2	1	20°C

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