ACPM-7371
UMTS 4x4 Power Amplifier
(880-915MHz)

Data Sheet

Description

The ACPM-7371, a Wide-band Code Division Multiple Access(WCDMA) Power Amplifier (PA), is a fully matched 10-pin surface mount module developed for WCDMA handset applications. This power amplifier module is developed to cover 880-915MHz bandwidth. The ACPM-7371 meets the stringent WCDMA linearity requirements for output power of up to 28dBm. The ACPM-7371 is also developed to meet HSDPA specs up to 27.5dBm.

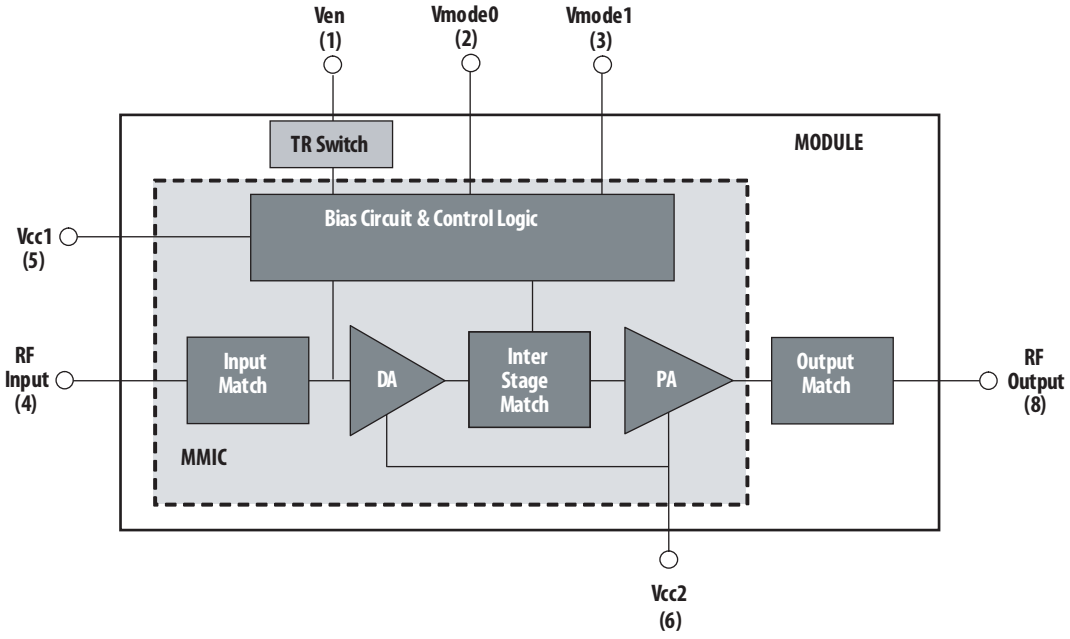
The ACPM-7371 is designed to enhance the efficiency at low and medium output power range by using 3-mode control scheme with 2 mode control pins. This provides extended talk time.

The ACPM-7371 is self contained, incorporating 50Ω input and output matching networks.

Order information

Part Number	No. of Devices	Container
ACPM-7371-TR1	1000	7"Tape and Reel
ACPM-7371-BLK	100	BULK

Functional Block Diagram



Features

- Excellent Linearity
- Low quiescent current
- High Efficiency
- 10-pin surface mounting package
  (4mmx4mmx1.1mm typ)
- Internal 50Ω matching networks for both RF input and output
- RoHS Compliant

Applications

- WCDMA Handset (HSDPA)

Table 1. Absolute Maximum Ratings

No damage assuming only one parameter is set at limit at a time with all other parameters set at or below typical value. Operation of any single parameter outside these conditions with the remaining parameters set at or below typical values may result in permanent damage

Parameter	Min	TYP	Max	Unit	Associated Pins
RF Input Power	–	–	10.0	dBm	RFIn
DC Supply Voltage	0	3.4	5.0	V	Vcc1, Vcc2
Enable Voltage	0	2.6	3.3	V	Ven
Mode Control Voltage	0	1.9	3.3	V	Vmode0, Vmode 1
Storage Temperature	-55	–	+125	℃	

Table 2. Recommended Operating Condition

Parameter		Min	Nominal	Max	Unit
DC Supply Voltage		3.2	3.4	4.2	V
Enable Voltage (Ven)	LOW HIGH	0 1.9	0.5 2.6	0.5 2.9	V
Mode Control Voltage (Vmode0, Vmode1)	LOW HIGH	0 1.8	0 1.9	0.5 2.9	V
Operating Frequency		880		915	MHz
Ambient Temperature		-20	25	90	℃

Table 3. Power Range Truth Table

Power Mode	Ven	Vmode0	Vmode1	Range
High Power Mode	High	Low	Low	~ 28dBm (WCMDA)
Mid Power Mode	High	High	Low	~ 16dBm
Low Power Mode	High	High	High	~ 8dBm
Shut Down Mode	Low	–	-	–

Table 4. Electrical Characteristics for WCDMA Mode

Vcc=3.4V, Ven=2.6V, Vmode0 and Vmode1= 0V or 1.9V, T=25°C, Zin/Zout=50Ω

Signal Configuration: 3GPP Uplink DPCCH + 1DPDCH

Characteristics		Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range			880	–	915	MHz
Gain		High Power Mode, Pout=28.0 dBm	23.5	26.5		dB
		Mid Power Mode, Pout=16.0 dBm	12.5	17		dB
		Low Power Mode, Pout=8.0 dBm	11.5	16		dB
Power Added Efficiency		High Power Mode, Pout=28.0 dBm	35.3	40.0		%
		Mid Power Mode, Pout=16.0 dBm	10.4	14.3		%
		Low Power Mode, Pout=8.0 dBm	3.3	5.2		%
Total Supply Current		High Power Mode, Pout=28.0 dBm		463	535	mA
		Mid Power Mode, Pout=16.0 dBm		80	110	mA
		Low Power Mode, Pout=8.0 dBm		35	55	mA
Quiescent Current		High Power Mode		96	120	mA
		Mid Power Mode		18	24	mA
		Low Power Mode		13	18	mA
Enable Current		High Power Mode		0.18	1	mA
		Mid Power Mode		0.18	1	mA
		Low Power Mode		0.18	1	mA
Control Current		Mid Power Mode (Imode0)		0.4	1	mA
		Low Power Mode (Imode1)		0.18	1	mA
		Low Power Mode (Imode0)		0.4	1	mA
Total Current in Power-down mode		Ven=0V		0.2	5	µA
Adjacent Channel Leakage Ratio	5 MHz offset 10 MHz offset	High Power Mode, Pout=28.0 dBm		-41 -54	-36 -46	dBc
	5 MHz offset 10 MHz offset	Mid Power Mode, Pout=16.0 dBm		-48 -61	-36 -46	dBc
	5 MHz offset 10 MHz offset	Low Power Mode, Pout=8.0 dBm		-40 -56	-36 -46	dBc
Harmonic Suppression	2fo 3fo	High Power Mode, Pout=28.0 dBm			-30 -45	dBc
Input VSWR	VSWR				2.5:1	
Stability (Spurious Output)		VSWR 5:1, All phase			-60	dBc
Noise Power in Rx Band		High Power Mode, Pout=28.0 dBm		-132	-130	dBm/Hz
Phase Discontinuity		low power mode <--> mid power mode, at Pout=8dBm			10	deg
		mid power mode <--> high power mode, at Pout=16dBm			30	deg
Ruggedness		Pout<28.0dBm, Pin<10dBm, All phase High Power Mode			10:1	VSWR

Table 5. Electrical Characteristics for HSDPA Mode

Vcc=3.4V, Ven=2.6V, Vmode0 and Vmode1=0V or 1.9V, T=25°C, Zin/Zout=50Ω

Signal configuration: DPCCH/DPDCH=12/15, HS-DPCCH/DPDCH=15/15

Characteristics		Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range			880	–	915	MHz
Gain		High Power Mode, Pout = 27.5 dBm	23.5	26		dB
		Mid Power Mode, Pout = 16.0 dBm	12.5	17		dB
		Low Power Mode, Pout = 8.0 dBm	11.5	16		dB
Power Added Efficiency		High Power Mode, Pout = 27.5 dBm	33.7	36.7		%
		Mid Power Mode, Pout = 16.0 dBm	10.4	14.7		%
		Low Power Mode, Pout = 8.0 dBm	3.3	5.2		%
Total Supply Current		High Power Mode, Pout = 27.5 dBm		450	490	mA
		Mid Power Mode, Pout = 16.0 dBm		78	110	mA
		Low Power Mode, Pout = 8.0 dBm		35	55	mA
Adjacent Channel Leakage Ratio	5 MHz offset 10 MHz offset	High Power Mode, Pout = 27.5 dBm	–	-40 -52	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	Mid Power Mode, Pout = 16.0 dBm	–	-44 -58	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	Low Power Mode, Pout = 8.0 dBm	–	-40 -56	-36 -46	dBc dBc

Characteristics Data

WCDMA, Vcc=3.4V, Ven=2.6V, Vmode0 and Vmode1=0V or 1.9V, T=25°, Zin/Zout=50Ω

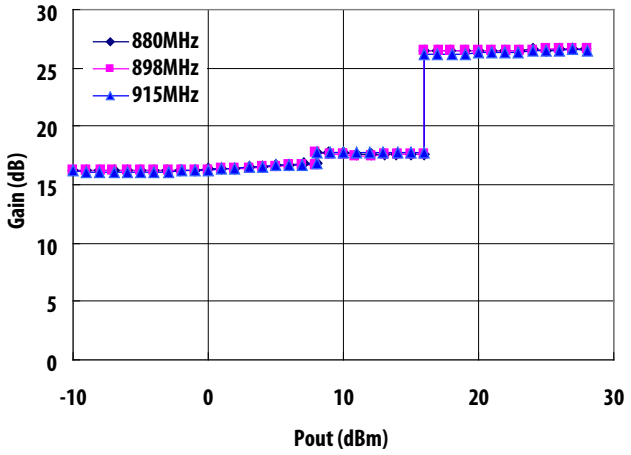


Figure 1. Gain vs. Output Power

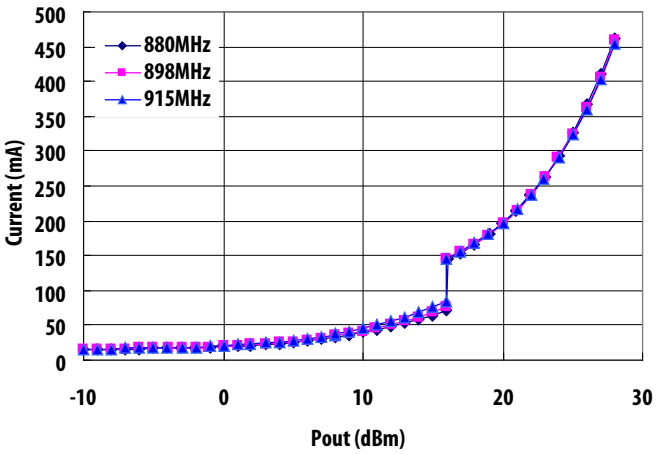


Figure 2. Total Current vs. Output Power

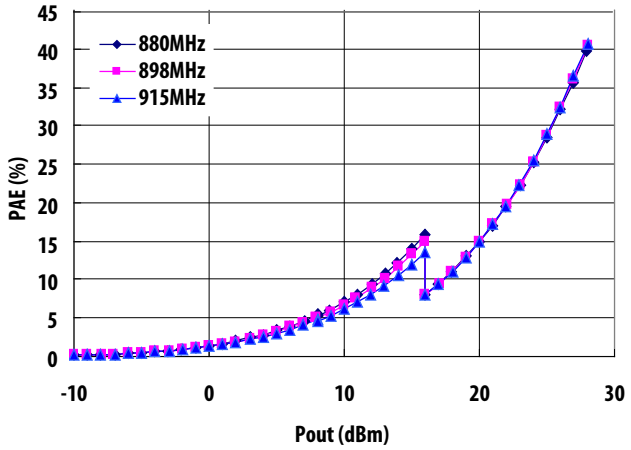


Figure 3. Power Added Efficiency vs. Output Power

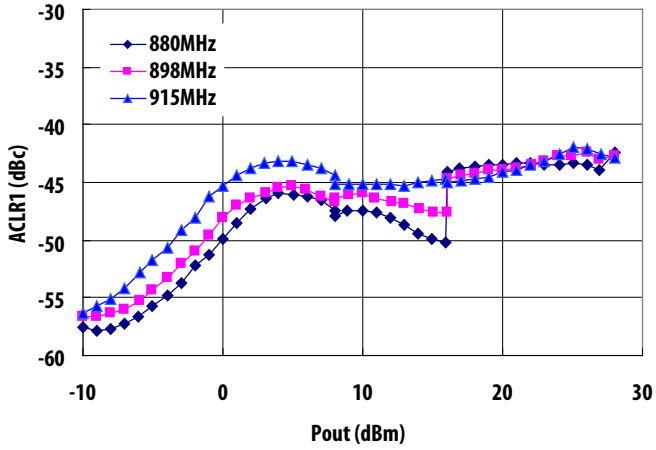


Figure 4. Adjacent Channel Leakage Ratio 1 vs. Output Power

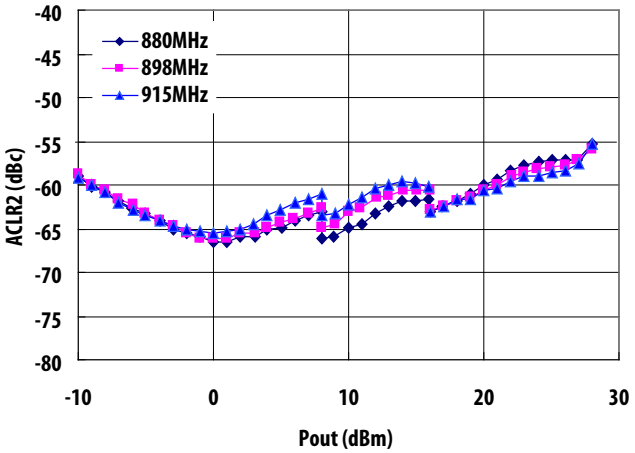


Figure 5. Adjacent Channel Leakage Ratio 2 vs. Output Power

Evaluation Board Description

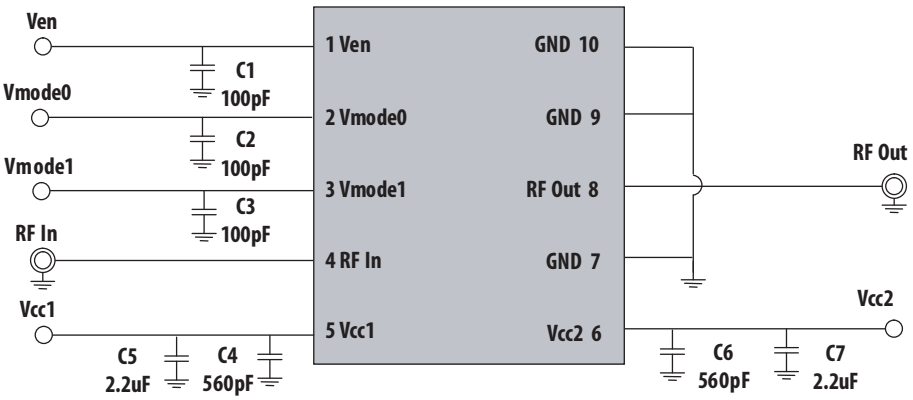


Figure 6. Evaluation Board Schematic

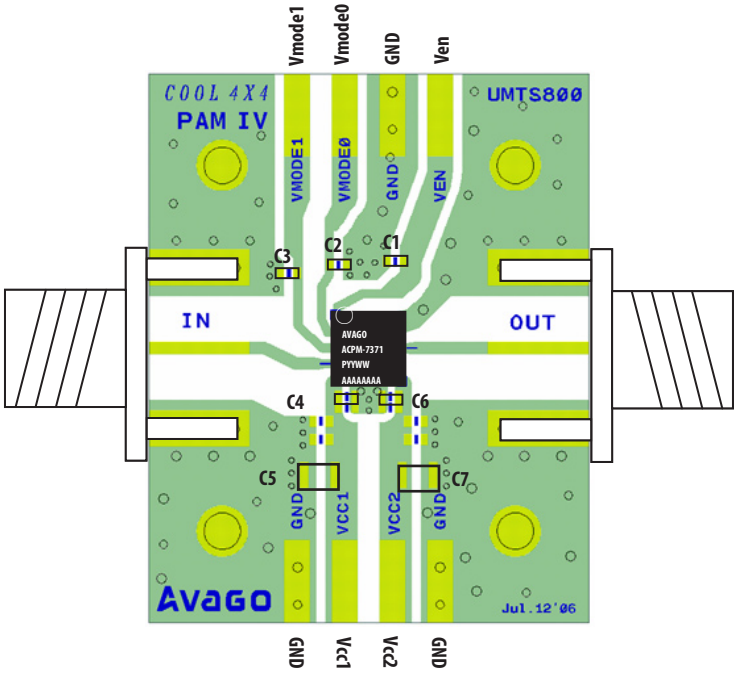


Figure 7. Evaluation Board Assembly Diagram

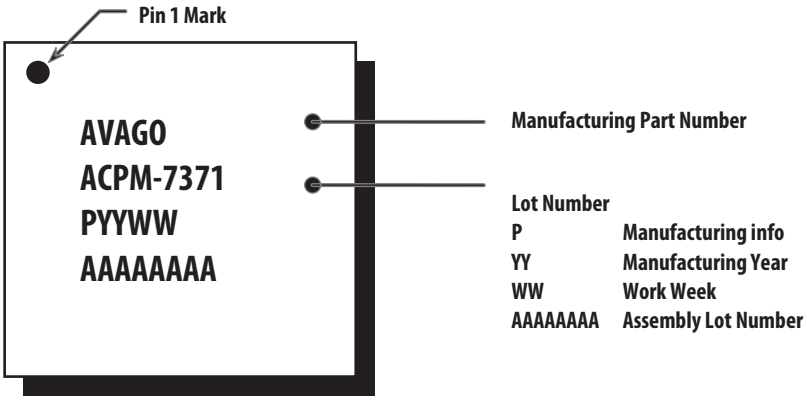
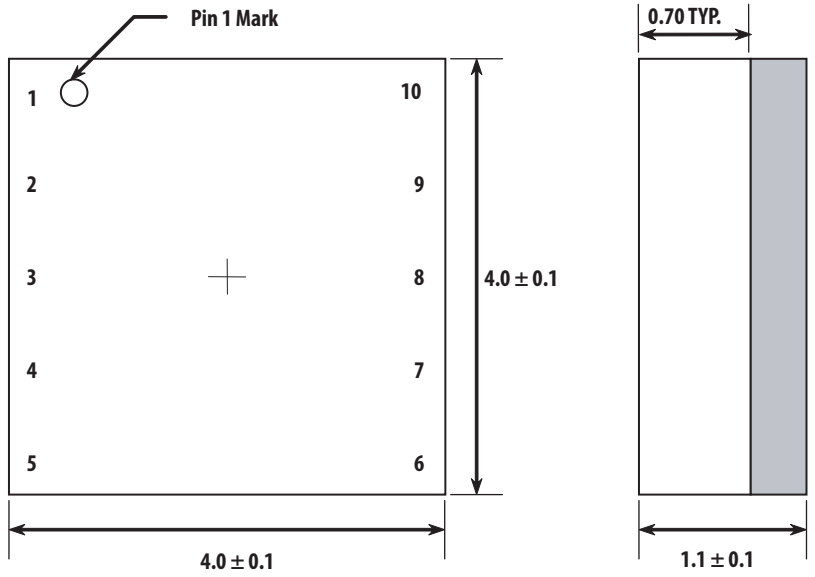
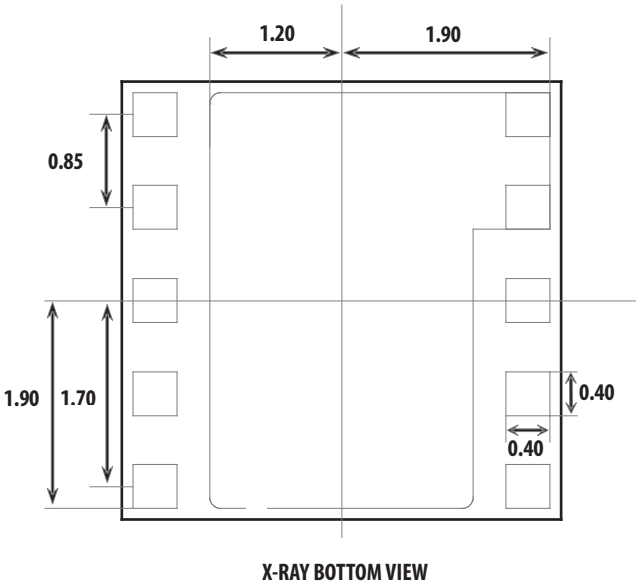


Figure 8. Marking Specifications

Package Dimensions and Pin Descriptions





PIN DESCRIPTIONS

Pin #	Name	Description
1	Ven	Enable Voltage
2	Vmode0	Control Voltage
3	Vmode1	Control Voltage
4	RFIn	RF Input
5	Vcc1	Supply Voltage
6	Vcc2	Supply Voltage
7	GND	Ground
8	RF Out	RF Output
9	GND	Ground
10	GND	Ground

Figure 9. Package Dimensional Drawing and Pin Descriptions (All dimensions are in millimeters)

CoolPAM

Avago Technologies' CoolPAM is stage-bypass PA technology which saves more power compared with conventional PA. With this technology, the ACPM-7371 has very low quiescent current and efficiencies at low and medium output power ranges are very high.

Incorporation of bias circuit

The ACPM-7371 has internal bias circuit, which removes the need for external constant voltage source (LDO). PA on/off is controlled by Ven. This is digitally control pin.

3-mode power control with two mode control pins

The ACPM-7371 supports three power modes (low power mode/mid power mode/high power mode) with two mode control pins (Vmode0 and Vmode1). This control scheme enables the ACPM-7371 to save more power, which accordingly gives extended talk time.

PDF (probability density function) in below figure showing distribution of output power of mobile in real field gives motivation for stage-bypass PA. Output power is less than 16dBm for most of operating time (during talking), so it is important to save power consumption at low and medium output power ranges.

Average current & Talk time

Average current consumed by PA can be calculated by summing up current at each output power weighted with probability. So it is expressed with integration of multiplication of current and probability at each output power.

$$Average\ current = \int (PDF \times Current)dp$$

Talk time is extended more as average current consumption is lowered.

Mode control pins

Vmode0 and Vmode1 are digitally controlled pins and they control operating mode of PA and truth table is summarized in Table 3. These pins do not require constant voltage for interface, and 1.9V is recommend at Vmode0 and Vmode1 pins.

Application on mobile board

Below figure shows one application example on mobile. C4 and C5 should be placed nearby pin1 and pin10. Transmission line length after PA output should be minimized to reduce conduction loss. When output voltage of mode control pins at base-band chipset is 2.6V, series resistor of 2Kohm is recommended for Vmode0 and 4.7kohm for Vmode1.

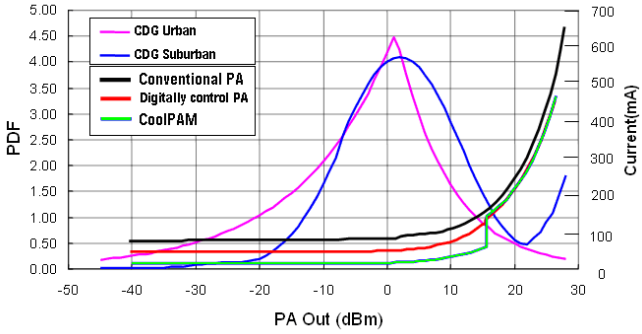


Figure 10. PDF and Current

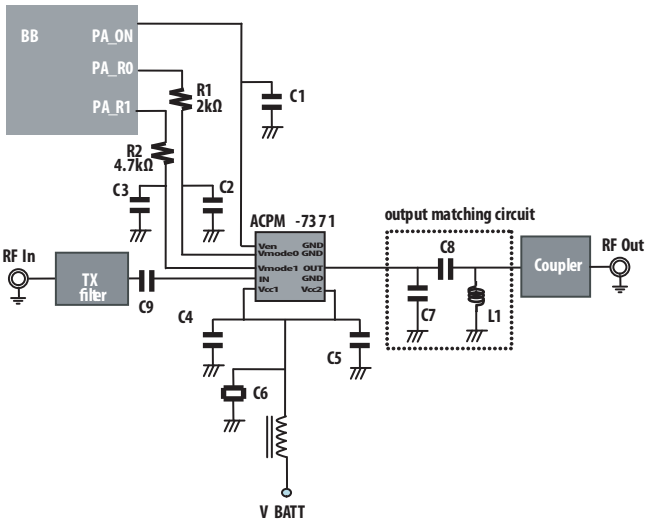


Figure 11. ACPM-7371 Application Example

PCB Design Guidelines

The recommended ACPM-7371 PCB land pattern is shown in Figure 12 and Figure13. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure14. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.10mm (4mils) or 0.127mm (5mils) thick stainless steel which is capable of producing the required fine stencil outline.

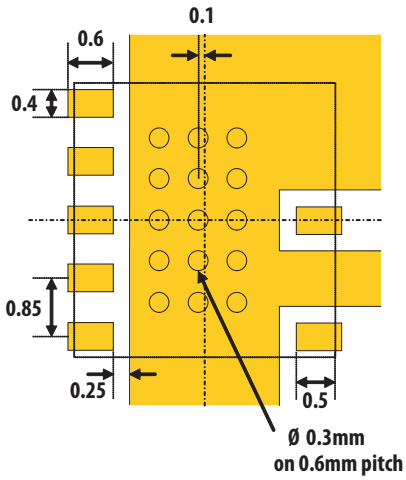


Figure 12. Metallization

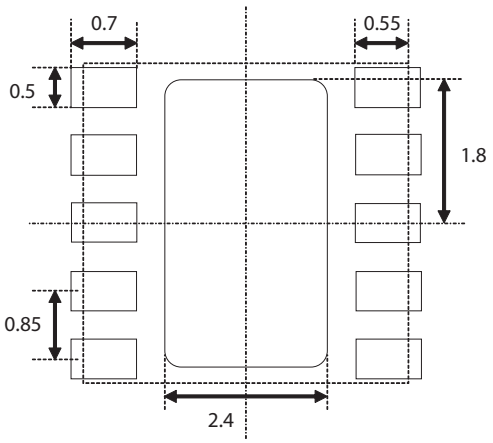


Figure 13. Solder Mask Opening

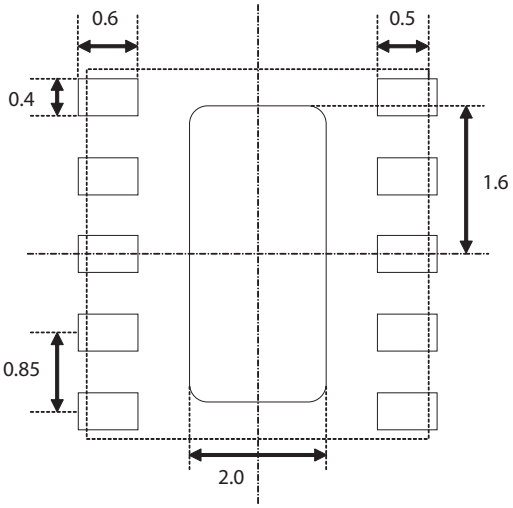
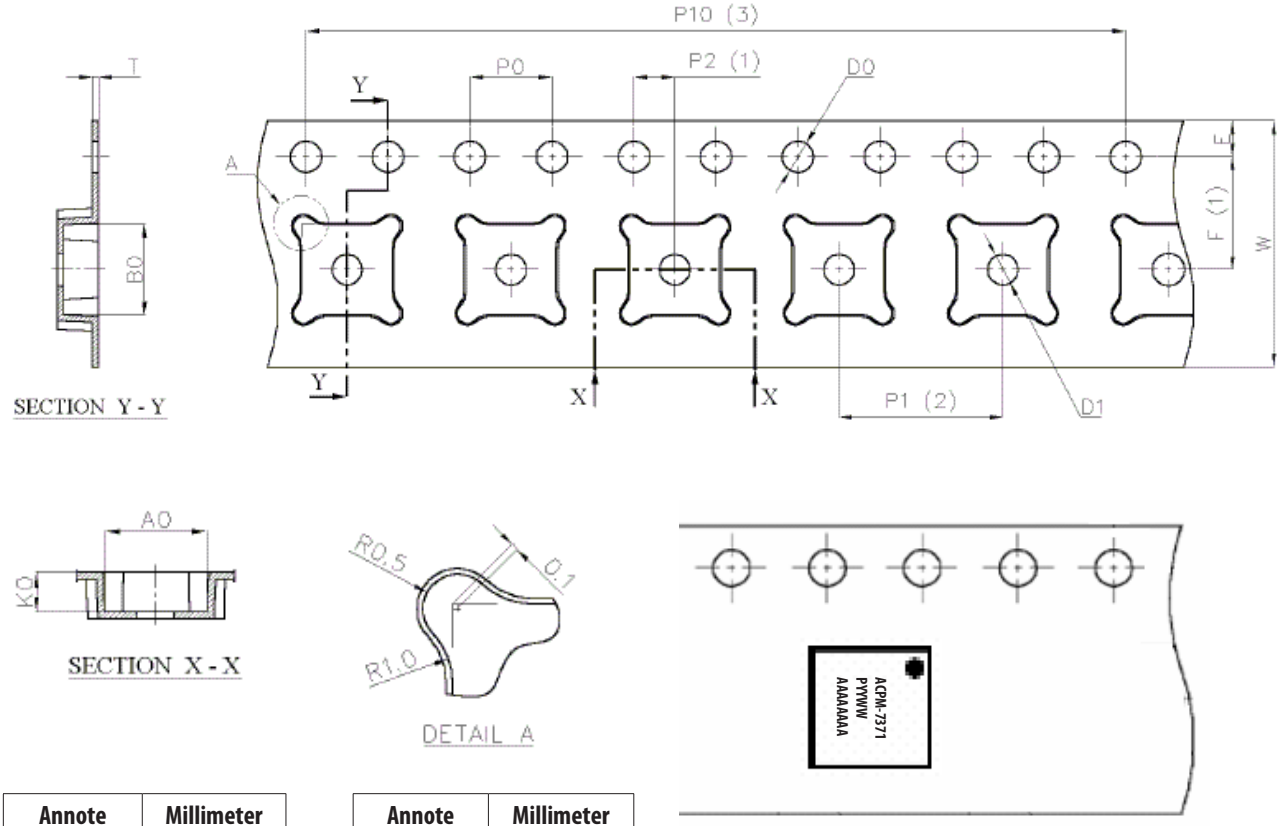


Figure 14. Solder Paste Stencil Aperture

Tape and Reel Information

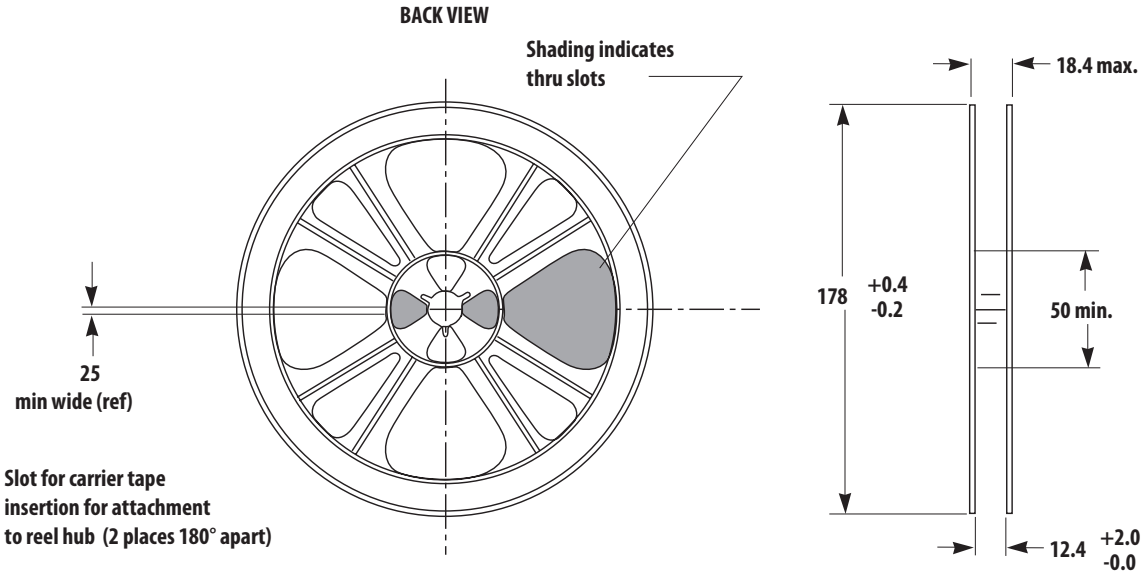


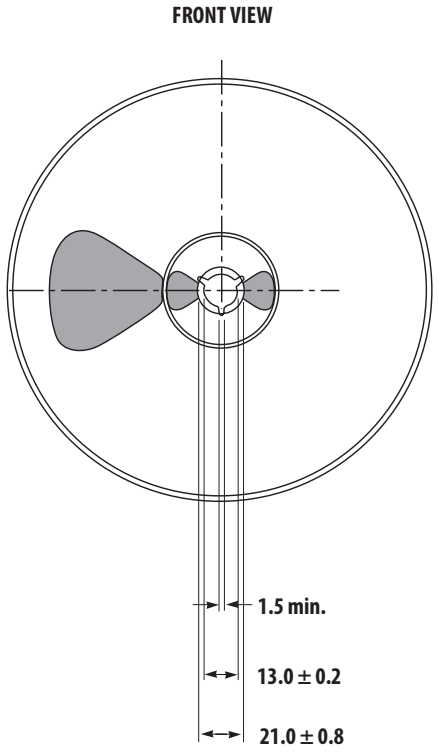
Annote	Millimeter
A0	4.40±0.10
B0	4.40±0.10
K0	1.70±0.10
D0	1.55±0.05
D1	1.60±0.10
P0	4.00±0.10
P1	8.00±0.10

Annote	Millimeter
P2	2.00±0.05
P10	40.00±0.20
E	1.75±0.10
F	5.50±0.05
W	12.00±0.30
T	0.30±0.05

Figure 15. Tape and Reel Format – 4 mm x 4 mm.

Reel Drawing





NOTES:

1. Reel shall be labeled with the following information (as a minimum).
   a. manufacturers name or symbol
   b. Avago Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance (c of c) shall be issued and accompany each shipment of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm)

Figure 16. Plastic Reel Format (all dimensions are in millimeters)

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature.

Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

ACPM-7381 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked. MSL classification reflow temperature for the ACPM-7381 is targeted at 260° +0/-5°C. Figure 17 and Table 7 show typical SMT profile for maximum temperature of 260 +0/-5°C.

Table 6. Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient ≤ 30°C/60% RH or as stated
1	Unlimited at ≤ 30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note :
1. The MSL Level is marked on the MSL Label on each shipping bag.

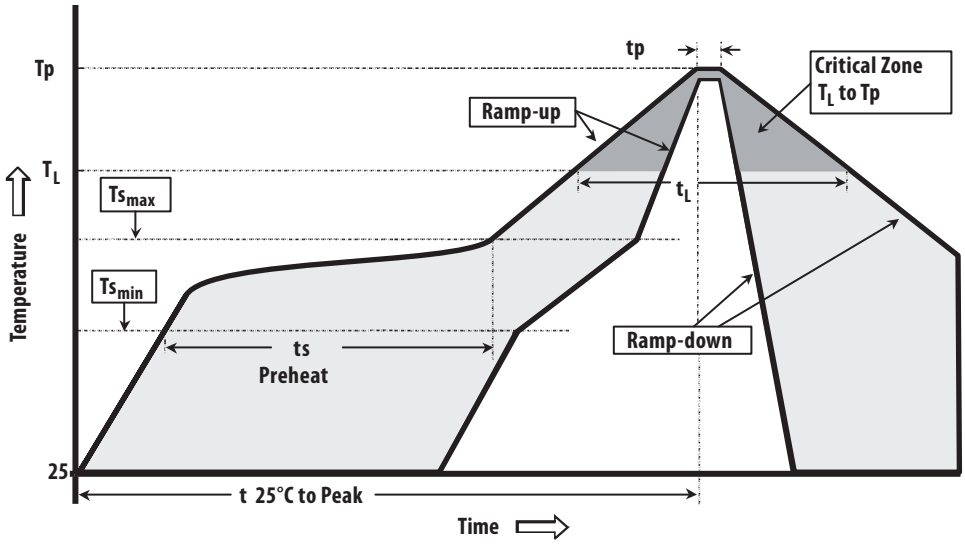


Figure 17. Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5°C

Table 7. Typical SMT Reflow Profile for Maximum Temperature = 260+0 / -5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (TL to TP)	3°C/sec max	3° C/sec max
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	 100°C 150°C 60-120 sec	 150°C 200°C 60-180 sec
Tsmax to TL - Ramp-up Rate		3°C /sec max
Time maintained above: - Temperature (TL) - Time (TL)	 183°C 60-150 sec	 217°C 60-150 sec
Peak temperature (Tp)	240 +0/-5°C	260 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 sec	20-40 sec
Ramp-down Rate	6°C /sec max	6°C /sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.

Storage Condition

Packages described in this document must be stored in sealed moisture barrier, antistatic bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p.7.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30°C and 60% RH.

Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125°C for 12 hours J-STD-033 p.8.

CAUTION

Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 andIPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in Table 6. This approach, however, does not work if the factory humidity or temperature is greater than the testing conditions of 30°/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device.

Table 8 lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperature, 20°, 25°, and 30°C.

This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating Table 9:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121exp (-0.35eV/kT) mm2/s (this used smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity = 1.320exp (-0.35eV/kT) mm2/s (this used largest known Diffusivity @ 30°C).

Table 8. Recommended Equivalent Total Floor Life (days) @ 20°C, 25 °C & 30 °C

For ICs with Novolac, Biphenyl and Multifunctional Epoxies.
(Reflow at same temperature at which the component was classified)

Maximum Percent Relative Humidity

Package Type and Body Thickness	Moisture Sensitivity Level	5%	10%	20%	30%	40%	50%	60%	70%	80%	90%	
Body Thickness ≥3.1 mm Including PQFPs >84 pin, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞	∞	∞	60	41	33	28	10	7	6	30°
		∞	∞	∞	78	53	42	36	14	10	8	25°
		∞	∞	∞	103	69	57	47	19	13	10	20°
	Level 3	∞	∞	10	9	8	7	7	5	4	4	30°
		∞	∞	13	11	10	9	9	7	6	5	25°
		∞	∞	17	14	13	12	12	10	8	7	20°
	Level 4	∞	5	4	4	4	3	3	3	2	2	30°
		∞	6	5	5	5	5	4	3	3	3	25°
		∞	8	7	7	7	7	6	5	4	4	20°
	Level 5	∞	4	3	3	2	2	2	2	1	1	30°
		∞	5	5	4	4	3	3	2	2	2	25°
		∞	7	7	6	5	5	4	3	2	3	20°
	Level 5a	∞	2	1	1	1	1	1	1	1	1	30°
		∞	3	2	2	2	2	2	1	1	1	25°
		∞	5	4	3	3	3	2	2	2	2	20°
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pin SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞	∞	∞	∞	86	39	28	4	3	2	30°
		∞	∞	∞	∞	148	51	37	6	4	3	25°
		∞	∞	∞	∞	∞	69	49	8	5	4	20°
	Level 3	∞	∞	19	12	9	8	7	3	2	2	30°
		∞	∞	25	15	12	10	9	5	3	3	25°
		∞	∞	32	19	15	13	12	7	5	4	20°
	Level 4	∞	7	5	4	4	3	3	2	2	1	30°
		∞	9	7	5	5	4	4	3	2	2	25°
		∞	11	9	7	6	6	5	4	3	3	20°
	Level 5	∞	4	3	3	2	2	2	1	1	1	30°
		∞	5	4	3	3	3	3	2	1	1	25°
		∞	6	5	5	4	4	4	3	3	2	20°
	Level 5a	∞	2	1	1	1	1	1	1	0.5	0.5	30°
		∞	2	2	2	2	2	2	1	1	1	25°
		∞	3	2	2	2	2	2	2	2	1	20°
Body Thickness <2.1 mm including SOICs <18 pin All TQFPs, TSOPs or All BGAs <1 mm body thickness	Level 2a	∞	∞	∞	∞	∞	∞	28	1	1	1	30°
		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°
	Level 3	∞	∞	∞	∞	∞	11	7	1	1	1	30°
		∞	∞	∞	∞	∞	14	10	2	1	1	25°
		∞	∞	∞	∞	∞	20	13	2	2	1	20°
	Level 4	∞	∞	∞	9	5	4	3	1	1	1	30°
		∞	∞	∞	12	7	5	4	2	1	1	25°
		∞	∞	∞	17	9	7	6	2	2	1	20°
	Level 5	∞	∞	13	5	3	2	2	1	1	1	30°
		∞	∞	18	6	4	3	3	2	1	1	25°
		∞	∞	26	8	6	5	4	2	2	1	20°
	Level 5a	∞	10	3	2	1	1	1	1	1	0.5	30°
		∞	13	5	3	2	2	2	1	1	1	25°
		∞	18	6	4	3	2	2	2	2	1	20°

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