ACPM-920502-TR1

3x4 CDMA (BC0/BC10 & BC1) CDMA Dual-Band Power Amplifier Module with Integrated Coupler

Preliminary Data Sheet

Description

The ACPM-920502 is the CDMA dual-band power amplifier module with integrated directional couplers designed for CDMA (3GPP2 BC0/BC10 & BC1) handsets as well as the wireless data card applications. It is designed to meet the stringent linearity requirements of the 3GPP and 3GPP2 standards including the cdma2000, 1xEV-DO Rev.0 and Rev.A while keeping excellent PAE over the entire power range by supporting 2 power modes (low and high power modes). This PA has low quiescent current and high PAE in both power modes. So the average power consumption is minimized to enhance the talk time.

The ACPM-920502 contains integrated directional couplers, 50Ω input and output matching networks, RF input & output DC blocking capacitors as well as the Vcc decoupling/bypass capacitors,. All these functions are integrated in a 16-pin surface-mount leadless package of 3x4 mm form factor and 0.9 mm thickness, so it can minimize the number of external components.

The integrated LB & HB directional couplers are daisy-chained internally. One coupler input port and one coupler output port are shared by the both bands.

The ACPM-920502 has integrated on-chip Vref and on-module bias switch, so the external LDO regulators and switches for external Vref are not required. It also makes the PA fully digital-controllable by the baseband chipset. The Ven pin turns the PA on and off by the digital control signal. All of the digital control input pins such as the Ven and Vmode are fully CMOS compatible down to the 1.8V logic.

The ACPM-920502 is manufactured on an advanced InGaP/GaAs HBT technology that provides excellent performance, temperature stability, ruggedness, and reliability.

Features

- CDMA dual-band PA supporting CDMA (BC0 / BC10, BC1)
- 2-mode power/gain control (low power and high power modes)
- Integrated daisy-chained LB & HB directional couplers
- High directivity (small coupled power or delivered power variation into mismatched load)
- Excellent PAE in low and mid power ranges.
- Low quiescent current in low power mode
- Excellent average power consumption and talk-time
- Spectral linearity supporting IS-95, cdma2k, 1xEV-DO Rev.0 & Rev.A
- Internally matched 50Ω RF input & output ports
- Internal RF input & output DC blocking capacitors
- Internal Vcc1 & Vcc2 bypass capacitors
- Internal Vref eliminating external LDO regulators and switches
- 1.8V CMOS compatible control logics (V_H=1.35V~3.1V)
- 3x4x0.9mm 16-pad leadless surface-mount package
- Lead-free, RoHS compliant, Halogen-free, Sb-free, Green

Applications

- CDMA (BC0 / BC10 & BC1) dual -band handsets, Wireless USB data card dongles and embedded data cards.

Ordering Information

Part Number	Number of Devices	Container
ACPM-920502-TR1	1000	Tape & Reel (7”)

Absolute Maximum Ratings

- Stresses in excess of the absolute ratings may cause permanent damage. Exposure to absolute ratings for extended periods of time may adversely affect reliability. Functional operation is not implied under these conditions.

Description	Condition	Min	Nominal	Max	Unit	Associated Pins
DC Supply Voltage (Vcc)	RF Off, Z_S=Z_L=50Ω	-	-	+5.0	V	Vcc1, Vcc2
	RF On, Z_S=Z_L=50Ω	-	-	+4.5	V	Vcc1, Vcc2
Enable Control Voltage (Ven_LB, Ven_HB)		-	-	+3.3	V	Ven_LB, Ven_HB
Mode Control Voltage (Vmode)		-	-	+3.3	V	Vmode
RF Input Power (Pin)	Z_S=Z_L=50Ω	-	-	+10	dBm	RFin_LB, RFin_HB
Storage Temperature (Tstg)		-55	-	+125	℃	

No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value

Recommended Operating Condition

Description		Min	Nominal	Max	Unit
DC Supply Voltage	VCC1 VCC2	3.2 0.5	3.4 3.4	4.35 3.4	V V
Enable Control Voltage (Ven_LB, Ven_HB)	V_{LOW} V_{HIGH}	0 1.35	0 1.8	0.5 3.1	V V
Enable Control Current (Ien_LB, Ien_HB)		-	-	0.1	mA
Mode Control Voltage (Vmode)	V_{LOW} V_{HIGH}	0 1.35	0 1.8	0.5 3.1	V V
Mode Control Current (Imode)		-	-	0.1	mA
Operating Frequency (fc)	LB – CDMA	817		849	MHz
	HB – CDMA	1850		1910	MHz
Case Temperature (Tc) – CDMA		-30	+25	+85	℃

Operating Logic Table

Selected Band & Power Mode	Vcc1 / Vcc2	Ven_LB	Ven_HB	Vmode
LB HPM (Low Band High Power Mode)	On	H	L	L
LB LPM (Low Band Low Power Mode)	On	H	L	H
HB HPM (High Band High Power Mode)	On	L	H	L
HB LPM (High Band Low Power Mode)	On	L	H	H
PDM (Power Down Mode)	On	L	L	X

Electrical Characteristics

- Conditions: Vcc=3.4V, Ta=25℃, Z_{SOURCE} = Z_{LOAD} = 50Ω
- Signal Configuration: cdma2k 1x RC1 RL unless specified otherwise

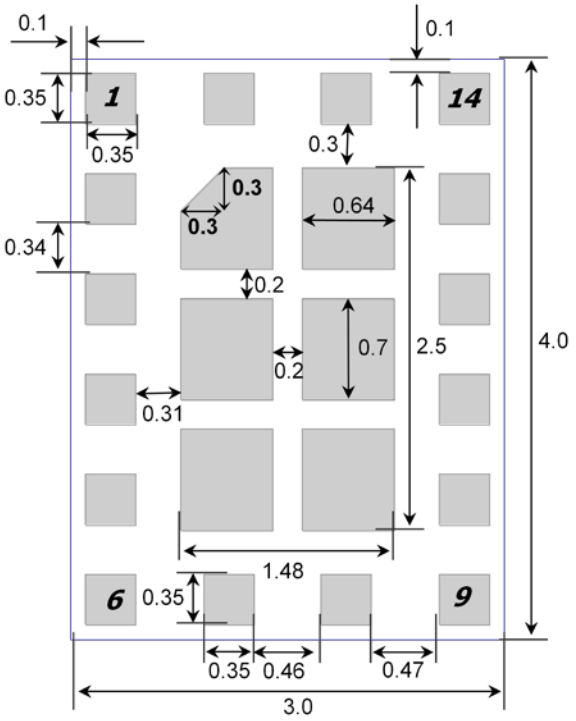
CDMA Cellular (3GPP2 BC0 / BC10)

Characteristics		Condition	Min	Typ	Max	Unit
Operating Frequency Range		CDMA	817	-	849	MHz
Maximum Linear Output Power		CDMA (1x RC1 RL), HPM	27.8	-	-	dBm
		CDMA (1x RC1 RL), LPM	16	-	-	dBm
Gain		HPM, Pout=27.8dBm, CDMA 1x RC1		27		dB
		LPM, Pout=16dBm, CDMA 1x RC1		16		dB
PAE		CDMA 1x RC1, HPM, Pout=27.8dBm		40.2		%
		CDMA 1x RC1, LPM, Pout=16dBm		14.3		%
Total Supply Current		CDMA 1x RC1, HPM, Pout=27.8dBm	-	440		mA
		CDMA 1x RC1, LPM, Pout=16dBm	-	80		mA
Quiescent Current		HPM	-	85		mA
		LPM	-	15		mA
Enable Control Current		HPM, Ven_HB=1.8V	-		10	μA
		LPM, Ven_HB=1.8V	-		10	μA
Mode Control Current		LPM, Vmode=1.8V	-		10	μA
Total Current in Power Down Mode		Ven_LB=Ven_HB=0V, Vmode=0V	-		5	μA
CDMA Adjacent Channel Power Ratio	fc+/-885kHz /30kHz	CDMA 1x RC1, HPM, Pout=27.8dBm CDMA 1x RC1, LPM, Pout=16dBm	-	-	-45 -45	dBc
	fc+/-1.98MHz /30kHz	CDMA 1x RC1, HPM, Pout=27.8dBm CDMA 1x RC1, LPM, Pout=16dBm	-	-	-56 -56	dBc
Out-Of-Band Emission to PSB	At 816MHz	CDMA 1x RC1, fc=817.9MHz		-	-35	dBm/30kHz
Harmonic Suppression	2nd 3rd	CDMA 1x RC1, HPM, Pout=27.8dBm, Harmonic Power over 1MHz	- -	- -	-30 -30	dBc
Input VSWR			-	2.0 : 1		
Rx Band Noise		HPM, Pout=27.8dBm, Vcc=4.2V	-	-	TBD	dBm/Hz
GPS Band Noise		HPM, Pout=27.8dBm, Vcc=4.2V	-	-	TBD	dBm/Hz
Coupling Factor		Pout - Pcpl, RFout & Coupled Port Z_{LOAD} = 50Ω	-	20	-	dB
Delivered Power Variation under Load Mismatch		Load VSWR = 2.5:1, All Phase, Constant Pcpl	-	±0.5	±1.0	dB
Stability (Spurious Output)		In-Band Load VSWR ≤ 5:1 All Phase, Pout≤27.8dBm & Pin≤6dBm	-	-	-60	dBc
Ruggedness		Pout≤27.8dBm & Pin≤10dBm, All Phase, No Damage or Degradation	-	-	10:1	VSWR

CDMA PCS (3GPP2 BC1)

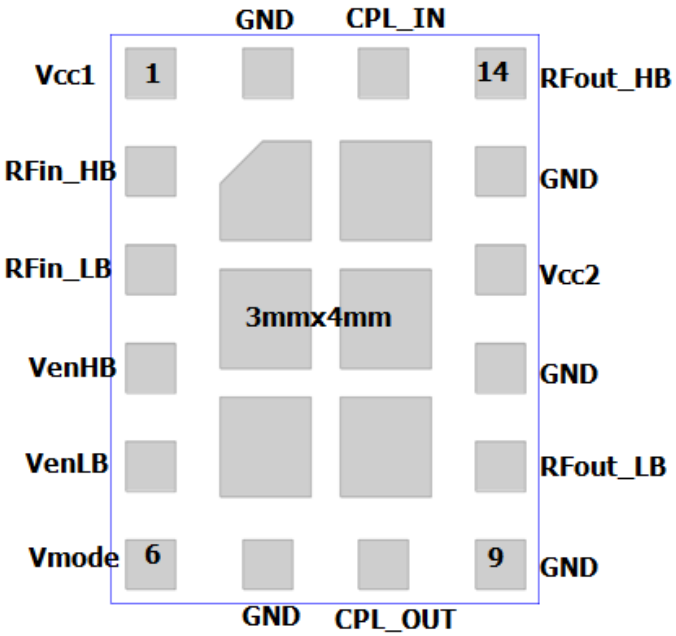
Characteristics		Condition	Min	Typ	Max	Unit
Operating Frequency Range		CDMA	1850	-	1910	MHz
Maximum Linear Output Power		CDMA (1x RC1 RL), HPM	28.4	-	-	dBm
		CDMA (1x RC1 RL), LPM	16	-	-	dBm
Gain		HPM, Pout=28.4dBm, CDMA 1x RC1		27		dB
		LPM, Pout=16dBm, CDMA 1x RC1		20		dB
PAE		CDMA 1x RC1, HPM, Pout=28.4dBm		43.2		%
		CDMA 1x RC1, LPM, Pout=16dBm		15.85		%
Total Supply Current		CDMA 1x RC1, HPM, Pout=28.4dBm	-	470		mA
		CDMA 1x RC1, LPM, Pout=16dBm	-	90		mA
Quiescent Current		HPM	-	85		mA
		LPM	-	16		mA
Enable Control Current		HPM, Ven_LB=1.8V	-		10	μA
		LPM, Ven_LB=1.8V	-		10	μA
Mode Control Current		LPM, Vmode=1.8V	-		10	μA
Total Current in Power Down Mode		Ven_LB=Ven_HB=0V, Vmode=0V	-		5	μA
CDMA Adjacent Channel Power Ratio	fc+/-1.25MHz /30kHz	CDMA 1x RC1, HPM, Pout=28.4dBm CDMA 1x RC1, LPM, Pout=16dBm	-	-	-45 -45	dBc
	fc+/-1.98MHz /30kHz	CDMA 1x RC1, HPM, Pout=28.4dBm CDMA 1x RC1, LPM, Pout=16dBm	-	-	-53 -53	dBc
Harmonic Suppression	2nd 3rd	CDMA 1x RC1, HPM, Pout=28.4dBm, Harmonic Power over 1MHz	- -	- -	-30 -40	dBc
Input VSWR			-	2.0:1		-
Rx Band Noise		HPM, Pout=28.4dBm, Vcc=4.2V	-	-	TBD	dBm/Hz
GPS Band Noise		HPM, Pout=28.4dBm, Vcc=4.2V	-	-	TBD	dBm/Hz
Coupling Factor		Pout - Pcpl, RFout & Coupled Port Z_{LOAD} = 50Ω	-	20	-	dB
Delivered Power Variation under Load Mismatch		Load VSWR = 2.5:1, All Phase, Constant Pcpl	-	±0.5	±1.0	dB
Stability (Spurious Output)		In-Band Load VSWR ≤ 5:1, All Phase, Pout≤28.4dBm & Pin≤6dBm	-	-	-60	dBc
Ruggedness		Pout≤28.4dBm & Pin≤10dBm, All Phase, No Damage or Degradation	-	-	10:1	VSWR

Foot Print



All dimensions are in mm

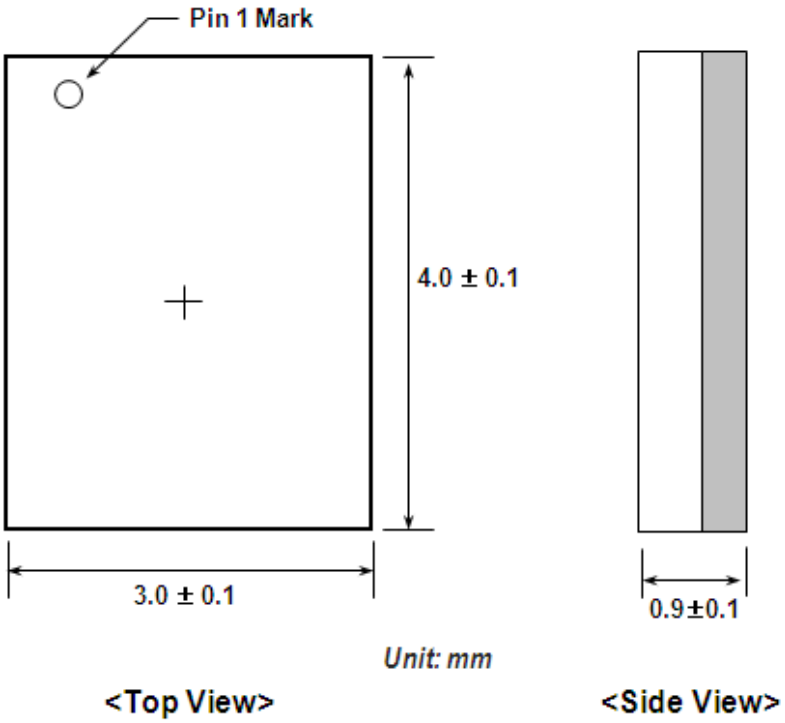
X-Ray Top View through Package



Pin Descriptions

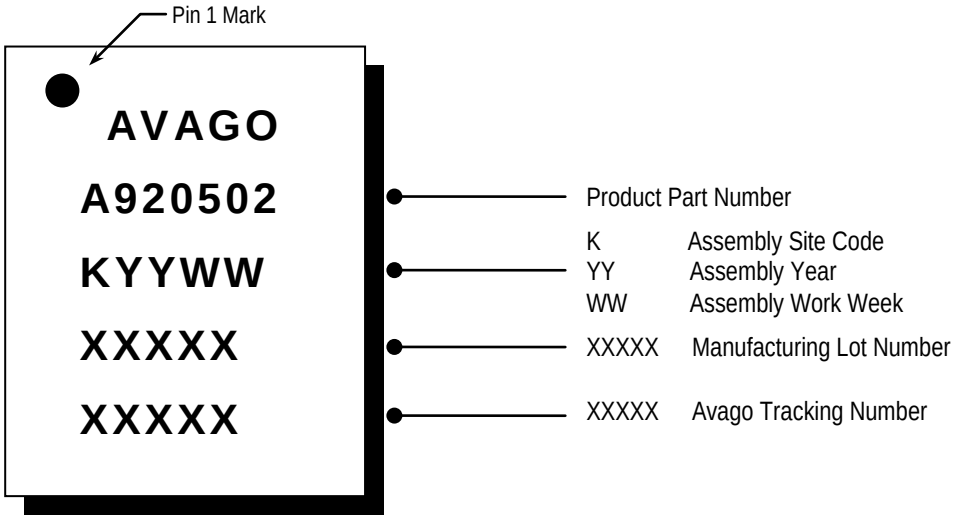
Pin #	Name	Description
1	Vcc1	Supply Voltage 1
2	RFin_HB	High Band RF Input
3	RFin_LB	Low Band RF Input
4	Ven_HB	High Band PA Enable
5	Ven_LB	Low Band PA Enable
6	Vmode	Mode Control
7	Gnd	Ground
8	Cpl_out	Coupled Out
9	Gnd	Ground
10	RFout_LB	Low Band RF Output
11	Gnd	Ground
12	Vcc2	Supply Voltage 2
13	Gnd	Ground
14	RFout_HB	High Band RF Output
15	Cpl_in	Coupled In
16	Gnd	Ground

Package Dimensions



All dimensions are in millimeter

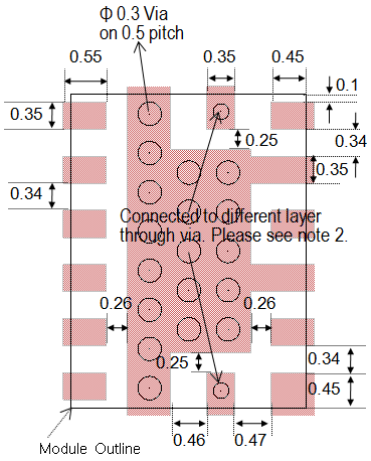
Marking Specification



Note:

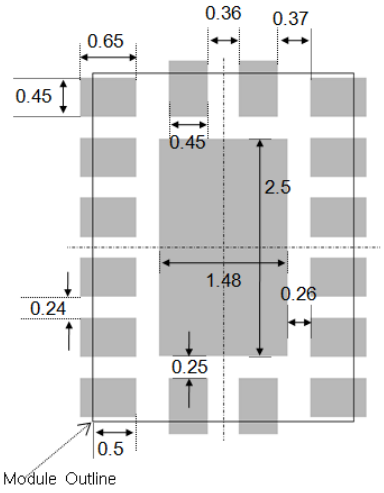
1. Prior to production release, the marking will be 'E920502'. After the completion of Avago qualification testing and production release, the marking will revert to 'A920502'.
2. Upon mass production lots or samples 5th coding line will be add in.

Metallization



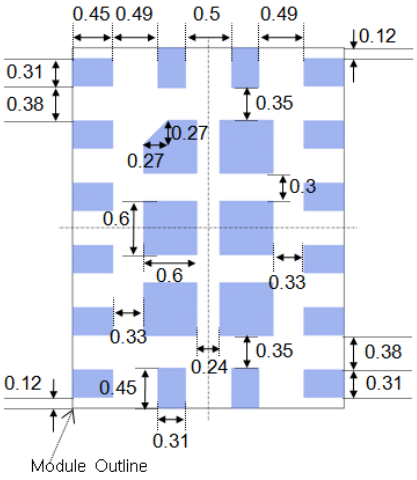
<X-Ray Top View>

Solder Mask Opening



<X-Ray Top View>

Solder Paste Stencil Aperture



<X-Ray Top View>

PCB Design Guidelines

The recommended PCB land pattern is shown in figures on the left side. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

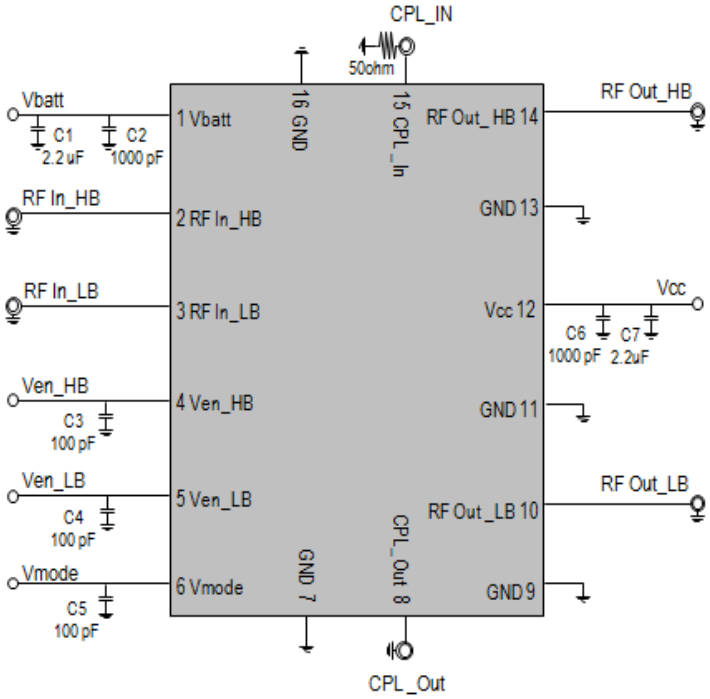
Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.

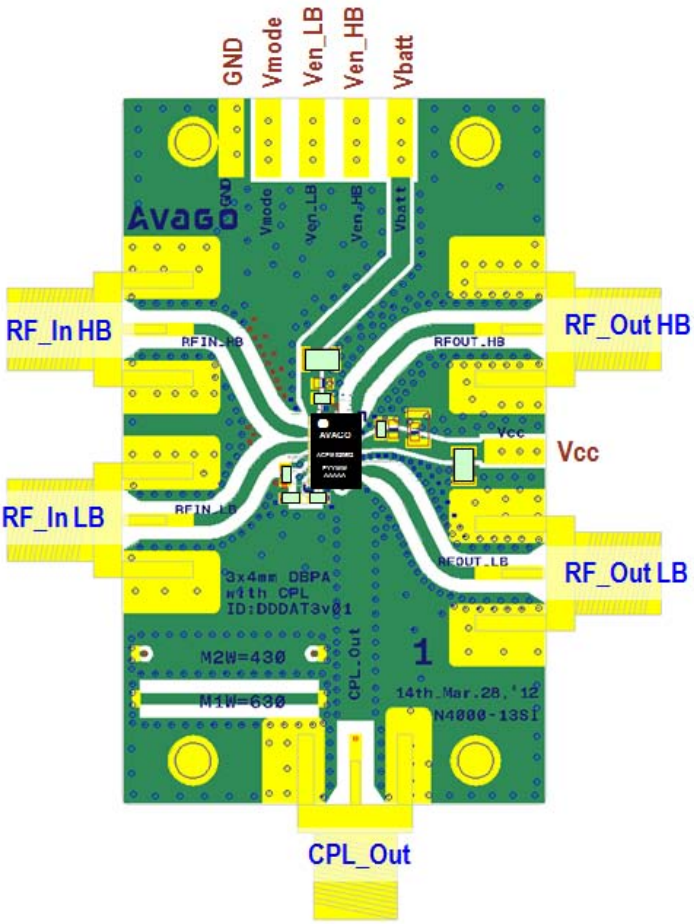
The recommended stencil layout is shown here. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100mm(4mils) or 0.127mm(5mils) thick stainless steel which is capable of producing the required fine stencil outline.

Notes :
1. Dimensions in millimeters
2. CPL line in the different layer from RF OUT_LB/HB line with proper isolation is preferable for accurate coupling power detection.

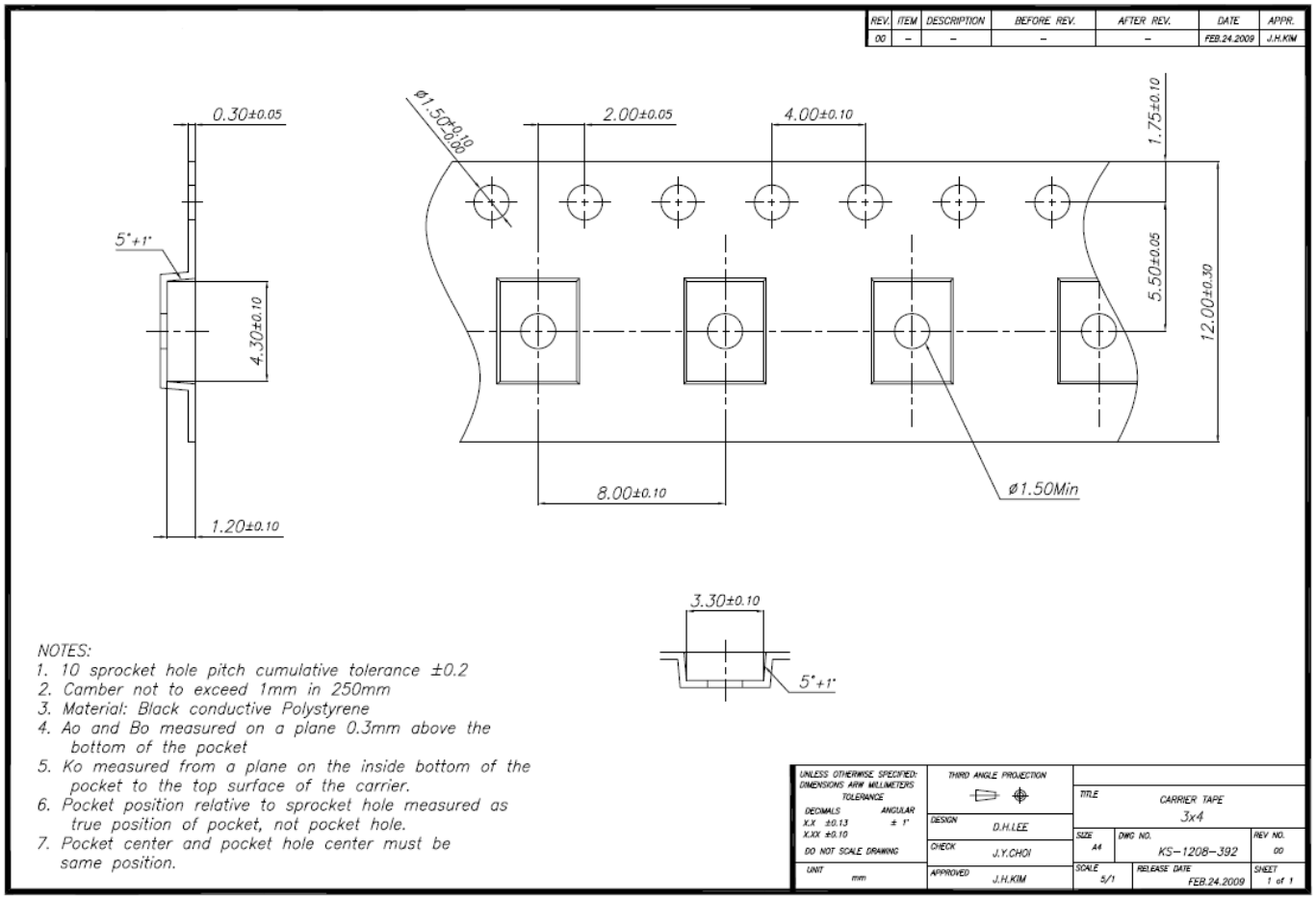
Evaluation Board Schematic

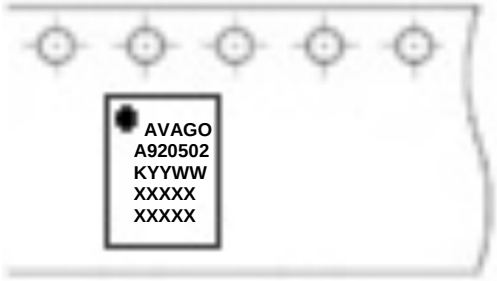


Evaluation Board Description



Tape and Reel Information

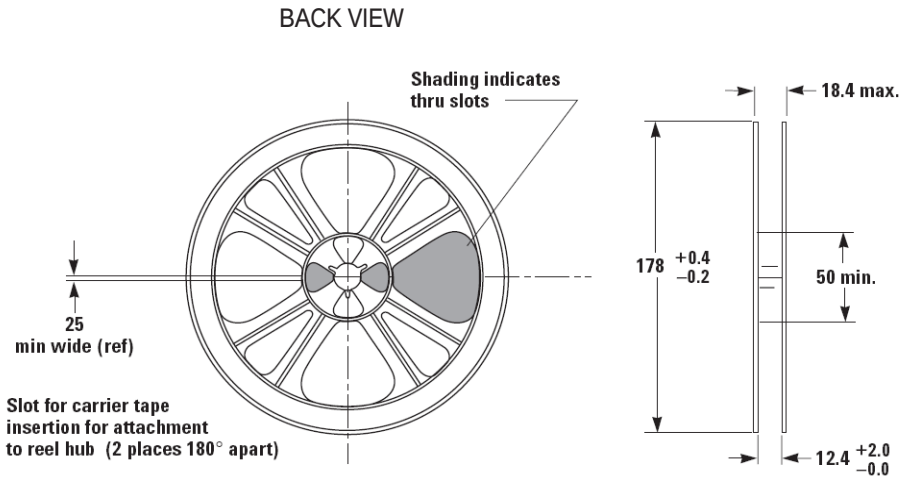


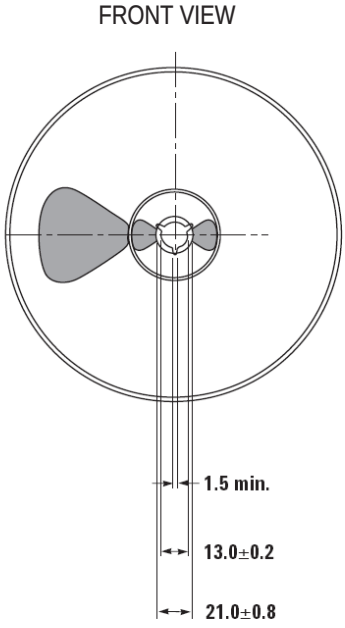


Dimension List

Tape and Reel Format – 3 mm x 4 mm.

Reel Drawing





NOTES:

1. Reel shall be labeled with the following information (as a minimum).
   a. manufacturers name or symbol
   b. Agilent Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance (c of c) shall be issued and accompany each shipment of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm)

Plastic Reel Format (all dimensions are in millimeters)

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature.

Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

The ACPM-920502 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked. MSL classification reflow temperature for the ACPM-920502 is targeted at 260℃ +0/-5℃. Figure and table on next page show typical SMT profile for maximum temperature of 260 +0/-5℃.

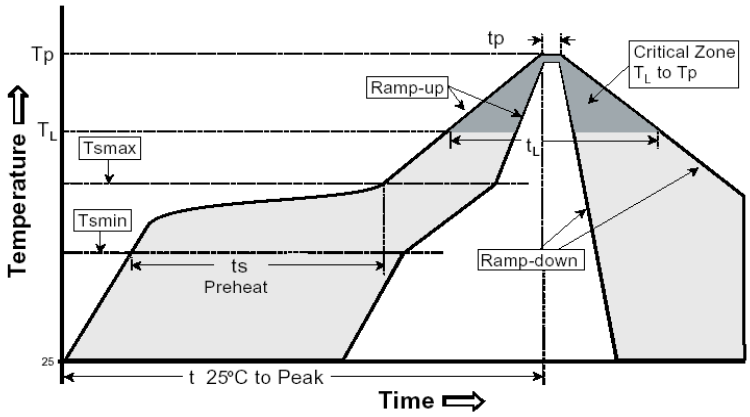
Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient =< 30oC/60% RH or as stated
1	Unlimited at =< 30oC/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note :

1. The MSL Level is marked on the MSL Label on each shipping bag.

Reflow Profile Recommendations



Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5℃

Typical SMT Reflow Profile for Maximum Temperature = 260 +0/ -5℃

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (TL to TP)	3℃/sec max	3℃ /sec max
Preheat		
- Temperature Min (Tsmin)	100℃	150℃
- Temperature Max (Tsmax)	150℃	200℃
- Time (min to max) (ts)	60-120 sec	60-180 sec
Tsmax to TL		
- Ramp-up Rate		3℃ /sec max
Time maintained above:		
- Temperature (TL)	183℃	217℃
- Time (TL)	60-150 sec	60-150 sec
Peak temperature (Tp)	240 +0/-5℃	260 +0/-5℃
Time within 5℃ of actual Peak Temperature (tp)	10-30 sec	20-40 sec
Ramp-down Rate	6℃ /sec max	6℃ /sec max
Time 25℃ to Peak Temperature	6 min max.	8 min max.

Storage Condition

moisture barrier, antistatic bags. Shelf life in a sealed moisture barrier bag is 12 months at <40℃ and 90% relative humidity (RH) J-STD-033 p.7.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30℃ and 60% RH.

Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125℃ for 12 hours J-STD-033 p.8.

CAUTION

Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200℃. This method will minimize moisture related component damage. If any component temperature exceeds 200℃, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125℃. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125℃. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 andIPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in next table. This approach, however, does not work if the factory humidity or temperature is greater than the testing conditions of 30℃/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidity and temperatures based on the nominal plastic thickness for each device.

Table on next page lists equivalent derated floor lives for humidity ranging from 20-90% RH for three temperature, 20℃, 25℃, and 30℃.

Table on next page is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating this table:

1. Activation Energy for diffusion = 0.35eV (smallest known value).

2. For ≤60% RH, use Diffusivity = 0.121exp (-0.35eV/kT) mm2/s

   (this used smallest known Diffusivity @ 30℃).

3. For >60% RH, use Diffusivity = 1.320exp (-0.35eV/kT) mm2/s

   (this used largest known Diffusivity @ 30℃).

Recommended Equivalent Total Floor Life (days) @ 20°C, 25 °C & 30 °C, 35 °C

For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified)
Maximum Percent Relative Humidity

Maximum Percent Relative Humidity												
Package Type and Body Thickness	Moisture Sensitivity Level	5%	10%	20%	30%	40%	50%	60%	70%	80%	90%	
Body Thickness ≥3.1 mm Including PQFPs >84 pin, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞	∞	94	44	32	26	16	7	5	4	35°C
		∞	∞	124	60	41	33	28	10	7	6	30°C
		∞	∞	167	78	53	42	36	14	10	8	25°C
		∞	∞	231	103	69	57	47	19	13	10	20°C
	Level 3	∞	∞	8	7	6	6	6	4	3	3	35°C
		∞	∞	10	9	8	7	7	5	4	4	30°C
		∞	∞	13	11	10	9	9	7	6	5	25°C
		∞	∞	17	14	13	12	12	10	8	7	20°C
	Level 4	∞	3	3	3	2	2	2	2	1	1	35°C
		∞	5	4	4	4	3	3	3	2	2	30°C
		∞	6	5	5	5	5	4	3	3	3	25°C
		∞	8	7	7	7	7	6	5	4	4	20°C
	Level 5	∞	2	2	2	2	1	1	1	1	1	35°C
		∞	4	3	3	2	2	2	2	1	1	30°C
		∞	5	5	4	4	3	3	2	2	2	25°C
		∞	7	7	6	5	5	4	3	3	3	20°C
	Level 5a	∞	1	1	1	1	1	1	1	1	1	35°C
		∞	2	1	1	1	1	1	1	1	1	30°C
		∞	3	2	2	2	2	2	1	1	1	25°C
		∞	5	4	3	3	3	2	2	2	2	20°C
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pin SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞	∞	∞	∞	58	30	22	3	2	1	35°C
		∞	∞	∞	∞	86	39	28	4	3	2	30°C
		∞	∞	∞	∞	148	51	37	6	4	3	25°C
		∞	∞	∞	∞	∞	69	49	8	5	4	20°C
	Level 3	∞	∞	12	9	7	6	5	2	2	1	35°C
		∞	∞	19	12	9	8	7	3	2	2	30°C
		∞	∞	25	15	12	10	9	5	3	3	25°C
		∞	∞	32	19	15	13	12	7	5	4	20°C
	Level 4	∞	5	4	3	3	2	2	1	1	1	35°C
		∞	7	5	4	4	3	3	2	2	1	30°C
		∞	9	7	5	5	4	4	3	2	2	25°C
		∞	11	9	7	6	6	5	4	3	3	20°C
	Level 5	∞	3	2	2	2	2	1	1	1	1	35°C
		∞	4	3	3	2	2	2	1	1	1	30°C
		∞	5	4	3	3	3	3	2	1	1	25°C
		∞	6	5	5	4	4	4	3	3	2	20°C
	Level 5a	∞	1	1	1	1	1	1	1	0.5	0.5	35°C
		∞	2	1	1	1	1	1	1	0.5	0.5	30°C
		∞	2	2	2	2	2	2	1	1	1	25°C
		∞	3	2	2	2	2	2	2	2	1	20°C
Body Thickness <2.1 mm including SOICs <18 pin All TQFPs, TSOPs or All BGAs <1 mm body thickness	Level 2a	∞	∞	∞	∞	∞	∞	17	1	0.5	0.5	35°C
		∞	∞	∞	∞	∞	∞	28	1	1	1	30°C
		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°C
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°C
	Level 3	∞	∞	∞	∞	∞	8	5	1	0.5	0.5	35°C
		∞	∞	∞	∞	∞	11	7	1	1	1	30°C
		∞	∞	∞	∞	∞	14	10	2	1	1	25°C
		∞	∞	∞	∞	∞	20	13	2	2	1	20°C
	Level 4	∞	∞	∞	7	4	3	2	1	0.5	0.5	35°C
		∞	∞	∞	9	5	4	3	1	1	1	30°C
		∞	∞	∞	12	7	5	4	2	1	1	25°C
		∞	∞	∞	17	9	7	6	2	2	1	20°C
	Level 5	∞	∞	7	3	2	2	1	1	0.5	0.5	35°C
		∞	∞	13	5	3	2	2	1	1	1	30°C
		∞	∞	18	6	4	3	3	2	1	1	25°C
		∞	∞	26	8	6	5	4	2	2	1	20°C
	Level 5a	∞	7	2	1	1	1	1	1	0.5	0.5	35°C
		∞	10	3	2	1	1	1	1	1	0.5	30°C
		∞	13	5	3	2	2	2	1	1	1	25°C
		∞	18	6	4	3	2	2	2	2	1	20°C

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