ACR3200VR33

Bypass Thyristor

Replaces DS6189-2 DS6189-3 September 2020 (LN40219)

FEATURES

- Double Side Cooling
- High Surge Capability
- Very Low Cosmic Ray FIT Rating
- High dV/dt Rating

APPLICATIONS

- Multi-level VSC Bypass thyristor for HVDC

KEY PARAMETERS

V_{DRM}	**1000V**
V_{DRM}	**3300V**
$I_{T(AV)}$	**3200A**
I_{TSM}	**43000A**
dV/dt	**10kV/µs**
dI/dt	**400A/µs**

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} (V)	Conditions
ACR3200VR33	1000 / 3300	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 400mA, V_{DRM}, V_{RRM} t_p = 10ms

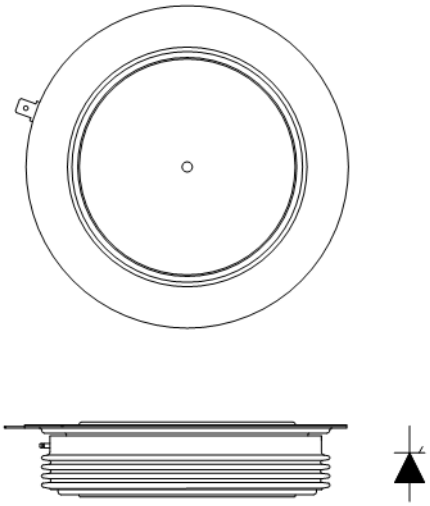
ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

ACR3200VR33

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.



Outline type code: V

(See Package Details for further information)

Fig. 1 Package outline

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3200	A
$I_{T(RMS)}$	RMS value	-	5030	A
I_T	Continuous (direct) on-state current	-	4900	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	43	kA
I^2t	I^2t for fusing	V_R = 0	9.24	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	0.00746	°C/W
		Single side cooled	Anode DC	-	0.0130	°C/W
			Cathode DC	-	0.0178	°C/W
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 54kN (with mounting compound)	Double side	-	0.002	°C/W
			Single side	-	0.004	°C/W
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			48	59	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	400	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 60°C, gate open		-	10000	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$ Gate source 30V, 10Ω t_r < 0.5µs, T_j = 125°C	Non-repetitive	-	400	A/µs
$V_{T(TO)}$	Threshold voltage - Low level	300A to 2300A at T_{case} = 125°C		-	0.83	V
	Threshold voltage - High level	2300A to 8000A at T_{case} = 125°C		-	1.04	V
r_T	On-state slope resistance - low level	300A to 2300A at T_{case} = 125°C		-	0.24	mΩ
	On-state slope resistance - High level	2300A to 8000A at T_{case} = 125°C		-	0.15	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, I_g = 3A t_r = 0.5µs, T_j = 25°C, t_p = 40µs		-	3	µs
V_{pu}	Pick-up Voltage	I_g = 3A, t_r = 0.5µs, T_j =25°C, t_p = 40µs		-	2	V
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V_{DRM}, T_{case} = 125°C	TBD	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	350	mA
I_{GD}	Gate non-trigger current	At 50% V_{DRM}, T_{case} = 125°C	TBD	mA

CURVES

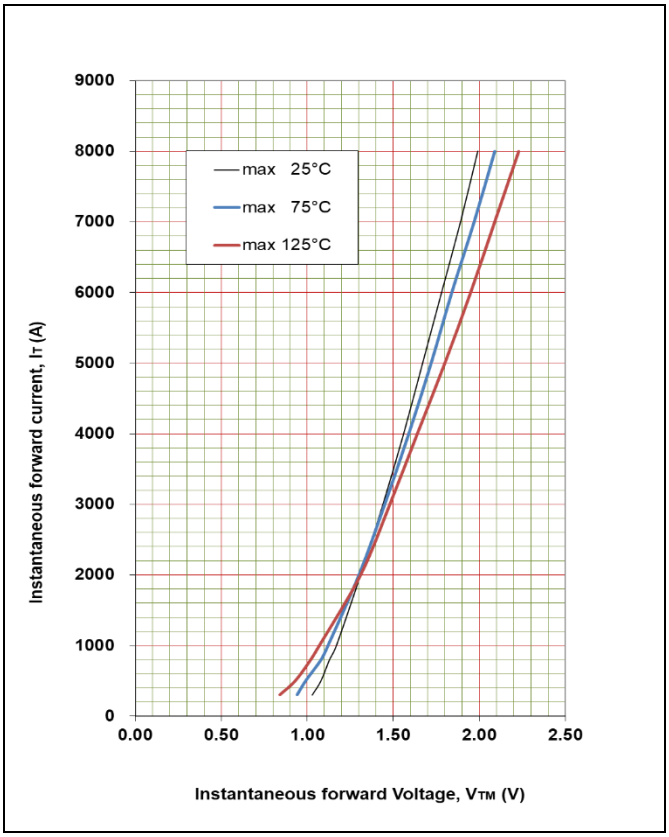


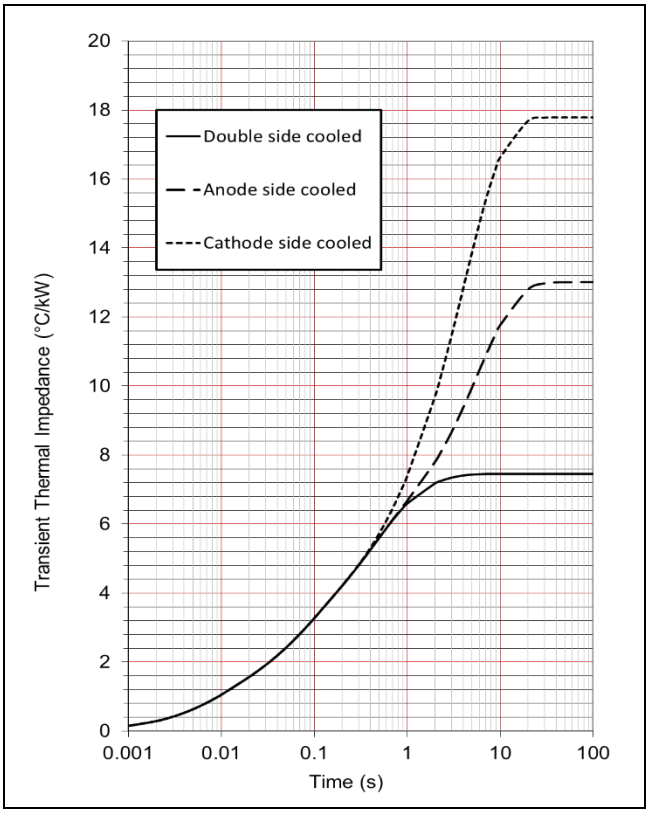
Fig. 2 Maximum on state characteristics

V_{TM} EQUATION

$V_{TM} = A + B.\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = -0.303672
B = 0.216168
C = 0.000164
D = -0.007999

These values are valid for T_j = 125°C for I_T 300A to 8000A



		1	2	3	4
Double side cooled	Ri(°C/kW)	0.9206	1.8299	3.4022	1.3044
	Ti(s)	0.007681	0.05795	0.4079	1.2085
Anode side cooled	Ri(°C/kW)	0.9032	1.6719	3.0101	7.4269
	Ti(s)	0.007587	0.05365	0.3145	5.6240
Cathode side cooled	Ri(°C/kW)	0.9478	2.0661	1.6884	13.0847
	Ti(s)	0.007844	0.06455	0.3894	4.1447

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	$\Delta Z_{th}(z)$	
θ°	sine.	rect.
180	1.34	0.88
120	1.57	1.30
90	1.83	1.54
60	2.08	1.81
30	2.27	2.11
15	2.36	2.28

Anode Side Cooling		
	$\Delta Z_{th}(z)$	
θ°	sine.	rect.
180	1.34	0.88
120	1.57	1.30
90	1.84	1.54
60	2.08	1.81
30	2.28	2.11
15	2.37	2.28

Cathode Sided Cooling		
	$\Delta Z_{th}(z)$	
θ°	sine.	rect.
180	1.33	0.88
120	1.57	1.29
90	1.83	1.53
60	2.07	1.80
30	2.26	2.10
15	2.35	2.26

Fig. 3 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

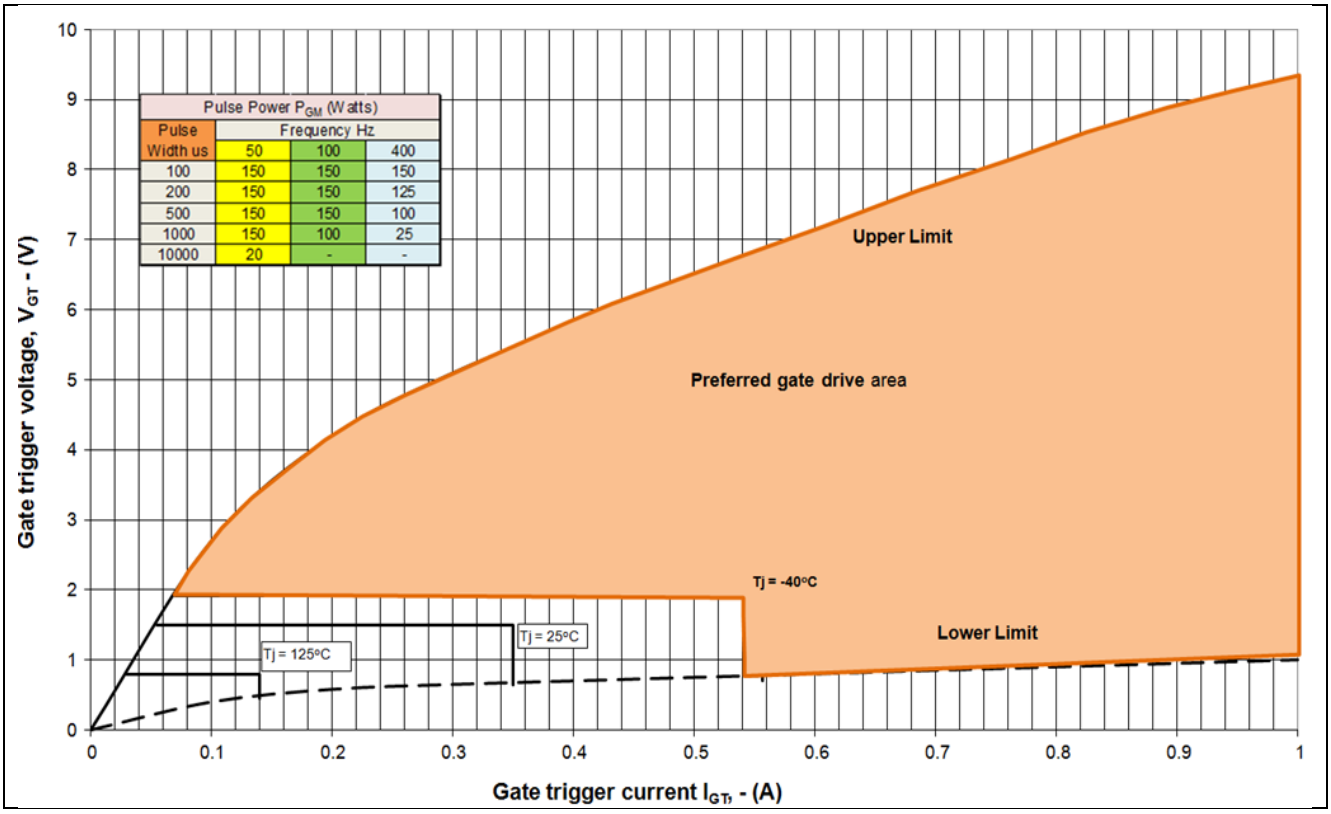


Fig. 4 Gate characteristics

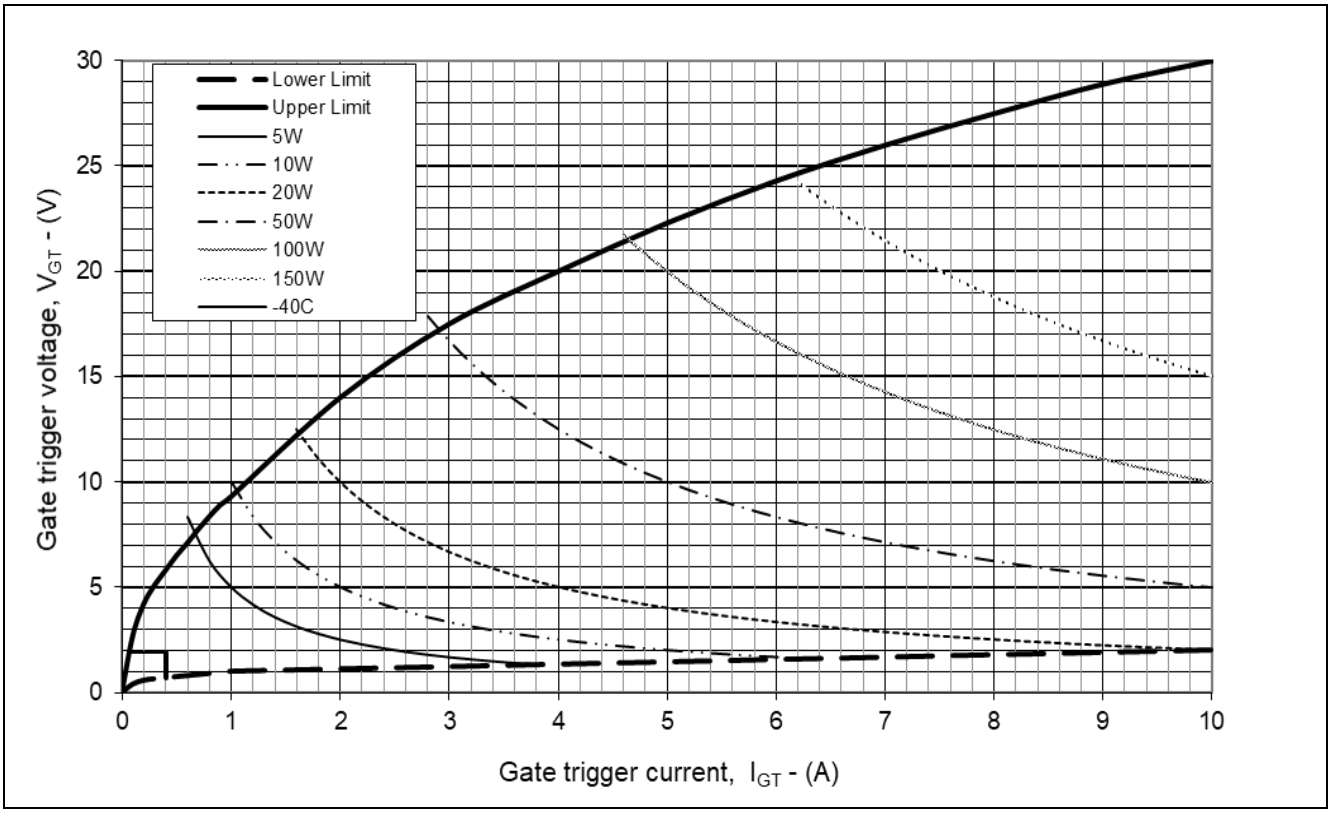


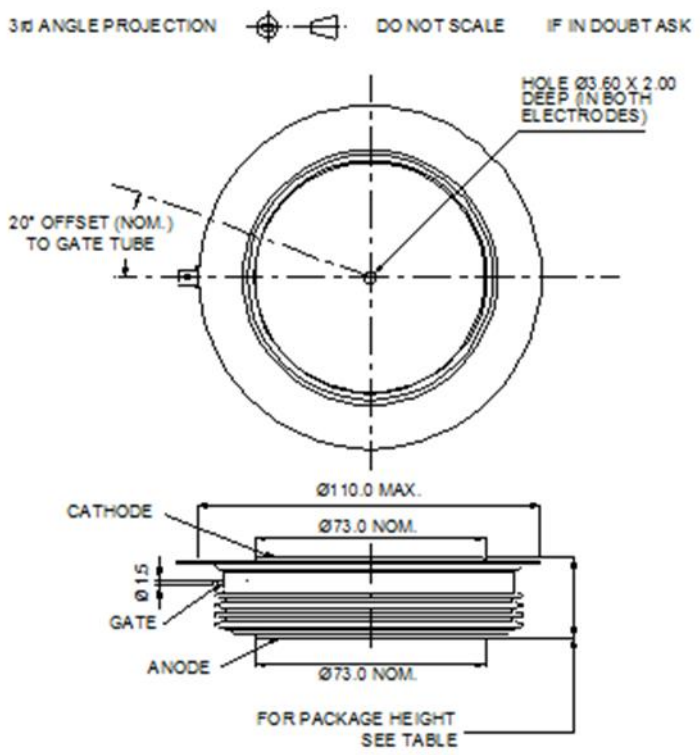
Fig. 5 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE



Device	Maximum Thickness (mm)	Minimum Thickness (mm)
ACR2900VR45	27.7	27.0
ACR3200VR33	**27.5**	**26.8**

Lead length: 420mm

Lead terminal connector: M4 ring

Package outline type code: V

Weight: 1100g

Fig. 6 Package outline

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HEADQUARTERS OPERATIONS

DYNEX SEMICONDUCTOR LIMITED
Doddington Road, Lincoln, Lincolnshire. LN6 3LF
United Kingdom.
Phone: +44 (0) 1522 500500
Fax: +44 (0) 1522 500550
Web: http://www.dynexsemi.com

CUSTOMER SERVICE

Phone: +44 (0) 1522 502753 / 502901

e-mail: powersolutions@dynexsemi.com