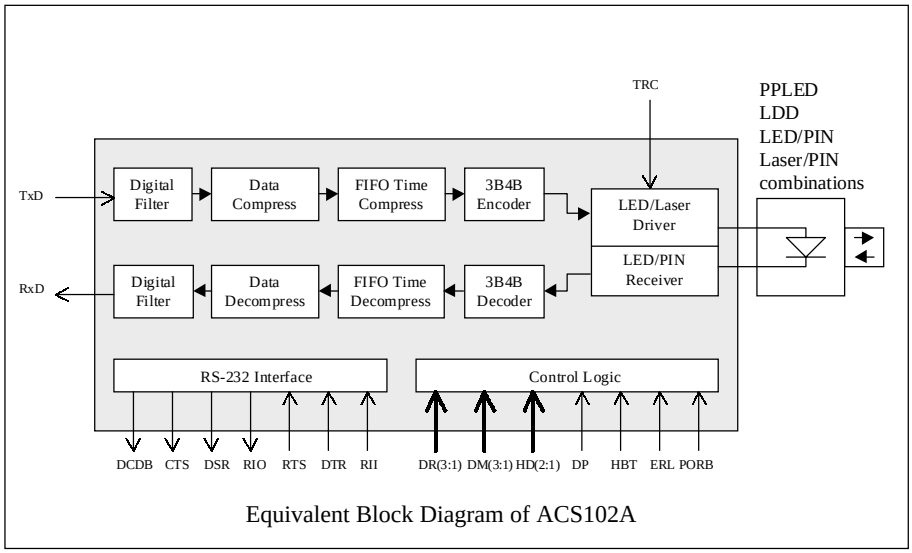
100 SERIES

ACS102A Revision 1.6 September 2000

ACS102A Fiber Modem

Features

* Full duplex serial transmission over single/twin fiber.
* Link lengths up to 25km.
* Supports asynchronous data rates from DC to 162kbps.
* Full diagnostic modes - Remote and Local loopback.
* Ultra low power consumption, typically 2-3mA, which could be extracted from the RS-232 port for self powered applications.
* Uses a single Ping Pong LED or Laser Duplex Device for single fiber applications, low cost LED/PIN or Laser/PIN combinations for twin fiber applications.
* Additional operating mode to support PIN with integrated TIA.
* Supports 3 additional low frequency asynchronous channels or the RS-232 handshake signals.
* Digital and differential voltage input modes, plus modes for non fiber applications - RF
* Bit Error Rate (BER) < 10^{-9}
* Available in 44 pin TQFP (part no: ACS102A-TQ) and 44 pin PLCC (part no: ACS102A-PL) packages.



Equivalent Block Diagram of ACS102A

Description

The ACS102A is a complete controller, driver and receiver IC, supporting full-duplex asynchronous transmission from DC to 162kbps over a single serial link. Although primarily designed for single optical fibre applications, any other simple serial media may be used. The ACS102A is optimised for very low power consumption, consuming only 2 - 3mA at RS-232 data rates including power provided to the LED and 'heartbeat' monitor. In applications where the power is extracted from the RS232 data lines, this leaves a generous amount of power left for any power extraction and RS-232 level shifting circuitry.

The ACS102A employs data compression and time compression techniques, affording high launch power in short bursts, leading to a low average power consumption. The advantage of this approach is that high link budgets can be achieved with inexpensive optical components.

For example, the recommended set-up for RS-232 applications (19.2kbps + handshake signals) assumes that the LED is driven with a peak current of approximately 15.4mA for 6 % of the time. The machine cycle is short enough to facilitate power supply smoothing with a small external capacitor in the region of 100µF.

Single/Dual Fiber Modem for Asynchronous Data Rates from DC to 160kbps

Transmitter and Receiver Functions

This device offers one high speed and three low speed full duplex channels to the user in a completely transparent way, appearing as 4 full duplex channels even though the medium connecting the devices may only be a single fiber link.

Data from the TxD and low frequency channels is time compressed in an internal FIFO and sent over the fiber link in a burst within a predefined window. The device at each end of the link automatically synchronise with each other such that the transmit and receive windows are interleaved. The TxD input data of the transmitting modem is also data compressed. The 3B4B encoding method is used for communication between ACS102As, thus ensuring that there is no DC component in the signal. The encoding and decoding is transparent to the user.

In the receiving modem, 3B4B encoding ensures easy extraction of the bit-clock. The received data is filtered, decoded, and then stored in the output memory. The memory provides time expansion, de-jittering and frequency compensation functions. The data is then decompressed and directed to the RxD output pin, appearing after a minimal delay, in the same format as that presented at the TxD pin at the far end.

Operational Modes

The ACS102A is compatible with the ACS102 but offers over twice the max data rate and incorporates the laser interface modes previously associate with the ACS402. The ACS102A is a pin and functional compatible replacement for both the ACS102 and ACS402. The following sections detail the operating modes for all configurations of LED, LASER and LED/PIN or LASER/PIN combinations. Additional modes are also described for new ways of interfacing the device with external PIN / amplifier modules.

LED Interface Modes

Mode 1 - Single Fiber LED mode

Setup : DP5=0, DP4=0, DP3=0, DP2=1, DP1=0

This is the operational mode for single fiber transmission with a PPLED. The LED is used for both transmission and reception of data over the fiber. An example circuit diagram showing the necessary connections is shown in figure 4. This also shows an example circuit for interfacing to the RS232 voltage levels of a PC serial port.

Mode 2 - Dual Fiber LED/PIN mode

Setup : DP5=0, DP4=0, DP3=0, DP2=1, DP1=1

This is a twin-fiber mode where the LED is used for transmission and a separate PIN Diode is used for reception. This allows the use of less expensive standard LEDs and PINs rather than bi-directional PPLEDs or Duplex devices. An example circuit diagram showing the necessary connections is shown in figure 5.

LASER Interface Modes

Mode 3 - Dual Fiber LASER/PIN mode

Setup : DP5=0, DP4=1, DP3=0, DP2=1, DP1=0

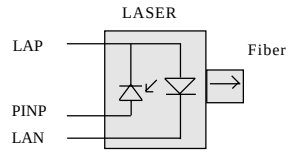
This is a twin-fiber mode where the LASER is used for transmission and a separate PIN Diode is used for reception. An example circuit diagram showing the necessary connections is shown in figure 6. Differential reception from the PIN diode is used to maximise sensitivity. Since PINP is also used for LASER current control via monitoring of the monitor diode current, the LAP and LAN pins are automatically floated during data reception.

Either 3 or 4 pin LASERs may be used in this mode. For 4 pin LASERS the extra pin of the monitor diode cathode is connected to the LASER anode, the same as it is shown in figure 6 with the internal connection of a typical 3-pin LASER.

Mode 4 - Single Fiber 3-pin LASER/PIN mode

Setup : DP5=0, DP4=0, DP3=1, DP2=0, DP1=1

This is a single-fiber mode where the LASER is used for transmission and the monitor PIN diode within the LASER is used for reception. Differential reception from the PIN diode is used to maximise sensitivity. Connections are shown below :

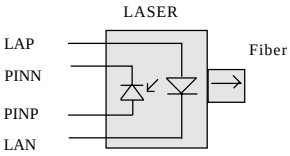


3-pin LASER single fiber mode

Mode 5 - Single Fiber 4-pin LASER/PIN mode

Setup : DP5=0, DP4=0, DP3=1, DP2=0, DP1=0

This is a single-fiber mode where the LASER is used for transmission and the monitor PIN diode within the LASER is used for reception. Differential reception from the PIN diode is used to maximise sensitivity. Connections are shown below :



4-pin LASER single fiber mode

LASER Duplex Device Use

The Laser duplex device is composed of a 3 or 4 pin Laser for transmission and a PIN diode for reception in a single housing. Mode 3, as detailed previously is used for interfacing to these devices. The Duplex devices are driven by the ACS102A in a half-duplex manner, even though to the user it appears as a full duplex link. As a consequence potential cross-talk between the transmitter and receiver is ignored, allowing excellent performance from low cost components.

Additional Alternative Modes

The previous modes detail the most common setups for most typical LED, LED/PIN or LASER/PIN combinations. Many other possible operating modes are possible via the DP1-5 pins setups.

Some of the other less common connection combinations are shown below. These include modes for using a LASER as a receiver as well as a transmitter in a single fiber link, where the LASER device supports this, receiving from both the LASER and monitor PIN, and modes for digital interfacing to external PIN/ transimpedance amplifier (TIA) modules. Only use those setups on DP1-5 indicated in this specification, other pin combinations may activate unpublicised functional or test modes which may lead to damage of the LASER, where this is used.

Mode 6 - Single Fiber 4-pin LASER/PIN mode (Las & mon recv)

Setup : DP5=0, DP4=0, DP3=0, DP2=0, DP1=0

This is a single-fiber mode where the LASER is used for transmission and the LASER and the monitor PIN diode within the LASER is used for reception. Connections are as in mode 5.

Mode 7 - Single Fiber 3-pin LASER/PIN mode (Laser recv)

Setup : DP5=0, DP4=0, DP3=0, DP2=0, DP1=0

This is a single-fiber mode where the LASER is used for transmission and only the LASER is used for reception. Connections are as in mode 4.

Preamp Interface modes

Mode 8 - Preamp Voltage Input & LED Drive

Setup : DP5=1, DP4=0, DP3=1, DP2=0, DP1=0, NSB=0

This is a mode for use with external amplifier and PIN modules. An LED is used for transmission and connected as normal with its anode to LAP and cathode to LAN. The differential voltage from an external PIN/TIA module is connected to PINN and PINP via 100pF capacitors to provide DC isolation. The signals should be connected such that PINP is connected to the TIA output that goes high when light is received. A single input can also be applied from a single ended PIN/TIA by feeding the input to PINP only, PINN is left floating. This mode uses the new NSB pin, in all other modes this pin should be left disconnected or connected to VA+.

Mode 9 - Preamp Voltage Input & LASER Drive

Setup : DP5=1, DP4=0, DP3=1, DP2=0, DP1=1, NSB=0

This is a mode for use with external amplifier and PIN modules. A LASER is used for transmission and connected as normal as described under mode 3. The differential voltage from an external PIN/TIA module is connected to PINN and PINP via 100pF capacitors to provide DC isolation. The signals should be connected such that PINP is connected to the TIA output that goes high when light is received. A single input can also be applied from a single ended PIN/TIA by feeding the input to PINP only. With a LASER drive the PINN and PINP inputs are also connected to the LASER monitor diode. This may induce extra noise but should not interfere with the operation. This mode uses the new NSB pin, in all other modes this pin should be left disconnected or connected to VA+.

Digital interface modes

Mode 10 - Digital Data Input & LASER Drive

Setup : DP5=0, DP4=1, DP3=1, DP2=0, DP1=0

This is a mode for use with external amplifier and PIN modules that provide fully digital output levels. A LASER is used for transmission and connected as normal as described under mode 3. The output from an external PIN/TIA module is connected to CNT. The polarity of the input should be such that CNT that goes high when light is received.

Mode 11 - Digital Data Input & LED Drive

Setup : DP5=1, DP4=1, DP3=0, DP2=1, DP1=0

This is a mode for use with external amplifier and PIN modules that provide fully digital output levels. An LED is used for transmission and connected as normal as shown in figure 5. The output from an external PIN/TIA module is connected to CNT. The polarity of the input should be such that CNT that goes high when light is received.

Transmit Current Control

LED current control

The LED transmit current is not critical though it is important not to exceed the LED manufacturer's recommendation for maximum current. The current is controlled by a resistance Rtrc connected between TRC and GND. The lower the value of Rtrc the greater the current. The lower limit for Rtrc is 800Ω while a practical maximum is 40kΩ.

The LED current is inversely proportional to Rtrc while Rtrc > 800Ω.

LED current = (100 / Rtrc) +/- 25 %

LASER current control

The LASER output current must be set for each individual device in accordance with the manufacturer's recommendations. The output current to the LASER is controlled by a variable resistor (Rtrc) between TRC and ground. The lower the value of Rtrc the greater the current. The minimum value of Rtrc is 800Ω. The ACS102A derives and controls the average optical power being produced by measuring the current in the LASER's monitor PIN diode and integrating this measurement using the capacitor on the CTX pin, which is typically 10nF. A control loop is established which works to maintain the average optical power at a constant level whilst parameters such as voltage, temperature and LASER efficiencies may vary. The average optical power is always one half of the peak power since the LASER is driven between full on and full off, with an average mark-space ratio of 50%. An example circuit arrangement is shown in figure 6.

Adjustment Procedure

Select the appropriate LASER drive mode using the pins DP1-5 (see section headed *Operational Modes).* The LASER drive current and hence transmitted optical power is set by adjusting Rtrc until the required output power is obtained, taking account of the maximum allowed drive current set by the LASER manufacturer.

There are two ways of measuring the output power and drive current, either dynamically in the normal operating mode or statically by setting the pin SETB low.

If measuring power dynamically during the normal mode, the output from the laser can be measured using an optical-power meter that is capable of detecting peak optical-power. If an averaging optical power meter is employed then a correction factor of 16 must be used to obtain the peak value :

LASER(peak power) = Laser(average power) * 16.

To measure power statically, the SETB pin must be pulled low to ground. This forces the device to constantly transmit through the LASER at a fixed level. This fixed level will be equivalent to half of the peak level, since the normal control loop within the device works to control the average power level through integrating out the alternating data pulses.

LASER(peak power) = Laser power(with SETB=0) * 2.

Since all currents are static in this mode, a simple optical power meter can be used and the drive current in the laser can be easily measured by connecting an ammeter between pin LMN and VA+. LMN provides a convenient means of monitoring the LASER drive current through the relationship :

LASER(current) = 100 x LMN(current) +/- 8%.

Dynamic measurement of the LMN current is also possible by connecting a resistor to LMN and measuring the voltage pulses.

Data-Rate Selection

The ACS102A benefits from data compression circuitry which reduces power consumption and improves the BER (Bit Error Rate). The compression technique employed, demands a minimum TxD data-bit time of 10 sample-clocks. This defines the maximum data rate:

Maximum data rate = sample-clock/10

However, an allowance must be made for any variation in the TxD data-bit period to accommodate frequency variation and jitter. Hence the maximum data rates specified in the following are decreased by 10% to include a sufficient safety margin.

The ACS102A includes an input pulse shaper which ensures that the system is very tolerant to jitter, and helps achieve a maximum data-rate close to the theoretical maximum of sample-clock/10 (bps). The pulse shaper will expand data pulses of less than 10 clock-samples to meet the compression criteria. This is performed on up to three consecutive data-bits which fail to meet the minimum pulse width criteria.

DR3	DR2	DR1	XTAL Clock	Sample Clock	Max TxD Data Rate
0	1	1	10MHz	XTAL/160	5.6kbps
1	0	0	10MHz	XTAL/80	11kbps
1	0	1	10MHz	XTAL/40	22kbps
1	1	0	10MHz	XTAL/20	45kbps
1	1	1	10MHz	XTAL/15	60kbps
1	1	1	20MHz	XTAL/15	120kbps
1	1	1	27MHz	XTAL/15	162kbps

Table 1. TxD Data-Rate Selection

Table 1. shows the maximum TxD data rate, which includes a 10% tolerance margin, when using various frequency crystals, other sample-clock frequencies may be generated by using the appropriate value XTAL in combination with the divide constant selected by DR(1:3) namely 15,20,40,80 or 160.

The advantage of using a slower crystal and a lower sample clock is the reduced power consumption of the device.

RS-232 Handshake Signals / Low Frequency Data Channels

Three additional low frequency data channels are provided on the ACS102A which are often used for the RS-232 handshake signals. The RS-232 handshake signals comprise the set RTS, CTS, DTR and DSR. These are treated as pass through data channels rather than using local handshaking. Hence the status of inputs RTS and DTR appear at the far-end outputs CTS and DSR respectively. An extra data channel has also been provided, which may be used for sending the RS232 Ring Indicator signal, for example. The input and output lines are RII and RIO respectively.

The transmission method employed on the ACS102 has been designed to give low skew (1 - 2 data-bits) on the main RTS, CTS, DTR and DSR handshake signals relative to the main TxD/RxD data channel, while maintaining low power consumption.

The handshake signals are updated by two stimuli:

i. an internal interval timer at a frequency proportional to the XTAL; at 10.0MHz this is approximately 1.6ms.

ii. changes detected on RTS and DTR.

The maximum bandwidth for the handshake signals may be programmed using pins HD(1:2) in accordance with the Table 2.

HD2	HD1	Sampling Frequency		Skew w.r.t. RxD
0	0*	600	Hz	10 ms.
0	1	10	kHz	1 - 2 data bits
1	0	5	kHz	1 - 2 data bits
1	1	2.5	kHz	1 - 2 data bits

Table 2. Handshake signal bandwidth allocation

* When HD2 = HD1 = 0 super-compress mode is selected. See section headed *Super-Compress mode.*

Handshake data rates which exceed the allocated bandwidth will be delayed, and consequently result in additional skew between handshake signals and data.

The HD pins enable the user to allocate a maximum bandwidth to the handshake signals and thus limit the power consumption of the device. The power consumption is, however, dependent on the actual bandwidth used and not the bandwidth selected. For example; if the handshake signals were toggled at 1kHz the power consumption would be the same for an allocated bandwidth of 2.5kHz as it would for an allocation of 10kHz. See section headed *Current and Power Consumption* for more details.

Super-Compress mode

This mode is selected when HD2 = HD1 = 0. Super-compress mode performs a second stage of data compression, thus further reducing the power consumption of the modem. Normally, data is compressed in a manner which is independent of the data type. In super-compress mode, an additional stage of compression further reduces the data by a factor of 1 to 3 depending on the data itself.

Example: The super-compress stage will compress DC data by an additional Compression Factor (CF) of 3, whilst data close to the maximum frequency will not be compressed beyond the standard CF of 1.

Super-compress mode provides benefits where the user is interested in low average power consumption (e.g. battery life) rather than peak power. If the intended system is idle for most of the time with periodic bursts of activity, the additional data compression afforded will approach a CF of 3.

Locking

To achieve low power consumption the ACS102A is active for a small percentage of the frame (machine-cycle) known as the 'transmit' window and the 'receive' window, collectively these windows are known as the 'active time'. Outside the 'active time' the device is largely dormant accept for the maintenance of the oscillator and basic 'house-keeping' functions.

Communicating modems attain a stable state known as 'locked', where the 'transmit' window of one modem coincides with the 'receive' window of the other, allowing for the delay through the optical link. Adjustments to machine cycles are made automatically during operation, to compensate for differences in XTAL frequencies which cause loss of synchronisation.

The ACS102A locking algorithm is statistical, and consequently the locking time will differ on each attempt to lock.

Diagnostic and Locking Modes

The diagnostic and operational modes, shown in Table 3, are selected using the DM pins.

DM3	DM2	DM1	Mode	Lock
0	0	0	Full-duplex	Drift
0	0	1	Full-duplex	Active
0	1	0	Full-duplex	Memory
1	0	1	Local loopback	Random
1	1	0	Remote loopback	Random
1	1	1	Full-duplex	Random

Table 3. Diagnostic and operational modes

Local Loopback

In local loopback mode TxD data is looped back inside the near-end modem and appears at its own RxD output. RTS, DTR and RII are also looped back appearing at their own CTS, DSR and RIO outputs respectively. The data is also sent to the far-end modem and synchronisation between the modems is maintained.

In local loopback mode data received from the far-end device is ignored, except to maintain lock. If concurrent requests occur for local and remote loopback, local loopback is selected.

The local loopback diagnostic mode is used to test data flow up to, and back from, the local ACS102A and does not test the integrity of the link itself, i.e. local loopback operates independently of synchronisation with a second modem.

Remote Loopback

In remote loopback mode, the near-end modem sends a request to the far-end modem to loopback its received data, thus returning the data so that it appears at the RxD of the initiating modem. RTS, DTR and RII follows the same path, returning data back to CTS, DSR and RIO respectively of the initiating modem. Data also appears at the far-end modem outputs RxD, CTS, DSR and RIO. In the process both modems are exercised completely, as well as the LED/PINs and the fiber optic link. The remote loopback test is normally used to check the integrity of the entire link from the near-end (initiating) modem. Whilst a device is responding to a request for remote loopback from the initiating modem (far-end), requests to initiate remote loopback will be ignored.

Drift lock

Communicating modems attain a stable state where the 'transmit' window of one modem coincides with the 'receive' window of the other, allowing for delay through the optical link. Adjustments to machine cycles are made automatically during operation to compensate for differences in XTAL frequencies which would otherwise cause loss of synchronisation.

Using drift lock, synchronisation described above depends on a difference in the XTAL frequencies at each end of the link, and the greater the difference the faster the locking. Therefore, if the difference between XTAL frequencies is very small (a few ppm), automatic locking may take tens of seconds or even minutes.

Drift lock will not operate if the two communicating devices are driven by a clock derived from a single source (i.e. tolerance of 0ppm).

Active Lock Mode

Active lock mode may be used to accelerate synchronisation of a pair of communicating modems. This mode synchronises the modems in less than 3 seconds by adjusting the machine cycles of the modems. Active lock reduces the machine cycle of the device by 0.5 % ensuring rapid lock. After synchronisation the machine cycle reverts automatically to normal.

Only one device may be configured in active lock mode at any one time. Active lock mode is usually invoked temporarily on power-up. This can be achieved on the ACS102A by connecting DM1 to an RC arrangement, i.e. with the capacitor to 5V and the resistor to GND, to create a 5V → 0V ramp on power-up. The RC time constant should be Ca. 5 seconds. Active lock will succeed even when communicating devices are driven from clocks derived from a single source (0ppm).

Random Lock

This mode achieves moderate locking times (typically 5 seconds, worst case 10 seconds) with the advantage that the ACS102's are configured as peers. Communicating modems may be permanently configured in this mode by hard wiring the DM pins.

Random lock will succeed even when communicating devices are driven from clocks derived from a single source (0ppm). Random lock mode is compatible with drift lock and active lock.

Memory Lock

Following the assertion of a reset (PORB = 0) communicating devices will initiate an arbitration process where within 10 seconds the communicating modems will achieve synchronisation with one establishing itself as an active lock modem and the other establishing itself as a drift lock modem. On subsequent attempts to lock, synchronisation will be achieved within 3 seconds. It is only necessary to apply reset to one device in the communicating pair to initiate an arbitration process.

Since memory lock uses on-chip storage, loss of power to the modem will require a new reset (PORB=0). Furthermore, should there be a need to synchronise with a third modem a reset will again be required.

Mixing Lock modes

It is possible to mix all combinations of locking modes once the modems are locked, however, prior to synchronisation two modems configured in active lock will not operate. The effect of mixing locking modes on locking speed is given in Table 4 :

Device A Mode	Device B Mode	Locking Speed
Drift	Drift	Drift
Drift	Active	Active
Drift	Random	Random
Drift	Memory	Random
Active	Active	Not allowed
Active	Random	Random
Active	Memory	Random
Random	Random	Random
Random	Memory	Random
Memory	Memory	Active (Random on first synchronisation)

Table 4. Mixing lock modes

PORB

The Power-On Reset or PORB resets the device if forced Low for 100ms or more. This pin should be connected as figure 4.

Crystal Clock

Normally, a parallel resonant crystal will be connected between the pins XLI and XLO with the appropriate padding capacitors. The crystal oscillator will operate with padding capacitors of value 0 -50pF, and the designer should endeavour to use padding capacitors of low value since this will ensure the lowest power consumption. The ACS102A has been designed to operate with a crystal tolerance of +/ - 250ppm giving a relative tolerance between communicating modem pairs of 500ppm. This wide tolerance will support the use of low value padding capacitors.

Alternatively, XLI may be driven directly by an external clock. The clock frequency for the purpose of this specification is referred to as the XTAL frequency. The operational range for the XTAL frequency is 5 - 27MHz, though communicating devices must use the same nominal value.

DCDB

The Data Carrier Detect (DCDB) signal goes Low when the modems are synchronised ('locked') and ready for data transmission. Prior to lock (DCDB = High), the data channel output RxD will be forced Low and the handshake outputs CTS and DSR will be forced High.

The status of DCDB is also given by the HBT pin. See section headed *HBT Status pin*.

CNT Capacitor

The CNT value is inversely proportional to the XTAL frequency. The capacitor is connected between pins CNT and GND. A 20 % tolerance on CNT is sufficient. For a XTAL frequency range of 5 to 27MHz the recommended value of the capacitor on CNT is from 47nF at 5MHz, 22nF at 10MHz down to 10nF at 27MHz . A ceramic type is required to ensure low leakage. The CNT capacitor value has an effect on the initial locking time and the receiver sensitivity limit. Higher values giving improved sensitivity and lower values giving faster locking.

ERL (Error Detector)

This signal can be used to give an indication of the quality of the optical link. Even when a DC signal is applied to the data and handshake inputs, the ACS102A modem transmits up to 200kbps over the link in each direction. This control data is used to maintain the timing and the relative positioning of 'transmit' and 'receive' windows.

The transmit and control data is constantly monitored to make sure it is compatible with the 3B4B format. If a coding error is detected, ERL will go High and will remain High until reset. ERL may be reset by asserting PORB, or by removing the fiber-optic cable from one side of the link thereby forcing the device temporarily out of lock.

Please note that ERL detects coding errors and not data errors, nevertheless because of the complexity of the coding rules on the ACS102A the absence of detected errors on this pin will give a good indication of a high quality link.

HBT Status pin ('Heartbeat' Indicator LED)

The ACS102A HBT pin affords a method of driving a display LED in a manner which is sympathetic to low power consumption. The HBT pin is pulsed to indicate 'locked' status (DCDB = 0) and 'out of lock' status (DCDB =1). The frequency of pulses is 8 times greater for 'out of lock' than for 'lock'. The LED 'on' indicates power-up whilst the frequency of pulsing denotes locking status.

Since the display LED is on for (at most) 3.2 % of the total time, the HBT requires little power which may be further reduced by employing high efficiency LEDs.

Powered-up, but not locked

Frequency (Hz):	XTAL / 3.89 * 10^6	
Duration (s):	61,440 / XTAL	
On time (%):	3.2 % of time.	
With 10MHz XTAL :	Frequency:	2.5Hz (approx.)
	Duration:	6.1ms (approx.)

Powered-up and locked

Frequency (Hz):	XTAL / 15.36 * 10^6	
Duration (s):	61,440 / XTAL	
On time (%):	0.4 % of time.	
With 10MHz XTAL :	Frequency:	0.65Hz (approx.)
	Duration:	6.1 ms (approx.)

The HBT pin is active High and can supply up to 16 mA at a voltage of > VDD - 0.5 Volts. The display LED should be placed between the HBT pin and GND with a series resistor. The resistor value is a function of the efficiency of the display LED, and the power budget.

Example: Calculating the HBT resistor value

LED on voltage:	2.0V
VDD (ACS102A):	5.0V
Resistor voltage:	3.0V
Current to LED:	2mA (high efficiency LED)
Resistor value:	$3/2*10^{-3} = 1500\Omega$
Average current:	64µA
Average power:	0.32mW

Note: The LED referred to in this section is of the inexpensive display type and should not be confused with the LED that interfaces with the fiber optic cable itself.

Power consumption considerations

The power consumption of the ACS102A is a function of the following:

i. The sample-clock DR(1:3)
ii. The transmit current setting (TRC)
iii. Handshake signals frequency
iv. XTAL frequency
v. Supply voltage

The sample-clock

The sample-clock selected by DR(1:3), see section headed *Data-Rate Selection,* determines the quantity of data transmitted over the fiber link. The 'transmit' window opens once each frame and closes when the time compress FIFO is empty. The 'receive' window is aligned with the 'transmit' window of the far-end modem, and tracks the 'transmit' window such that it closes on detection of the last data bit. Clearly, the lower the sample-clock the smaller the active time and the lower the power consumption.

The transmit current setting

The formula given in section headed *LED current control,* relates to the peak current delivered to the LED. The average current however is very much lower. The DC balanced nature of data encoding means the LED consumes current for approximately 50 % of the 'transmit' window time. The average current delivered to the LED is therefore a function of both the peak current and the duration of the 'transmit' window.

Handshake signals frequency

Handshake data which is interleaved with the main data channel is generated and written to the time compress FIFO each time a change is detected on either RTS or DTR. The power consumption is lower when the signals change at low frequency or are held at a DC level. It is possible to limit the power consumption dedicated to the handshake signals by limiting the frequency of operation using HD(1:2) input pins. See section headed *RS-232 Handshake Signals.*

XTAL frequency

The ACS102A uses CMOS technology and therefore the power consumption is proportional to the frequency of switching. Consequently, the effect of reducing the value of the XTAL alone will result in lower power consumption. However, the current component delivered to the LED and sourced from outputs such as RxD and HBT are static and as such are independent of the XTAL frequency.

It is worth noting that a modem pair configured with an XTAL of 10MHz and a sample-clock of XTAL/40 will yield the same performance as a modem pair configured with an XTAL of 5MHz and a sample-clock of XTAL/20. However, the modem pair with the lower value XTAL is likely to consume the higher power with a higher data delay (see section headed *Data delay and skew*). This is because, although the dynamic power has reduced, the higher sample-clock leads to a much longer active time, a factor which dominates the overall power calculation.

Current and Power Consumption

The average current consumption may be split into two components; the dynamic component and the static component. The dynamic component is dependent on the XTAL frequency while the static component is dependent on static current loads. (See *Calculating average current and power consumption* for details).

Since the peak current can be very much greater than the average current, it is important to use a substantial smoothing capacitor on VA+ and VD+. The recommended values are at least 47µF* for VD+ and 100µF* for VA+. The configuration can be seen in Figure 1. (* Capacitor tolerance +/- 20 %)

Data delay and skew

The Full Duplex Delay (FDD) through the system, which applies to TxD → RxD, RTS → CTS and DTR → DSR, is shown in Table 5.

DR3	DR2	DR1	FDD
0	1	1	6.5ms
1	0	0	3.8ms
1	0	1	2.8ms
1	1	0	2.3ms
1	1	1	2.0ms

Table 5. FDD with XTAL = 10MHz

The FDD is inversely proportional to the XTAL frequency and may be calculated for other XTALs using the formula below:

$FDD_{XTAL} = (10^7 / XTAL) * FDD_{10MHz}$

The skew between the main TxD data channel and handshake signals is 1 - 2 data bits as long as the maximum handshake data-rate of 2kbps is respected. For handshake frequencies above 2kbps, the skew will be proportional to the handshake signal frequency.

LED considerations & Suppliers

Since LEDs from different suppliers may emit different wavelengths, it is recommended that the LEDs in a communicating pair of modems are obtained from the same supplier. The ACS102A can support any wavelength LED or LASER. Furthermore, the emission spectrum is a function of temperature, so a temperature difference between the ends of a link reduces the responsivity of the receiving LED, resulting in a reduction in the link budget. Information is given in the suppliers' data sheets. The following manufacturers have components that will be tested with the ACS102A and Acapella will be glad to assist with contact names and addresses on request:

MITEL	(e.g. 1A-212ST, 1A-212SMA)
Acapella	(e.g. A-ST, A-SMA)
GCA	(e.g. 1A-212-ST-05, 1A-212-SM-02)
Honeywell	(e.g. HFE4214-013, HFE4404-013)

Power Supply Decoupling

The ACS102A contains a highly sensitive amplifier, capable of responding to extremely low current levels. To exploit this sensitivity it is important to reduce external noise to a low level compared to the input signal from the LED or PIN. The modem should have an independent power trace to the point where power enters the board.

Figures 4 to 6 all show the recommended power supply decoupling. The LED/PIN/LASER should be sited very close to the PINP, PINN, LAN and LAP pins. A generous ground plane should be provided, especially around the sensitive PINP, PINN, LAN and LAP pins. The modem should be protected from EMI/RFI sources in the standard ways.

Link Budgets

The link budget is the difference between the power coupled to the fiber via the transmit LED and the power required to realise the minimum input-amplifier current via the receive LED/PIN. The link budget is normally specified in dB or dBm, and represents the maximum attenuation allowed between communicating LEDs. The budget is utilised in terms of the cable length, cable connectors and splices. It usually includes an operating margin to allow for degradation in LED performance. The power coupled to the cable, is a function of the efficiency of the LED, the current applied to the LED and the type of the fiber optic cable employed. The conversion current produced by the reverse biased LED is a function of the LED efficiency and the fiber type.

PIN DESCRIPTION

PLCC-44 Pin	TQFP-44 Pin	Symbol	IO	Name	Description
1	6	DP1	I	Mode Selection	Selects operating mode for use with PPLED, LED/PIN or LASER/PIN.
2	7	GND	-	Ground	Power Supply
3	8	DCDB	O	Data Carrier Detect	Modem control signal - LOW when modems locked
4	9	RTS	I	Request To Send & Data Channel 2 i/p	Modem control signal or additional low frequency data channel input
5	10	RIO	O	Ring indicator output	An alternative data channel which may be for the propagation of the RS232 Ring indicator signal.
6	11	DSR	O	Data Set Ready & Data Channel 3 o/p	Modem control signal or additional low frequency data channel output
7	12	LMN	O	Laser monitor	A pull down current equal to 1/100 th of the Laser current.
8	13	RxD	O	Received Data	Received data
9	14	DR3	I	Data Rate Select	The DR(1:3) inputs select the Data Rates, see p2.
10 11	15 16	XLI XLO	I O	Oscillator Crystal	Connect fundamental parallel resonance crystal with padding capacitors to GND
12	17	GND	-	Ground	Power Supply ground.
13	18	DP5	I	Mode Selection	Selects operating mode for use with PPLED, LED/PIN or LASER/PIN.
14	19	VD+	-	+ve power supply	Power Supply, 3.3-5.25 Volts
15	20	TxD	I	Transmit Data	Transmitted data
16	21	ERL	O	Error Detector	Indicates quality of line. If a coding infringement is detected, ERD goes High. Reset by PORB to Low
17	22	DTR	I	Data Terminal Ready/Data / Channel 3 i/p	Modem contrrol signal or additional low frequency data channel input
18	23	HBT	O	'Heart beat' Lock & power up indicator	Indicates power up and modem lock, pulses slowly when locked, fast unlocked.
19	24	HD1	I	Handshake Delay	Sets the Handshake bandwidth, see p4
20	25	CTS	O	Clear To Send & Data Channel 2 o/p	Modem control signal or additional low frequency data channel output
21	26	HD2	I	Handshake Delay	Sets the Handshake bandwidth, see p4
22	27	PORB	I	Power-on-Reset	Will reset the device when PORB = 0. Connect to an RC circuit as in figure 4, so a reset performed on power-up.
23 24	28 29	DR1 DR2	I	Data Rate Select	The DR(1:3) inputs select the Data Rates, see p3
25 26 28	30 31 33	DM3 DM2 DM1	I	Diagnostic Modes	DM(1:3) input select for Diagnostic Modes such as local loopback and remote loopback
27	32	SETB	I	Setup for Laser testing	Force low to put LASER in constant transmit mode for power adjustment. Leave disconnected when using LEDs.
29	34	NSB	I	New Slice Bar	Connect to GND.
30	35	GND	-	Ground	Ground Supply
31	-	NC	-	Not connected	Not connected
32	36	CNT	IO	Capacitor Integration	Integrating capacitor is placed between CNT and GND of value 10nF-47nF with an XTAL of 27-5Mhz
-	37	GND	-	Ground	Ground Supply
33 34	38 39	PINN PINP	I I	PIN Cathode PIN Anode	Connections to a PIN diode or LASER monitor diode.
35 36	40 41	LAN LAP	IO IO	LED Cathode LED Anode	Connections to LED or LASER
37	42	VA+	-	+ve Supply	Power supply, 3.3-5.25 Volts
38	43	CTX	IO	Capacitor for Laser transmit	A 10 nF capacitor is connected between this pin and ground for LASER applications. It is used in monitoring of the average transmit power. Can be left disconnected when using LEDs.
39	44	TRC	I	Transmit Current	Defines transmit current to the LED. Minimum and maximum values are set by connecting TRC to GND via a resistor, value R defined by equation on page 2.
40	1	RII	I	Ring indicator input	An alternative data channel which may be for the propagation of the RS232 Ring indicator signal.
41	2	DP4	I	Mode Selection	Selects operating mode for use with PPLED, LED/PIN or LASER/PIN.
42	3	DP3	I	Mode Selection	Selects operating mode for use with PPLED, LED/PIN or LASER/PIN.
43	4	VD+	-	+ve Supply	Power Supply, 3.3-5.5 Volts
44	5	DP2	I	Mode Selection	Selects operating mode for use with PPLED, LED/PIN or LASER/PIN.

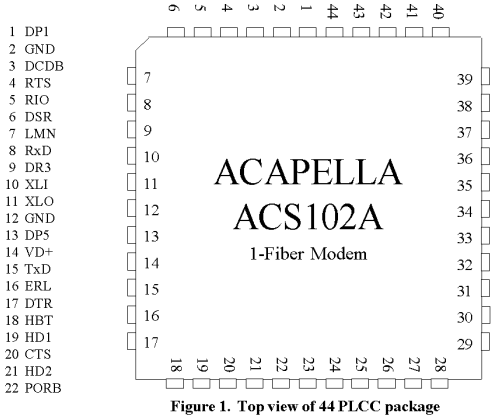


Figure 1. Top view of 44 PLCC package

Single Fiber link

Link Budget Example (Rtrc set so LED launch current = 50mA peak)

Fiber type	**Plastic**	**Glass**	**Glass**
Fiber size	**1000 micron**	**62.5micron**	**50 micron**
Minimum Transmit Couple power to fiber (µW)	1000	60	40
Minimum LED responsivity (A/W)	0.01	0.16	0.16
Minimum ACS102A sensitivity (nA)	500	500	500
Minimum input power to ACS102A amplifier (µW)	50	3.1	3.1
Link Budget (dB)	10	13	11
Average current consumption TxD = 19.2kbps (mA)	3.8	3.8	3.8
Average current consumption TxD = 64kbps (mA)	7.2	7.2	7.2

Dual Fiber link optimised for performance

Link Budget Example (Rtrc set so LED launch current = 100mA peak)

Fiber type	Plastic	Glass	Glass
Fiber size	**1000 micron**	**62.5 micron**	**50 micron**
Minimum Transmit Couple power to fiber (µW)	1000	120	80
Minimum PIN responsivity (A/W)	0.1	0.6	0.6
Minimum ACS102A sensitivity (nA)	500	500	500
Minimum input power to ACS102A amplifier (µW)	5	0.83	0.83
Link Budget (dB)	23	21	19.8
Average current consumption TxD = 19.2kbps (mA)	7	7	7
Average current consumption TxD = 64kbps (mA)	14	14	7.6

Dual Fiber link optimised for low power & low cost optical components

Link Budget Example (Rtrc set so LED launch current = 12.5mA peak)

Fiber type	Plastic	Glass	Glass
Fiber size	**1000 micron**	**62.5micron**	**50 micron**
Minimum Transmit Couple power to fiber (µW)	125	13	6.5
Minimum PIN responsivity (A/W)	0.1	0.6	0.6
Minimum ACS102A sensitivity (nA)	500	500	500
Minimum input power to ACS102A amplifier (µW)	5	0.83	0.83
Link Budget (dB)	13.9	12	9
Average current consumption TxD = 19.2kbps (mA)	2.2	2.2	2.2
Average current consumption TxD = 64kbps (mA)	3.4	3.4	3.4

Calculating average current and power consumption

Average current

I_{av} (mA) = XTAL* 10^{-7} (1.3 + 3*(A + U *H)) + I_{trc} (A + U * H) + I_{out} + I_{hbt}

Power

P (mW) = I_{av} (mA) * V

Terms used in current/power calculation:

XTAL = Crystal Oscillator Frequency, Hz

H = Handshake on
H=1 for handshakes active
H=0 for handshakes at DC level

U = Handshake constant
U = 0.001 when HD 2/1 = 0/0
U = 0.028 when HD 2/1 = 0/1
U = 0.014 when HD 2/1 = 1/0
U = 0.007 when HD 2/1 = 1/1

A = Active window constant
A = 0.022 when DR 3/2/1 = 0/1/1
A = 0.03 when DR 3/2/1 = 1/0/0
A = 0.045 when DR 3/2/1 = 1/0/1
A = 0.08 when DR 3/2/1 = 1/1/0
A = 0.11 when DR 3/2/1 = 1/1/1

I_{out} = Average current sourced from digital outputs such as (RxD,CTS,DSR,DCD) mA

I_{hbt} = Average current sourced from HBT pin. (see section *HBT Status pin*) mA

I_{trc} = Peak Transmit current set by TRC pin. mA

V = Voltage supply to the ACS102 V
Power formula is only accurate for voltage supply = 5 Volts

Note : An application note on power extraction from the RS232 lines is available from Acapella. This shows a typical example circuit diagram for powering the ACS102A, the optics and all related circuitry from the RS232 data lines.

ELECTRICAL SPECIFICATION

Important Note: The "Absolute Maximum Ratings" are stress ratings only, and functional operation of the device at conditions other than those indicated in the "Operating Conditions" sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power supply VD+ and VA+ (VDD = VD+ or VA+)	VDD	-0.3	6.0	V
Input voltage (non-supply pins)	Vin	GND - 0.3	VDD + 0.3	V
Input current (except LAN,LAP,PINN,PINP,CNT)	Iin	-	10.0	mA
Input current (LAN,LAP,PINN,PINP,CNT)	Iin	-	1.0	mA
Storage temperature	Tstor	-50	160	ºC

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power supply (VA+ and VD+)	V+	3.3	5.0	5.25	V
Ambient temperature range	TA	-40	-	85	ºC

Static Digital Input Conditions (for specified operating conditions)

For Digital Input pins: TxD, RTS, DTR, PORB, RII, DP, DR(3:1), DM(3:1), HD(2:1).

Parameter	Symbol	Min	Typ	Max	Units
Vin High	Vih	2.0	-	-	V
Vin Low	Vil	-	-	0.8	V
Input current (High)	Iin	-	0.2	5	µA
Input current (Low)	Iin	-	8	15	µA

Static Digital Output Conditions (for specified operating conditions)

For Digital Output pins: RxD, DSR, CTS, DCDB, ERRL, RIO, HBT.

Parameter	Symbol	Min	Typ	Max	Units
Vout Low	Vol	0	-	0.5	V
Vout High	Voh	VDD-0.5	-	-	V
Isource and Isink (except HBT) (Note 1)	Iout	4	-	-	mA
Isource and Isink (HBT)	Iout	16	-	-	mA
Max load capacitance	Cl	-	-	50	pF

Note 1: Output source and sink currents should be kept to a minimum in order to achieve low power consumption.

Dynamic Characteristics (for specified operating conditions)

Parameter	Symbol	Min	Typ	Max	Units
Crystal frequency (XTI, XTO)	XTAL	5		27	MHz
External clock (XTI) High or Low time	fclp	40	-	60	%
RxD and TxD data rate Function of DR(1:3) setting	fclf	DC	-	XTAL/150	Hz
Digital output - fall time	tf	-	-	100	ns
Digital output - rise time	tr	-	-	100	ns
Power consumption (Note 2)	Pc	-	20	-	mW

Note 2: See section on *Calculating average current and power consumption*

Matching Characteristics (for specified operating conditions)

Parameter	Symbol	Min	Typ	Max	Units
Crystal tolerance use parallel resonate crystal and recommended padding capacitors	Ct	-250	0	250	ppm
Amplifier sensitivity input current	Irec	500	-	-	nA
Maximum amplifier input current	Imax	-	-	500	µA
Rtrc placed between TRC and GND	Rtrc	0.8k	-	40k	Ω
LED current Rtrc = 1 kOhm Rtrc = 40 kOhms	Iled	 75 1.8	 100 2.5	 125 3.2	mA
Block Error Rate	BER	-	-	10^{-9}	
Single Fiber mode Parameters					
LED capacitance with Vr =0 with Irec = 500 nA with Irec = 1000 nA	Cl	 - -	 - -	50 100	pF
LED leakage with Vr = 1.4 V	Lleak	-	-	150	nA
LED reverse bias	Vr	-	0	-	V
Dual Fiber mode Parameters					
PIN capacitance with Vr = 0	Cl	-	-	20	pF
PIN leakage current	Lleak	-	-	150	nA
Pin reverse bias	Vr	-	0	-	V

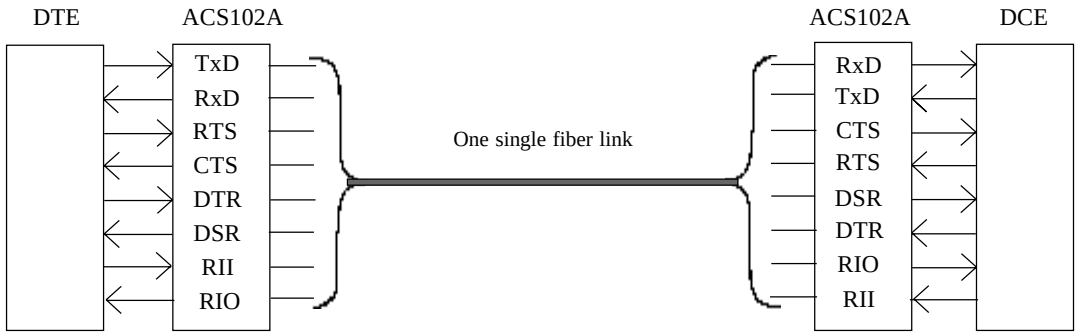
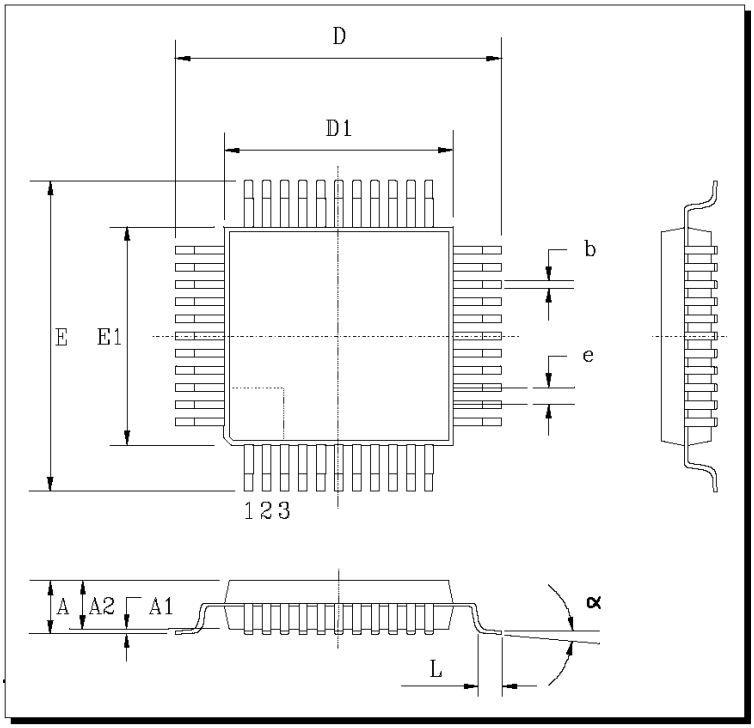
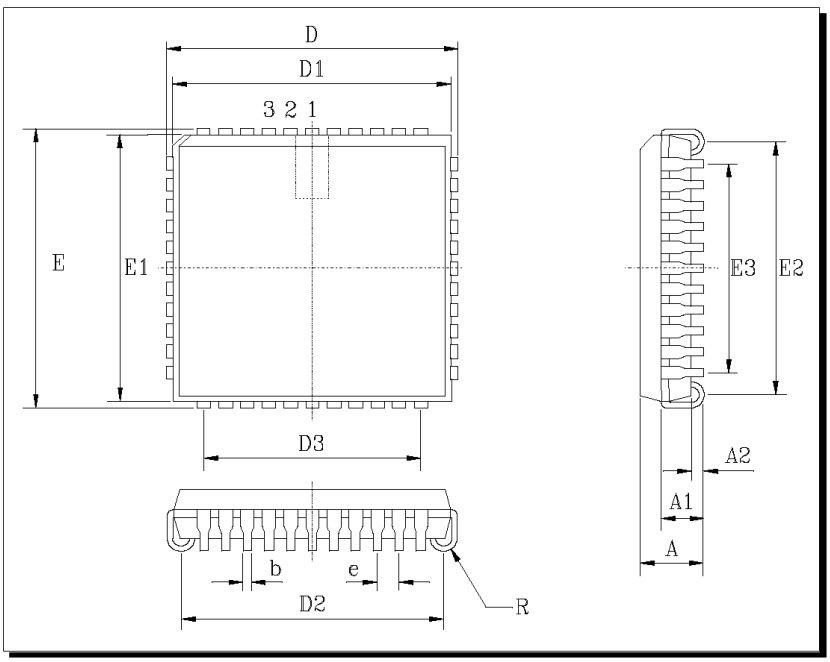


Figure 2. Data and handshake signals transmitted over a single fiber.

PACKAGE INFORMATION



TQFP44	D1/E1	A	A1	A2	e	b	L	α	E/D	Copl
min			0.05	1.35		0.30	0.45	0°		
Dimensions in mm	10.00				0.80				12.00	
max		1.60	0.15	1.45		0.45	0.75	7°		0.10



PLCC44	D/E	D1/E1	D2/E2	D3/E3	A	A1	A2	e	b	R	Copl.
min	17.40	16.51	14.99		4.20	2.29	0.51		0.33	0.64	
Dimensions in mm				12.70				1.27			
max	17.65	16.66	16.00		4.57	3.04			0.53	1.14	0.10

Figure 3. Package Dimensions, PLCC44 & TQFP44

APPLICATION CIRCUITS

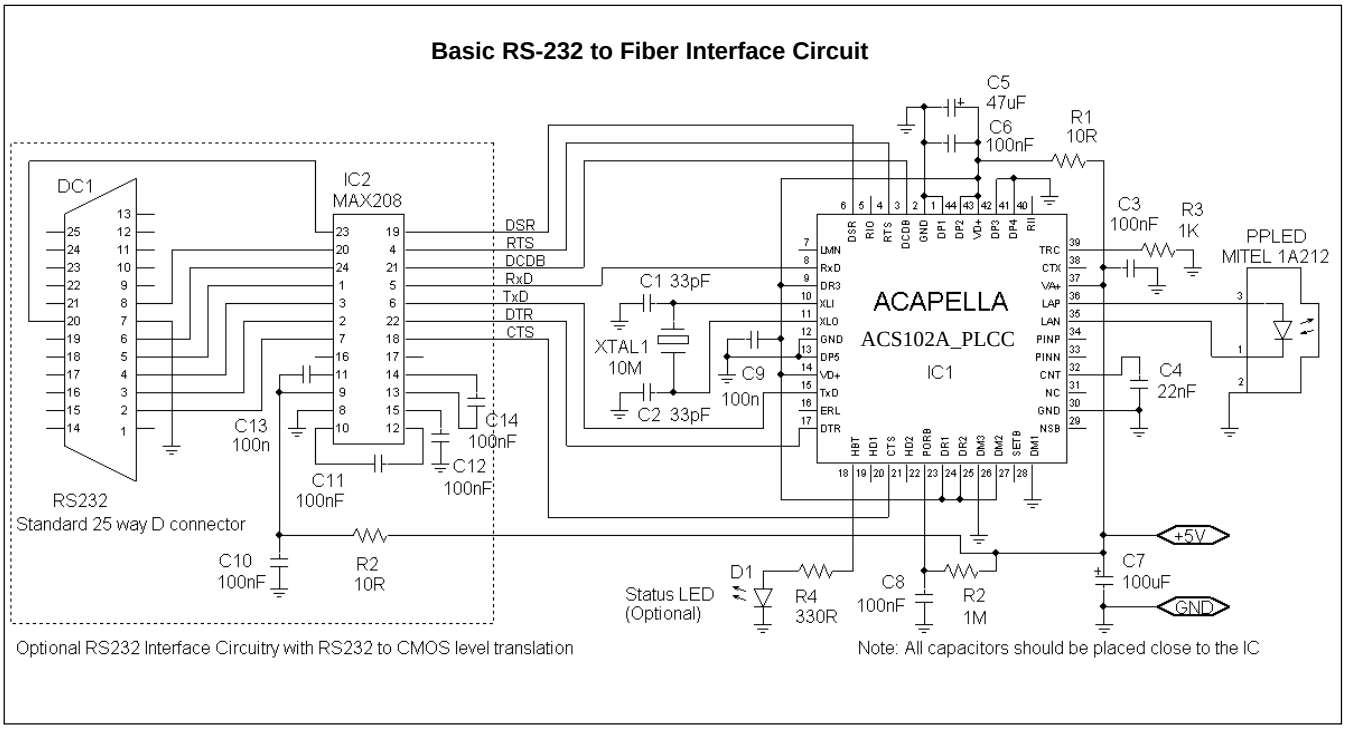


Figure 4. Typical application circuit for linking two PC Serial Ports via a Single Fiber Optic Cable using Ping-Pong LEDs
This diagram shows a PLCC44 package being used. The TQFP44 package option can be used with the same component layout.

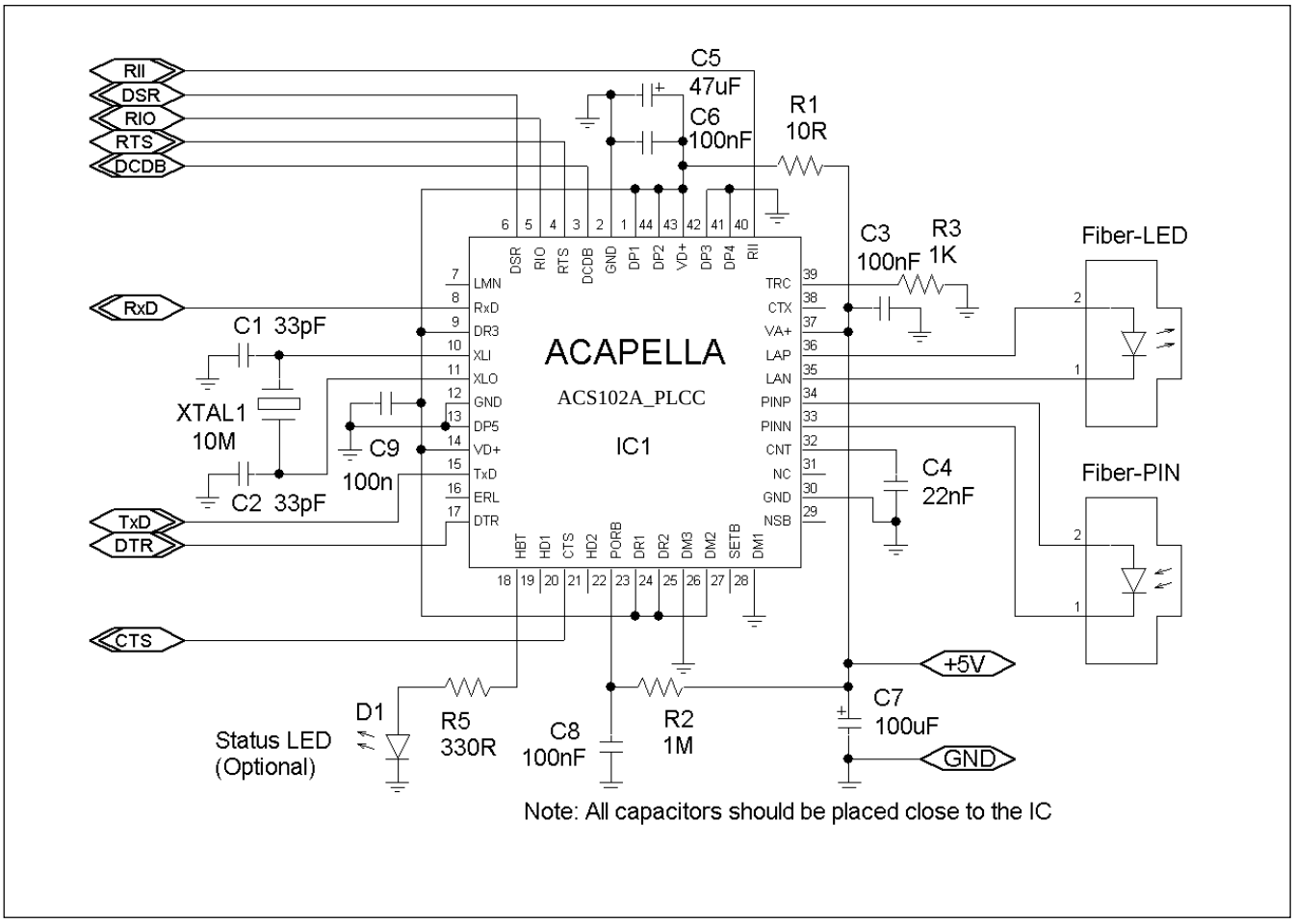


Figure 5. Basic Circuit for a Twin Fiber Link using LED and PIN.

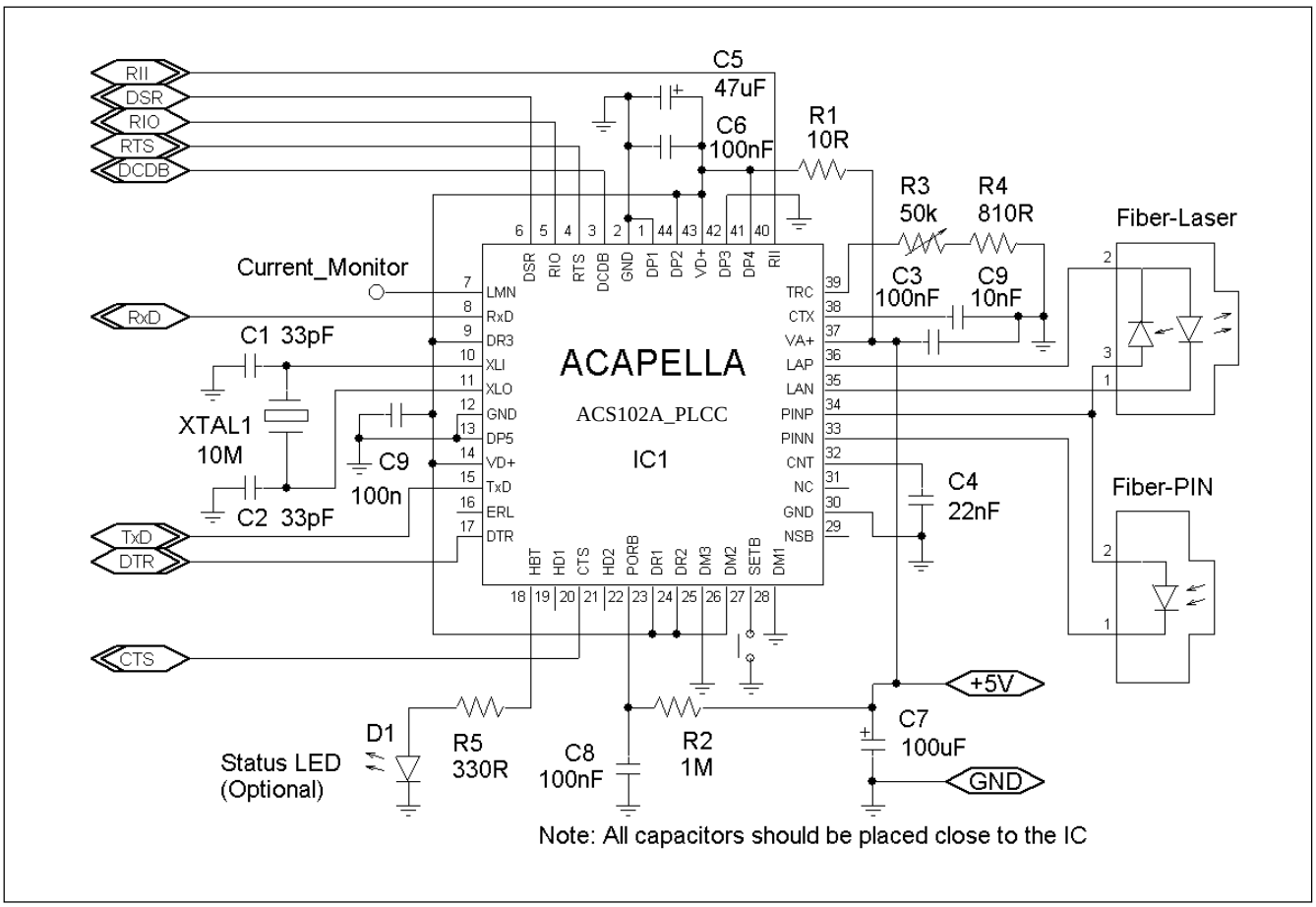


Figure 6. Basic Circuit for a Twin Fiber Link using LASER and PIN.

ORDERING INFORMATION

Device Code	Package	Temperature
ACS102A-TQ	TQFP44	-40 to 85°C(ambient)
ACS102A-PL	PLCC44	-40 to 85°C(ambient)

For additional information, contact the following:

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