

ACT-S128K32V High Speed 3.3Volt 4 Megabit SRAM Multichip Module

Features

- 4 Low Power CMOS 128K x 8 SRAMs in one MCM
- Overall configuration as 128K x 32
- Input and Output TTL Compatible
- 17, 20, 25, 35, 45 & 55ns Access Times, 15ns Available by Special Order
- Full Military (-55°C to +125°C) Temperature Range
- +3.3V Power Supply
- Choice of Surface Mount or PGA Type Co-fired Packages:
 - 68-Lead, Dual-Cavity CQFP (F2), .88"SQ x .20"max (.18"max thickness available, contact factory for details) (Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)
 - 66-Lead, PGA-Type (P7), 1.08"SQ x .160"max
- Internal Decoupling Capacitors
- DESC SMD# Pending



General Description

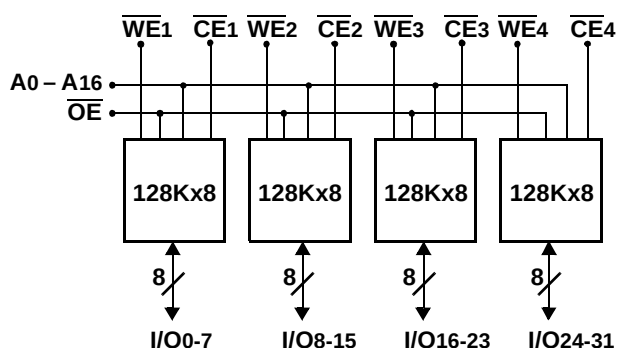
The ACT-S128K32V is a High Speed 4 megabit CMOS SRAM Multichip Module (MCM) designed for full temperature range, 3.3V Power Supply, military, space, or high reliability mass memory and fast cache applications.

The MCM can be organized as a 128K x 32 bits, 256K x 16 bits or 512k x 8 bits device and is input and output TTL compatible. Writing is executed when the write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are low. Reading is accomplished when $\overline{WE}$ is high and $\overline{CE}$ and output enable ($\overline{OE}$) are both low. Access time grades of 17ns, 20ns, 25ns, 35ns, 45ns and 55ns maximum are standard.

The products are designed for operation over the temperature range of -55°C to +125°C and screened under the full military environment. DESC Standard Military Drawing (SMD) part numbers are pending.

The ACT-S128K32V is manufactured in Aeroflex's 80,000ft² MIL-PRF-38534 certified facility in Plainview, N.Y.

Block Diagram – PGA Type Package(P7) & CQFP(F2)



Pin Description

I/O0-31	Data I/O
A0-16	Address Inputs
$\overline{WE}1-4$	Write Enables
$\overline{CE}1-4$	Chip Enables
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings

Symbol	Rating	Range	Units
T_C	Case Operating Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_D	Maximum Package Power Dissipation		
	P7 Packages	3.0	W
	F2 Package	2.7	W
θ_{J-C}	Hottest Die, Max Thermal Resistance - Junction to Case		
	P7 Packages	3.0	°C/W
	F2 Package	9.0	°C/W
V_G	Maximum Signal Voltage to Ground	-0.5 to +4.6	V
T_L	Maximum Lead Temperature (10 seconds)	300	°C

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+3.0	+3.6	V
V_{IH}	Input High Voltage	+2.0	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	+0.8	V

Truth Table

Mode	CE	OE	WE	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Read	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data In	Active

Capacitance

(f = 1MHz, T_C = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	$A_0 - A_{16}$ Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
C_{WE}	Write Enable Capacitance	20	pF
C_{CE}	Chip Enable Capacitance	20	pF
$C_{I/O}$	$I/O_0 - I/O_{31}$ Capacitance	20	pF

Capacitance is guaranteed by design but not tested.

DC Characteristics

(3.0Vdc ≤ V_{CC} ≤ 3.6Vdc, V_{SS} = 0V, T_C = -55°C to +125°C, Unless otherwise specified)

Parameter	Sym	Conditions	-017 & -020		-025 & -035		-045 & -055		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	$V_{CC} = \text{Max}, V_{IN} = 0 \text{ or } V_{CC}$		10		10		10	μA
Output Leakage Current	I_{LO}	$\overline{CE} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = 0 \text{ or } V_{CC}$		10		10		10	μA
Operating Supply Current 32 Bit Mode	$I_{CC \times 32}$	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}, f = 5 \text{ MHz}, V_{CC} = \text{Max}, \text{CMOS Compatible}$		750		500		420	mA

DC Characteristics (continued)

(3.0Vdc ≤ V_{CC} ≤ 3.6Vdc, V_{SS} = 0V, T_C = -55°C to +125°C, Unless otherwise specified)

Parameter	Sym	Conditions	-017 & -020		-025 & -035		-045 & -055		Units
			Min	Max	Min	Max	Min	Max	
Standby Current	I _{SB}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$, f = 5 MHz, V _{CC} = Max, CMOS Compatible		80		60		60	mA
Output Low Voltage	V _{OL}	I _{OL} = 8 mA, V _{CC} = Min		0.4		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA, V _{CC} = Min	2.4		2.4		2.4		V

AC Characteristics

(V_{CC} = 3.3V, V_{SS} = 0V, T_C = -55°C to +125°C)

Read Cycle

Parameter	Sym	-017		-020		-025		-035		-045		-055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	17		20		25		35		45		55		ns
Address Access Time	t _{AA}		17		20		25		35		45		55	ns
Chip Enable Access Time	t _{ACE}		17		20		25		35		45		55	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		0		ns
Output Enable to Output Valid	t _{OE}		9		12		15		20		25		30	ns
Chip Enable to Output in Low Z *	t _{CLZ}	3		3		3		3		3		3		ns
Output Enable to Output in Low Z *	t _{OLZ}	0		0		0		0		0		0		ns
Chip Deselect to Output in High Z *	t _{CHZ}		12		12		12		15		20		20	ns
Output Disable to Output in High Z *	t _{OHZ}		10		11		12		15		20		20	ns

* Parameters guaranteed by design but not tested

Write Cycle

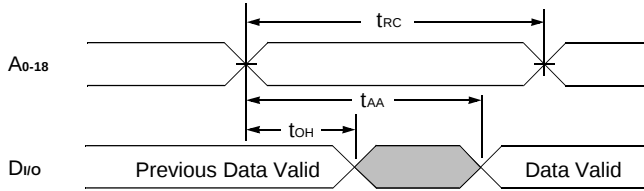
Parameter	Sym	-017		-020		-025		-035		-045		-055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	17		20		25		35		45		55		ns
Chip Enable to End of Write	t _{CW}	12		15		20		25		30		40		ns
Address Valid to End of Write	t _{AW}	12		15		20		25		30		40		ns
Data Valid to End of Write	t _{DW}	10		12		15		18		20		20		ns
Write Pulse Width	t _{WP}	13		15		20		25		30		40		ns
Address Setup Time	t _{AS}	0		0		0		0		0		0		ns
Output Active from End of Write *	t _{OW}	3		3		3		4		4		4		ns
Write to Output in High Z *	t _{WHZ}		10		10		10		15		15		15	ns
Data Hold from Write Time	t _{DH}	0		0		0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		0		0		ns

* Parameters guaranteed by design but not tested

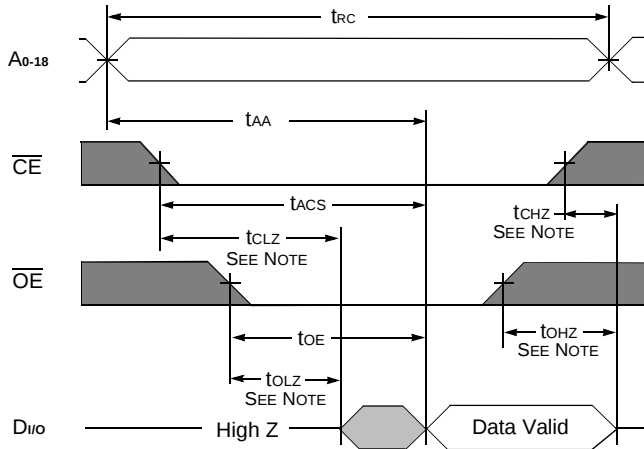
Timing Diagrams

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



Read Cycle 2 ($\overline{WE} = V_{IH}$)

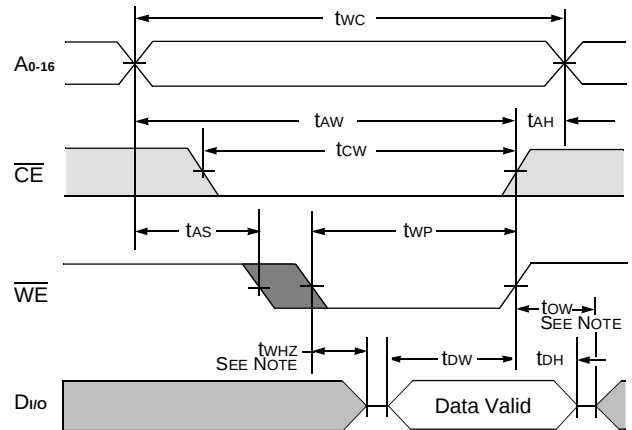


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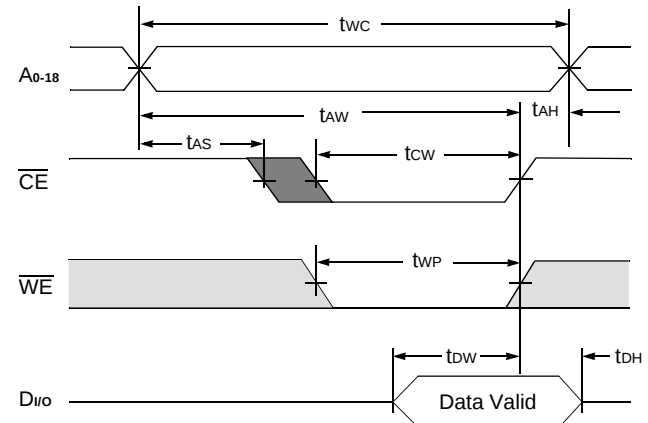
DON'T CARE

Write Cycle Timing Diagrams

Write Cycle 1 ($\overline{WE}$ Controlled, $\overline{OE} = V_{IL}$)

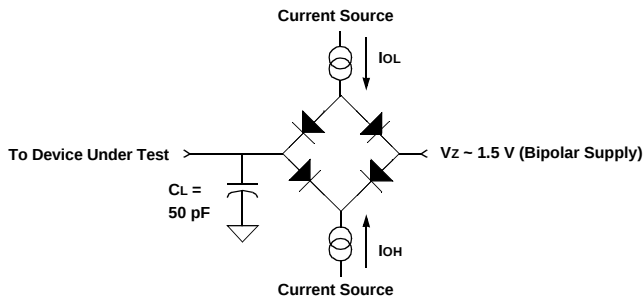


Write Cycle 2 ($\overline{CE}$ Controlled, $\overline{OE} = V_{IH}$)



Note: Guaranteed by design, but not tested.

AC Test Circuit



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

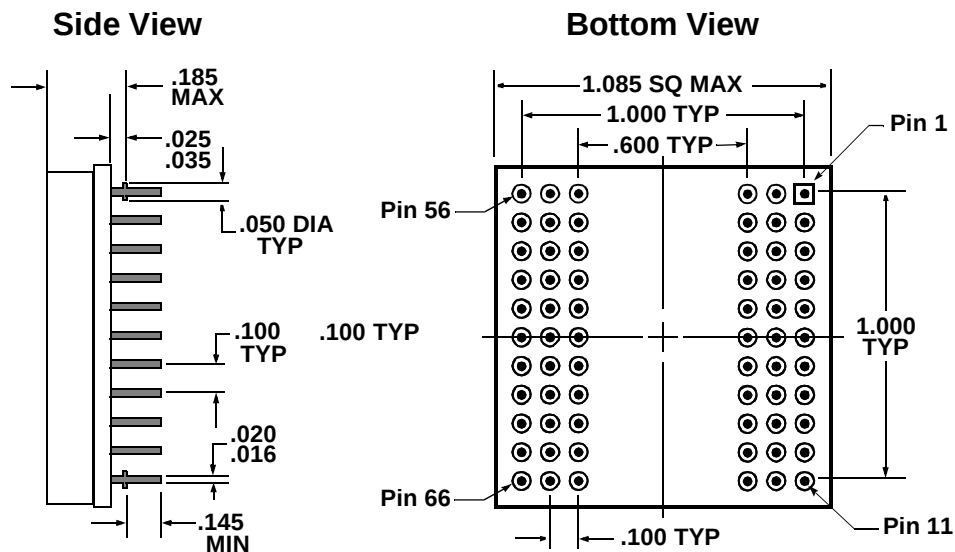
Notes:

- 1) V_Z is programmable from -2V to +4.6V.
- 2) I_{OL} and I_{OH} programmable from 0 to 16 mA.
- 3) Tester Impedance $Z_0 = 75\Omega$.
- 4) V_Z is typically the midpoint of V_{OH} and V_{OL} .
- 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit.
- 6) ATE Tester includes jig capacitance.

Pin Numbers & Functions

66 Pins — PGA-Type													
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O8	11	I/O2	21	NC	31	I/O6	41	A9	51	A5	61	A1
2	I/O9	12	$\overline{WE}_2$	22	I/O3	32	I/O5	42	I/O16	52	$\overline{WE}_3$	62	A2
3	I/O10	13	$\overline{CE}_2$	23	I/O15	33	I/O4	43	I/O17	53	$\overline{CE}_3$	63	I/O23
4	A13	14	GND	24	I/O14	34	I/O24	44	I/O18	54	GND	64	I/O22
5	A14	15	I/O11	25	I/O13	35	I/O25	45	V _{CC}	55	I/O19	65	I/O21
6	A15	16	A10	26	I/O12	36	I/O26	46	$\overline{CE}_4$	56	I/O31	66	I/O20
7	A16	17	A11	27	OE	37	A6	47	$\overline{WE}_4$	57	I/O30		
8	NC	18	A12	28	NC	38	A7	48	I/O27	58	I/O29		
9	I/O0	19	V _{CC}	29	$\overline{WE}_1$	39	NC	49	A3	59	I/O28		
10	I/O1	20	$\overline{CE}_1$	30	I/O7	40	A8	50	A4	60	A0		

"P7" — 1.08" SQ PGA Type Package Standard (with shoulders on Pins 1, 11, 56 & 66)

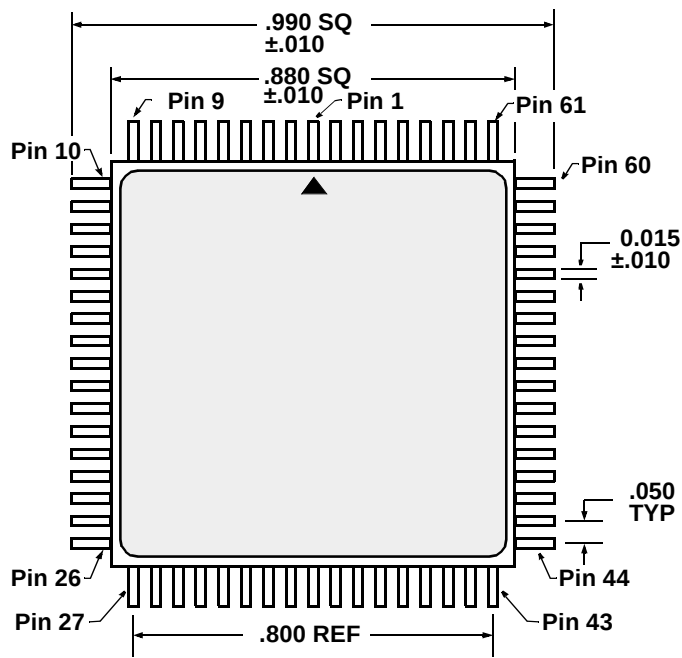


Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O ₈	36	$\overline{CE}_2$	53	I/O ₂₃
3	A ₅	20	I/O ₉	37	NC	54	I/O ₂₂
4	A ₄	21	I/O ₁₀	38	$\overline{WE}_2$	55	I/O ₂₁
5	A ₃	22	I/O ₁₁	39	$\overline{WE}_3$	56	I/O ₂₀
6	A ₂	23	I/O ₁₂	40	$\overline{WE}_4$	57	I/O ₁₉
7	A ₁	24	I/O ₁₃	41	NC	58	I/O ₁₈
8	A ₀	25	I/O ₁₄	42	NC	59	I/O ₁₇
9	NC	26	I/O ₁₅	43	NC	60	I/O ₁₆
10	I/O ₀	27	V _{CC}	44	I/O ₃₁	61	V _{CC}
11	I/O ₁	28	A ₁₁	45	I/O ₃₀	62	A ₁₀
12	I/O ₂	29	A ₁₂	46	I/O ₂₉	63	A ₉
13	I/O ₃	30	A ₁₃	47	I/O ₂₈	64	A ₈
14	I/O ₄	31	A ₁₄	48	I/O ₂₇	65	A ₇
15	I/O ₅	32	A ₁₅	49	I/O ₂₆	66	A ₆
16	I/O ₆	33	A ₁₆	50	I/O ₂₅	67	$\overline{WE}_1$
17	I/O ₇	34	$\overline{CE}_1$	51	I/O ₂₄	68	$\overline{CE}_4$

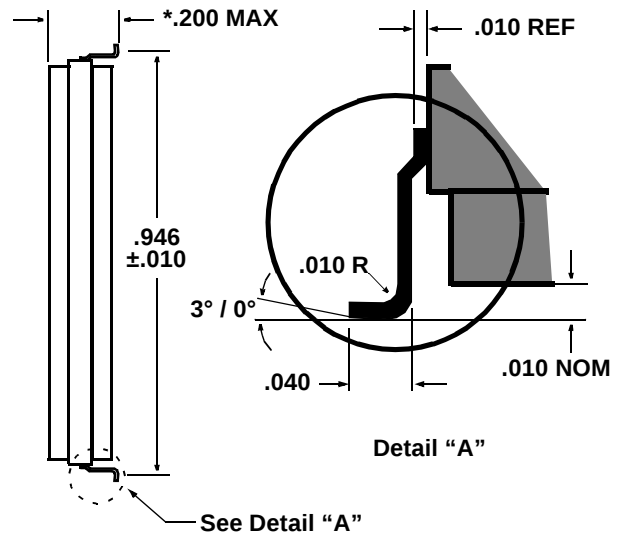
Package Outline "F2" — Dual-Cavity CQFP

Top View



All dimensions in inches

(* .180 MAX available, call factory for details)



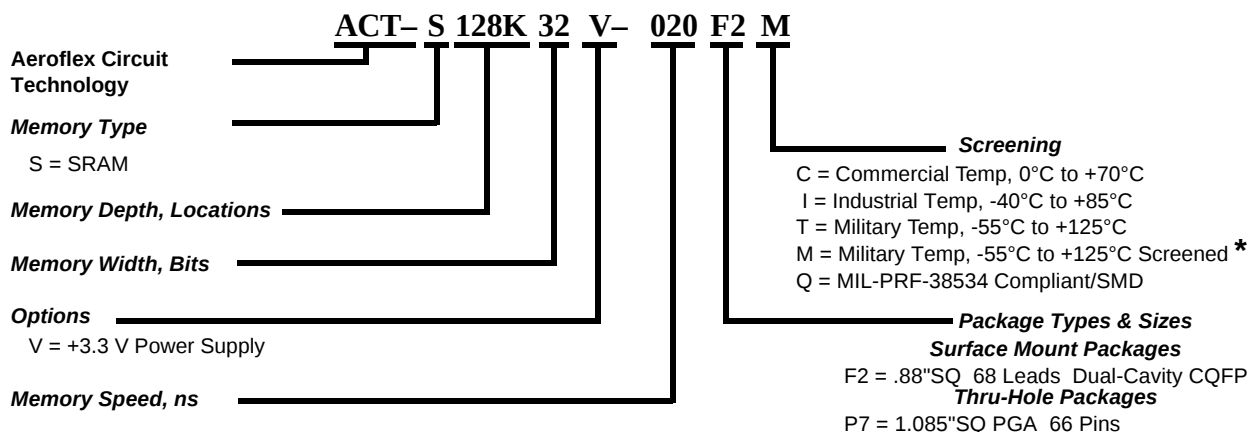
Note: Metallic lids and walls – both sides



DESC Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT-S128K32V-017F2Q	Pending	17ns	.88"sq CQFP
ACT-S128K32V-020F2Q	Pending	20ns	.88"sq CQFP
ACT-S128K32V-025F2Q	Pending	25ns	.88"sq CQFP
ACT-S128K32V-035F2Q	Pending	35ns	.88"sq CQFP
ACT-S128K32V-045F2Q	Pending	45ns	.88"sq CQFP
ACT-S128K32V-055F2Q	Pending	55ns	.88"sq CQFP
ACT-S128K32V-017P7Q	Pending	17ns	1.085"sq PGA-Type
ACT-S128K32V-020P7Q	Pending	20ns	1.085"sq PGA-Type
ACT-S128K32V-025P7Q	Pending	25ns	1.085"sq PGA-Type
ACT-S128K32V-035P7Q	Pending	35ns	1.085"sq PGA-Type
ACT-S128K32V-045P7Q	Pending	45ns	1.085"sq PGA-Type
ACT-S128K32V-055P7Q	Pending	55ns	1.085"sq PGA-Type

Part Number Breakdown



* Screened to the individual test methods of MIL-STD-883

Specifications subject to change without notice

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