ACT–SF2816 High Speed 128Kx16 SRAM / 512Kx16 FLASH Multichip Module

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FEATURES

- 2 – 128K x 8 SRAMs & 2 – 512K x 8 Flash Die in One MCM
- Access Times of 25ns (SRAM) and 60ns (Flash) *or* 35ns (SRAM) and 70 or 90ns (Flash)
- Organized as 128K x 16 of SRAM and 512K x 16 of Flash Memory with Separate Data Buses
- Both Blocks of Memory are User Configurable as 512KX8 AND 1MX8 Respectively
- Low Power CMOS
- Input and Output TTL Compatible Design
- MIL-PRF-38534 Compliant MCMs Available
- Decoupling Capacitors and Multiple Grounds for Low Noise
- Industrial and Military Temperature Ranges
- Industry Standard Pinouts

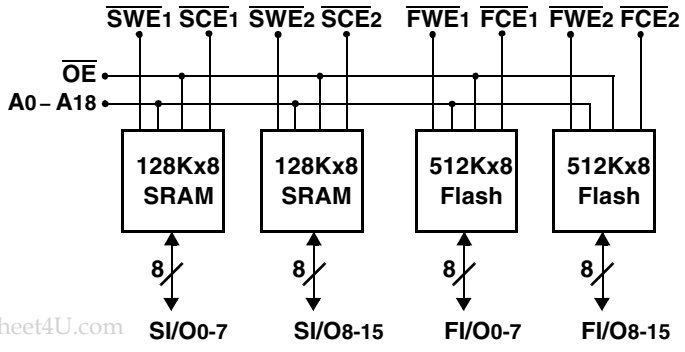
Note: Programming information available upon request

- Packaging – Hermetic Ceramic
  - 66 Pin, 1.08" x 1.08" x .160" PGA Type, No Shoulder, Aeroflex code# "P3"
  - 66 Pin, 1.08" x 1.08" x .185" PGA Type, With Shoulder, Aeroflex code# "P7"
  - 68 Lead, .94" x .94" x .140" Single-Cavity Small Outline Gull Wing, Aeroflex code# "F18" *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
- DESC SMD – TBD

FLASH MEMORY FEATURES

- Sector Architecture (Each Die)
  - 8 Equal Sectors of 64K bytes each
  - Any combination of sectors can be erased with one command sequence
- +5V Programing, +5V Supply
- Embedded Erase and Program Algorithms
- Hardware and Software Write Protection
- Internal Program Control Time.
- 10,000 Erase / Program Cycles

Block Diagram – PGA Type Packages (P3 & P7) & CQFP (F18)



Pin Description

FI/O0-15	Flash Data I/O
SI/O0-15	SRAM Data I/O
A0–18	Address Inputs
$\overline{FWE}$1-2	Flash Write Enables
$\overline{SWE}$1-2	SRAM Write Enables
$\overline{FCE}$1-2	Flash Chip Enables
$\overline{SCE}$1-2	SRAM Chip Enables
$\overline{OE}$	Output Enable
NC	Not Connected
Vcc	Power Supply
GND	Ground

Absolute Maximum Ratings

Symbol	Rating	Range	Units
T_C	Operating Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
V_G	Maximum Signal Voltage to Ground	-0.5 to +7	V
T_L	Maximum Lead Temperature (10 seconds)	300	°C

Parameter	
Flash Data Retention	10 Years
Flash Endurance (Write/Erase Cycles)	10,000

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V

Capacitance

(V_{IN} = 0V, f = 1MHz, T_C = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	A_0 – A_{18} Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
$C_{WE1,2}$	F/S Write Enable Capacitance	20	pF
$C_{CE1,2}$	F/S Chip Enable Capacitance	20	pF
$C_{I/O}$	I/O_0 – I/O_{15} Capacitance	20	pF

These parameters are guaranteed by design but not tested

DC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, Tc = -55°C to +125°C, unless otherwise indicated)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = 0 to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{FCE}$ = $\overline{SCE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = 0 to V_{CC}		10	µA
SRAM Operating Supply Current x 16 Mode	I_{CC}x16	$\overline{SCE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = Max, $\overline{FCE}$ = V_{IH}		325	mA
Standby Current	I_{SB}	$\overline{FCE}$ = $\overline{SCE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = Max		40	mA
SRAM Output Low Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min, $\overline{FCE}$ = V_{IH}		0.4	V
SRAM Output High Voltage	V_{OH}	I_{OH} = -4.0 mA, , V_{CC} = Min, $\overline{FCE}$ = V_{IH}	2.4		V
Flash Vcc Active Current for Read (1)	I_{CC1}	$\overline{FCE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, $\overline{SCE}$ = V_{IH}		130	mA
Flash Vcc Active Current for Program or Erase (2)	I_{CC2}	$\overline{FCE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, $\overline{SCE}$ = V_{IH}		150	mA
Flash Output Low Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min, $\overline{SCE}$ = V_{IH}		0.45	V
Flash Output High Voltage	V_{OH}	I_{OH} = -2.5 mA, , V_{CC} = Min, $\overline{SCE}$ = V_{IH}	0.85 x V_{CC}		V
Flash Low Vcc Lock Out Voltage	V_{LKO}		3.2		V

Notes: 1) The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5MHz). The frequency component typically is less than 2mA/MHz, with $\overline{OE}$ at V_{IH} 2) I_{CC} active while Embedded Algorithim (program or erase) is in progress 3) DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

SRAM AC Characteristics

(VCC = 5.0V, VSS= 0V, Tc= -55°C to +125°C)

Read Cycle

Parameter	Symbol	–025		–035		Units
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time	t_{AA}		25		35	ns
Chip Select Access Time	t_{ACE}		25		35	ns
Output Hold from Address Change	t_{OH}	0		0		ns
Output Enable to Output Valid	t_{OE}		15		20	ns
Chip Select to Output in Low Z *	t_{CLZ}	3		3		ns
Output Enable to Output in Low Z *	t_{OLZ}	0		0		ns
Chip Deselect to Output in High Z *	t_{CHZ}		12		20	ns
Output Disable to Output in High Z *	t_{OHZ}		12		20	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Symbol	–025		–035		Units
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		35		ns
Chip Select to End of Write	t_{CW}	20		25		ns
Address Valid to End of Write	t_{AW}	20		25		ns
Data Valid to End of Write	t_{DW}	15		20		ns
Write Pulse Width	t_{WP}	20		25		ns
Address Setup Time	t_{AS}	0		0		ns
Output Active from End of Write *	t_{OW}	0		0		ns
Write to Output in High Z *	t_{WHZ}		10		20	ns
Data Hold from Write Time	t_{DH}	0		0		ns
Address Hold Time	t_{AH}	0		0		ns

* Parameters guaranteed by design but not tested

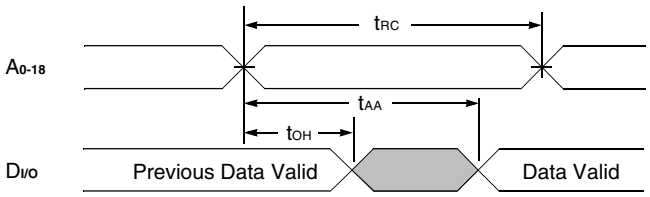
Truth Table

Mode	$\overline{SCE}$	$\overline{OE}$	$\overline{SWE}$	Data I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	Data Out	Active
Output Disable	L	H	H	High Z	Active
Write	L	X	L	Data In	Active

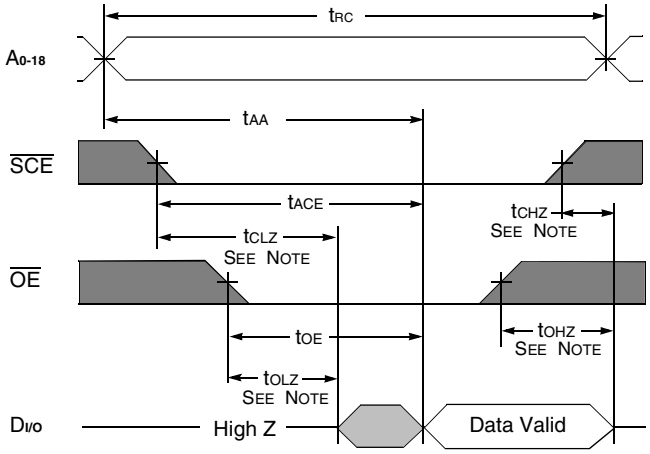
Timing Diagrams — SRAM

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{SCE}$ = $\overline{OE}$ = V_{IL}, $\overline{SWE}$ = V_{IH})



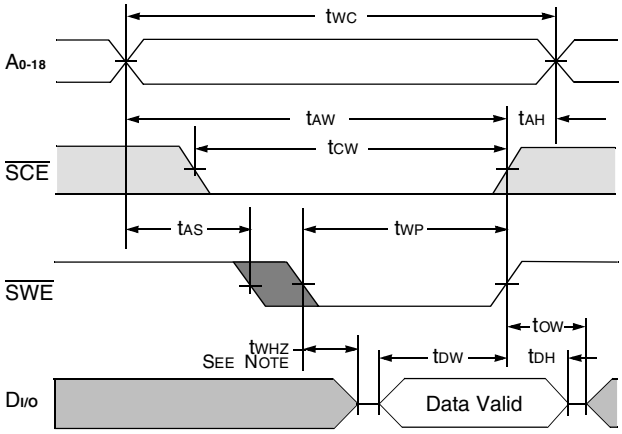
Read Cycle 2 ($\overline{SWE}$ = V_{IH})



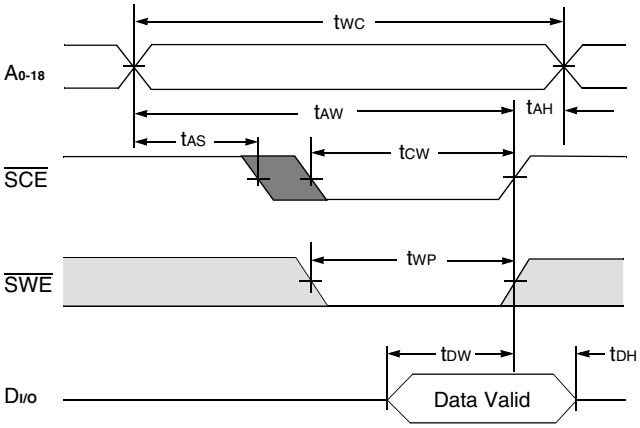
UNDEFINED DON'T CARE

Write Cycle Timing Diagrams

Write Cycle ($\overline{SWE}$ Controlled, $\overline{OE}$ = V_{IH})

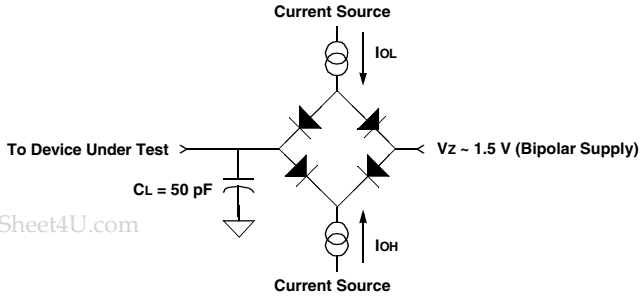


Write Cycle ($\overline{SCE}$ Controlled, $\overline{OE}$ = V_{IH})



Note: Guaranteed by design, but not tested.

AC Test Circuit



AC Test Conditions

Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

Notes:
1) V_Z is programmable from -2V to +7V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance Z_O = 75Ω. 4) V_Z is typically the midpoint of V_{OH} and V_{OL}. 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

Flash AC Characteristics – Read Only Operations

(Vcc = 5.0V, Vss = 0V, Tc = -55°C to +125°C)

Parameter	Symbol JEDEC	Symbol Stand'd	–60 Min	–60 Max	–70 Min	–70 Max	–90 Min	–90 Max	Units
Read Cycle Time	t_{AVAV}	t_{RC}	60		70		90		ns
Address Access Time	t_{AVQV}	t_{ACC}		60		70		90	ns
Chip Enable Access Time	t_{ELQV}	t_{CE}		60		70		90	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		30		35		35	ns
Chip Enable to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		20	ns
Output Enable High to Output High Z(1)	t_{GHQZ}	t_{DF}		20		20		20	ns
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change, Whichever is First	t_{AXQX}	t_{OH}	0		0		0		ns

Note 1. Guaranteed by design, but not tested

Flash AC Characteristics – Write / Erase / Program Operations, $\overline{FWE}$ Controlled

(Vcc = 5.0V, Vss = 0V, Tc = -55°C to +125°C)

Parameter	Symbol JEDEC	Symbol Stand'd	–60 Min	–60 Max	–70 Min	–70 Max	–90 Min	–90 Max	Units
Write Cycle Time	t_{AVAC}	t_{WC}	60		70		90		ns
Chip Enable Setup Time	t_{ELWL}	t_{CE}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	40		45		45		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	40		45		45		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		45		45		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Programming Operation	t_{WHWH1}		14	TYP	14	TYP	14	TYP	µs
Sector Erase Time	t_{WHWH2}			30		30		30	Sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		µs
Vcc Setup Time		t_{VCE}		50		50		50	µs
Chip Programming Time			50		50		50		Sec
Chip Enable Hold Time		t_{OEH} [1]	10		10		10		ns
Chip Erase Time	t_{WHWH3}			120		120		120	Sec

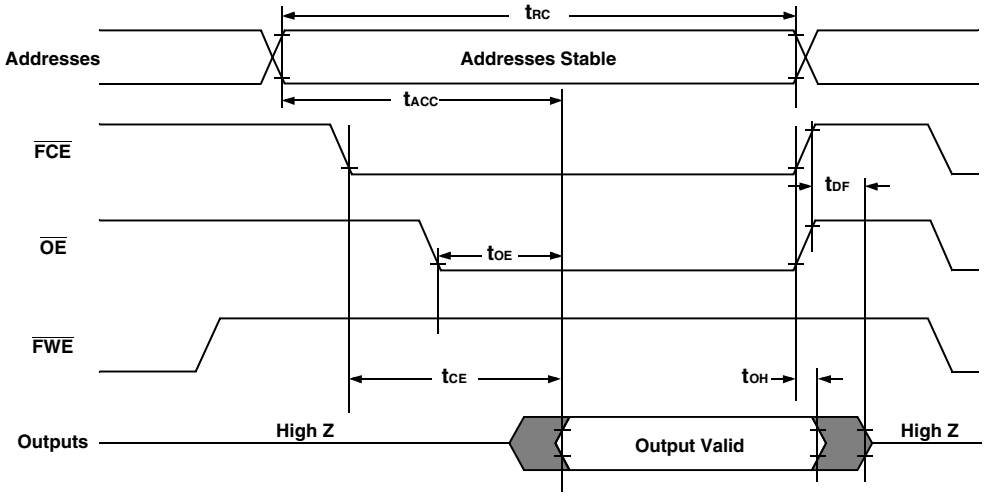
1. Toggle and Data Polling only.

Flash AC Characteristics – Write / Erase / Program Operations, $\overline{FCE}$ Controlled

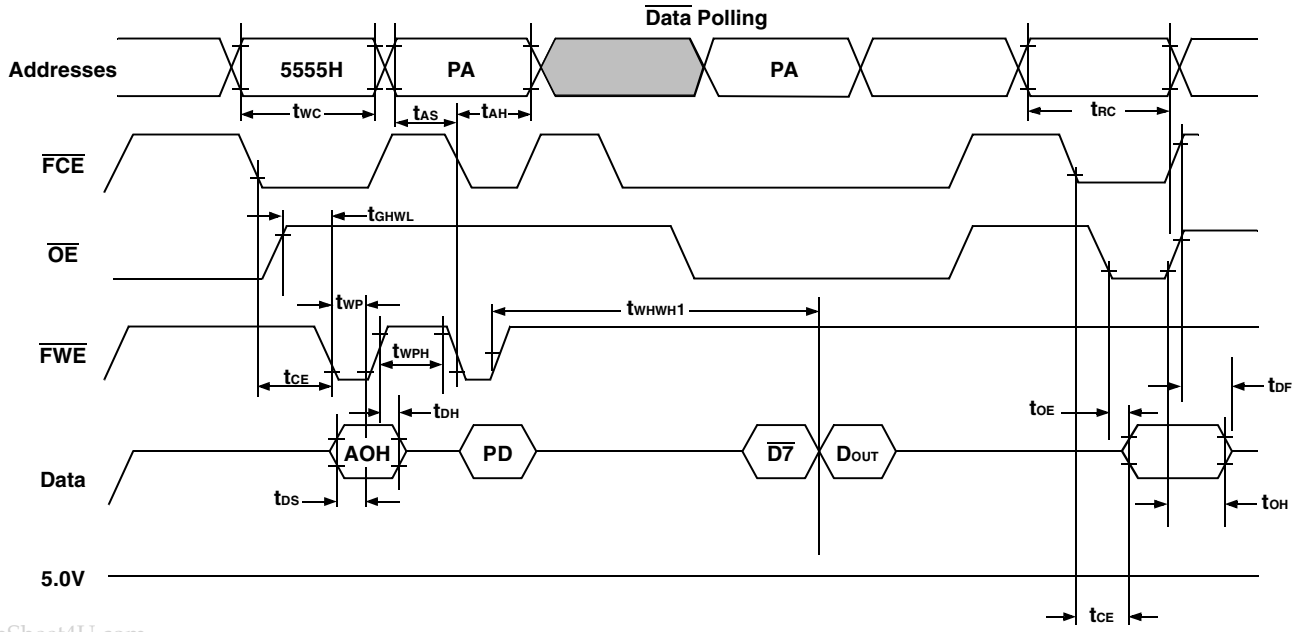
(Vcc = 5.0V, Vss = 0V, Tc = -55°C to +125°C)

Parameter	Symbol JEDEC	Symbol Stand'd	–60 Min	–60 Max	–70 Min	–70 Max	–90 Min	–90 Max	Units
Write Cycle Time	t_{AVAC}	t_{WC}	60		70		90		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Enable Pulse Width	t_{ELEH}	t_{CP}	40		45		45		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	40		45		45		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		45		45		ns
Chip Enable Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming	t_{WHWH1}		14	TYP	14	TYP	14	TYP	µs
Sector Erase Time	t_{WHWH2}			30		30		30	Sec
Read Recovery Time	t_{GHEL}		0		0		0		ns
Chip Programming Time				50		50		50	Sec
Chip Erase Time	t_{WHWH3}			120		120		120	Sec

AC Waveforms for Flash Memory Read Operations



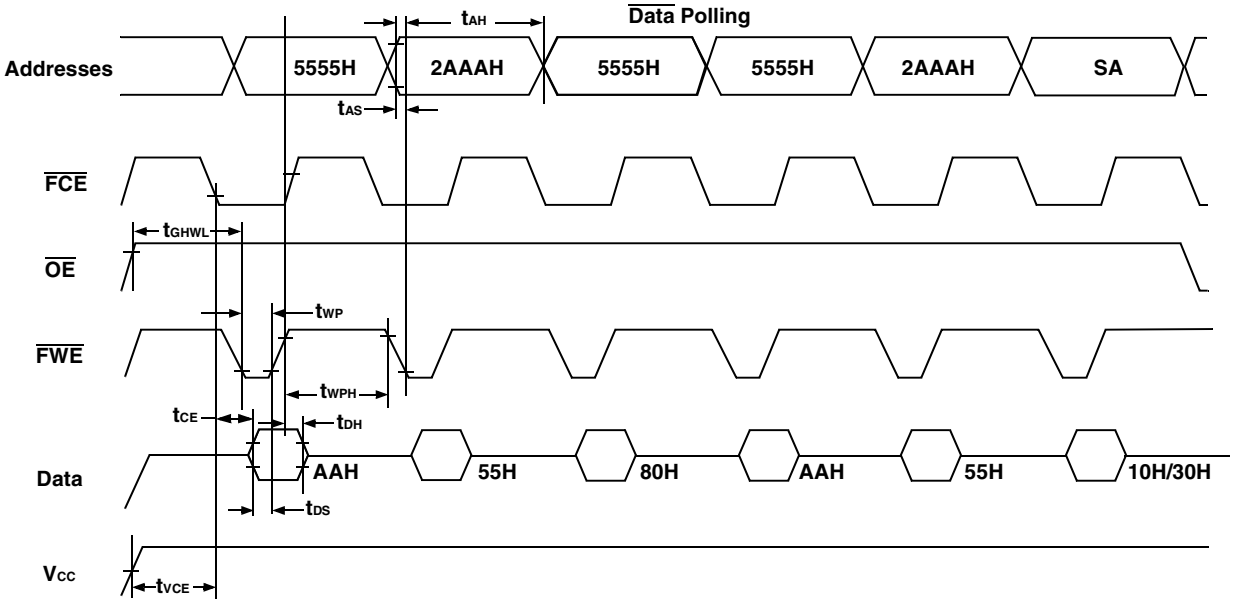
Write/Erase/Program Operation for Flash Memory, FWE Controlled



Notes:

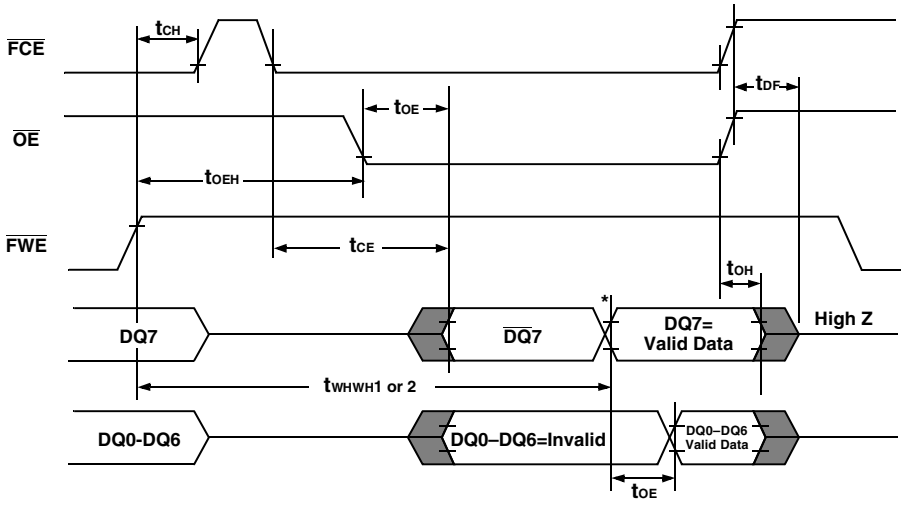
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the 0utput of the complement of the data written to the deviced.
4. Dout is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC Waveforms Chip/Sector Erase Operations for Flash Memory



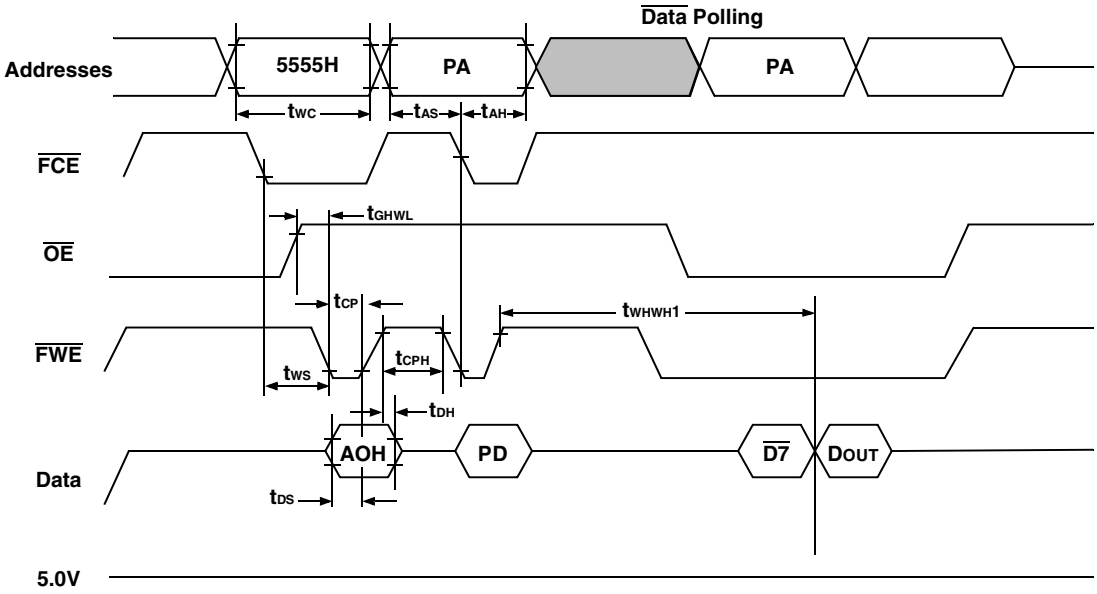
Notes:
1. SA is the sector address for sector erase.

AC Waveforms for Data Polling During Embedded Algorithm Operations for Flash Memory



** DQ7=Valid Data (The device has completed the Embedded operation).*

Write/Erase/Program Operation for Flash Memory, $\overline{FCE}$ Controlled



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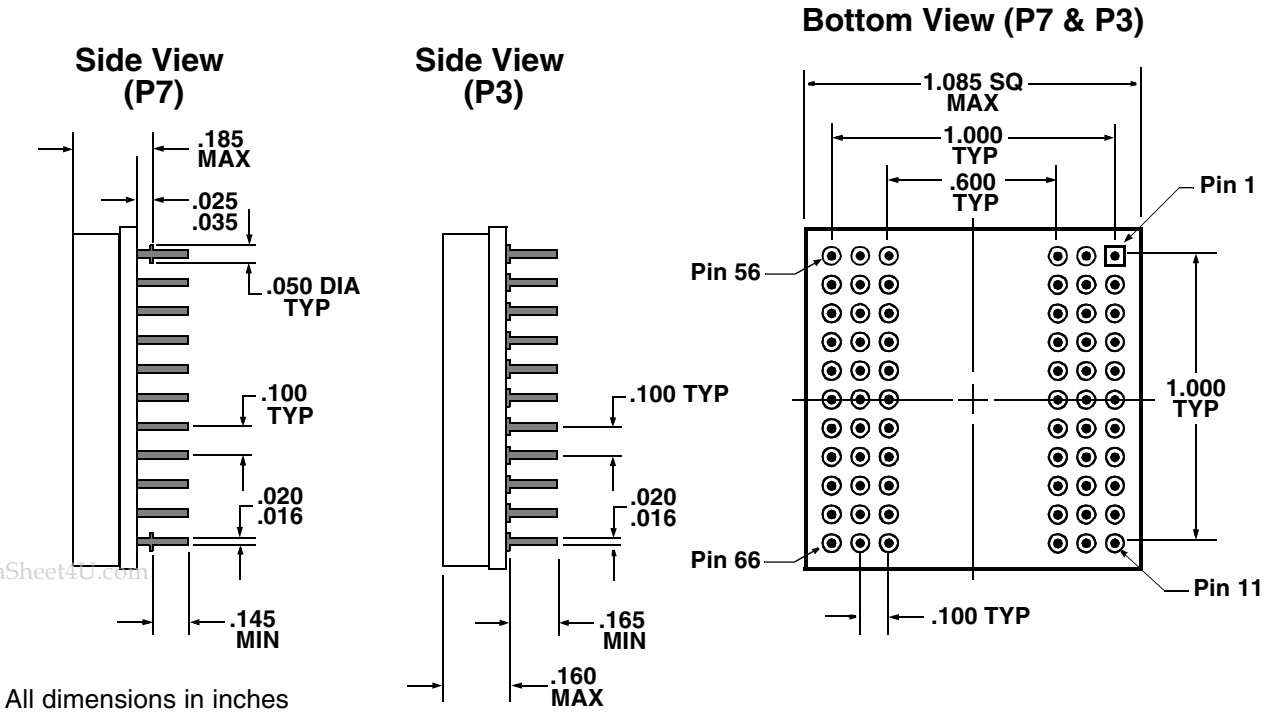
3. $\overline{D7}$ is the 0utput of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Pin Numbers & Functions

66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	SI/O8	18	A12	35	FI/O9	52	$\overline{FWE_1}$
2	SI/O9	19	Vcc	36	FI/O10	53	$\overline{FCE_1}$
3	SI/O10	20	$\overline{SCE_1}$	37	A6	54	GND
4	A13	21	NC	38	A7	55	FI/O3
5	A14	22	SI/O3	39	NC	56	FI/O15
6	A15	23	SI/O15	40	A8	57	FI/O14
7	A16	24	SI/O14	41	A9	58	FI/O13
8	A17	25	SI/O13	42	FI/O0	59	FI/O12
9	SI/O0	26	SI/O12	43	FI/O1	60	A0
10	SI/O1	27	$\overline{OE}$	44	FI/O2	61	A1
11	SI/O2	28	A18	45	Vcc	62	A2
12	$\overline{SWE_2}$	29	$\overline{SWE_1}$	46	$\overline{FCE_2}$	63	FI/O7
13	$\overline{SCE_2}$	30	SI/O7	47	$\overline{FWE_2}$	64	FI/O6
14	GND	31	SI/O6	48	FI/O11	65	FI/O5
15	SI/O11	32	SI/O5	49	A3	66	FI/O4
16	A10	33	SI/O4	50	A4		
17	A11	34	FI/O8	51	A5		

"P3" — 1.08" SQ PGA Type Package Standard (without shoulders)
"P7" — 1.08" SQ PGA Type Package (with shoulders on Pins 1, 11, 56 & 66)

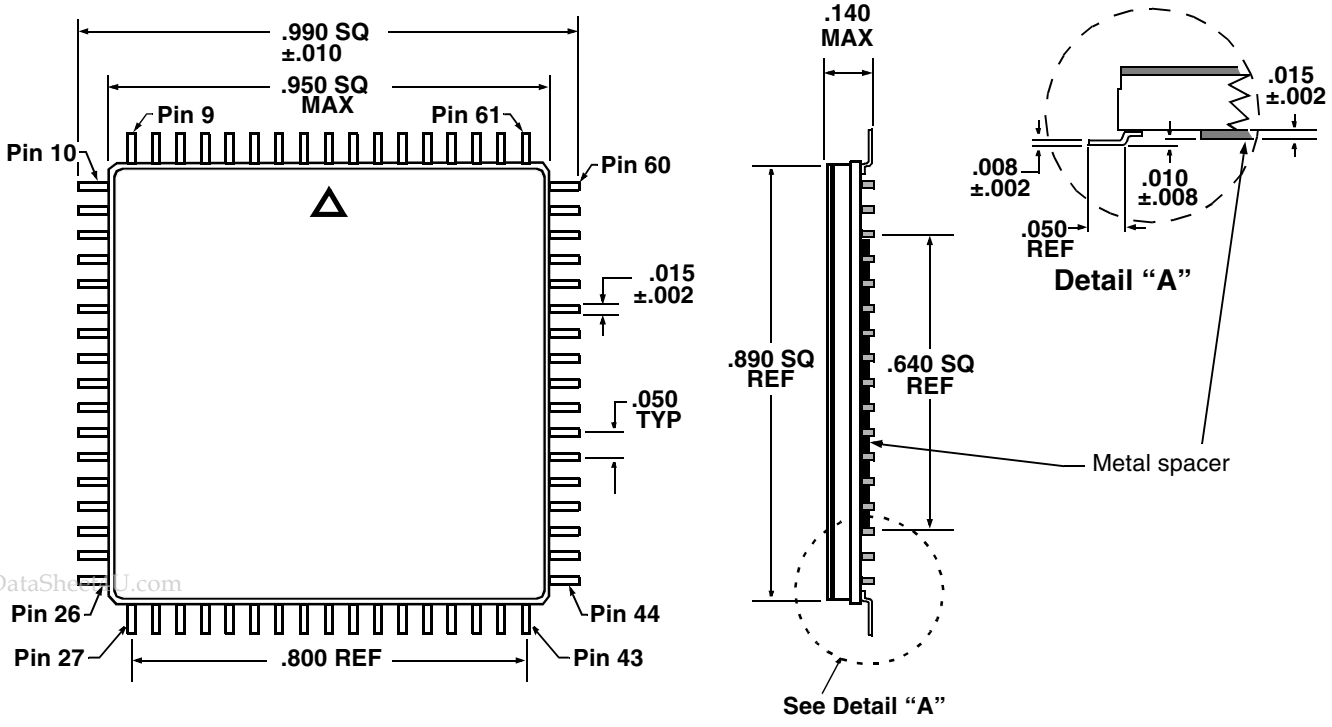


All dimensions in inches

Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{FCE_1}$	19	SI/O8	36	$\overline{SCE_2}$	53	FI/O7
3	A5	20	SI/O9	37	A17	54	FI/O6
4	A4	21	SI/O10	38	$\overline{SWE_2}$	55	FI/O5
5	A3	22	SI/O11	39	$\overline{FWE_1}$	56	FI/O4
6	A2	23	SI/O12	40	$\overline{FWE_2}$	57	FI/O3
7	A1	24	SI/O13	41	A18	58	FI/O2
8	A0	25	SI/O14	42	NC	59	FI/O1
9	NC	26	SI/O15	43	NC	60	FI/O0
10	SI/O0	27	Vcc	44	FI/O15	61	Vcc
11	SI/O1	28	A11	45	FI/O14	62	A10
12	SI/O2	29	A12	46	FI/O13	63	A9
13	SI/O3	30	A13	47	FI/O12	64	A8
14	SI/O4	31	A14	48	FI/O11	65	A7
15	SI/O5	32	A15	49	FI/O10	66	A6
16	SI/O6	33	A16	50	FI/O9	67	$\overline{SWE1}$
17	SI/O7	34	$\overline{SCE_1}$	51	FI/O8	68	$\overline{FCE_2}$

"F18" — CQFP Package



All dimensions in inches

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Ordering Information

Model Number	DESC SMD Number	Speed	Package
ACT–SF2816N–26P3Q	TBD	25(S) / 60(F) ns	1.08"sq PGA-Type
ACT–SF2816N–37P3Q	TBD	35(S) / 70(F) ns	1.08"sq PGA-Type
ACT–SF2816N–39P3Q	TBD	35(S) / 90(F) ns	1.08"sq PGA-Type
ACT–SF2816N–26P7Q	TBD	25(S) / 60(F) ns	1.08"sq PGA-Type
ACT–SF2816N–37P7Q	TBD	35(S) / 70(F) ns	1.08"sq PGA-Type
ACT–SF2816N–39P7Q	TBD	35(S) / 90(F) ns	1.08"sq PGA-Type
ACT–SF2816N–26F18Q	TBD	25(S) / 60(F) ns	.94"sq CQFP
ACT–SF2816N–37F18Q	TBD	35(S) / 70(F) ns	.94"sq CQFP
ACT–SF2816N–39F18Q	TBD	35(S) / 90(F) ns	.94"sq CQFP

Note: (S) = Speed for SRAM, (F) = Speed for FLASH

Part Number Breakdown

ACT– S F 28 16 N– 26 P7 Q

Aeroflex Circuit Technology

Memory Type
SF = SRAM Flash Combo Module

Memory Depth
2 = 2M SRAM, 8 = Locations

Memory Width, Bits

Options, N = none

Memory Speed Code
26 = 25ns SRAM & 60ns FLASH
37 = 35ns SRAM & 70ns FLASH
39 = 35ns SRAM & 90ns FLASH

Screening
C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screening *
Q = MIL-PRF-38534 Compliant / SMD

Package Type & Size

Surface Mount Packages
F18 = .94"SQ 68 Lead Dual-Cavity CQFP

Thru-Hole Packages
P3 = 1.085"SQ PGA 66 Pins with out shoulder
P7 = 1.085"SQ PGA 66 Pins with shoulder

*** Screened to the individual test methods of MIL-STD-883**

Specifications subject to change without notice.

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