ACT4050

Rev 2, 01-Jul-11

Wide Input 3.5A Step Down Converter

FEATURES

- **3.5A Output Current**
- **Up to 96% Efficiency**
- **4.5V to 15V Input Range**
- **12μA Shutdown Supply Current**
- **400kHz Switching Frequency**
- **Adjustable Output Voltage From 0.817V**
- **Cycle-by-Cycle Current Limit Protection**
- **Thermal Shutdown Protection**
- **Frequency Fold-Back at Short Circuit**
- **Stability with Wide Range of Capacitors, Including Low ESR Ceramic Capacitors**
- **SOP-8/EP (Exposed Pad) Package**

APPLICATIONS

- **Digital TV**
- **Portable DVDs**
- **Car-Powered or Battery-Powered Equipments**
- **Set-Top Boxes**
- **Telecom Power Supplies**
- **Consumer Electronics**

GENERAL DESCRIPTION

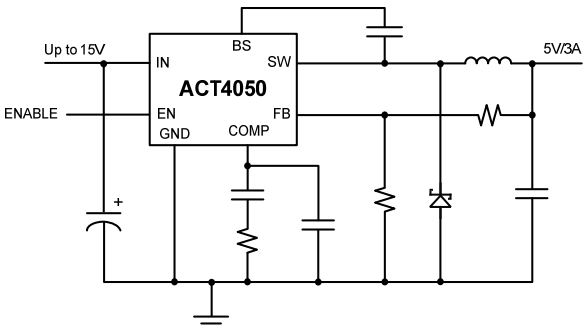
The ACT4050 is a current-mode step-down DC/DC converter that provides up to 3.5A of output current at 400kHz switching frequency. The device utilizes Active-Semi's proprietary high voltage process for operation with input voltages up to 15V.

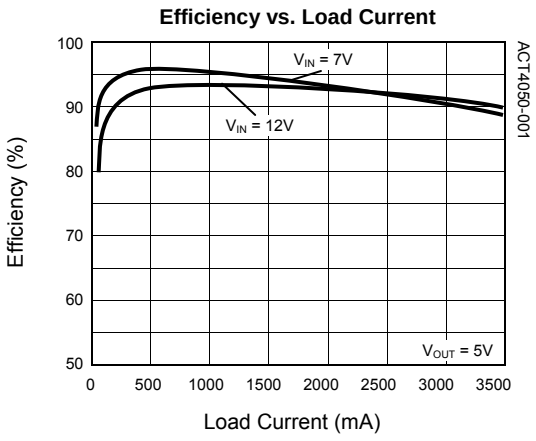
The ACT4050 provides fast transient response and eases loop stabilization while providing excellent line and load regulation. This device features a very low ON-resistance power MOSFET which provides peak operating efficiency up to 96%. In shutdown mode, the ACT4050 consumes only 12μA of supply current.

This device also integrates protection features including cycle-by-cycle current limit, thermal shutdown and frequency fold-back at short circuit.

The ACT4050 is available in a SOP-8/EP (Exposed Pad) package and requires very few external devices for operation.

TYPICAL APPLICATION CIRCUIT

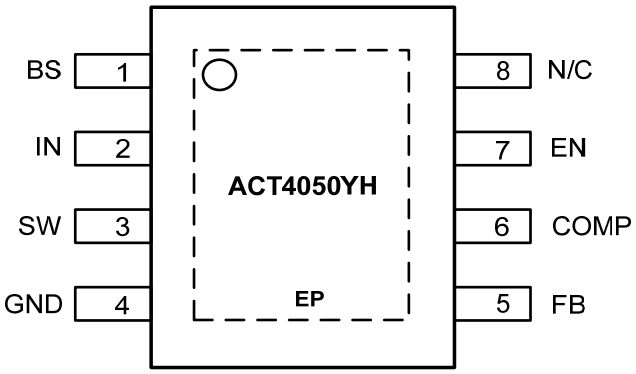




ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
ACT4050YH	-40°C to 85°C	SOP-8/EP	8	TUBE
ACT4050YH-T	-40°C to 85°C	SOP-8/EP	8	TAPE & REEL

PIN CONFIGURATION



SOP-8/EP

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	BS	Bootstrap. This pin acts as the positive rail for the high-side switch's gate driver. Connect a 10nF capacitor between BS and SW.
2	IN	Input Supply. Bypass this pin to GND with a low ESR capacitor. See *Input Capacitor* in the *Application Information* section.
3	SW	Switch Output. Connect this pin to the switching end of the inductor.
4	GND	Ground.
5	FB	Feedback Input. The voltage at this pin is regulated to 0.817V. Connect to the resistor divider between output and ground to set output voltage.
6	COMP	Compensation Pin. See *Stability Compensation* in the *Application Information* section.
7	EN	Enable Input. When higher than 1.3V, this pin turns the IC on. When lower than 0.9V, this pin turns the IC off. Output voltage is discharged when the IC is off. When left unconnected, EN is pulled up to 4.5V typical with a 2μA pull-up current.
8	N/C	Not Connected.
EP	EP	Exposed Pad shown as dashed box. The exposed thermal pad should be connected to board ground plane and pin 4. The ground plane should include a large exposed copper pad under the package for thermal dissipation (see package outline). The leads and exposed pad should be flush with the board, without offset from the board surface.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
IN Supply Voltage	-0.3 to 15	V
SW Voltage	-1 to V_{IN} + 1	V
BS Voltage	V_{SW} - 0.3 to V_{SW} + 8	V
EN, FB Voltage	-0.3 to 6	V
Continuous SW Current	Internally Limited	A
Junction to Ambient Thermal Resistance (θ_{JA})	46	°C/W
Maximum Power Dissipation	1.8	W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

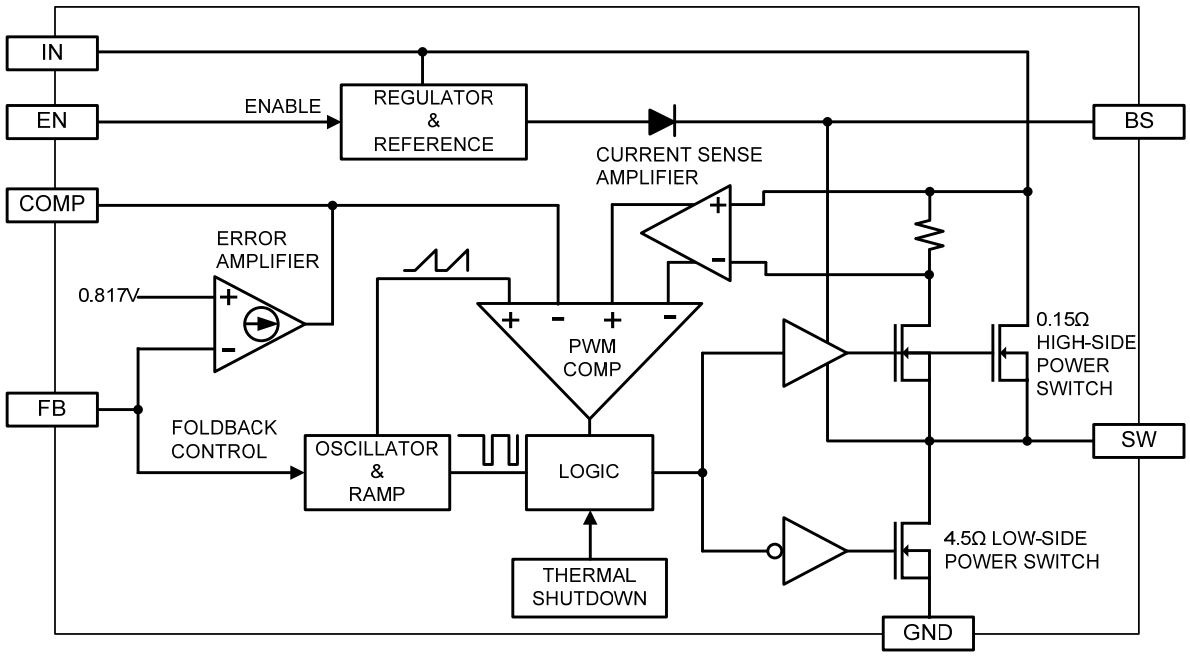
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{OUT} = 3V, I_{LOAD} = 0V to 1A	4.5		15	V
Feedback Voltage	V_{FB}	5V ≤ V_{IN} ≤ 15V	0.8	0.817	0.834	V
High-Side Switch On Resistance	R_{ONH}			0.15		Ω
Low-Side Switch On Resistance	R_{ONL}			4.5		Ω
SW Leakage		V_{EN} = 0		0	10	μA
High-Side Switch Peak Current Limit	I_{LIM}	Duty Cycle = 50%		5.4		A
COMP to Current Limit Transconductance	G_{COMP}			2.5		A/V
Error Amplifier Transconductance	G_{EA}	ΔI_{COMP} = ±10μA		650		μA/V
Error Amplifier DC Gain	A_{VEA}			4000		V/V
Switching Frequency	f_{SW}		350	400	450	kHz
Short Circuit Switching Frequency		V_{FB} = 0		60		kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V		95		%
Minimum On Time	Ton_Min			400		ns
Minimum Duty Cycle		V_{FB} = 0.9V			0	%
Enable Threshold Voltage		Hysteresis = 0.1V	0.8	1.1	1.4	V
Enable Pull-Up Current		Pin pulled up to 4.5V typically when left unconnected		2		μA
Supply Current in Shutdown		V_{EN} = 0		12	20	μA
IC Supply Current in Operation		V_{EN} = 3V, V_{FB} = 0.9V		0.5	1	mA
Thermal Shutdown Temperature		Hysteresis = 10°C		160		°C

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As seen in *Functional Block Diagram*, the ACT4050 is a current mode pulse width modulation (PWM) converter. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off and the Low-Side Power Switch turns on. At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again.

The High-Side Power Switch is driven by logic using BS as the positive rail. This pin is charged to V_{SW} + 6V when the Low-Side Power Switch turns on.

The COMP voltage is the integration of the error between FB input and the internal 0.817V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Current limit happens when COMP reaches its maximum clamp value of 2.15V.

The Oscillator normally switches at 400kHz. However, if FB voltage is less than 0.7V, then the switching frequency decreases until it reaches a typical value of 60kHz at V_{FB} = 0.5V.

Shutdown Control

The ACT4050 EN pin contains a precision 1.1V comparator with 100mV hysteresis, as well as a 2μA pull-up current source. This combination can be used to control the on/off operation of ACT4050 using several methods:

1) First, "always-on" operation can be enabled simply by floating the EN pin. Any time power is applied to VIN, the EN pull-up current source will bring the pin above 1.1V and enable the IC. In this case, under-voltage lockout will be controlled by an internal 4.2V comparator on VIN.

2) Second, an open-drain or open-collector logic device can be used to pull the EN pin low to provide digital ON/OFF control. When the logic pull-down is disabled, the internal 2μA pull-up current will bring the EN pin high and enable the chip.

3) Third, a known startup delay time can be created by adding a small capacitor from EN to GND in

addition to the open-drain or open-collector logic device. When the logic pull-down is disabled, the voltage at EN will ramp up at a rate determined by the 2μA EN pull-up current and the capacitor. Once the voltage at EN exceeds the 1.1V threshold, the device will be enabled. For the case of using multiple ACT4050, time-based output sequencing can be generated by placing different capacitors at each ACT4050 EN pin.

The start up time delay can be calculated as a simple function of the EN capacitor using the equation:

$T\ (ms) = 0.55 \times C_{EN}\ (nF)$

Table 1:

Enable Delay Time vs. EN Capacitor Value

CAPACITOR VALUE	DELAY TIME (ms)
2.2nF	1.2
3.3nF	1.9
10nF	5.5

4) Fourth, by using the 1.1V precision comparator in the EN circuitry, "power-OK" type output sequencing can be generated. By connecting the EN pin of one ACT4050 to the output of another device, the ACT4050 will only start up once the second device's output has exceeded the 1.1V level. A resistor divider can be used to adjust the ACT4050 startup to any point on the second device's output range.

5) Finally, the EN comparator can be used for "Line UVLO" to prevent the ACT4050 from starting up before the input voltage is high enough to support the output. By using a resistor divider from VIN to GND (center tap = 1.1V EN threshold), the device can be enabled and disabled based on the voltage at VIN. Since the internal UVLO voltage is 4.2V, Line UVLO is recommended for outputs above this 4.2V level to ensure clean startup. For the example of a 5V output, it is desirable to prevent IC startup until VIN has exceeded the 5V level. To start the IC at 6V input, we place a 10kΩ/47kΩ resistor divider from VIN to EN to GND, which enables the IC at VIN greater than 6.3V and disables the IC when VIN decreases below 5.2V.

Thermal Shutdown

The ACT4050 automatically turns off when its junction temperature exceeds 160°C and automatically turns on again when the junction temperature falls below 140°C .

APPLICATIONS INFORMATION

Output Voltage Setting

Figure 1:

Output Voltage Setting

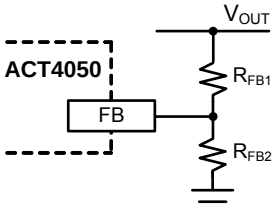


Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Typically, use R_{FB2} ≈ 10kΩ and determine R_{FB1} from the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.817\,V} - 1\right) \quad (1)$$

Note: To achieve best performance with 12V input application, we recommend to use output voltage greater than 1.4V.

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value: higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUTMAX} K_{RIPPLE}} \quad (2)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, I_{OUTMAX} is the maximum output current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum output current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK\text{-}PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}} \quad (3)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK\text{-}PK} \quad (4)$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK\text{-}PK} \quad (5)$$

L_{LIM} is the internal current limit, as shown in Electrical Characteristics Table.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10µF. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1µF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{V_{IN}}{28 \times f_{SW}^{\,2} L C_{OUT}} \quad (6)$$

where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output capacitor, typically choose a capacitance of about 22µF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

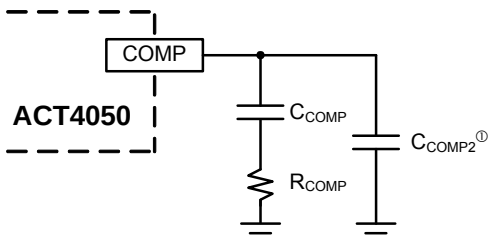
Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

STABILITY COMPENSATION

Figure 2:

Stability Compensation



①: C_{COMP2} is needed only for high ESR output capacitor

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 2. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.82V}{I_{OUT}} A_{VEA} G_{COMP} \quad (7)$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}} \quad (8)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}} \quad (9)$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}} \quad (10)$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}} \quad (11)$$

The following steps should be used to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R_{COMP}:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \times 0.82V}$$

$$= 1.88 \times 10^{8} V_{OUT} C_{OUT} \quad (\Omega) \quad (12)$$

but limit R_{COMP} to 15kΩ maximum.

STEP 2. Set the zero f_{Z1} at 1/4 of the cross over frequency. If R_{COMP} is less than 15kΩ, the equation for C_{COMP} is:

$$C_{COMP} = \frac{1.6 \times 10^{-5}}{R_{COMP}} \quad (F) \quad (13)$$

If R_{COMP} is limited to 15kΩ, then the actual cross over frequency is 3.4 / ($V_{OUT}C_{OUT}$). Therefore:

$$C_{COMP} = 1.2 \times 10^{-5} V_{OUT} C_{OUT} \quad (F) \quad (14)$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESRCOUT} \geq Min\left(\frac{1.1 \times 10^{-6}}{C_{OUT}}, 0.012 \times V_{OUT}\right) \quad (\Omega) \quad (15)$$

And the proper value for C_{COMP2} is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}} \quad (16)$$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.

Table 3 shows some calculated results based on the compensation method above.

Table 2:

Typical Compensation for Different Output Voltages and Output Capacitors

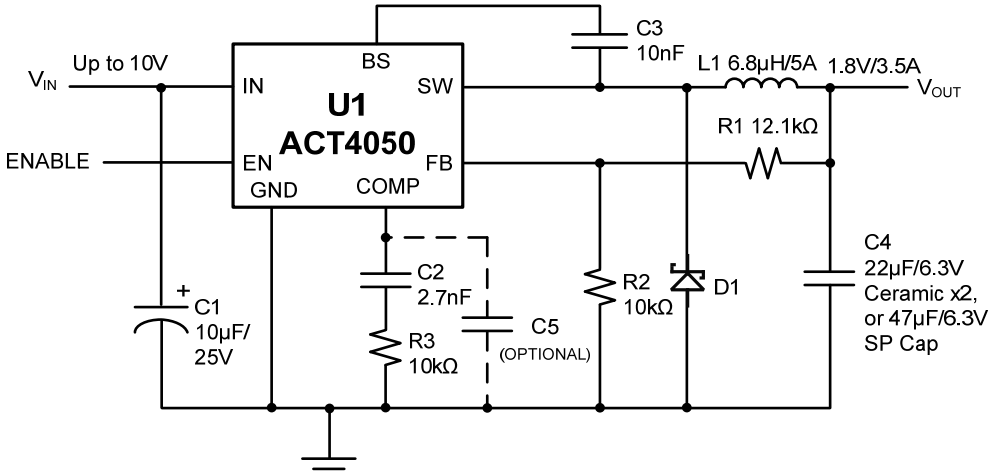
V_{OUT}	C_{OUT}	R_{COMP}	C_{COMP}	C_{COMP2}①
2.5V	2x22µF Ceramic	8.2kΩ	2.2nF	None
3.3V	2x22µF Ceramic	12kΩ	1.5nF	None
5V	2x22µF Ceramic	15kΩ	1.5nF	None
2.5V	47µF SP CAP	15kΩ	1.5nF	None
3.3V	47µF SP CAP	15kΩ	1.8nF	None
5V	47µF SP CAP	15kΩ	2.7nF	None
2.5V	470µF/6.3V/30mΩ	15kΩ	15nF	1nF
3.3V	470µF/6.3V/30mΩ	15kΩ	22nF	1nF
5V	470µF/6.3V/30mΩ	15kΩ	27nF	None

①: C_{COMP2} is needed for high ESR output capacitor.

Figure 3 shows an example ACT4050 application circuit generating a 2.5V/3.5A output.

Figure 3:

ACT4050 1.8V/3.5A Output Application①



①: D1 is a 30V, 5A Schottky diode with low forward voltage, a B530C equivalent. C4 can be either a ceramic capacitor (Panasonic ECJ-3YB1C226M) or SP-CAP (Specialty Polymer) Aluminum Electrolytic Capacitor such as Panasonic EEFCD0J470XR. The SP-Cap is based on aluminum electrolytic capacitor technology, but uses a solid polymer electrolyte and has very stable capacitance characteristics in both operating temperature and frequency compared to ceramic, polymer, and low ESR tantalum capacitors.

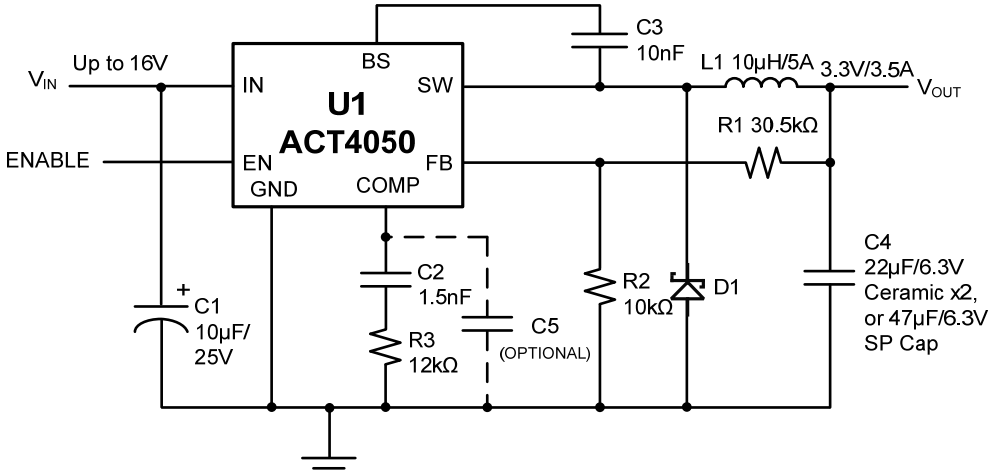
Table 3:

ACT4050EV Bill of Materials (Apply for 1.8V Output Application)

ITEM	DESCRIPTION	MANUFACTURER	QTY	REFERENCE
1	IC, ACT4050	Active-Semi	1	U1
2	Resistor, 12.1kΩ , 1%, SMT, 0603	FengHua, Neohm, Yageo	1	R1
3	Resistor, 10kΩ, 1%, SMT, 0603	FengHua, Neohm, Yageo	1	R2
4	Resistor, 10kΩ, 5%, SMT, 0603	FengHua, Neohm, Yageo	1	R3
5	Capacitor, Ceramic, 10µF/35V, X7R, SMT, 1206	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C1
6	Capacitor, Ceramic, 22µF/6.3V, X7R, SMT, 1206	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	2	C4
7	Capacitor, Ceramic, 10nF/50V, X7R, SMT, 0603	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C3
8	Capacitor, Ceramic, 2.7nF/6.3V, X7R, SMT, 0603	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C2
9	Capacitor, Ceramic, 220pF/6.3V, X7R, SMT, 0603	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C5 (OPTIONAL)
10	Schottky Diode SK53/30V, 5A, SMC	Diodes	1	D1
11	Inductor, CDRH8D43-6R8NC, 6.8µH	Sumida	1	L1

Figure 4:

ACT4050 3.3V/3.5A Output Application①



①: D1 is a 30V, 5A Schottky diode with low forward voltage, a B530C equivalent. C4 can be either a ceramic capacitor (Panasonic ECJ-3YB1C226M) or SP-CAP (Specialty Polymer) Aluminum Electrolytic Capacitor such as Panasonic EEFCD0J470XR. The SP-Cap is based on aluminum electrolytic capacitor technology, but uses a solid polymer electrolyte and has very stable capacitance characteristics in both operating temperature and frequency compared to ceramic, polymer, and low ESR tantalum capacitors.

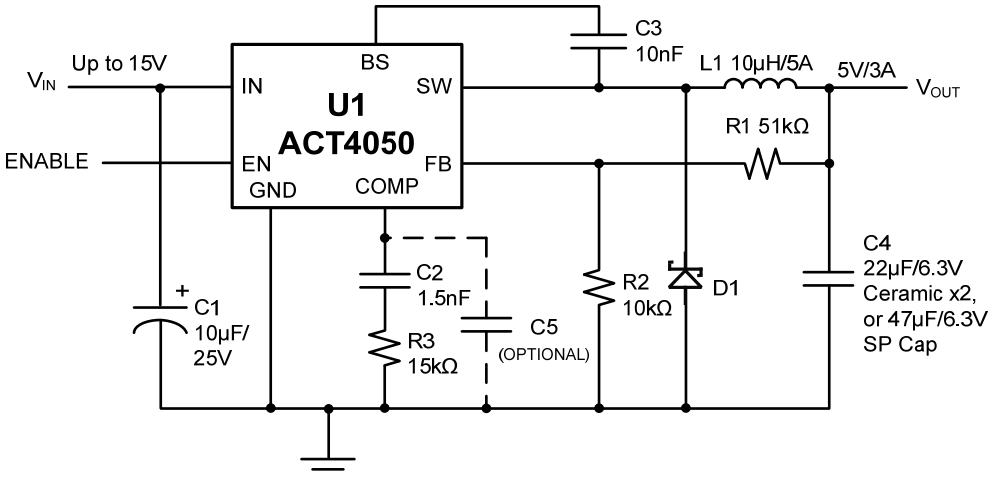
Table 4:

ACT4050EV Bill of Materials (Apply for 3.3V Output Application)

ITEM	DESCRIPTION	MANUFACTURER	QTY	REFERENCE
1	IC, ACT4050	Active-Semi	1	U1
2	Resistor, 30.5kΩ , 1%, SMT, 0603	FengHua, Neohm, Yageo	1	R1
3	Resistor, 10kΩ, 1%, SMT, 0603	FengHua, Neohm, Yageo	1	R2
4	Resistor, 12kΩ, 5%, SMT, 0603	FengHua, Neohm, Yageo	1	R3
5	Capacitor, Ceramic, 10µF/35V, X7R, SMT, 1206	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C1
6	Capacitor, Ceramic, 22µF/6.3V, X7R, SMT, 1206	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	2	C4
7	Capacitor, Ceramic, 10nF/50V, X7R, SMT, 0603	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C3
8	Capacitor, Ceramic, 1.5nF/6.3V, X7R, SMT, 0603	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C2
9	Capacitor, Ceramic, 220pF/6.3V, X7R, SMT, 0603	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C5 (OPTIONAL)
10	Schottky Diode SK53/30V, 5A, SMC	Diodes	1	D1
11	Inductor, CDRH8D43-100NC, 10µH	Sumida	1	L1

Figure 5:

ACT4050 5V/3A Output Application①



①: D1 is a 30V, 5A Schottky diode with low forward voltage, a B530C equivalent. C4 can be either a ceramic capacitor (Panasonic ECJ-3YB1C226M) or SP-CAP (Specialty Polymer) Aluminum Electrolytic Capacitor such as Panasonic EEFCD0J470XR. The SP-Cap is based on aluminum electrolytic capacitor technology, but uses a solid polymer electrolyte and has very stable capacitance characteristics in both operating temperature and frequency compared to ceramic, polymer, and low ESR tantalum capacitors.

Table 5:

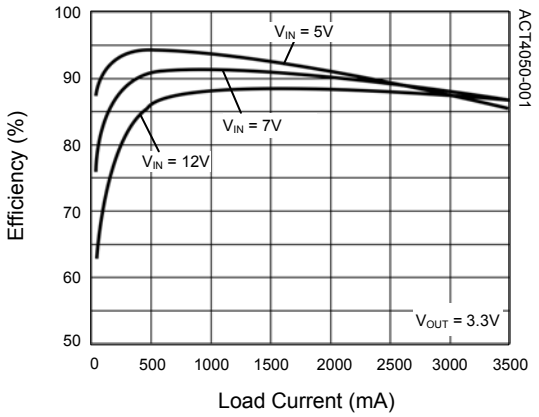
ACT4050EV Bill of Materials (Apply for 5V Output Application)

ITEM	DESCRIPTION	MANUFACTURER	QTY	REFERENCE
1	IC, ACT4050	Active-Semi	1	U1
2	Resistor, 51kΩ , 1%, SMT, 0603	FengHua, Neohm, Yageo	1	R1
3	Resistor, 10kΩ, 1%, SMT, 0603	FengHua, Neohm, Yageo	1	R2
4	Resistor, 15kΩ, 5%, SMT, 0603	FengHua, Neohm, Yageo	1	R3
5	Capacitor, Ceramic, 10μF/35V, X7R, SMT, 1206	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C1
6	Capacitor, Ceramic, 22μF/6.3V, X7R, SMT, 1206	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	2	C4
7	Capacitor, Ceramic, 10nF/50V, X7R, SMT, 0603	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C3
8	Capacitor, Ceramic, 1.5nF/6.3V, X7R, SMT, 0603	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C2
9	Capacitor, Ceramic, 220pF/6.3V, X7R, SMT, 0603	Panasonic, Kemet, Murata, TDK, FengHua, Taiyo Yuden	1	C5 (OPTIONAL)
10	Schottky Diode SK53/30V, 5A, SMC	Diodes	1	D1
11	Inductor, CDRH8D43-100NC, 10μH	Sumida	1	L1

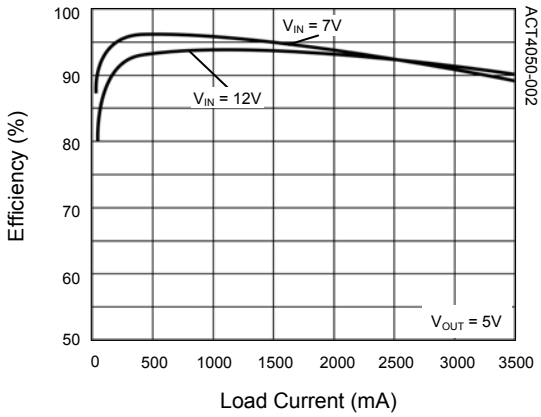
TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit of Figure 5, unless otherwise specified.)

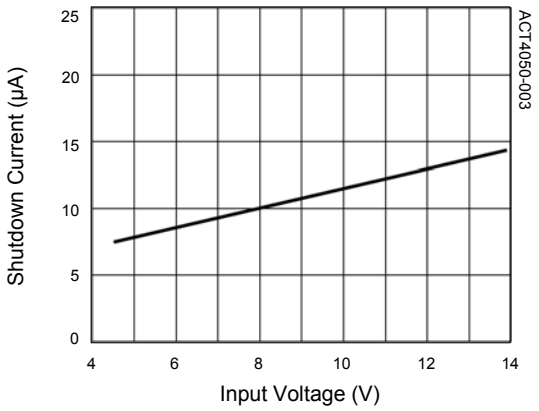
Efficiency vs. Load Current



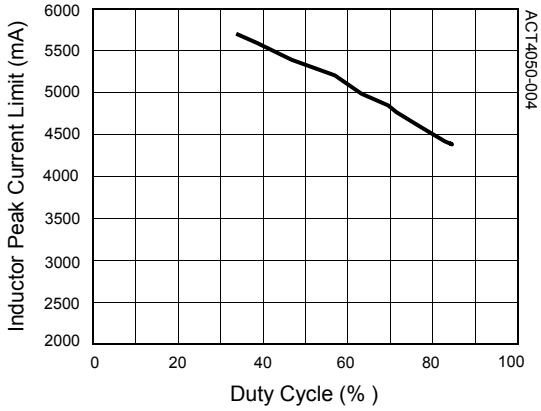
Efficiency vs. Load Current



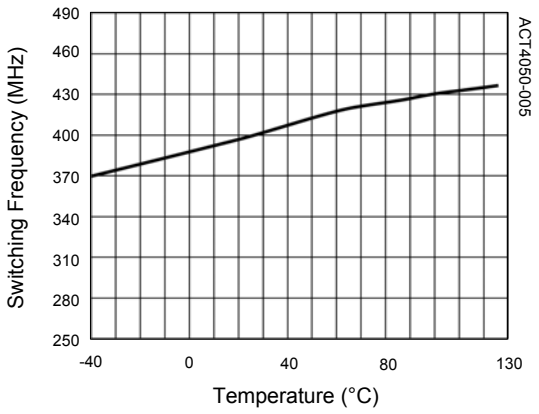
Shutdown Current vs. Input Voltage



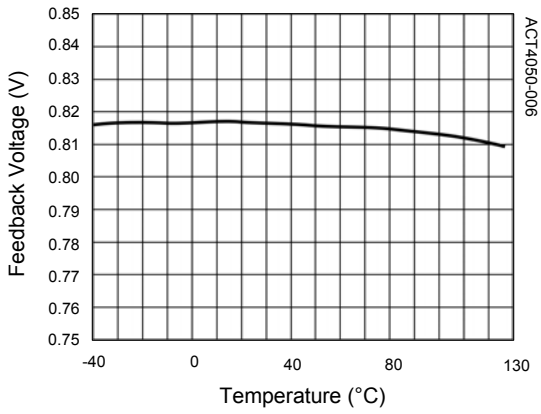
Inductor Peak Current Limit vs. Duty Cycle



Switching Frequency vs. Temperature



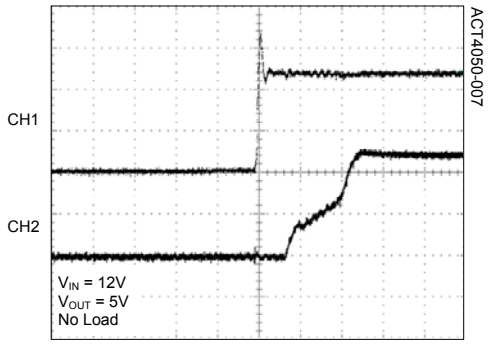
Feedback Voltage vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

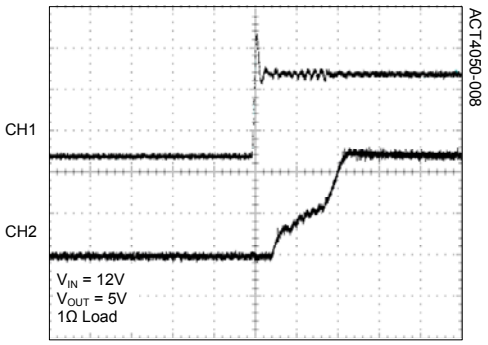
(Circuit of Figure 5, unless otherwise specified.)

Start-up/Shutdown by VIN Pin



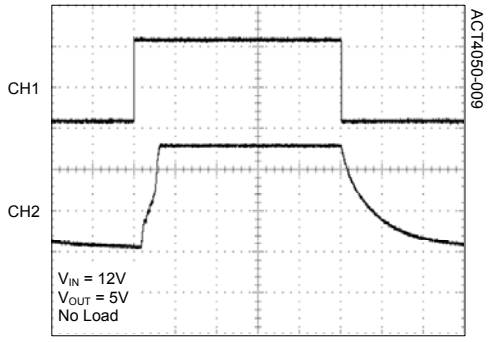
CH1: V_{IN}, 5.0V/div
CH2: V_{OUT}, 2V/div
TIME: 100μs/div

Start-up/Shutdown by VIN Pin



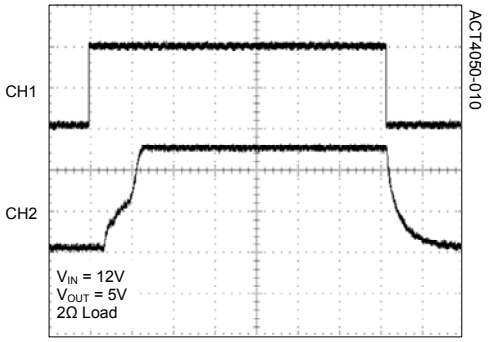
CH1: V_{IN}, 5.0V/div
CH2: V_{OUT}, 2V/div
TIME: 100μs/div

Start-up/Shutdown by EN Pin



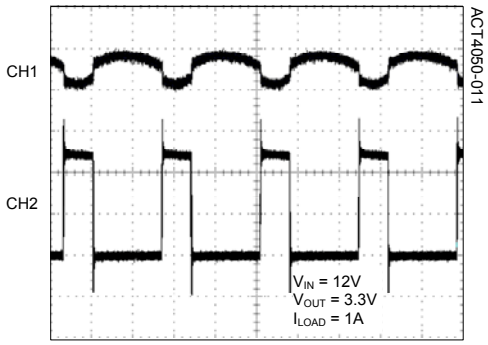
CH1: V_{EN}, 2.0V/div
CH2: V_{OUT}, 2.0V/div
TIME: 400μs/div

Start-up/Shutdown by EN Pin



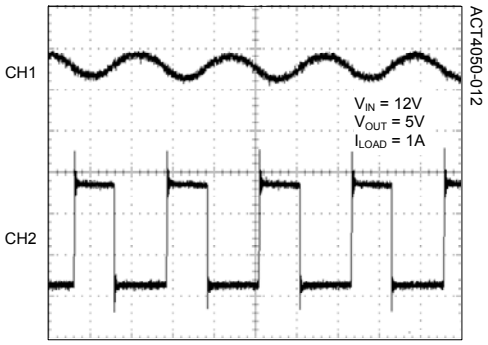
CH1: V_{EN}, 2.0V/div
CH2: V_{OUT}, 2.0V/div
TIME: 200μs/div

Switching Waveform



CH1: V_{OUT}, 20mV/div (AC COUPLED)
CH2: V_{SW}, 5.0V/div
TIME: 1μs/div

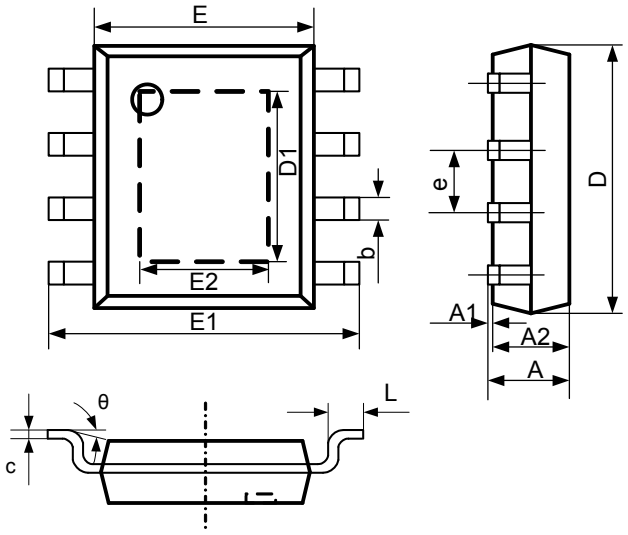
Switching Waveform



CH1: V_{OUT}, 20mV/div (AC COUPLED)
CH2: V_{SW}, 5.0V/div
TIME: 1μs/div

PACKAGE OUTLINE

SOP-8/EP PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.700	0.053	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°