Standard Products

ACT4487 Single Transceiver

for MIL-STD-1553A/B, MIL-STD-1760 & SAE-AS15531

www.aeroflex.com/Avionics

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FEATURES

- Small size, light weight and low power dissipation, single transceiver
- +5V / ±15V DC power supply operation
- Outstanding MIL-STD-1553 / SAE-AS15531 performance
- Monolithic construction
- Input and output TTL compatible design
- Designed for commercial, industrial and aerospace applications
- MIL-PRF-38534 compliant devices available
- Aeroflex-Plainview is a Class H & K MIL-PRF-38534 manufacturer

GENERAL DESCRIPTION

The Aeroflex-Plainview ACT4487 is the next generation monolithic transceiver design which provides full compliance with MIL-STD-1553A/B, MIL-STD-1760 and meets SAE-AS15531 requirements in the smallest package with lower pin count for those designs with less board space. The ACT4487 performs the front-end analog function of inputting and outputting data through a transformer to the MIL-STD-1553 data bus.

Design of this transceiver reflects particular attention to active filter performance. This results in low bit and word error rate with superior waveform purity and minimal zero crossover distortion. Efficient transmitter electrical and thermal design provides low internal power dissipation and heat rise at high as well as low duty cycles.

TRANSMITTER

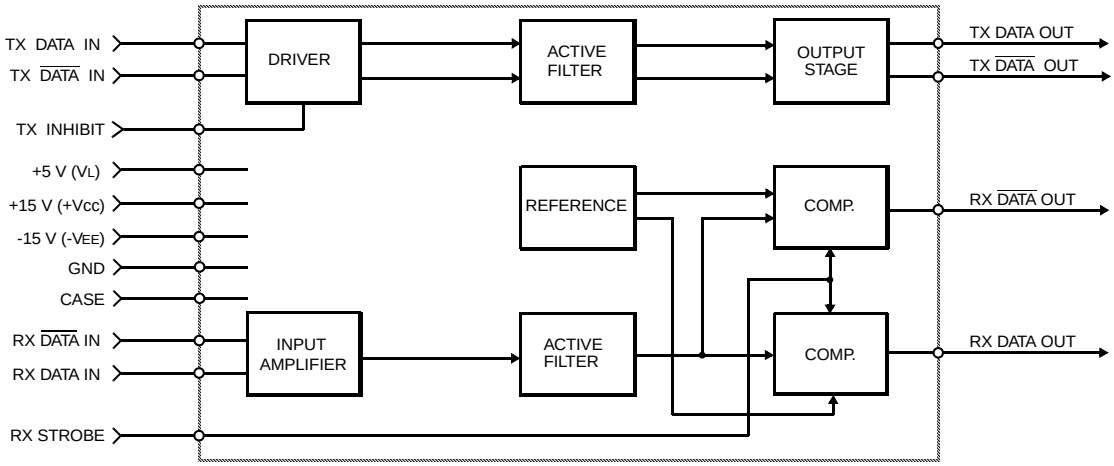
The transmitter section accepts bi-phase TTL data at the input and when coupled to the data bus with a 1.4:1 ratio transformer the data bus signal is typically 7.5 Volts P-P at Point A (See Figure 5). When both DATA and $\overline{\text{DATA}}$ inputs are held low or high, the transmitter output becomes a high impedance and is “removed” from the line. In addition, an overriding “INHIBIT input provides for the removal of the transmitter output from the line. A logic “1” applied to the “INHIBIT” takes priority over the condition of the data inputs and disables the transmitter (See Figure 1 Transmitter Logic Waveform). The Transmitter may be safely operated for an indefinite period with the bus (Point A) short circuited at 100% duty cycle.

RECEIVER

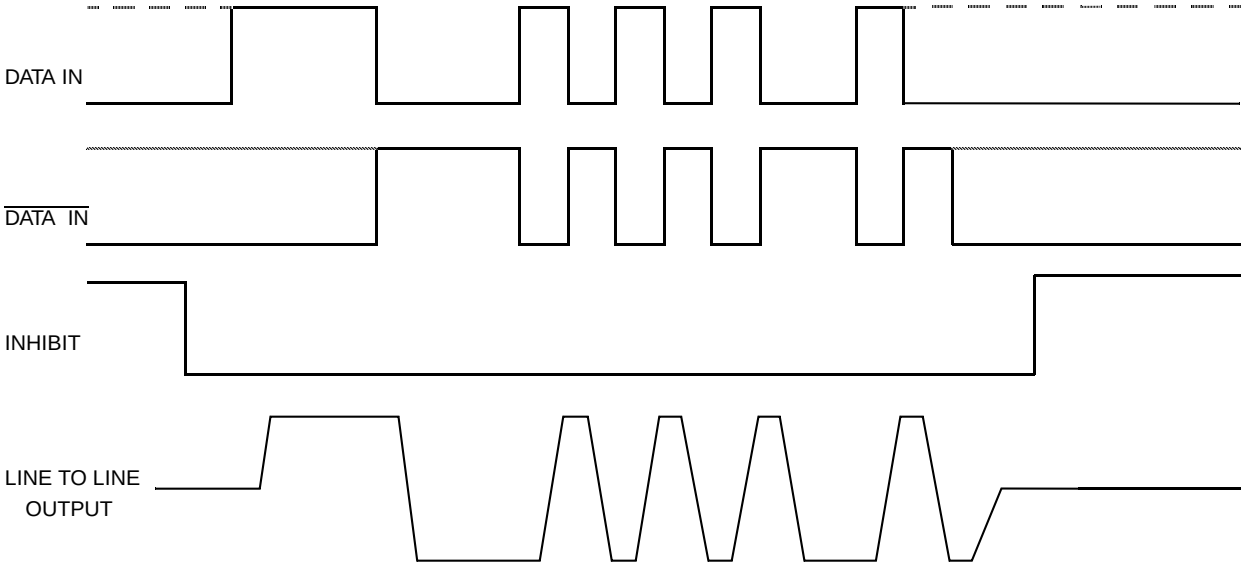
The Receiver section accepts bi-phase differential data at the input and produces two TTL signals at the output. The outputs are DATA and $\overline{\text{DATA}}$, and represent positive and negative excursions of the input beyond a pre-determined threshold (See Figure 2 Receiver Logic Waveform).

The pre-set internal thresholds will detect data bus signals exceeding 1.20 Volts P-P and reject signals less than 0.6 Volts P-P when used with a transformer (See Figure 5 for transformer data and typical connections).

A low level at the Strobe input inhibits the DATA and $\overline{\text{DATA}}$ outputs. If unused, a 2K pull-up to +5 Volts is recommended.

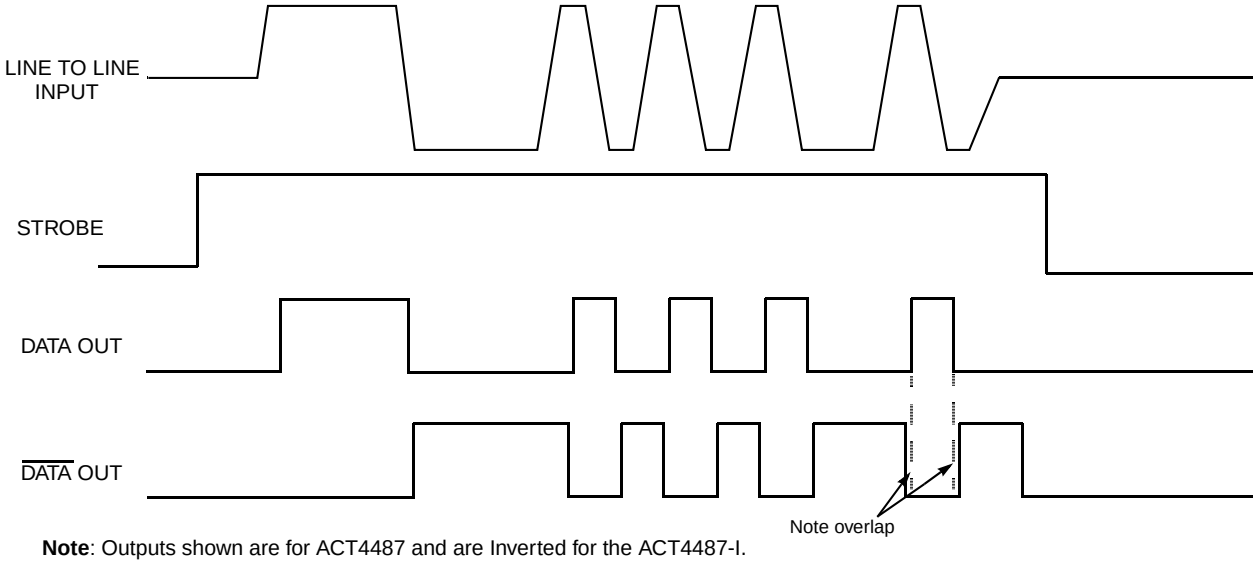


BLOCK DIAGRAM (WITHOUT TRANSFORMER)



Note: DATA and DATA inputs must be complementary waveforms or 50% duty cycle average, with no delays between them, and must be in the same state during off times (both high or low).

FIGURE 1 – TRANSMITTER LOGIC WAVEFORMS IDEALIZED



Note: Outputs shown are for ACT4487 and are Inverted for the ACT4487-I.

FIGURE 2 – RECEIVER LOGIC WAVEFORMS IDEALIZED

ABSOLUTE MAXIMUM RATINGS

Operating case temperature	-55°C to +125°C
Storage case temperature	-65°C to +150°C
Power supply voltage VCC VEE VL	 -0.3 VDC to +18 VDC +0.3 VDC to -18 VDC -0.3 VDC to +7.0 VDC
Logic input voltage	-0.3VDC to +5.5VDC
Receiver differential input	±40 Vp-p
Receiver input voltage (common mode)	±10V
Driver peak output current	200 mA
Total package power dissipation over the full operating case temperature range	2.5 Watt
Maximum junction to case temperature	10°C
Thermal resistance – Junction to case	4°C/W

ELECTRICAL CHARACTERISTICS – DRIVER SECTION

INPUT CHARACTERISTICS, TX DATA IN OR TX $\overline{\text{DATA}}$ IN (Notes 2 & 3 Apply)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
"0" Input Current	V_{IN} = 0.4V	I_{ILD}	-	-0.2	-0.2	mA
"1" Input Current	V_{IN} = 2.7V	I_{IHD}	-	1	40	µA
"0" Input Voltage		V_{ILD}	-	-	0.7	V
"1" Input Voltage		V_{IHD}	2.0	-	-	V

INHIBIT CHARACTERISTICS

"0" Input Current	V_{IN} = 0.4V	I_{ILI}	-	-0.1	-0.2	mA
"1" Input Current	V_{IN} = 2.7V	I_{IHI}	-	1.0	40	µA
"0" Input Voltage		V_{ILI}	-	-	0.7	V
"1" Input Voltage		V_{IHI}	2	-	-	V
Delay from TX inhibit, (0→1) to inhibited output		t_{DXOFF}	-	175	200	nS
Delay from TX inhibit, (1→0) to active output		t_{DXON}	-	90	200	nS
Differential Output Noise, inhibit mode		V_{NOI}	-	2	10	mVp-p
Differential Output Impedance (inhibited) Note 1 See Figure 5	Point B	Z_{OI}	2K	-	-	Ω
	Point C	Z_{OI}	1K	-	-	Ω

OUTPUT CHARACTERISTICS

Differential output level	Figure 5 Point A	V_O	6	7.5	9	Vp-p
Rise and fall times (10% to 90% of p-p output)		t_r	100	200	300	nS
Output offset. See Figure 3. 2.5 µS after midpoint crossing of the parity bit of the last word of a 660µS message.		V_{OS}	-	-	±90	mVpeak
Delay from 50% point of TX DATA or $\overline{\text{TX DATA}}$ input to zero crossing of differential signal		t_{DTX}	-	100	200	nS

ELECTRICAL CHARACTERISTICS – RECEIVER SECTION

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Differential Voltage Range (See Figure 5, Point B)	TXFMR 1.4:1	V_{IDR}	-	14	20	Vpk
Common Mode Rejection Ratio (Note 3)		CMRR	45	-	-	dB
"1" State – Rx Data or Rx $\overline{\text{Data}}$ Output	I_{OH} = -0.4 mA	V_{OH}	2.5	3.7	-	V
"0" State – Rx Data or Rx $\overline{\text{Data}}$ Output	I_{OI} = 4 mA	V_{OL}	-	0.35	0.5	V
Delay (average) from Differential Input Zero Crossings to RX DATA and RX $\overline{\text{DATA}}$ Output 50% points		t_{DRX}	-	270	400	nS
Input Threshold Voltage (referred to the bus)	100KHz–1MHz	V_{TH}	0.60	0.75	1.20	Vp-p

STROBE CHARACTERISTICS (LOGIC "0" INHIBITS OUTPUT)

"0" Input Current	V_S = 0.4V	I_{IL}	-	-0.1	-0.2	mA
"1" Input Current	V_S = 2.7V	I_{IH}	-	1	+40	µA
"0" Input Voltage		V_{IL}	-	-	0.7	V
"1" Input Voltage		V_{IH}	2.0	-	-	V
Strobe Delay (Turn-on or Turn-off)		t_{SD}	-	50	100	nS

POWER DATA

POWER SUPPLY CURRENTS

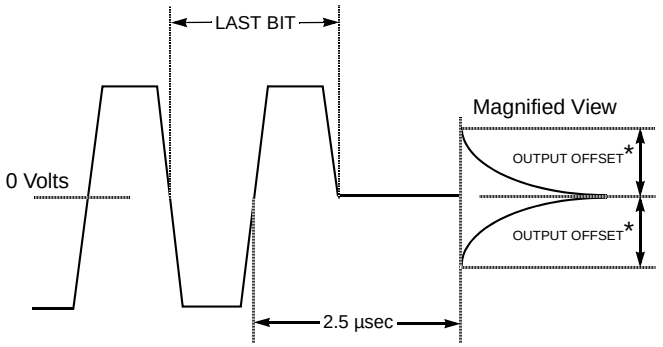
Transmitter Standby	Note 4	I_{CC} I_{EE} I_L	- - -	0 12 18	1 16 30	mA
25% Duty Cycle		I_{CC} I_{EE} I_L	- - -	45 12 18	50 20 30	
50% Duty Cycle		I_{CC} I_{EE} I_L	- - -	90 12 18	100 20 30	
100% Duty Cycle		I_{CC} I_{EE} I_L	- - -	180 12 18	200 20 30	

POWER SUPPLY VOLTAGE

±15V Operating Power Supply Voltage Range		V_{CC} V_{EE}	+14.25 -14.25	+15.00 -15.00	+15.75 -15.75	V V
+5V Operating Power Supply Voltage Range		V_L	+4.50	+5.00	+5.50	V

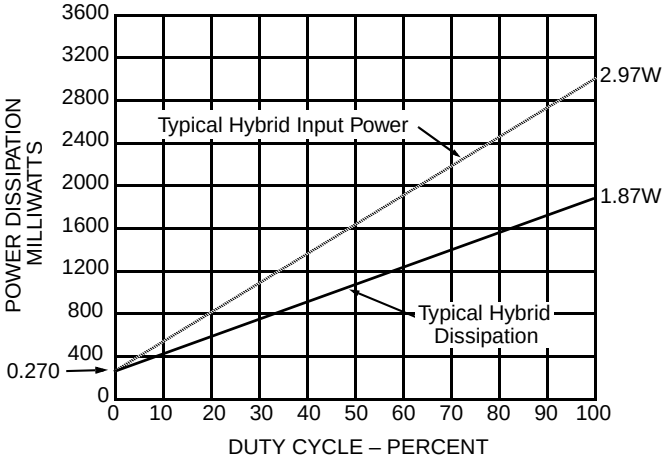
NOTES:

1. Power on or off, measured from 75KHz to 1MHz at Point A and transformer self impedance of 3KΩ minimum at 1MHz.
2. Power Supplies: ±15VDC ±0.75V & +5VDC ±0.5V, bypassed by by 10 µF (Tantalum recommended) Capacitor minimum. All measurements & specifications apply over the temperature range of -55°C to +125°C (case temperature) unless otherwise specified.
3. When measured as shown in Figure 5 with ±10Vp, line to ground, DC to 2MHz.
4. Typical power is measured with V_{bus} at Point A = 7.5 Vp-p.



*Offset measured at Point A in Figure 5

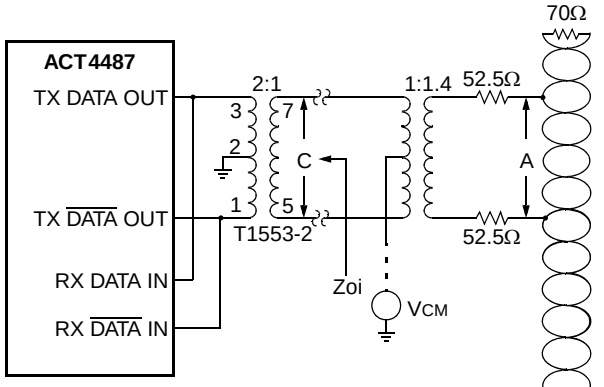
FIGURE 3 – TRANSMITTER (TX) OUTPUT OFFSET



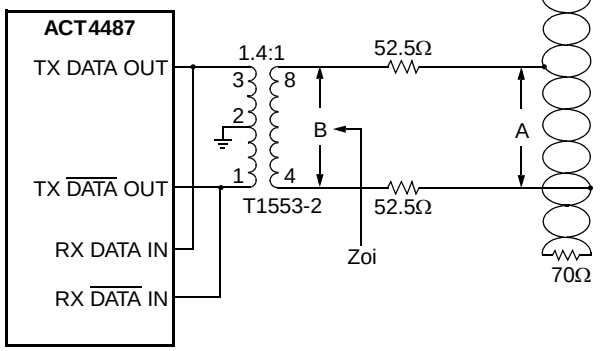
Note: Vcc= +15V, V_{EE} = -15V, V_L= +5V, Transformer ratio 1.4:1, V_{BUS} (Point A) at 7.5VP-P.

FIGURE 4 – POWER DISSIPATION VS. DUTY CYCLE

Transformer Coupled Stub



Direct Coupled Stub



Transformer Model use Technitrol Part# 1553-2 or equivalent

FIGURE 5 – TYPICAL 1553 BUS CONNECTIONS

PIN NUMBERS & FUNCTIONS

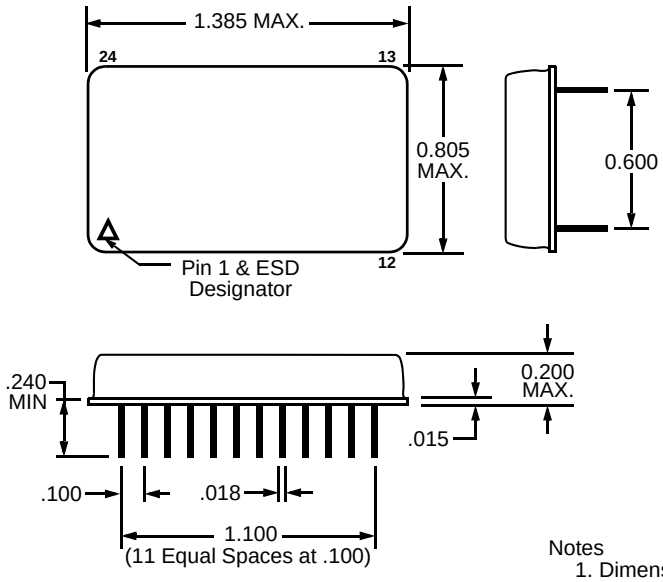
Pin #	Function
1	TX DATA OUT
2	TX $\overline{\text{DATA}}$ OUT
3	GROUND
4	NC
5	NC
6	NC
7	RX DATA OUT
8	STROBE
9	GROUND
10	RX $\overline{\text{DATA}}$ OUT
11	NC
12	NC
13	V_{CC}
14	NC
15	RX DATA IN
16	RX $\overline{\text{DATA}}$ IN
17	NC
18	CASE
19	V_{EE}
20	+5 V
21	TX INHIBIT
22	TX DATA IN
23	TX $\overline{\text{DATA}}$ IN
24	NC

CONFIGURATIONS AND ORDERING INFORMATION

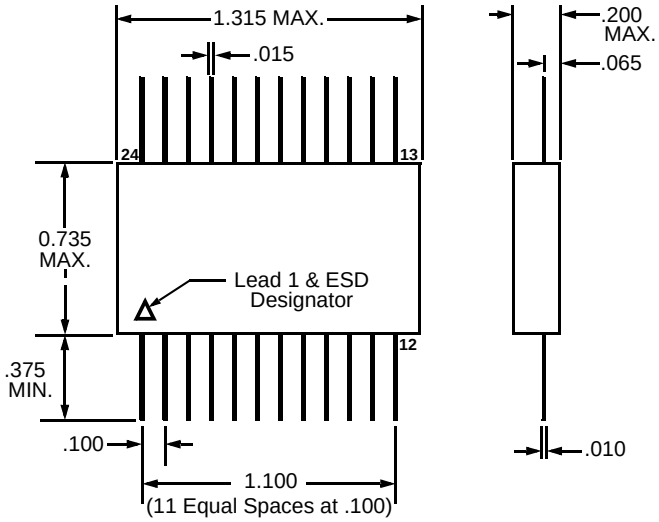
Model No.	Receiver Data level	Case	Configuration
ACT 4487	Normally Low	Plug In	Single
ACT 4487-I	Normally High		
ACT 4487-F	Normally Low	Flat Package	
ACT 4487-FI	Normally High		

PACKAGE CONFIGURATION OUTLINES

Plug In Package Outline



Flat Package Outline



Notes
1. Dimensions shown are in inches
2. Pins are equally spaced at 0.100±0.002 tolerance, non-cumulative, each row

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