ACT4524

40V/3.5A Buck Converter with Dual Output and Separated Over Current Protection

FEATURES

- 40V Input Voltage Surge
- 4.5V-36V operational Input Voltage
- Dual 5.1V Outputs with 1% Accuracy
- Up to 3.5A Output Current
- 2.65A Constant Current Regulation for VOUT1
- 1.2A Constant Current Regulation for VOUT2
- Hiccup Mode Protection at Output Short
- >90% Efficiency at Full Load
- <0.5mA Low Standby Input Current
- 5.7V Output Over Voltage Protection
- Cord Voltage Drop Compensation
- Meet EN55022 Class B Radiated EMI Standard
- SOP-8EP Package

APPLICATIONS

- Car Charger
- Cigarette Lighter Adaptor (CLA)
- Rechargeable Portable Devices
- CC/CV regulation DC/DC converter

GENERAL DESCRIPTION

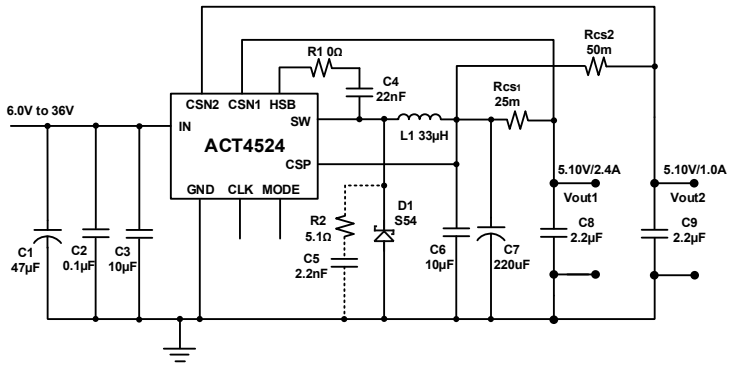
ACT4524 is a wide input voltage, high efficiency step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. ACT4524 has separated output current limits for dual ports CLA application. With the separated current limits, the CLA can meet Apple's MFI standard.

ACT4524 provides up to 3.5A output current at 125kHz switching frequency. ACT4524 utilizes adaptive drive technique to achieve good EMI performance while maintain 90% efficiency at full load for mini size CLA designs.

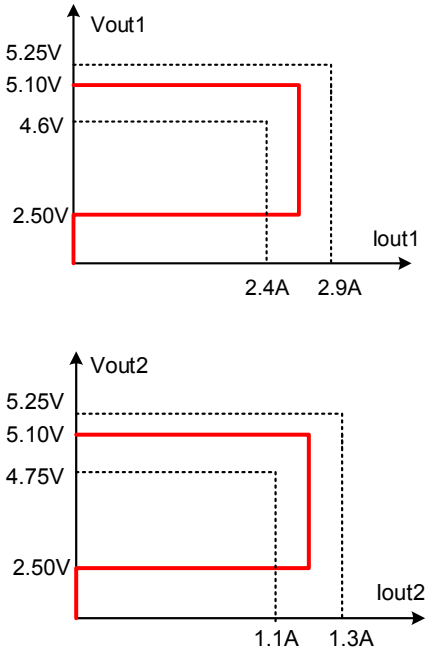
ACT4524 also has built in hiccup mode output short circuit protection. The average output current is reduced to below 6mA when output is shorted to ground. Other features include output over voltage protection and thermal shutdown.

ACT4524 is available in a SOP-8EP package and require very few external components for operation.

TYPICAL APPLICATION CIRCUIT



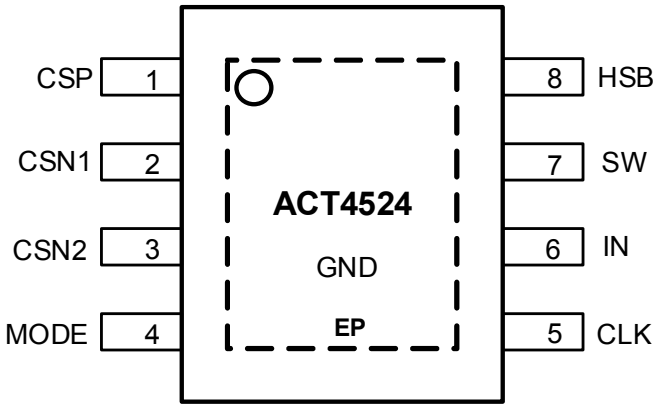
OUTPUT VI PROFILE



ORDERING INFORMATION

PART NUMBER	OPERATION AMBIENT TEMPERATURE RANGE	PACKAGE	PINS	PACKING
ACT4524YH-T	-40°C to 85°C	SOP-8EP	8	TAPE & REEL

PIN CONFIGURATION



SOP-8EP

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CSP	Voltage Feedback Input. The voltage at this pin is regulated to 5.10V. Connect this pin to the positive terminal of current sense resistor. CSP, CSN1 and CSN2 Kevin sense is recommended.
2	CSN1	Output current sense. Connect to the negative terminal of current sense resistor for VOUT1.
3	CSN2	Output current sense. Connect to the negative terminal of current sense resistor for VOUT2.
4	MODE	Mode pin with internal pull up current to determine device should operate in Native, Master, or Slave mode. If the pin is floated, the device operates in native mode; if the pin is grounded ,the device operates in Slave mode and receives CLK signal from another device; if the pin is connected to 82kOhm resistor, the device is configured in Master mode.
5	CLK	Synchronization of dual chips. Two chips operate synchronously out of phase with CLK pin connected.
6	IN	Power Supply Input. Bypass this pin with a 10μF ceramic capacitor to GND, placed as close to the IC as possible.
7	SW	Power switching output to external inductor.
8	HSB	High Side Bias pin. This pin provides power to the internal high-side MOSFET gate driver. Connect a 22nF capacitor from HSB pin to SW pin.
9	GND	Ground and heat dissipation pad. Connect this exposed pad to large ground copper area and other ground planes by thermal vias.

ABSOLUTE MAXIMUM RATING①

PARAMETER	VALUE	UNIT
IN to GND	-0.3 to 40	V
SW to GND	-1 to V_{IN} + 1	V
HSB to GND	V_{SW} - 0.3 to V_{SW} + 7	V
CSP, CS1, CS2, CLK, MODE to GND	-0.3 to + 6	V
Junction to Ambient Thermal Resistance	46	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Junction Temperature	-55 to 150	°C
Lead Temperature (Soldering 10 sec.)	300	°C

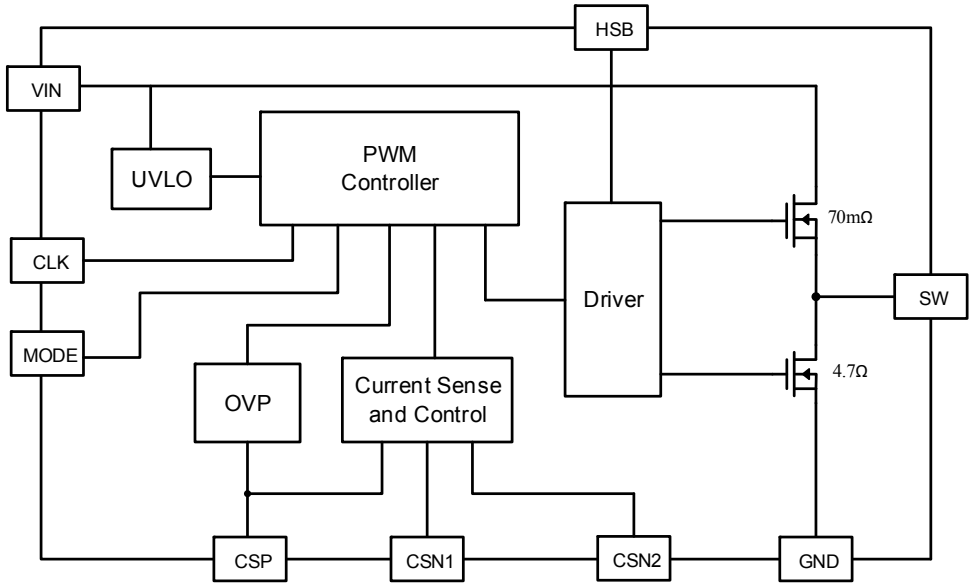
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERSTICS

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input over voltage protection	VIN_OVP	Rising	40	42	44	V
Input under voltage lockout (UVLO)	VIN	Rising	4.15	4.5	4.75	V
Input UVLO hysteresis	VIN			300		mV
Output voltage regulation	CSP		5.05	5.10	5.15	V
Output voltage cord compensation		R_{CS1}=25mΩ, Output current 2.4A at V_{OUT1}		100		mV
Cord Compensation Factor		K factor		1.667		
Output over voltage protection			5.5	5.7	6.0	V
Output over voltage deglitch time				500		ns
Output over voltage protection hysteresis				0.3		V
Output under voltage protection (UVP)	VOUT	VOUT falling	2.25	2.50	2.75	V
UVP hysteresis	VOUT	VOUT rising		0.2		V
UVP hiccup time				4		s
UVP blanking time at startup				3.5		ms
Output constant current limit	CS1	R_{CS}=25kΩ	2.50	2.65	2.80	A
	CS2	R_{CS}=50kΩ	1.1	1.2	1.3	A
Maximum duty cycle				99		%
Soft-start time				2.0		ms
Out voltage ripples		Cout=470uF/22uF ceramic		80		mV
Thermal shut down				160		°C
Thermal shut down hysteresis				30		°C
ESD on CSP, CSN1, CSN2		HBM		2.0		kV

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Output Current Sensing and Regulation

The conventional cycle-by-cycle peak current mode is implemented with high-side FET current sense.

Sense resistors are connected to the channel 1 and channel 2 outputs, respectively. The sensed differential voltage is compared with interval reference to regulate current. CC loop and CV loop are in parallel. The current loop response is allowed to have slower response compared to voltage loop. However, during current transient response, the inductor current overshoot/ undershoot should be controlled within +/-25% to avoid inductor saturation.

Input Over Voltage Protection

The converter is disabled if the input voltage is above 42V (+/-2V). Device resumes operation automatically 40ms after OVP is cleared.

Output Over Voltage Protection

Device stops switching when output over-voltage is sensed, and resumes operation automatically when output voltage drops to OVP- hysteresis.

Output Under-Voltage Protection / Hiccup Mode

There is a under voltage protection (UVP) threshold. If the UVP threshold is hit for 10us, an over current or short circuit is assumed, and the converter goes into hiccup mode by disabling the converter and restarts in 4 seconds and restarts.

Cord Compensation

In some applications, the output voltage is increased with output current to compensate the potential voltage drop across output cable. The compensation is based on the high side feedback resistance.

For ACT4524, the compensation voltage can be derived as:

$\Delta Vout = R_{CS} * I_O * K$

Where R_{CS} is the V_{OUT1} current resistance, I_O is the output current, and K is the cord compensation factor. This voltage difference could be added on the reference or turning the (V_{CSP}-V_{CSN}) voltage into a sink current at FB pin to pull Vout higher than programmed voltage.

The cord compensation loop should be very slow to avoid potential disturbance to the voltage loop. The voltage loop should be sufficiently stable on various cord compensation setting.

Thermal Shutdown

If the T_J increases beyond 160°C, ACT4524 goes into HZ mode and the timer is preserved until T_J drops by 30°C.

FUNCTIONAL DESCRIPTION

CLK Mode

There are three clock modes that depend on the mode pin configuration. During power up, device checks MODE pin condition (floating, 82k resistor to ground or grounded) to decide which mode (native, master or slave) device should operate in.

If only single ACT4524 is required, mode pin can be left float, and ACT4524 runs at native mode using internal oscillator clock.

For high load current application (>3.5A), it's possible to use two ACT4524 to operate in parallel with one device as master to provide clock for the other (slave). Two devices operate on the same frequency, but in opposite phase to optimize supply loading and EMI performance.

APPLICATIONS INFORMATION

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple which is determined by the inductance value.

Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}\, f_{SW}\, I_{LOADMAX}\, K_{RIPPLE}} \quad (1)$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}} \quad (2)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \quad (3)$$

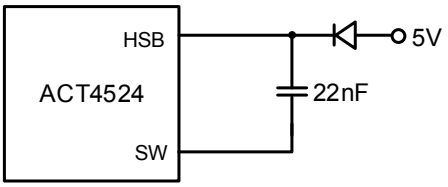
The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK} \quad (4)$$

L_{LIM} is the internal current limit.

External High Voltage Bias Diode

It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148 or BAT54.



Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10µF. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the VIN and GND pins of the IC, with the shortest traces as possible. In the case of tantalum or electrolytic types, they can be placed a little bit away of IC if a paralleled ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX}\, K_{RIPPLE}\, R_{ESR} + \frac{V_{IN}}{28 \times {f_{SW}}^2 L C_{OUT}} \quad (5)$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductance, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and only contributes a very small portion of the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor should be chosen to have sufficiently low ESR.

For ceramic type output capacitor, typically choose a capacitance of about 22µF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR. A 330µF or 470µF electrolytic capacitor is recommended.

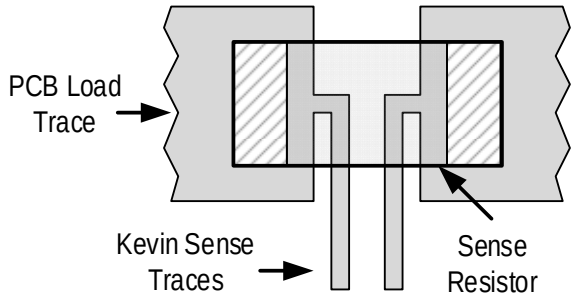
APPLICATIONS INFORMATION

Rectifier Diode

Use a low forward voltage drop (Vf<0.5V) Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

Current Sense Resistor

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors, trace resistance shared with the load can cause significant errors. It is recommended to connect the sense resistor pads directly to the CSP and CSN pins using “Kelvin” or “4-wire” connection techniques as shown below.

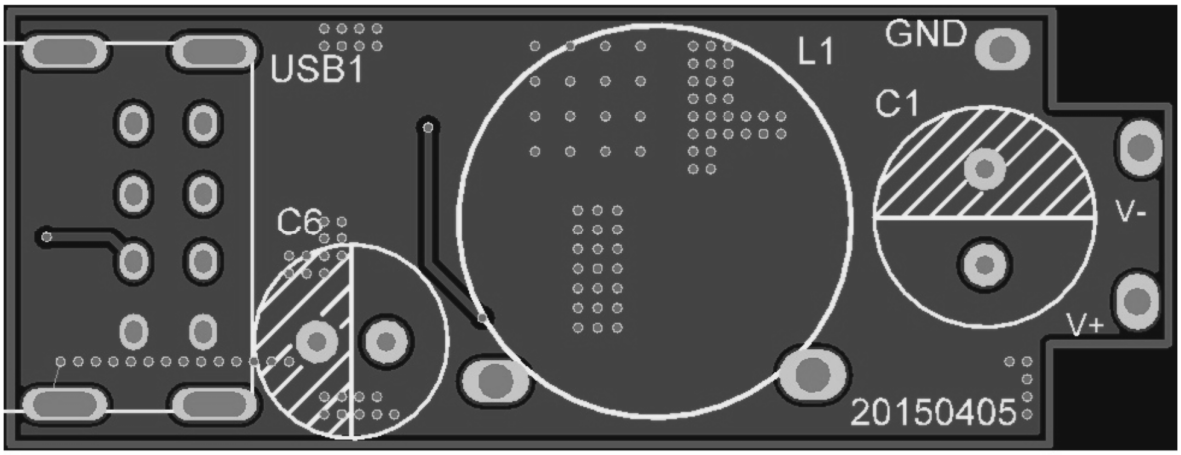


PCB Layout Guidance

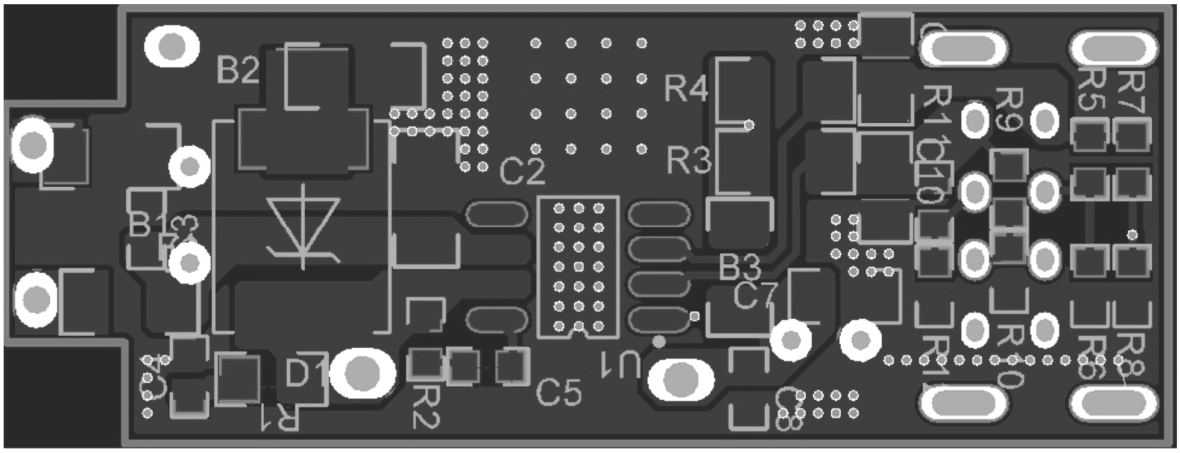
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1) Arrange the power components to reduce the AC loop size consisting of CIN, VIN pin, SW pin and the Schottky diode.
2) The high power loss components, e.g. the controller, Schottky diode, and the inductor should be placed carefully to make the thermal spread evenly on the board.
3) Place input decoupling ceramic capacitor CIN as close to VIN pin as possible. CIN should be connected to power GND with several vias or short and wide copper trace.
4) Schottky anode pad and IC exposed pad should be placed close to ground clips in CLA applications.
5) Use “Kelvin” or “4-wire” connection techniques from the sense resistor pads directly to the CSP and CSN1, CSN2 pins. The CSP, CSN1, and CSN2 traces should be in parallel to avoid interference.
6) Place multiple vias between top and bottom GND planes for best heat dissipation and noise immunity.
7) Use short traces connecting HSB-CHSB-SW loop.
8) SW pad is noise node switching from VIN to GND. It should be isolated away from the rest of circuit for good EMI and low noise operation.

Example PCB Layout

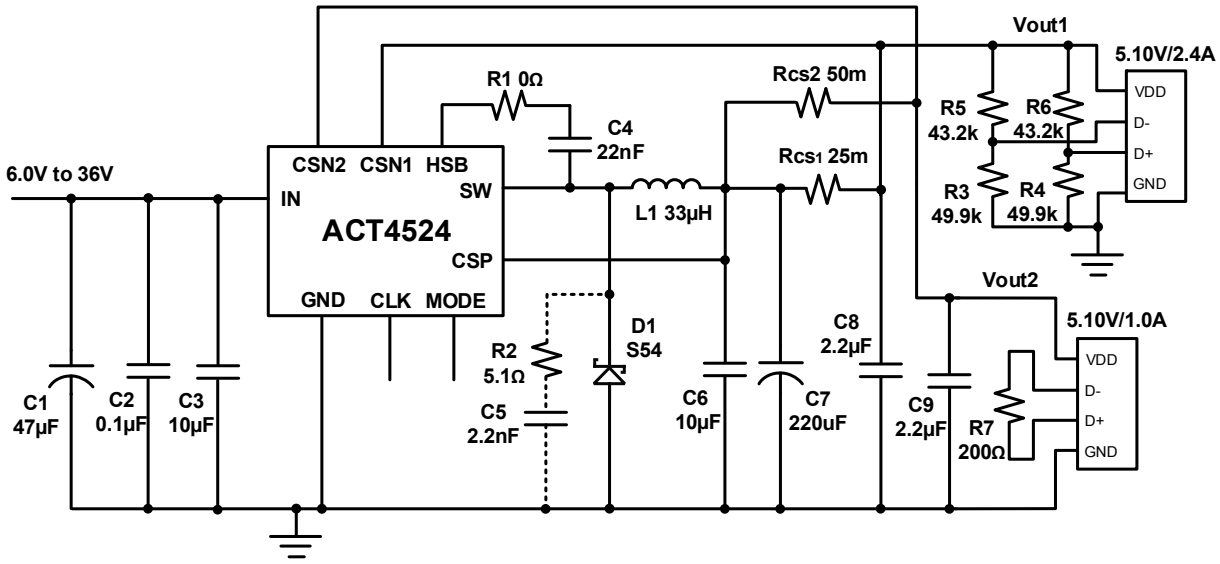


Top Layer



Bottom Layer

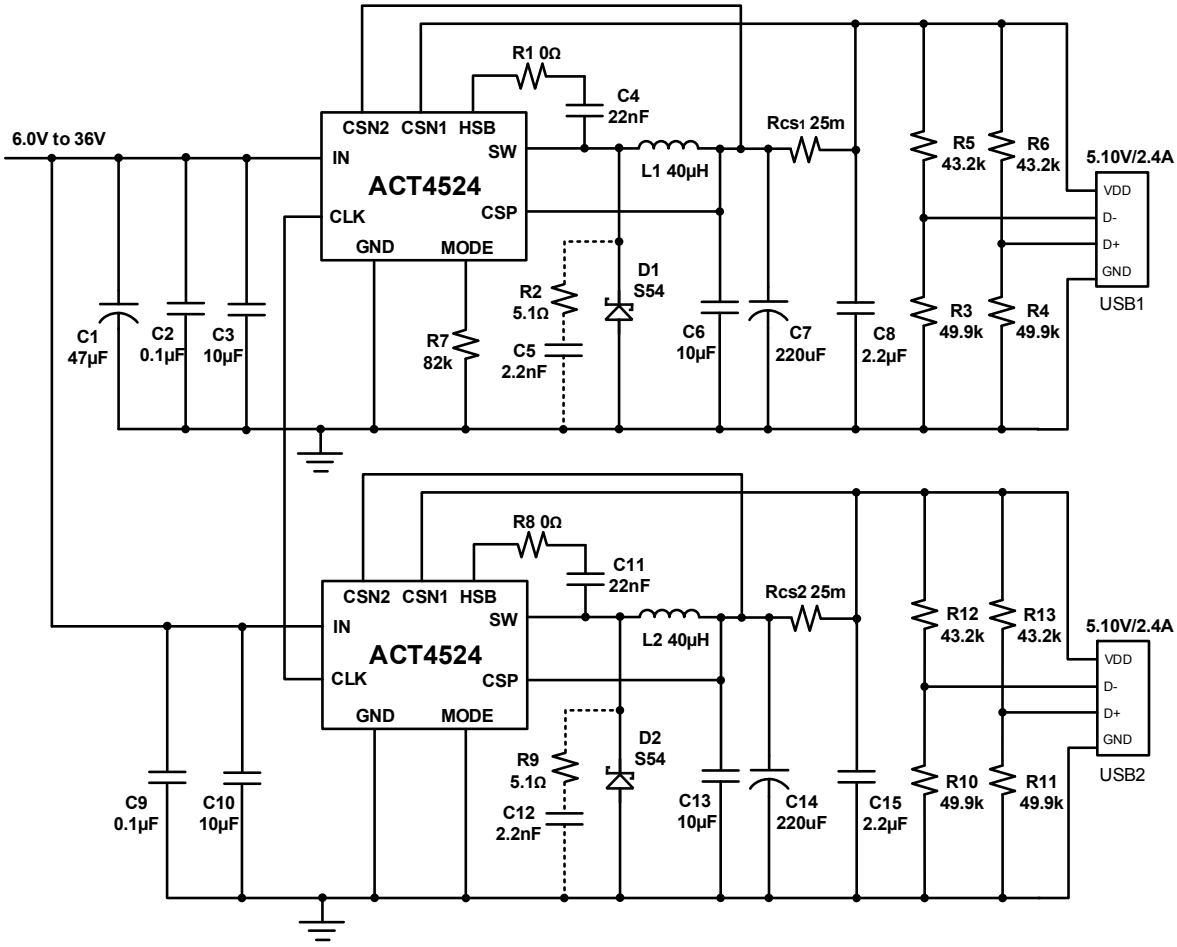
Figure 1:
Typical Application Circuit for 5V/3.4A Car Charger



BOM List for 5V/3.4A Car Charger

ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT4524TH-T, SOP-8EP	Qorvo	1
2	C1	Capacitor, Electrolytic, 47μF/35V, 6.3x7mm	Murata, TDK	1
3	C2	Capacitor, Ceramic, 0.1μF/35V, 0805, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 10μF/35V, 1206, SMD	Murata, TDK	1
5	C4	Capacitor, Ceramic, 22nF/25V, 0603, SMD	Murata, TDK	1
6	C5	Capacitor, Ceramic, 2.2nF/10V, 0603, SMD, optional	Murata, TDK	1
7	C6	Capacitor, Ceramic, 10uF/10V, 1206, SMD	Murata, TDK	1
8	C7	Capacitor, Electrolytic, 220uF/10V, 6.3x7mm	Murata, TDK	1
9	C8, C9	Capacitor, Ceramic, 2.2μF/10V, 0805, SMD	Murata, TDK	2
10	L1	Inductor, 33μH, 6.0A, 20%, DCR=15mΩ	Murata, TDK	1
11	D1	Diode, Schottky, 40V/5A, S54	Vishay	1
12	R1	Chip Resistor, 0Ω, 1/10W, 5%, 0603	Murata, TDK	1
13	R2	Chip Resistor, 5.1Ω, 1/8W, 5%, 0805, optional	Murata, TDK	1
14	Rcs1	Chip Resistor, 25mΩ, 1/4W, 1%, 1206	Murata, TDK	1
15	Rcs2	Chip Resistor, 50mΩ, 1/4W, 1%, 1206	Murata, TDK	1
16	R3, R4	Chip Resistor, 49.9kΩ, 1/10W, 5%, 0603	Murata, TDK	2
17	R5, R6	Chip Resistor, 43.2kΩ, 1/10W, 5%, 0603	Murata, TDK	2
18	R7	Chip Resistor, 200Ω, 1/10W, 5%, 0603	Murata, TDK	1
19	USB	USB Rev A		2

Figure 2:
Typical Application Circuit for 5V/4.8A（2*ACT4524）Car Charger



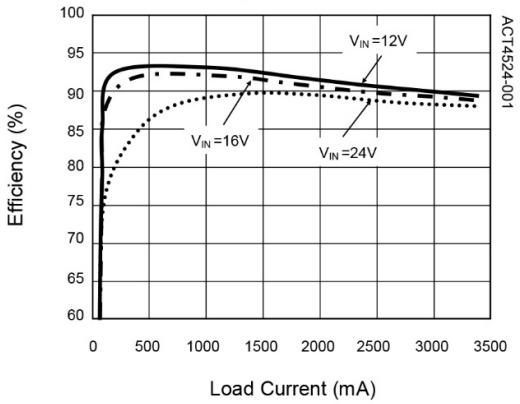
BOM List for 5V/4.8A Car Charger

ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1,U2	IC, ACT4524YH-T, SOP-8EP	Qorvo	1
2	L1,L2	Inductor, 40μH, 6.0A, 20%, DCR=15mΩ	Murata, TDK	1
3	D1,D2	Diode, Schottky, 40V/5A, S54	Vishay	1
4	C1	Capacitor, Electrolytic, 47uF/35V, 6.3x7mm	Murata, TDK	1
5	C2,C9	Capacitor, Ceramic, 0.1μF/35V, 0805, SMD	Murata, TDK	1
6	C3,C10	Capacitor, Ceramic, 10μF/35V, 1206, SMD	Murata, TDK	1
7	C4,C11	Capacitor, Ceramic, 22nF/25V, 0603, SMD	Murata, TDK	1
8	C5,C12	Capacitor, Ceramic, 2.2nF/10V, 0603, SMD, optional	Murata, TDK	1
9	C6,C13	Capacitor, Ceramic, 10uF/10V, 1206, SMD	Murata, TDK	2
10	C7,C14	Capacitor, Electrolytic, 220uF/10V, 6.3x7mm	Murata, TDK	1
11	C8,C15	Capacitor, Ceramic, 2.2μF/10V, 0805, SMD	Murata, TDK	1
12	R1,R8	Chip Resistor, 0Ω, 1/10W, 5%, 0603	Murata, TDK	1
13	R2,R9	Chip Resistor, 5.1Ω, 1/8W, 5%, 0805, optional	Murata, TDK	1
14	Rcs1,Rcs2	Chip Resistor, 25mΩ, 1/4W, 1%, 1206	Murata, TDK	1
15	R3,R4,R10,R11	Chip Resistor, 49.9kΩ, 1/10W, 5%, 0603	Murata, TDK	1
16	R5,R6,R12,R13	Chip Resistor, 43.2kΩ, 1/10W, 5%, 0603	Murata, TDK	2
17	R7	Chip Resistor, 82kΩ, 1/10W, 5%, 0603	Murata, TDK	2
18	USB	USB Rev A		1

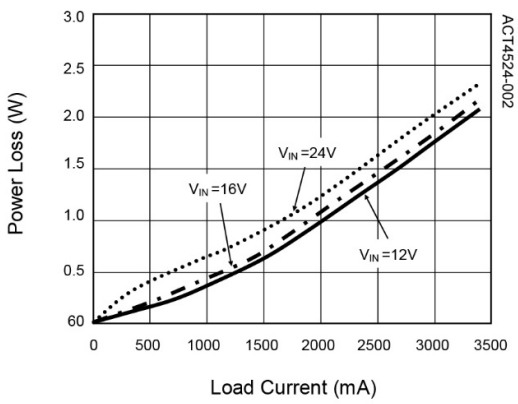
TYPICAL PERFORMANCE CHARACTERISTICS

(Schematic as show in Figure 1, Ta = 25°C, unless otherwise specified)

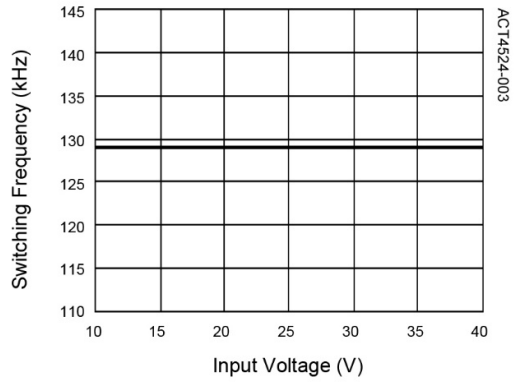
Efficiency vs. Load current



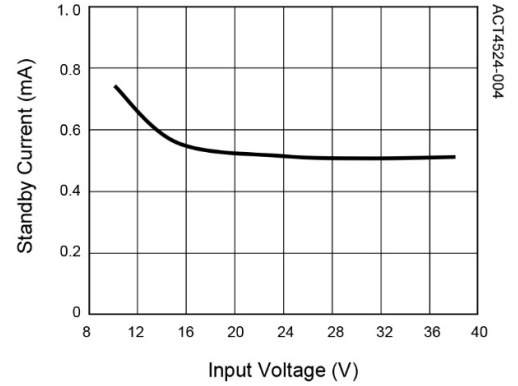
Power Loss vs. Load current



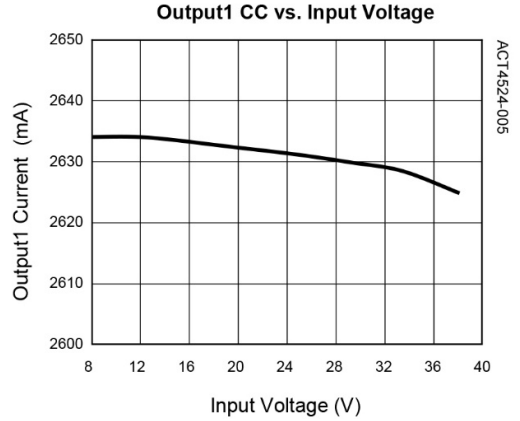
Switching Frequency vs. Input Voltage



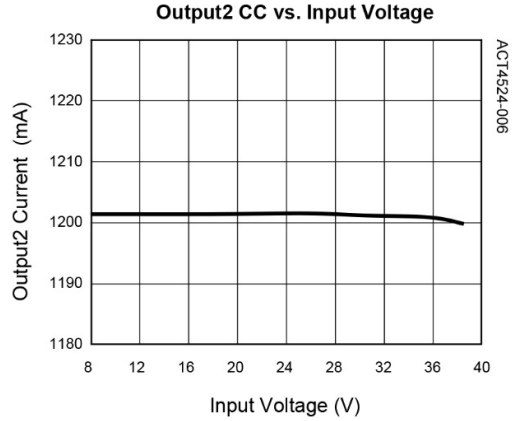
Standby Current vs. Input Voltage



Output1 CC vs. Input Voltage



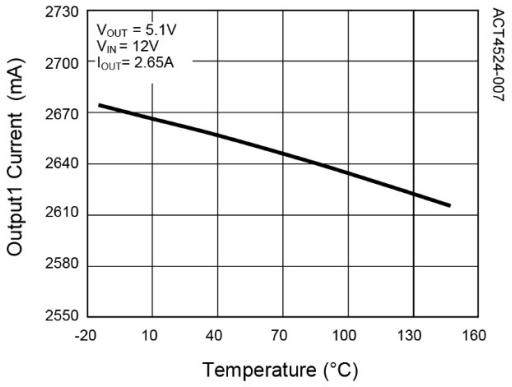
Output2 CC vs. Input Voltage



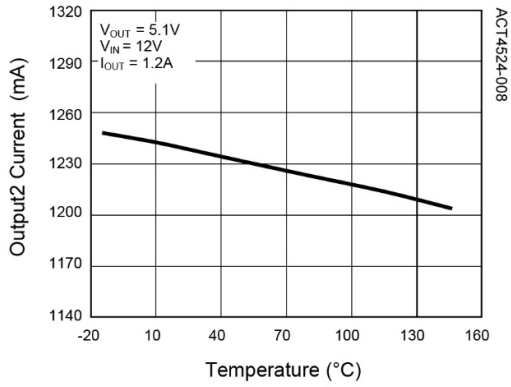
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(Schematic as show in Figure 1, Ta = 25°C, unless otherwise specified)

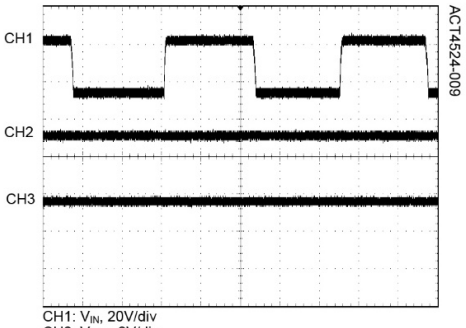
Output1 Current vs. Temperature



Output2 Current vs. Temperature

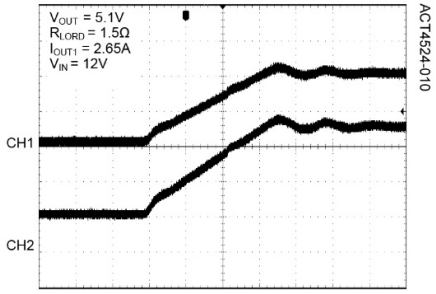


Input Surge Test



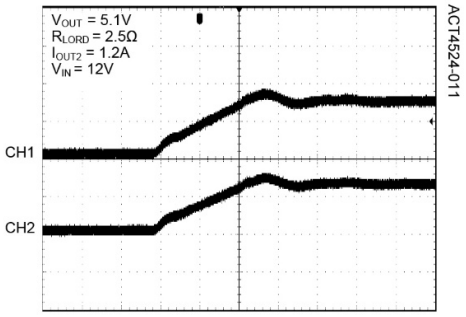
CH1: V_{IN}, 20V/div
CH2: V_{OUT}, 2V/div
CH3: I_{OUT}, 2A/div
TIME: 100ms/div

Start up into CC Mode



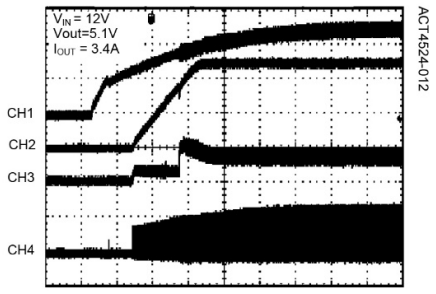
CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 1A/div
TIME: 400μs/div

Start up into CC Mode



CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 1A/div
TIME: 400μs/div

Start up with CC load

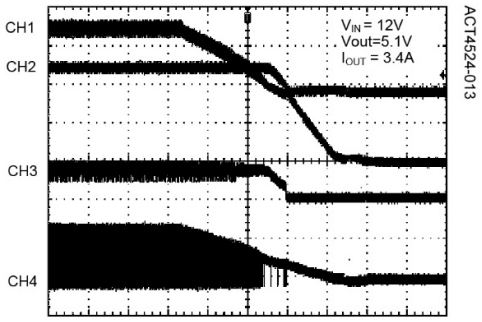


CH1: V_{IN}, 5V/div
CH2: V_{OUT}, 2V/div
CH3: I_L, 5A/div
CH4: SW, 10V/div
TIME: 1ms//div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

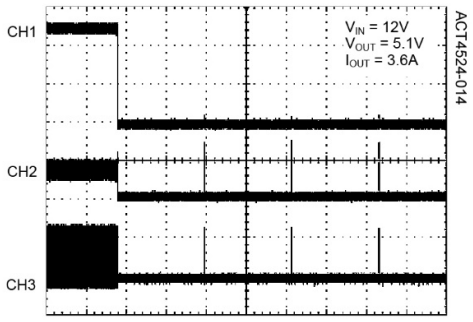
(Schematic as show in Figure 1, Ta = 25°C, unless otherwise specified)

Power Off from CC load



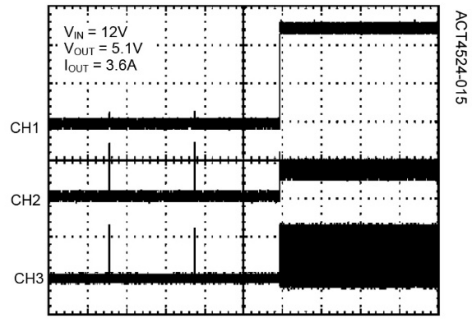
CH1: V_{IN}, 5V/div
CH2: V_{OUT}, 2V/div
CH3: I_L, 5A/div
CH4: SW, 10V/div
TIME: 1ms//div

Output Short Test



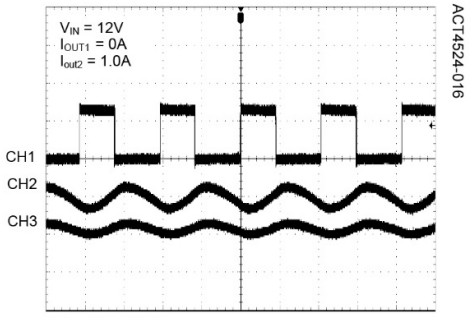
CH1: V_{OUT}, 2V/div
CH2: I_L, 5A/div
CH3: SW, 10V/div
TIME: 2s//div

Output Short Recovery



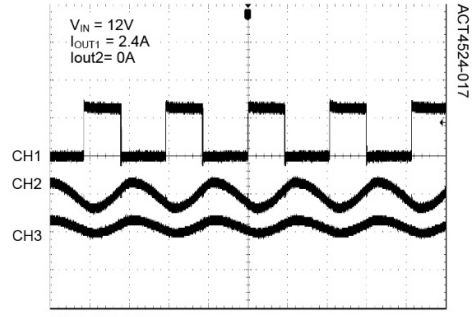
CH1: V_{OUT}, 2V/div
CH2: I_L, 5A/div
CH3: SW, 10V/div
TIME: 2s//div

SW vs. Output Voltage Ripples



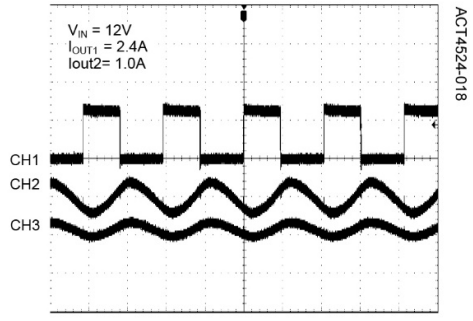
CH1: SW, 10V/div
CH2: V_{OUT1} Ripple, 50mV/div
CH3: V_{OUT2} Ripple, 50mV/div
TIME: 4μs/div

SW vs. Output Voltage Ripples



CH1: SW, 10V/div
CH2: V_{OUT1} Ripple, 50mV/div
CH3: V_{OUT2} Ripple, 50mV/div
TIME: 4μs/div

SW vs. Output Voltage Ripples

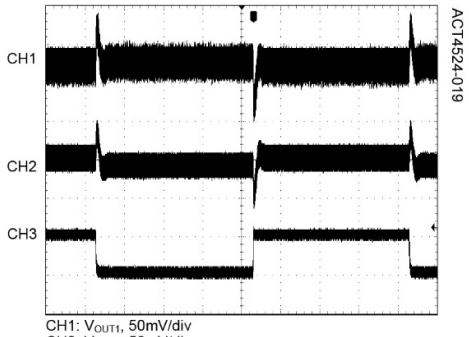


CH1: SW, 10V/div
CH2: V_{OUT1} Ripple, 50mV/div
CH3: V_{OUT2} Ripple, 50mV/div
TIME: 4μs/div

TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(Schematic as show in Figure 1, Ta = 25°C, unless otherwise specified)

Load Transient (0mA-500mA-0mA)

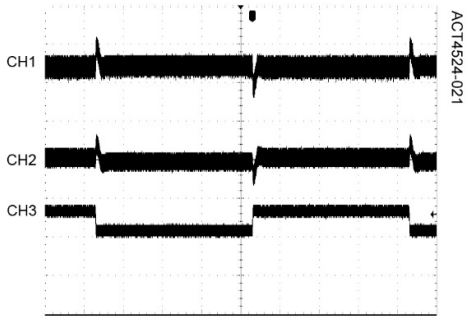


CH1: V_{OUT1}, 50mV/div
CH2: V_{OUT2}, 50mV/div
CH3: I_{OUT1}, 500mA/div
TIME: 1ms//div

Load Transient (500mA-1A-500mA)

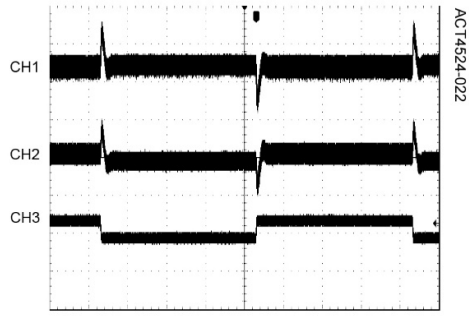
CH1: V_{OUT1}, 50mV/div
CH2: V_{OUT2}, 50mV/div
CH3: I_{OUT1}, 500mA/div
TIME: 1ms//div

Load Transient (1A-1.5A-1A)



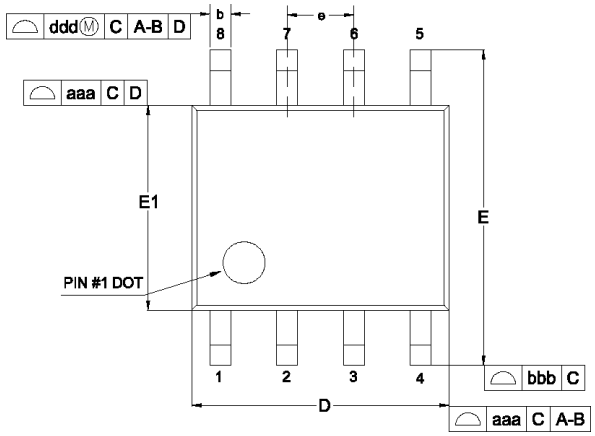
CH1: V_{OUT1}, 100mV/div
CH2: V_{OUT2}, 100mV/div
CH3: I_{OUT1}, 1A/div
TIME: 1ms//div

Load Transient (1.5A-2.4A-1.5A)

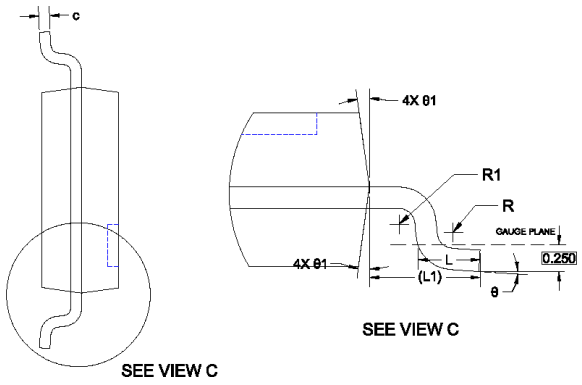


CH1: V_{OUT1}, 100mV/div
CH2: V_{OUT2}, 100mV/div
CH3: I_{OUT1}, 2A/div
TIME: 1ms//div

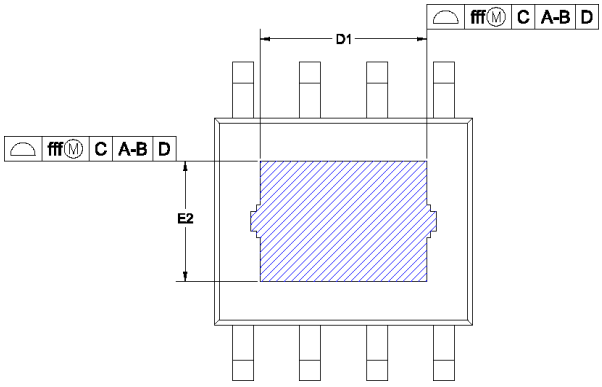
PACKAGE OUTLINE AND DIMENSIONS



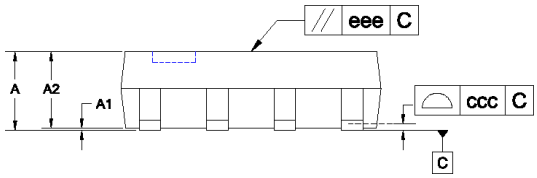
Top View



Side View



Bottom View



Side View

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	1.300	--	1.700
A1	0.000	--	0.100
A2	1.350	--	1.550
b	0.330	--	0.510
c	0.170	--	0.250
D	4.900BSC		
E	6.000BSC		
E1	3.900BSC		
D1	3.150BSC		
E2	2.260BSC		
e	1.270 BSC		
L	0.400	--	1.270
L1	1.050REF.		
R	0.070	--	--
R1	0.070	--	--
θ	0°	--	8°
θ1	5°	--	15°
Tol. of Form&Position			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		
fff	0.15		

Notes

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5-2009.
2. All DIMENSIONS ARE IN MILLIMETERS.
3. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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