ACT4530M

40 V/3.0 A CV/CC Buck Converter Featuring QC2.0, USB Auto-Detect and USB-PD

FEATURES

- AEC-Q100 Automotive Qualified
- -40 °C ~ 125 °C Junction Temperature Range
- 12 V Input Optimized (Automotive Applications)
- QC2.0 Decoding + USB Auto-Detect + USB-PD Type-C Support
- Apple MFi and 2.4 A compatible
- Samsung and BC1.2 compatible
- 40 V Input Voltage Surge
- 4.5 V - 36 V Operational Input Voltage
- 5.1 V/9.1 V Output with +/-1% Accuracy
- Up to 3.0 A Output current
- Constant Current Regulation Limit
- Hiccup Mode Protection at Output Short
- >90% Efficiency at Full Load
- 0.5 mA Low Standby Input Current
- 5.7 V/10.1 V Output Over-voltage Protection for 5.1 V/9.1 V Outputs
- Cord Voltage Compensation
- Meet EN55022 Class B Radiated EMI Standard
- 8 kV ESD HBM Protection on DP and DM
- SOP-8EP Package

APPLICATIONS

- Car Charger
- Cigarette Lighter Adaptor (CLA)
- Rechargeable Portable Device
- CV/CC regulation DC/DC converter

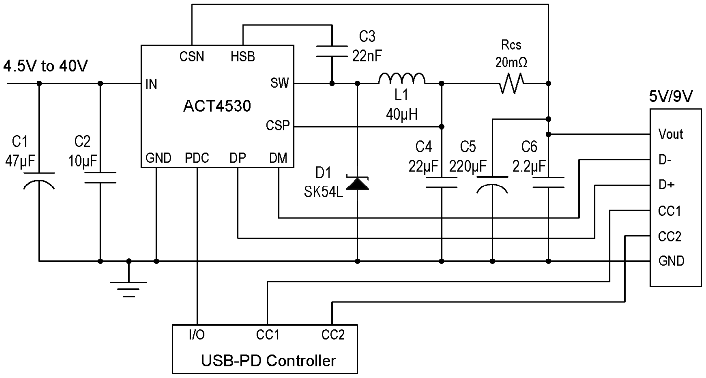
GENERAL DESCRIPTION

ACT4530M is a wide input voltage, high efficiency step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. It is an improvement over the ACT4529 with its QC2.0 compatibility in 12 V automotive applications. The ACT4530M eliminates the issue with QC2.0 buck converters that try to operate with V_{IN} = 12 V to Vout = 12 V. In addition to QC2.0, it also supports Apple, Samsung and BC1.2 protocols. ACT4530M also has an optional input pin, PDC, that accepts a tri-state input for USB-PD control. The ACT4530M also filters out non-QC2.0 compatible communication pulses generated by some phones' communication protocols.

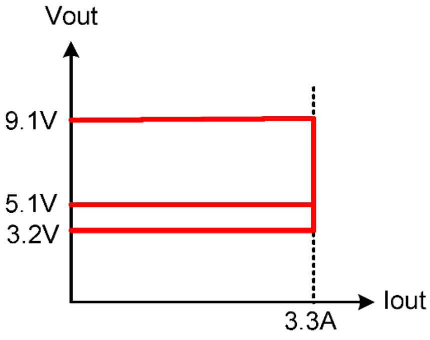
ACT4530M has accurate output current limits under constant current regulation to meet MFi specification. It provides up to 3.0 A output current at 125 kHz switching frequency. ACT4530M utilizes adaptive drive technique to achieve good EMI performance while main >90% efficiency at full load for mini size CLA designs. It also has output short circuit protection with hiccup mode. The average output current is reduced to below 6 mA when output is shorted to ground. Other features include output over voltage protection and thermal shutdown.

This device is available in a SOP-8EP package and require very few external components for operation.

Typical Application Circuit



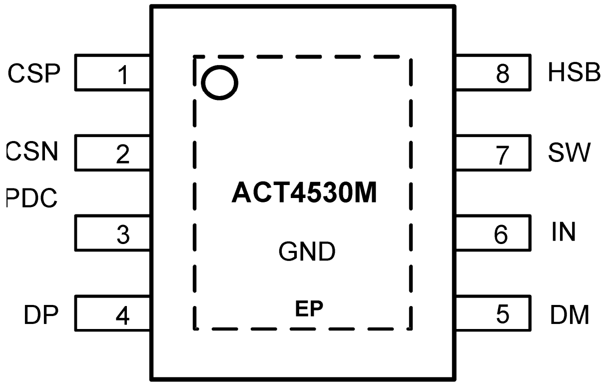
V/I Profile



ORDERING INFORMATION

PART NUMBER	PDC	USB AUTO DETECT	QC2.0	CERTIFICATION	PACKAGE
ACT4530MYH-T0010	Yes	No	Yes	N/A	SOP-8EP

PIN CONFIGURATION



SOP-8EP

Top View

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CSP	Voltage Feedback Input. Connect to node of the inductor and output capacitor. CSP and CSN Kevin sense is recommended.
2	CSN	Negative input terminal of output current sense. Connect to the negative terminal of current sense resistor.
3	PDC	USB-PD Control Pin. When PDC is floating, V_{OUT} = 5.1 V. When PDC is pulled low, V_{OUT} = 9.1 V. When PDC is pulled high, the IC ignores the PDC pin and the output voltage does not change from the previous setting.
4	DP	Data Line Positive Input. Connected to D+ of attached portable device data line. This pin passes 8 kV HBM ESD.
5	DM	Data Line Negative Input. Connected to D- of attached portable device data line. This pin passes 8 kV HBM ESD.
6	IN	Power Supply Input. Bypass this pin with a 10 µF ceramic capacitor to GND, placed as close to the IC as possible.
7	SW	Power Switching Output to External Inductor.
8	HSB	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22 nF capacitor from HSB pin to SW pin.
9	GND	Ground and Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
IN to GND	-0.3 to 40	V
SW to GND	-1 to V_{IN} +1	V
HSB to GND	V_{SW} - 0.3 to V_{SW} + 7	V
CSP, CSN to GND	-0.3 to +15	V
PDC to GND	-0.3 to +6	V
All other pins to GND	-0.3 to +6	V
Junction to Ambient Thermal Resistance	46	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Junction Temperature	-55 to 150	°C
Lead Temperature (Soldering 10 sec.)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, T_J = -40 °C ~ 125 °C, unless otherwise specified.)

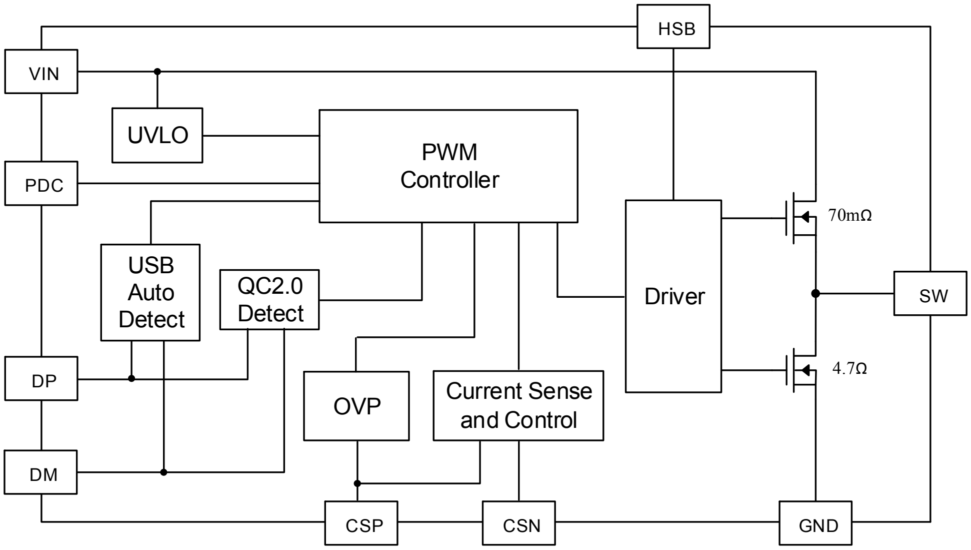
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Over Voltage Protection	V_{IN}_OVP	Rising	40	42	44	V
Input Over Voltage Hysteresis				4		V
Input Over Voltage Response Time	T_V_{IN}_OVP	V_{IN} step from 30 V to 45 V		250		ns
Input Under Voltage Lockout (UVLO)	V_{IN}	Rising		4.5		V
Input UVLO Hysteresis				200		mV
Input Voltage Power Good Deglitch Time		No OVP		40		ms
Input Voltage Power Good Deglitch Time		No UVP		10		us
Input Standby Current		V_{IN} = 12 V, V_{OUT} = 5.1 V, I_{LOAD} = 0		500		uA
Output Voltage Regulation	CSP	5.1 V setting 9.1 V setting	5.05 9.0	5.1 9.1	5.15 9.2	V
Output Over Voltage Protection (OVP)		Output rising, 5.1 V setting Output rising, 9.1 V setting		5.7 10.1		V
Output Over Voltage Deglitch Time				1.0		us
Output Voltage Cord Compensation		ACT4530MYH-T0010 - 66 mV between CSP and CSN	-15%	200	+15%	mV
Output Under Voltage Protection (UVP)	V_{OUT}	V_{OUT} falling	-10%	3.2	10%	V
UVP Hysteresis	V_{OUT}	V_{OUT} falling		0.2		V
UVP Deglitch Time	V_{OUT}			10		us
UVP Blanking Time at Startup				3.5		ms

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, T_J = -40 °C ~ 125 °C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Constant Current Limit		Rcs = 20 mΩ	3.1	3.3	3.5	A
Hiccup Waiting Time				4.13		S
Top FET Cycle by Cycle Current Limit			4.5	5.8		A
Top FET Rds on				70		mΩ
Bot FET Rds on				4.7		Ω
Maximum Duty Cycle			99			%
Switching Frequency			-10%	125	+10%	kHz
Soft-start Time				2.0		ms
Out Voltage Ripples		C_{OUT} = 220 uF/22 uF ceramic		80		mV
V_{OUT} Discharge Current		For high to lower voltage transition		60		mA
Voltage transition time for QC 2.0 transition or USB PD Type C		9 V - 5 V			100	ms
Voltage transition time for QC 2.0 transition or USB PD Type C		5 V - 9 V			100	ms
Line Transient Response		Input 12 V - 40 V - 12 V with 1 V/us slew rate, V_{OUT} = 5 V, I_{LOAD} = 0 A and 2.4 A	4.75		5.25	V
Load Transient Response		80 mA - 1.0 A - 80 mA load with 0.1 A/us slew rate	4.9	5.15	5.4	V
		80 mA - 1.0 A - 80 mA load with 0.1 A/us slew rate	8.7	9.1	9.5	V
Thermal Shut Down				160		°C
Thermal Shut Down Hysteresis				30		°C
ESD of DP, DM		HBM		8		kV
PDC Floating				1.5		V
PDC High			2.0			V
PDC Low					0.8	V
PDC Maximum Voltage					5.5	V
PDC Drive Current				10		uA

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The ACT4530M is wide input range (40 V) buck converter that is optimized for CLA (cigarette lighter adapter) car charger applications. It operates at 125 kHz for automotive EMI compatibility. It supports all major communication protocols including Q2.0, USB PD, Apple, Samsung, and BC1.2. It requires very few external components, resulting in small solution sizes.

Improved QC2.0 Functionality (DP and DM communication)

The ACT4530M implements an improved QC2.0 functionality. It overcomes the typical issues seen with 12 V automotive QC2.0 applications that request a 12 V output. A typical buck converter cannot deliver a 12 V output voltage from a 12 V input voltage. The typical buck converter goes to maximum duty cycle and is unable to accurately regulate the output voltage or current. The ACT4530M resolves this issue by accepting all QC2.0 voltage requests, but it only responds to 5 V and 9 V requests. Any 12 V request is ignored, and the output voltage does not change.

PDC Pin

The PDC pin is an optional input that allows external controllers to program the ACT4530M output voltage. This pin is typically used in USB PD applications. Opening PDC (floating input) programs Vout to 5.1 V. Pulling PDC low programs Vout to 9.1 V. Pulling PDC high does not change the previously programmed output voltage. Starting the IC with PDC already pulled high results in Vout starting at 5 V.

Output Current Sensing and Regulation

The output current sense resistor is connected between CSP and CSN. The sensed differential voltage is compared with an internal reference voltage to regulate the maximum output current. CC loop and CV loop are in parallel. The current loop response has a slower response compared to voltage loop. During load current transients, the inductor current can be up to +/-25% higher than steady state condition. The customer should confirm that the inductor does not saturate during these peak conditions.

Cycle-by-Cycle Current Control

The conventional cycle-by-cycle peak current mode is implemented with high-side FET current sense.

Input Over Voltage Protection

The converter is disabled if the input voltage is above 42 V (+/-2 V). Device resumes operation automatically 40 ms after OVP is cleared.

Output Over Voltage Protection

Device stops switching when output over-voltage is sensed, and resumes operation automatically when output voltage drops to OVP- hysteresis.

FUNCTIONAL DESCRIPTION

Output Over Voltage Discharge

Discharge circuit starts to discharge output through CSP pins when output over voltage is detected. Discharge circuit brings 9 V down to 5 V in less than 100 ms.

Output Under-Voltage Protection / Hiccup Mode

The ACT4530M implements an under voltage protection (UVP) threshold to protect against fault conditions. If the output voltage is below UVP threshold for more than 10 us, an over current or short circuit is assumed, and the converter goes into hiccup mode by disabling the converter and restarting after hiccup waiting period of 4.3s .

Thermal Shutdown

If the junction temperature, T_J, increases beyond 160 °C, the ACT4530 shuts down until T_J drops below 130 °C.

Cord Compensation

The ACT4530M implements cord compensation to account for voltage drops due to output cable resistance. It accomplishes this by increasing the output voltage with increasing output current. The increased output voltage is measured at the CSP pin.

The cord compensation voltage is derived as:

$\Delta V_{OUT} = (V_{CSP}-V_{CSN})*K$

Where K = 3.03

The cord compensation loop is very slow to avoid disturbing to the voltage loop when there are load transients.

APPLICATIONS INFORMATION

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value.

Higher inductance reduces the peak-to-peak ripple current. The trade-off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}\, f_{SW}\, I_{LOADMAX}\, K_{RIPPLE}} \qquad (1)$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}} \qquad (2)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \qquad (3)$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK} \qquad (4)$$

L_{LIM} is the internal current limit.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large currents flow in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10 µF. The best choice is a ceramic capacitor. However, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. Active Semi recommends using a ceramic capacitor in parallel with a tantalum or electrolytic. This combination provides the EMI and noise performance. The input capacitor must be placed close to the IN and GND pins of the IC, with the shortest traces possible. If using a tantalum or electrolytic capacitor in parallel with ceramic capacitor, the ceramic capacitor must be placed closer to the IC.

Output Capacitor

The ACT4530 output capacitance must be split between the left and right side of the output current sense resistor. The left side of the current sense resistor (CSP pin) requires a 22 uF ceramic capacitor. The right side of the current sense resistor should contain enough capacitance to keep the output voltage ripple below the required level.

$$V_{RIPPLE} = I_{LPK-PK} \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \qquad (5)$$

This output capacitance should have low ESR to keep low output voltage ripple. The output ripple voltage is:

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. From the equation above, V_{RIPPLE} is the combination of ESR and real capacitance.

In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR}. In this case, the output capacitor must be chosen to have sufficiently low ESR.

For ceramic output capacitors, typically choose a capacitance of about 22 µF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50 mΩ ESR. If an 330 uF or 470 uF electrolytic cap or tantalum cap is used and the output voltage ripple is dominated by ESR, add a 2.2 uF ceramic in parallel with the tantalum or electrolytic.

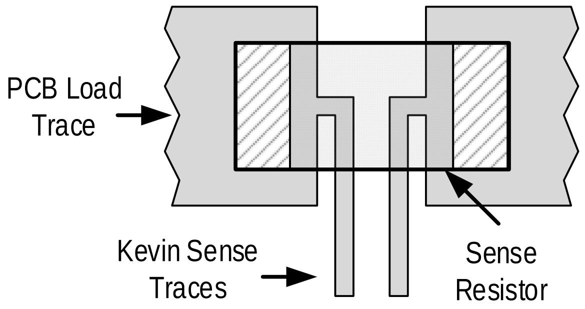
Rectifier Schottky Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage. Furthermore, the low forward voltage Schottky is preferable for high efficiency and smoothly operation.

APPLICATIONS INFORMATION

Current Sense Resistor

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors, trace resistance shared with the load can cause significant errors. It is recommended to connect the sense resistor pads directly to the CSP and CSN pins using “Kelvin” or “4-wire” connection techniques as shown below.



Current Limit Setting

If output current hits current limit, output voltage drops to keep the current to a constant value.

The following equation calculates the constant current limit.

$$ILimit\ (A) = \frac{66\ mV}{Rcs\ (m\Omega)} \quad (6)$$

Where Rcs is current sense resistor.

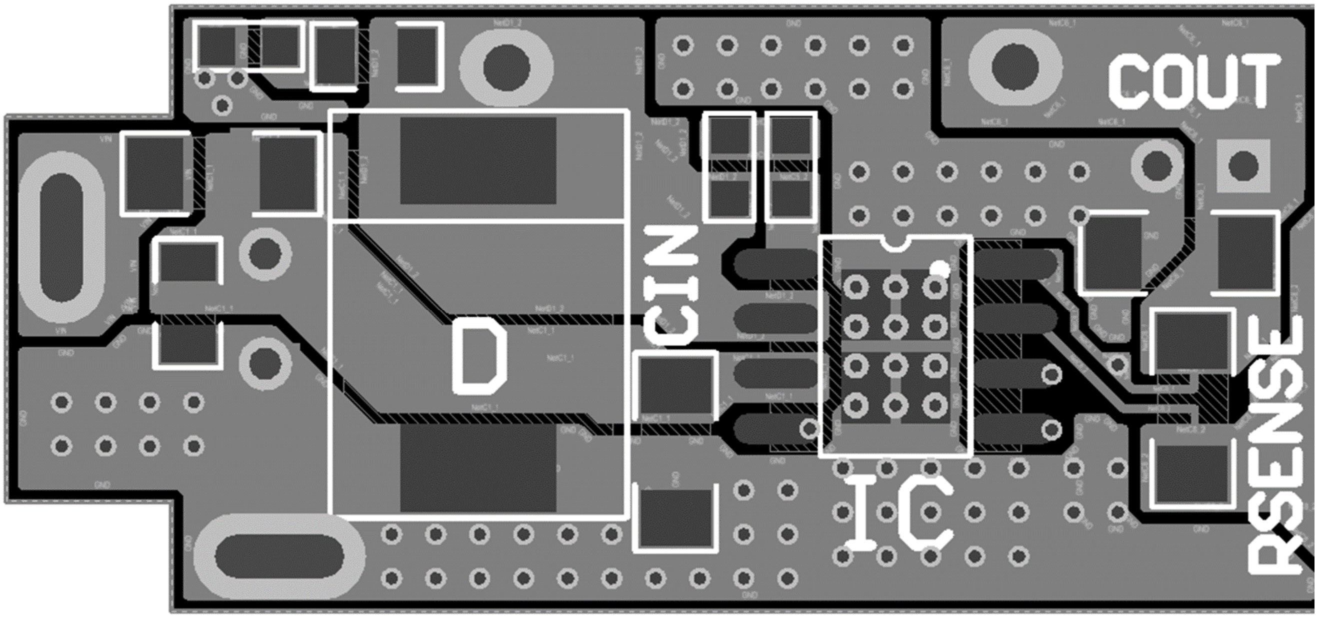
APPLICATIONS INFORMATION

PCB Layout Guidance

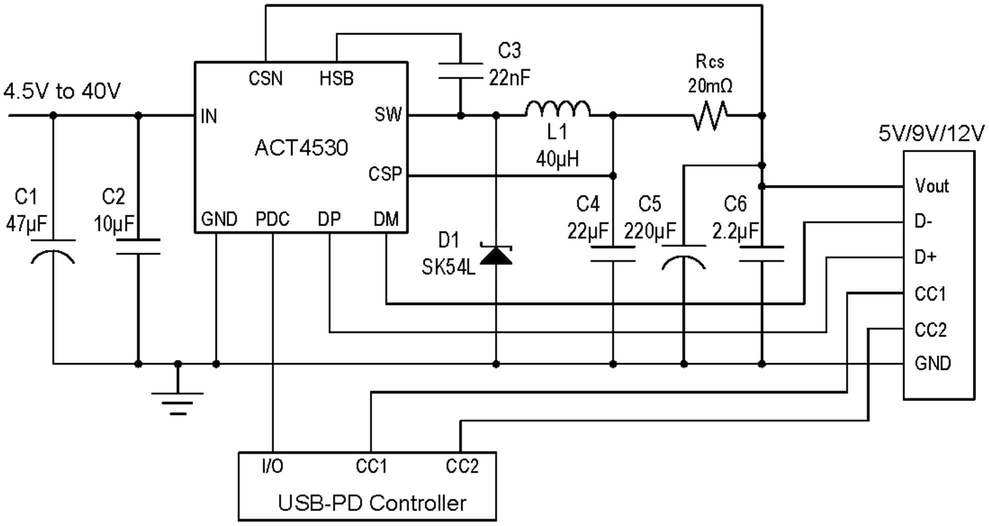
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1. Arrange the power components to reduce the AC loop size consisting of C_{IN}, V_{IN} pin, SW pin and the Schottky diode.
2. The high power loss components, e.g. the controller, Schottky diode, and the inductor should be placed carefully to make the thermal spread evenly on the board.
3. Place input decoupling ceramic capacitor C_{IN} as close as possible to the V_{IN} pin and power pad. C_{IN} must be connected to power GND with a short and wide copper trace.
4. Schottky anode pad and IC exposed pad should be placed close to ground clips in CLA applications.
5. Use "Kelvin" or "4-wire" connection techniques from the sense resistor pads directly to the CSP and CSN pins. The CSP and CSN traces should be in parallel to avoid interference.
6. Place multiple vias between top and bottom GND planes for best heat dissipation and noise immunity.
7. Use short traces connecting HSB-C_{HSB}-SW loop.
8. SW pad is noise node switching from V_{IN} to GND. It should be isolated away from the rest of circuit for good EMI and low noise operation.

Example PCB Layout



Typical Application Circuit

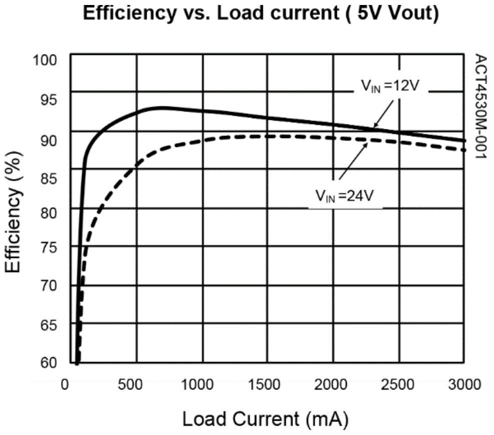


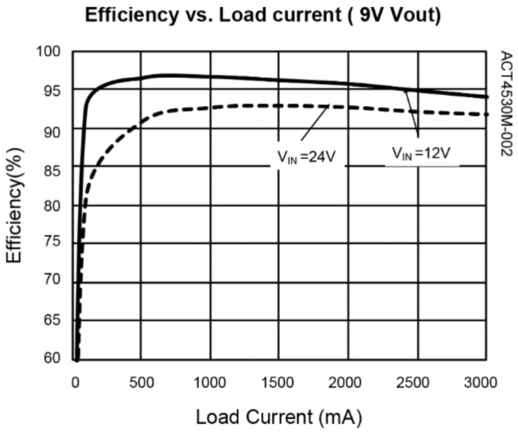
BOM List for 2.4 A Car Charger

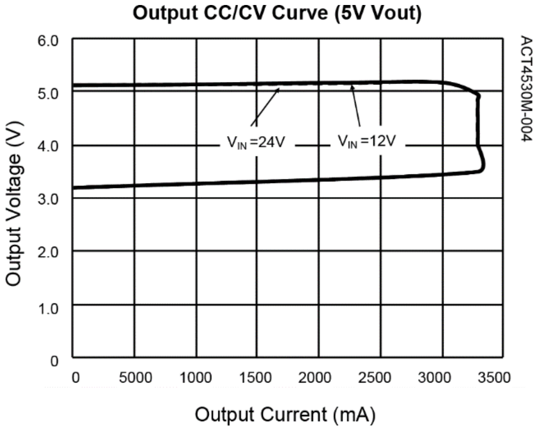
ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT4530M, SOP-8EP	Active-Semi	1
2	C1	Capacitor, Electrolytic, 47 μF/35 V	Murata, TDK	1
3	C2	Capacitor, Ceramic, 10 μF/25 V, 1206, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 22 nF/25 V, 0603, SMD	Murata, TDK	1
5	C4	Capacitor, Ceramic, 22 μF/16 V, 1206, SMD	Murata, TDK	1
6	C5	Capacitor, Electrolytic, 220 μF/16 V	Murata, TDK	1
7	C6	Capacitor, Ceramic, 2.2 μF/16 V, 0805, SMD	Murata, TDK	1
8	L1	Inductor, 40 μH, 4 A, 20%		1
9	D1	Diode, Schottky, 40 V/5 A, SK54L	Panjit	1
10	Rcs	Chip Resistor, 20 mΩ, 1206, 1%	Murata, TDK	1

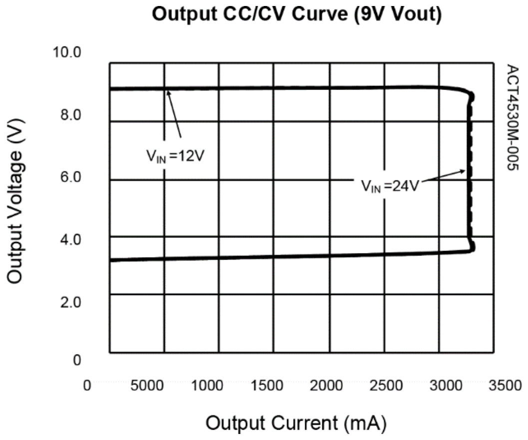
TYPICAL PERFORMANCE CHARACTERISTICS

(Schematic as shown in typical application circuit, T_a = 25 °C, unless otherwise specified)


Efficiency vs. Load current (5V Vout)


Efficiency vs. Load current (9V Vout)

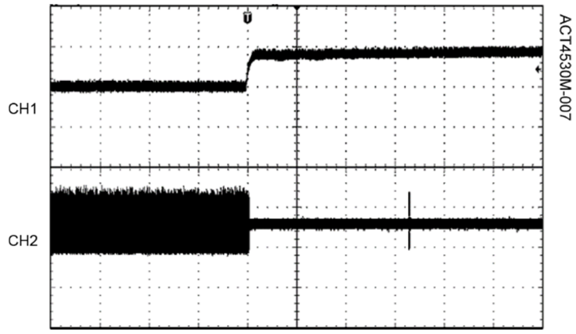

Output CC/CV Curve (5V Vout)


Output CC/CV Curve (9V Vout)

TYPICAL PERFORMANCE CHARACTERISTICS

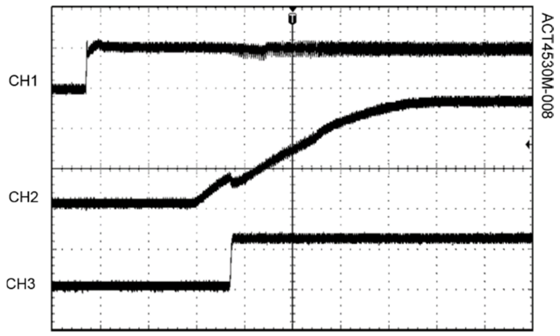
(Schematic as shown in typical application circuit, T_a = 25 °C, unless otherwise specified)

Output Over Voltage (5V Vout)



CH1: V_{OUT}, 1V/div
CH2: SW, 10V/div
TIME: 1ms/div

Start up into CC Mode



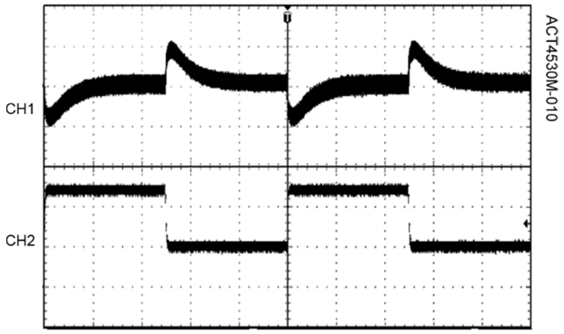
CH1: V_{IN}, 10V/div
CH2: V_{OUT}, 2V/div
CH3: I_{OUT}, 2A/div
TIME: 400µs/div

V_{OUT} = 5.1V
R_{LORD} = 1.5Ω
I_{OUT} = 2.65A
V_{IN} = 12V

Load Transient (80mA-1A-80mA)
Vin=12V, Vout=5V

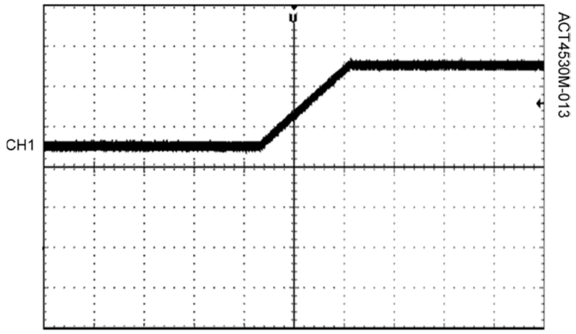
CH1: V_{OUT}, 100mV/div
CH2: I_{OUT}, 1A/div
TIME: 400us//div

Load Transient (1A-2.4A-1A)
Vin=12V, Vout=5V



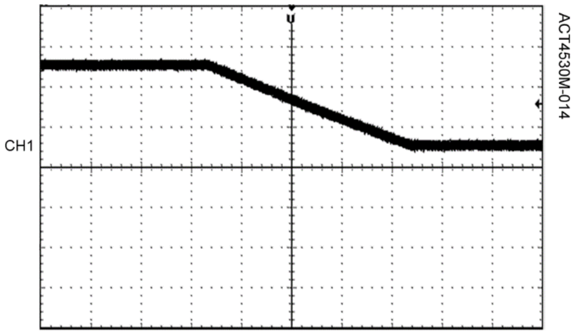
CH1: V_{OUT}, 200mV/div
CH2: I_{OUT}, 1A/div
TIME: 400us//div

Voltage Transient (5V-9V)



CH1: V_{OUT}, 2V/div
TIME: 10ms//div

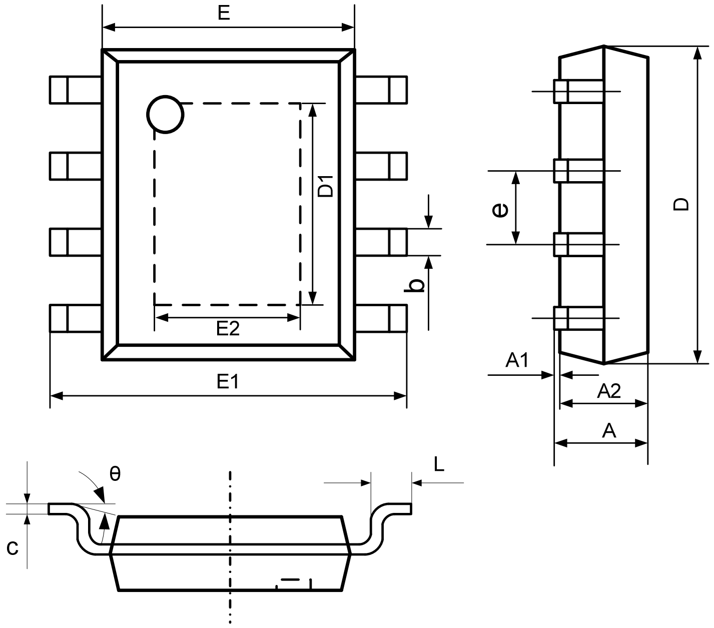
Voltage Transient (9V-5V)



CH1: V_{OUT}, 2V/div
TIME: 10ms//div

PACKAGE OUTLINE

SOP-8EP PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.727	0.053	0.068
A1	0.000	0.152	0.000	0.006
A2	1.245	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.734	4.000	0.147	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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