ACT85610

Integrated High Voltage Power Loss Protection with PMIC

BENEFITS and FEATURES

- **HIGH PERFORMANCE POWER LOSS PROTECTION**
  - Wide 2.7-to-14V Operating Input Range with 14.4V OVP
  - 20V Max Input Withstand Voltage
  - Adjustable Start-Up Slew Rate
  - Inrush Current Control
  - Configurable Power Failure Levels
  - Programmable 10A Input Current Limit
  - Programmable 5.5V to 31V Boost Storage Voltage
  - 31V@8A Synchronous Buck Supports 100% Duty Cycle
  - Programmable up to 2.25MHz Buck Operating Frequency for Small Inductor Size
  - Undetectable Transition from Input Supply to Capacitor Bank Power
  - Compatible with Different Types of Storage Caps: Super Caps, Electrolytic, Tantalum, POSCAP etc.
  - Autonomous Health Monitoring
  - Early Storage Capacitor Failure Detection
  - Storage Capacitance Measurement
  - eFuse, Boost, and Buck UV/OV/OC Protection

- **High Efficiency PMIC with Integrated FETs**
  - 4 High Voltage DC-DC Buck Converters
  - Integrated Synchronous Power Stage.
  - Up to 96% Efficiency
  - Optimized Single Stage Conversion from 12V for Outputs as Low as 0.6V
  - Excellent Dynamic Response
  - Proprietary COT Control Algorithm
  - Small Inductor Sizes
  - Fast Transient Response
  - 1 High Voltage Nonsynhronous Boost Regulator
  - 1 LDO with Programmable Output Voltage
  - 500 kHz – 2.0MHz Configurable Frequency Range
  - Near Constant Frequency
  - Sensorless Over Current Protection (OCP)
  - Output UV and OV Detection
  - Ceramic Capacitor Stable

- **SYSTEM CONTROL AND INTERFACE**
  - Dedicated Power Loss Indicator Pin (PLI)
  - 6 Programmable General Purpose I/O (6 X GPIOs)
  - I2C Serial Interface & Password Protection
  - ADC Monitoring of Critical Signals
  - Independent On & Off Sequencing Control.
  - Reset /Power Good Output
  - Configurable Rails On/Off though I2C/GPIO
  - Input Power, UV and OV Monitoring
  - Configurable Interrupts to Inform Host for any Faults/Status Change
  - Thermal Alert and Protection

- **SYSTEM MANAGEMENT**
  - Versatile GPIO Functions
  - Watchdog Supervision
  - Interrupt Function Available
  - I2C Safety bits to Enhance Immunity against Spurious I2C Transactions.
  - Thermal Enhanced FCQFN Package

APPLICATIONS

- Solid State Drives
- Industrial Applications
- Backup Power
- Hot Plug Devices

GENERAL DESCRIPTION

The ACT85610 device is a highly integrated, high configurable multiple output power management unit (PMIC) with built-in power loss protection (PLP) IC. There are four high efficiency Bucks that can supply 3 x 4A and 1 x 2A current with the output as low as 0.6V. In addition, there is a Boost regulator with 12V output and a fixed output Buck to provide the power for IC itself and to supply power to the gate drivers in regulators for maximum efficiency.

The power loss protection provides backup storage power in the event of an input power failure. A built-in Boost converter provides high voltage energy storage to minimize storage capacitor size requirements. The built-in supplement Buck converter regulates the storage voltage to a fixed output voltage. It contains internal, back-to-back eFuse FETs to provide bi-directional input to output isolation. The IC also provides hot swap and inrush current control.

The ACT85610 features programmable storage capacitor voltage to optimize the storage capacitor sizing and system run time. The internal ADC and health monitoring provide an extra layer of protection and improve system reliability and early capacitor failure notification. It automatically checks the storage capacitor health and notifies the user when the energy in the storage caps is not sufficient for backup power. The ADC also measures the input voltage, output voltage, storage voltage, eFuse current, and die temperature. The built-in synchronous supplement Buck converter maximizes energy transfer from the storage caps to the system.

The high voltage step-down regulators use a proprietary control architecture that is based on a constant on-time (COT) topology. It is designed for high efficiency, has programmable switching frequency options, is suitable for high conversion ratios to support output voltages as low as 0.6V and can therefore operate at very low duty cycles as required in low output voltage cases. It is therefore suitable for a variety of step-down applications.

The proprietary architecture allows the regulators to work at near constant frequency at a given operating point, determined by the input and output voltage. As load is varied, the regulator operates at a near constant frequency while operating in continuous conduction mode. The frequency is selectable to accommodate a variety of inductor values and sizes. When load current is reduced, frequency is automatically scaled back to maintain high efficiency in discontinuous mode (DCM) operation. The regulator achieves high efficiencies even at light loads as a result.

Depending on the application, a suitable inductor must be selected with careful considerations of the desired transient response requirements and efficiency targets which can be affected by the inductor choice and the maximum DCR of the inductor. Based on these criteria, a suitable switching frequency can then be selected to ensure stable and well controlled output voltage regulation and to maintain high efficiency. Careful analysis of operating points - input and output voltage ratio and load profiles, such as typical operating currents where efficiency is most important, peak switching currents, inductor current ripple and the desired dynamic response should all be considered while selecting inductors and for selecting the frequency of operation. The regulators are all internally compensated for stable operation using proprietary methodology. This allows the PMIC to work with a variety of inductor values and switching frequencies and allows the end user to balance requirements such as efficiency, dynamic load transient response, inductor form factors and current ratings, peak inductor current ripple and output voltage ripple. All the configurable options have programmable defaults and can be accessed and modified by the user using I2C and the regulators can be independently optimized.

The ACT85610 also has a Boost regulator. The input to the Boost regulator is typically in the range of 2.5V – 14V and the output voltage is configurable in the range of 10.8V – 13.2V in Boost mode.

The fixed output Buck regulator is used as the power supply to the IC itself and to supply power to the gate drivers in the regulators, with 100mA max current capability for external circuits and LDO input.

When input is 3.3V or 5V, the VCC pin is tied to VBUS directly. The integrated LDO can support 300mA output current. For applications when input voltage is higher than 3.5V, Buck VCC is running, the maximum LDO output current is limited at 50mA.

ACT85610 provides an I^2C bus interface to allow MCU control and monitoring. There are supervisor monitors for the input voltage, output voltage, and storage voltage. There are 6 configurable GPIOs available that can be programmed to implement a variety of system

functions. They can be programmed to generate interrupts - as an interrupt request pin (nIRQ pin), to control and sequence external regulators, to enable or disable internal regulators, as input lines to control entry or exit from low power state and other such system related functions. The GPIOs can also be used to perform dynamic voltage scaling or DVS for the buck regulators or control the external DC-DC regulators. This function allows the user to scale the output voltage of buck regulators high during normal cases and lower to conserve power during low power mode.

As a safety measure a register passcode is used to enable I2C transactions as such. Need to write 0xAA to byte 0x0A for both PLP and PMIC to enable I2C writing. If this byte has value different 0xAA then cannot do a I2C writing. A die ID and electrical revision ID read out is possible via register read out.

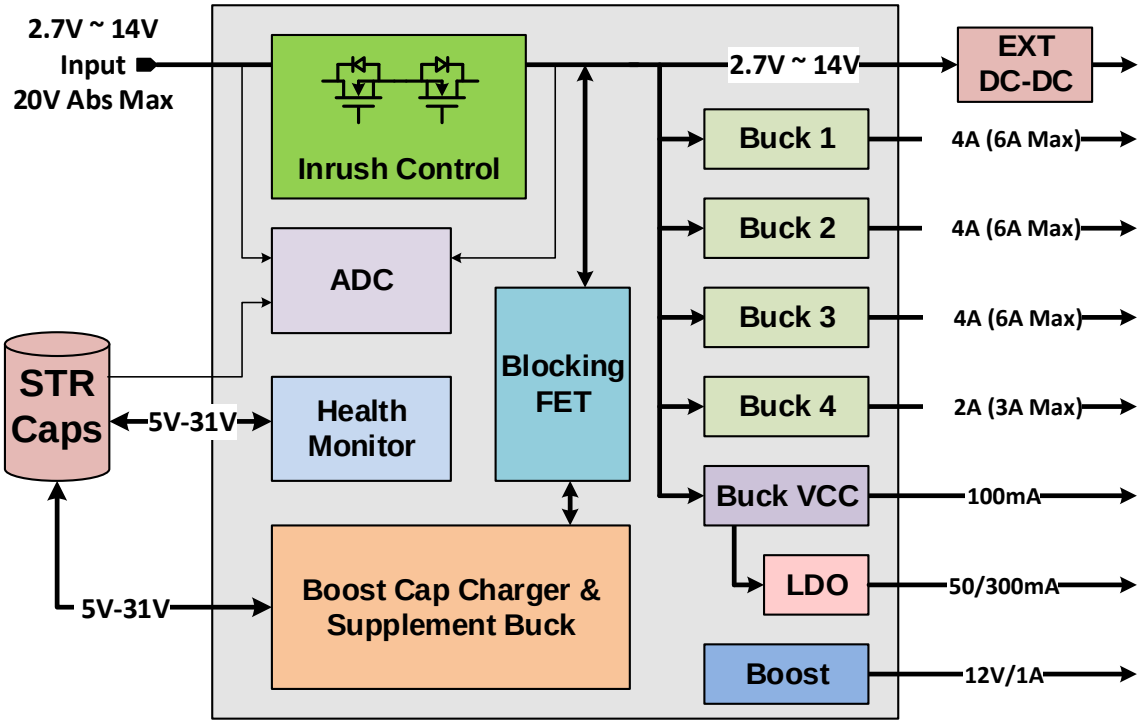
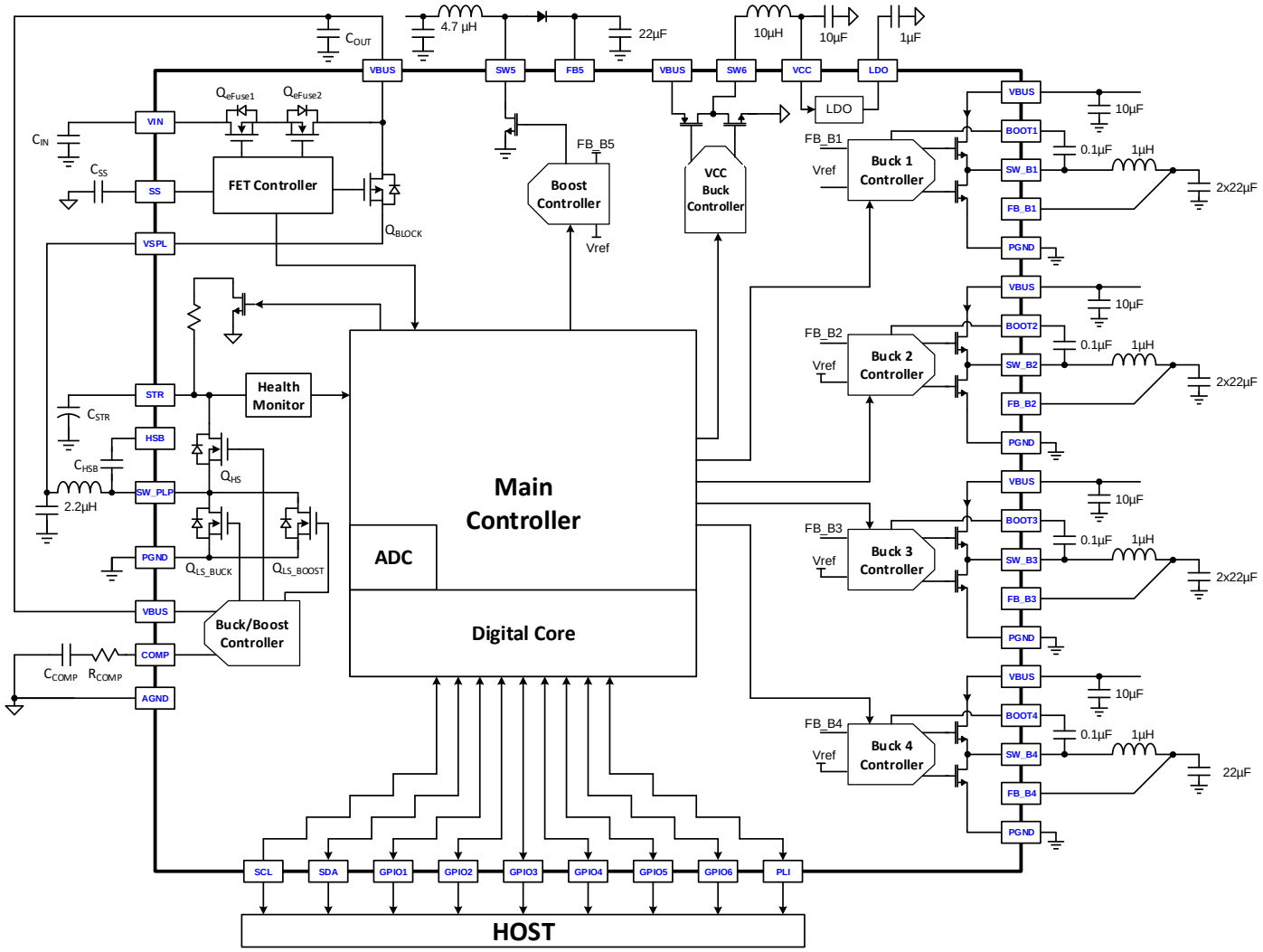


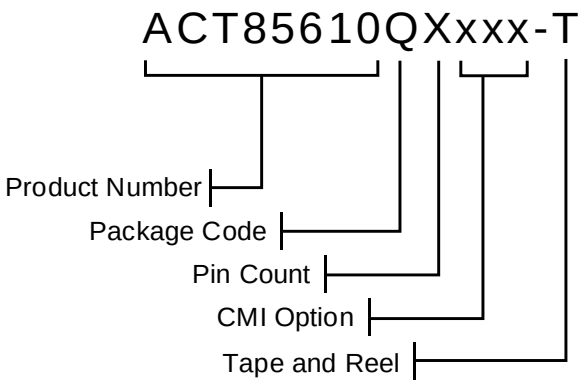
Figure 1: ACT85610 Blocks

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	V_{IN}	V_{STR}	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{OUT5}	CMI ID 0x19h
ACT85610QX101-T	12V	28V	0.95V	0.95V	0.95V	1.2V	1.8V	0001b



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Qorvo components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator. “Q” represents QFN.

Note 4: Pin Count designator. “X” represents 52 pins.

Note 5: “xxx” represents the CMI (Code Matrix Index) option The CMI identifies the IC’s default register settings.

PIN CONFIGURATION

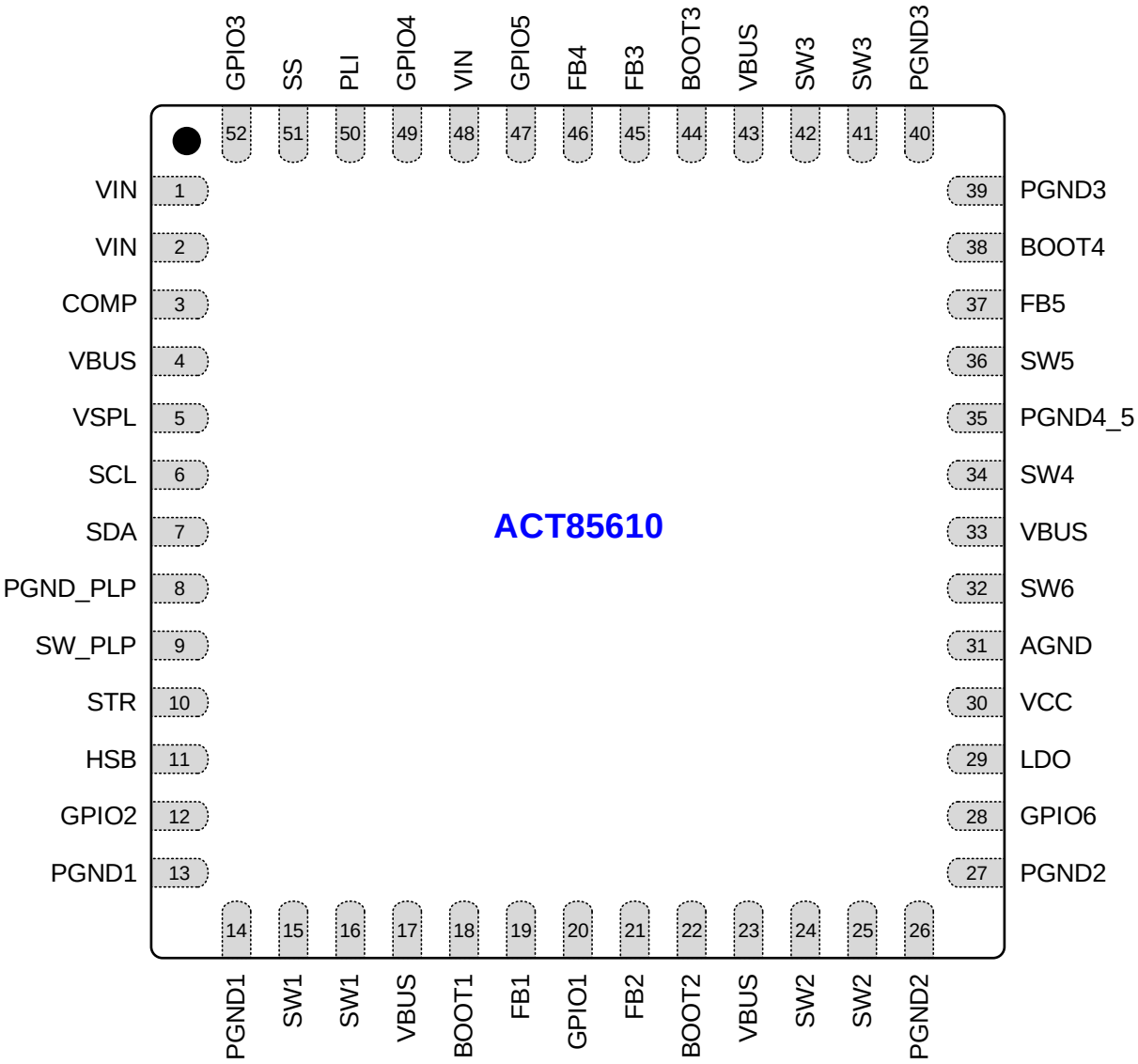


Figure 2: Pin Configuration – Top View – QFN6x6-52

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1, 2, 48	VIN	Power Supply Input. Input to the eFuse. Connect a 0.1μF capacitor between VIN and PGND as close to the IC as possible.
3	COMP	Compensation input pin for the supplement Buck converter.
4, 17, 23, 33, 43	VBUS	Output for by-pass mode, in-rush, and eFuse functionality. VBUS is also the input voltage bus for the downstream regulators.
5	VSPL	Supplement Buck circuit output and Boost circuit input pin. It is isolated from VBUS with the internal blocking FET. Place the inductor between VSPL and SW_PLP.
6	SCL	I^2C Clock Input. Needs an external pull up resistor.
7	SDA	I^2C Data Input and Output. Needs an external pull up resistor.
8	PGND_PLP	PLP Power Ground. Connect to large ground plane on PCB
9	SW_PLP	Power loss protection Buck switching node. This is the boost converter switch node and the buck converter switch node. Place the inductor between VSPL and SW_PLP.
10	STR	Storage Capacitor Input. Connect the storage capacitors to STR. STR requires a minimum capacitor of 100μF to PGND.
11	HSB	High Side Bias, Boot-strap pin. This provides power to the internal high-side MOSFET gate driver circuitry. Connect a 47nF capacitor from HSB pin to SW_PLP pin.
12	GPIO2	GPIO2 Pin
13, 14	PGND1	Buck1 Power Ground. Connect to large ground plane on PCB
15, 16	SW1	Switch pin for HV Buck1 regulator
18	BOOT1	Boot strap voltage for HV Buck1 regulator. Connect a 0.1μF capacitor between BOOT1 and SW_B1.
19	FB1	Output and feedback pin for HV Buck1 regulator
20	GPIO1	GPIO1 Pin
21	FB2	Output and feedback pin for HV Buck2 regulator
22	BOOT2	Boot strap voltage for HV Buck2 regulator. Connect a 0.1μF capacitor between BOOT2 and SW_B2.
24, 25	SW2	Switch pin for HV Buck2 regulator
26, 27	PGND2	Buck2 Power Ground. Connect to large ground plane on PCB
28	GPIO6	GPIO6 Pin
29	LDO	LDO output pin. Place 1uF or large ceramic between this pin and AGND.
30	VCC	Output and feedback pin for VCC Buck regulator
31	AGND	Analog Ground. Kelvin connect AGND to the PGND plane.

32	SW6	Switch pin for VCC Buck regulator
34	SW4	Switch pin for HV Buck4 regulator
35	PGND4_5	Buck4 and Boost Power Ground. Connect to large ground plane on PCB
36	SW5	Switch pin for Boost regulator
37	FB5	Output and feedback pin for Boost regulator
38	BOOT4	Boot strap voltage for HV Buck4 regulator. Connect a 0.1μF capacitor between BOOT4 and SW_B4.
39, 40	PGND3	Buck3 Power Ground. Connect to large ground plane on PCB
41, 42	SW3	Switch pin for HV Buck3 regulator
44	BOOT3	Boot strap voltage for HV Buck3 regulator. Connect a 0.1μF capacitor between BOOT3 and SW_B3.
45	FB3	Output and feedback pin for HV Buck3 regulator
46	FB4	Output and feedback pin for HV Buck4 regulator
47	GPIO5	GPIO5 Pin
49	GPIO4	GPIO4 Pin
50	PLI	Power Loss Indicator Open-Drain Output for VIN. PLI goes high when the eFuse is turned on and goes low when the IC enters supplement mode. PLI is referenced to AGND.
51	SS	Soft Start Input. Place a capacitor from SS to VSS to control the eFuse startup voltage slew rate.
52	GPIO3	GPIO3 Pin
Exposed Pad		Tie to top layer ground plane. All PGNDx pins must be directly connected to the exposed pad on the top layer.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
All Pins to GND unless stated otherwise below	-0.3 to 6	V
VIN to PGND	-0.3 to 20	V
VBUS to PGND	-0.3 to 14.8	V
VSPL to AGND	-0.3 to VBUS+0.3	V
HSB to SW_PLP	-0.3 to 6	V
SW_PLP to PGND_PLP	-1 to STR+ 0.3	V
STR to PGND	-0.3 to 33	V
PGND1, PGND2, PGND3,PGND4_5, PGND_PLP to AGND	-0.3 to + 0.3	V
SW1,2,3,4 to PGND	-1 to VBUS + 1	V
BOOTx to SWx (BOOT1 to SW1, BOOT2 to SW2 etc.)	-0.3 to SWx + 6	V
SW5 to PGND	-0.3 to 18	V
FB5 to AGND	-0.3 to 15.5	V
FB1,2,3,4 to AGND	-0.3 to 6	V
VCC to PGND	-0.3 to min (6, VBUS+0.3)	V
SW6 to PGND	-1 to VBUS + 1	V
SCL, SDA to AGND	-0.3 to 6.0	V
GPIOx to AGND	-0.3 to 6.0	V
PLI to AGND	-0.3 to 6.0	V
SS to AGND	-0.3 to 6.0	V
LDO to AGND	-0.3 to min (6, VCC+0.3)	V
AGND, PGND	-0.3 to + 0.3	V
ESD Rating (human body model), all pins	2	kV
Storage Temperature	-40 to 150	°C
Operating Junction Temperature (T_J)	-40 to 150	°C
Junction to Ambient Thermal Resistance (θ_{JA})	35	°C/W
Lead Temperature (Soldering, 10 sec)	300	°C

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note2: All other pins meet +/- 2kV HBM ESD

Note3: Measured on Qorvo Evaluation Kit

DIGITAL I/O ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIOx Input Low				0.35	V
GPIOx Input High		1.25			V
GPIOx Open Drain Leakage Current	Output = 5V			1	μA
GPIOx Open Drain Output Low	IOL = 1mA			0.35	V
GPIOx Input Deglitch Time (falling)			20		μs
GPIOx Input Deglitch Time (rising)			10		μs

ELECTRICAL CHARACTERISTICS: PLP SYSTEM CHARACTERISTICS

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply					
Input Supply Voltage Range	VIN (Note 1)	2.7		14	V
Input Supply Over Voltage Lock Out (VIN_OVLO)			14.4		V
Input Under Voltage Lock Out (VIN_UVLO)	VIN Rising	2.5	2.6	2.7	V
	VIN_UVLO hysteresis	20	50	80	mV
Input Operation Current	eFuse Enabled and Soft start completed Buck/Storage Regulator Disabled ADC Disabled Storage Health Check Disabled All PMIC BUCKs turned on, no load PMIC_Boost turned on, no load VIN=12V		3.3		mA
	eFuse Enabled and Soft start completed Buck/Storage Regulator Disabled ADC Enabled Storage Health Check Disabled All PMIC BUCKs turned on, no load PMIC_Boost turned on, no load VIN=12V		4.1		mA
Input Current (Shutdown)	VIN=12V, GPIO5 set as FORCE_OFF pin to turn off IC.		0.59		mA
Thermal					
Thermal Warning Rising	Sets nIRQ		125		°C
Thermal Warning Hysteresis			34		°C
Thermal Shutdown 1 Rising – Disables buck and boost			145		°C
Thermal Shutdown 1 Hysteresis			28		°C
Thermal Shutdown 2 Rising – Disables eFuse			155		°C
Thermal Shutdown 2 Hysteresis			28		°C
STR Thresholds					
Input Under Voltage Lock Out (STR_UVLO)	STR Falling	2.7	2.8	3.1	V
Input Under Voltage Lock Out (STR_UVLO)	STR Rising		3.1		V

VIN UV & OV Thresholds					
Under Voltage Falling Threshold Programmable Range	UV REF after POR release (-40°C ~ 125°C), percentage of VIN_SEL	80		95	%
Under Voltage Threshold Accuracy		-5	0	5	%
UV Hysteresis			2		%
Overvoltage Reference Rising Threshold Programmable Range	OV REF after POR release, percentage of VIN_SEL	106		120	%
Over Voltage Threshold Accuracy		-5.5	1%	5.5	%
OV Hysteresis			2		%

(Note 1): PLP System will only turn on when VIN>VIN_UVLO rising threshold, but it will stay on until VIN bellows VIN UV falling threshold.

ELECTRICAL CHARACTERISTICS: PLP REGULATOR

(VSTR = 28V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage Range	V_{STR}	3		31	V
Programmable Output Voltage Range		2.5		13.2	V
Standby Supply Current	V_{BUS} = 103%, Regulator Enabled, No Load, not switching	300	550	800	µA
Output Voltage Accuracy	V_{BUS} = 12V, I_{BUS} = 2A	-2	V_{NOM}	2	%
Line Regulation	V_{STR} = 31V to 16V, V_{BUS} = 12V, PWM Regulation		0.02		%/V
Load Regulation	V_{STR} = 28V, I_{OUT} = 500mA to 4A, V_{BUS} = 12V PWM Regulation		0.125		%/A
Power Good Threshold	V_{BUS} Rising		95		%V_{NOM}
Power Good Hysteresis	V_{BUS} Falling		2		%V_{NOM}
Overvoltage Fault Threshold	V_{BUS} Rising	105	110	115	%V_{NOM}
Overvoltage Fault Hysteresis	V_{BUS} Falling		3		%V_{NOM}
Programmable Switching Frequency Range	Not user selectable. Set by factory with CMI		562 1125 1500 2250		kHz
Current Limit, Cycle-by-Cycle	BK_CLIM = 000 BK_CLIM = 001 BK_CLIM = 010 BK_CLIM = 011 BK_CLIM = 100 BK_CLIM = 101 BK_CLIM = 110 BK_CLIM = 111		3 4 5 6 7 8 9 10		A
Current Limit, Cycle-by-Cycle Tolerance	At default BK_CLIM	-15		+15	%
	At other settings	-20		+20	%
Current Limit, Shutdown	Above BK_CLIM	+ 30	+55	+ 80	%
High Side On-Resistance	I_{SW} = -3A, V_{STR} = 12V		60		mΩ
Low Side On-Resistance	I_{SW} = 3A, V_{STR} = 12V		35		mΩ
SW Leakage Current	V_{STR} = 31V, V_{SW} = 0 or 31V			42	µA

ELECTRICAL CHARACTERISTICS: PLP EFUSE

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Normal Mode					
Operating Voltage Range	VIN (Note 1)	2.7		14	V
eFuse On-Resistance (2 FETs Combined)	I_{SW} = -2A, VIN= 3.3V, 5V, and 12V, T_J = 25°C		17		mΩ
	I_{SW} = -2A, VIN= 3.3V, 5V, and 12V, T_J = 100°C		23		mΩ
Programmable eFuse Over Current Limit Range (ISET)	Set by ISET[3:0] (0x2D[3:0])	1.5		12	A
ISET Accuracy		-10		+10	%
Programmable eFuse Current Warning Threshold	VIN = 12V, Triggers nIRQ Pin, percentage vs ISET	75	90	99	%
	VIN = 3.3V, Triggers nIRQ Pin, percentage vs ISET	75	90	99	%
eFuse Overcurrent Detection Deglitch			10		µs
Current Limit Restart Time	Retry time when hit Over current limit when starting up		100		ms
eFuse Soft start slew	VBUS slew with CSS = 10nF	5.70	6.60	7.26	mV/us

Note 1: eFUSE can only start when VIN above VIN_UVLO rising threshold. But eFUSE will stays on until VIN can hit VIN UV falling threshold.

ELECTRICAL CHARACTERISTICS: PLP BLOCKING FET

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Normal Mode					
Blocking FET On-Resistance	I_{SW} = -2A, V_{BUS}= 12V, T_J = 25°C		30		mΩ
	I_{SW} = -2A, V_{BUS}= 12V, T_J = 100°C		41		mΩ
Programmable Blocking FET Startup Soft Start Current	bfet_ISS = 00 bfet_ISS = 01 bfet_ISS = 10 bfet_ISS = 11 (not allowed)		150 210 305 n/a		mA
Current limit threshold	Full turn on state		2		A

ELECTRICAL CHARACTERISTICS: PLP STORAGE BOOST REGULATOR

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Storage Boost Converter					
Operating Input Voltage Range	V_{BUS}	2.7		14	V
Programmable Output Voltage Range		5.5V or VIN		31	V
Peak switching Current	BST _CLIM = 00 BST _CLIM = 01 BST _CLIM = 10 BST _CLIM = 11		250 500 950 1500		mA
Standby Supply Current	V_{STR} = 103%, Regulator Enabled, not switching		125	215	µA
Output Voltage Accuracy	V_{STR} = 28V, I_{OUT} = 15mA (continuous PWM mode)	-3%	V_{NOM}	3%	V
Power Good Threshold (STR_UV)	V_{STR} Rising		95		%V_{NOM}
Power Good Hysteresis	V_{STR} Falling		5		%V_{NOM}
Overvoltage Fault Threshold	V_{STR} Rising		110		%V_{NOM}
Overvoltage Fault Hysteresis	V_{STR} Falling		3		%V_{NOM}
Minimum On-Time			50		ns
Low Side FET On-Resistance	I_{SW} = 325mA		200		mΩ

ELECTRICAL CHARACTERISTICS: PLP HEALTH MONITOR

(VIN = 12V, TA = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Health Monitor					
Operating Voltage Range		4.2		31	V
Sink Current Source		9	10	11	mA
Programmable Health Monitor Current Sink Timer Range		2		2340	ms
Programmable Storage Capacitor power good Threshold	Configurable 0.5% steps	90.5		98	%
STR Capacitor Measurement Range		47		8000	µF
STR Capacitor Measurement Accuracy		-15		15	%
ADC Monitoring					
Supply Current	Enabled		2		mA
Total Error	5V scale and 12-bit range			1	LSB
Conversion Time	Total time for all channels			100	ms
Conversion Time	Total time for single channel			10	ms
Full Scale Input Range		0		2.5	V
Input Resistance			10		kΩ
Input Capacitance			5		pF

ELECTRICAL CHARACTERISTICS: PMIC SYSTEM CONTROL

(VBUS = 12.0V, VCC = 5.0V, TA = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{BUS}	2.7		14	V
Input UV Threshold, falling.		2.5	2.6	2.7	V
Input UV Threshold, hysteresis			110		mV
Input UV detection deglitch time.		75	100	125	µs
Power Up Delay after initial VIN	Time from VBUS > UVLO threshold to time when regulator starts turning on.		1200		µs
Transition time from Low Power State to Active State	Time from I^2C command to clear LPM EN register bit (exit low power state) to time when the first regulator starts turning on.		510		µs
Oscillator Frequency		2.10	2.25	2.42	MHz
Regulator Programmable Startup Delay Timings between turn on events.	ONDLY=000 ONDLY=001 ONDLY=010 ONDLY=011 ONDLY=100 ONDLY=101 ONDLY=110 ONDLY=111		0 0.25 0.5 1 2 4 8 16		ms
Regulator Programmable Turn Off Delay	Configurable in 1ms steps	0		15	ms
nRESET, Programmable Delay Timing	Configurable to 20, 40, 60, and 100ms	20		100	ms
Retry time after entering PMIC Fault state	Time when all regulators are forced off before trying ON sequence again		100		ms
Watch dog timer	Monitors I^2C inactivity and time out function		8		s
Hard reset wait timer	Hard reset turns off the regulators, waits in the reset state for a “hard-reset time delay” and restarts the on sequence.		0.5		s

ELECTRICAL CHARACTERISTICS: PMIC BUCK1,2,3 STEP-DOWN DC/DC REGULATOR

(VBUS = 12.0V, VCC = 5.0V TA = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage		2.7		14	V
FB1,2,3, Output Voltage Range	Configurable in 20mV steps	0.6		5.26	V
	Configurable in 5mV steps	0.6		1.875	V
Continuous Output Current	DC current output, 0.47µH, Switching frequency = 1.0MHz, FB1,2,3, = 1.2V	4.0			A
Standby Supply Current	FB1,2,3 >= 103%, Regulator Enabled, FB1,2,3 = 1.8V, No Load		400		µA
DC Output Voltage Accuracy	0.6V > FB1,2,3 > 1.25V, IOUT = 3A (Continuous Conduction or CCM mode)	-12.5	VNOM	12.5	mV
	FB1,2,3 >= 1.25V, IOUT = 3A (Continuous Conduction or CCM mode)	-1	VNOM	1	%
Line Regulation	FB1,2,3 = 1.8V, VBUS = 5.0V to 13.2V, (Continuous Conduction or CCM mode)		0.5		%
Load Regulation	FB1,2,3 = 1.8V,0.1AA to 4.0A (Continuous Conduction or CCM mode)		0.6		%
Power Good Threshold / POK	FB1,2,3 Rising, POK [] = 1	86	90	94	%VNOM
	FB1,2,3 Rising, POK [] = 0	83	87	91	%VNOM
Power Good Hysteresis / POK	FB1,2,3 Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	FB1,2,3 Rising, relative to regulation point	107	114	118	%VNOM
Overvoltage Fault Hysteresis	FB1,2,3 Falling, relative to regulation point		3		%VNOM
Emulated Switching Frequency, CCM - Continuous Conduction Mode.	Freq = 0000, VIN = 12.0V, VFB1,2 = 1.0V		0.4		MHz
	Freq = 0001, VIN = 12.0V, VFB1,2 = 1.0V		0.5		MHz
	Freq = 0010, VIN = 12.0V, VFB1,2 = 1.0V		0.6		MHz
	Freq = 0011, VIN = 12.0V, VFB1,2 = 1.2V		0.7		MHz
	Freq = 0100, VIN = 12.0V, VFB1,2 = 1.2V		0.8		MHz
	Freq = 0101, VIN = 12.0V, VFB1,2 = 1.2V		0.9		MHz
	Freq = 0110, VIN = 12.0V, VFB1,2 = 1.8V		1.0		MHz
	Freq = 0111, VIN = 12.0V, VFB1,2 = 1.8V		1.1		MHz
	Freq = 1000, VIN = 12.0V, VFB1,2 = 1.8V		1.2		MHz
	Freq = 1001, VIN = 12.0V, VFB1,2 = 2.5V		1.3		MHz
	Freq = 1010, VIN = 12.0V, VFB1,2 = 2.5V		1.4		MHz
	Freq = 1011, VIN = 12.0V, VFB1,2 = 2.5V		1.5		MHz
	Freq = 1100, VIN = 12.0V, VFB1,2 = 3.3V		1.6		MHz

	Freq = 1101, VIN = 12.0V, VFB1,2 = 3.3V		1.7		MHz
	Freq = 1110, VIN = 12.0V, VFB1,2 = 3.3V		1.8		MHz
	Freq = 1111, VIN = 12.0V, VFB1,2 = 3.3V		1.9		MHz
Emulated switching frequency accuracy	At the default switching frequency setting	-20		20	%
TMIN, Minimum on Time			50		ns
Soft-Start Period TSS	5% to 95% VNOM	540	1000	1500	µs
Tstart, Time from EN to PG	Time from enable to PGOOD		1350		µs
Peak Current Limit, Cycle-by-Cycle	ILIM set = 00		5		A
	ILIM set = 01		6		A
	ILIM set = 10		7		A
	ILIM set = 11		8		A
Peak Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-15		15	%
Valley Current Limit, Cycle-by-Cycle	ILIM set = 00		5		A
	ILIM set = 01		6.1		A
	ILIM set = 10		6.8		A
	ILIM set = 11		7.5		A
Valley Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-33		33	%
LS FET reverse conduction current limit			3.6		A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	115	125	135	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	69	78	91	%
HS On-Resistance	ISW = 1A, VCC5 = 5.0V		33		mΩ
LS NMOS On-Resistance	ISW = 1A, VCC5 = 5.0V		16		mΩ
SW Leakage Current	VIN = 12.0V, VSW = 0 or 12.0V			1	µA
Dynamic Voltage Scaling Rate	Buck output voltage range set to 5mV steps		0.022		mV/us
	Buck output voltage range set to 20mV steps		0.088		mV/us
Output Pull Down Resistance	Pull Down Enabled when the regulator is turned off. PD_OPTION[]=0		6		Ohms
	PD_OPTION[]=1		20		Ohms

ELECTRICAL CHARACTERISTICS: PMIC BUCK4 STEP-DOWN DC/DC REGULATOR

(VBUS = 12.0V, VCC = 5.0V, TA = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage		2.7		14	V
FB4, Output Voltage Range	Configurable in 20mV steps	0.6		5.26	V
	Configurable in 5mV steps	0.6		1.875	V
Continuous Output Current	DC current output, 0.47µH, Switching frequency = 1.0MHz, FB4 = 1.2V.	2.0			A
Standby Supply Current	FB4 >= 103%, Regulator Enabled, FB4 = 1.8V, No Load		428		µA
DC Output Voltage Accuracy	0.6V > FB4 > 1.25V, IOUT = 1A (Continuous Conduction or CCM mode)	-12.5	VNOM	12.5	mV
	FB4 >= 1.25V, IOUT = 1A (Continuous Conduction or CCM mode)	-1	VNOM	1	%
Line Regulation	FB4 = 1.8V, VBUS = 5.0V to 13.2V, (Continuous Conduction or CCM mode)		0.5		%
Load Regulation	FB4 = 1.8V, 0.1A to 2.0A (Continuous Conduction or CCM mode)		0.6		%
Power Good Threshold / POK	FB4 Rising, POK [] = 1	86	90	94	%VNOM
	FB4 Rising, POK [] = 0	83	87	91	%VNOM
Power Good Hysteresis / POK	FB4 Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	FB4 Rising, relative to regulation point	108	114	118	%VNOM
Overvoltage Fault Hysteresis	FB4 Falling, relative to regulation point		3		%VNOM
Emulated Switching Frequency, CCM - Continuous Conduction Mode.	Freq = 0000, VIN = 12.0V, VFB3,4 = 1.0V		0.4		MHz
	Freq = 0001, VIN = 12.0V, VFB3,4 = 1.0V		0.5		MHz
	Freq = 0010, VIN = 12.0V, VFB3,4 = 1.0V		0.6		MHz
	Freq = 0011, VIN = 12.0V, VFB3,4 = 1.2V		0.7		MHz
	Freq = 0100, VIN = 12.0V, VFB3,4 = 1.2V		0.8		MHz
	Freq = 0101, VIN = 12.0V, VFB3,4 = 1.2V		0.9		MHz
	Freq = 0110, VIN = 12.0V, VFB3,4 = 1.8V		1.0		MHz
	Freq = 0111, VIN = 12.0V, VFB3,4 = 1.8V		1.1		MHz
	Freq = 1000, VIN = 12.0V, VFB3,4 = 1.8V		1.2		MHz
	Freq = 1001, VIN = 12.0V, VFB3,4 = 2.5V		1.3		MHz
	Freq = 1010, VIN = 12.0V, VFB3,4 = 2.5V		1.4		MHz
	Freq = 1011, VIN = 12.0V, VFB3,4 = 2.5V		1.5		MHz
	Freq = 1100, VIN = 12.0V, VFB3,4 = 3.3V		1.6		MHz

	Freq = 1101, VIN = 12.0V, VFB3,4 = 3.3V		1.7		MHz
	Freq = 1110, VIN = 12.0V, VFB3,4 = 3.3V		1.8		MHz
	Freq = 1111, VIN = 12.0V, VFB3,4 = 3.3V		1.9		MHz
Emulated switching frequency accuracy	At the default switching frequency setting	-20		20	%
TMIN, Minimum on Time			50		ns
Soft-Start Period TSS	5% to 95% VNOM	540	1000	1500	µs
Tstart, Time from EN to PG	Time from enable to PGOOD		1350		µs
Peak Current Limit, Cycle-by-Cycle	ILIM set = 00		2		A
	ILIM set = 01		2.6		A
	ILIM set = 10		3.1		A
	ILIM set = 11		4		A
Peak Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-15		15	%
Valley Current Limit, Cycle-by-Cycle	ILIM set = 00		2.0		A
	ILIM set = 01		2.5		A
	ILIM set = 10		3.1		A
	ILIM set = 11		3.8		A
Valley Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-33		33	%
LS FET reverse conduction current limit			2.9		A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	110	125	135	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	69	80	91	%
HS On-Resistance, Buck 1	ISW = 1A, VCC5 = 5.0V		60		mΩ
LS NMOS On-Resistance, Buck 1	ISW = 1A, VCC5 = 5.0V		30		mΩ
HS On-Resistance, Buck 2	ISW = 1A, VCC5 = 5.0V		60		mΩ
LS NMOS On-Resistance, Buck 2	ISW = 1A, VCC5 = 5.0V		30		mΩ
SW Leakage Current	VIN = 12.0V, VSW = 0 or 12.0V			1	µA
Dynamic Voltage Scaling Rate	Buck output voltage range set to 5mV steps		0.022		mV/us
	Buck output voltage range set to 20mV steps		0.088		mV/us
Output Pull Down Resistance	Pull Down Enabled when the regulator is turned off. PD_OPTION[]=0		6		Ohms

	PD_OPTION[]=1	20	Ohms

ELECTRICAL CHARACTERISTICS: PMIC BOOST STEP-UP DC/DC REGULATOR

(VBUS = 12V, VCC = 5.0V, TA = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Boost Operating Input Voltage	Can be external supply not connected to ACT85610	2.5		13.2	V
Output Voltage Range	Configurable in 50mV steps	MAX (VIN, 10.8)	12	13.2	V
Output Step Size			50		mV
Output Voltage Accuracy	VINB = 5.0V, VOUT = 12.0V, IOUT = 0.5A	-2		2	%
	VINB = 5.0V, VOUT = 12.0V, IOUT = 0.1A	-2		2	%
Continuous Output Current	VINB = 12.0V, 4.7µH, VOUT = 12.0V, ILIM set = 11.			2	A
	VINB = 5.0V, 4.7µH, Switching frequency = 1MHz, VOUT = 12.0V, ILIM set = 11.			1	A
	VINB = 3.3V, 4.7µH, Switching frequency = 1MHz, VOUT = 12.0V, ILIM set = 11.			0.6	A
Iq, Supply Current.	Regulator is switching, no load		120		µA
SW5 leakage from VINB and VOUT (input or output)	SW5 = 0V / 12V, VINB =12V			1	µA
Line Regulation (DC)	VOUT = 12V, VINB = 3V-11V, Iout = 200mA.		0.5		%
Load Regulation	VOUT = 12.0V, VINB = 5.0V, 0.1A to 0.5A.		0.2		%
Power Good Threshold	VOUT Rising, relative to regulation point	82	86	90	%VNOM
Power Good Hysteresis	VOUT Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	VOUT Rising, relative to regulation point	109	112	116	%VNOM
Overvoltage Fault Hysteresis	VOUT Falling, relative to regulation point		3		%VNOM
Switching Frequency, CCM - Continuous Conduction Mode.	Frequency VINB = 5.0V, VOUT = 12.0V	-7 %	1125	+7 %	kHz
Soft-Start Period TSS	5% to 95% VNOM, VOUT = 12.0V		10		ms
Tstart, Time from EN to PG	Time from enable to PGOOD		11		ms
Current Limit, Cycle-by-Cycle	ILIM set = 00, Boost Mode		1.2		A
	ILIM set = 01, Boost Mode		1.7		A
	ILIM set = 10, Boost Mode		2.1		A
	ILIM set = 11, Boost Mode		2.5		A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	115	125	140	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	69	80	90	%
LS1 NMOS On-Resistance	ISW = 0.2A, VCC = 5.0V,		0.1	0.15	Ω

ELECTRICAL CHARACTERISTICS: VCC REGULATOR

(VBUS = 12.0V, VCC = 5.0V, TA = 25°C, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage Range	VCC Regulator input voltage	2.7		14	V
Output Current	For external circuit and LDO input			100	mA
Output Voltage – mini-Buck			4.9 5.0 5.1 5.2		V
Output Voltage – mini-Buck Accuracy	With 100mA Current	-5		5	%
Output Voltage – mini-LDO	mBK_5V_LDO = 0 mBK_5V_LDO = 1		4.5 5		V
Output Voltage – mini- LDO Accuracy	With 10mA Current	-6		6	%
HS PMOS on Resistance	VBUS = 12.0V		520		mΩ
LS NMOS on Resistance	VBUS = 12.0V		470		mΩ
Recommended Component Values					
Input Capacitor, C_{VBUS}	25V, SMT, 0603		1		µF
Output Capacitor, C_{OUTVCC}	10V, SMT, 0402		0.22		µF
Output Capacitor, C_{OUTVCC}	10V, SMT, 0603		10		µF
Inductor	10uH, I_{SAT} > 500mA		10		µH

ELECTRICAL CHARACTERISTICS: LDO

(VIN_LDO = 5V, TA = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.6		5.5	V
Output Voltage Range – VSET	Configurable in 25mV steps	0.8		3.75	V
Output Voltage Accuracy	V_{IN_LDO} - V_{LDO_OUT} > 0.4V	-2	V_{SET}	2	%
Line Regulation	V_{IN_LDO} - V_{LDO_OUT} > 0.4V V_{IN_LDO} = 2.8V to 5.5V I_{LDO_OUT} = 1mA		0.026		% / V
Load Regulation	I_{LDO_OUT} = 1mA to 100mA, LDO_ILIM=1X		-1	0.5	% / A
Power Supply Rejection Ratio	f = 1kHz, I_{LDO_OUT} = 20mA, V_{LDO_OUT} = 1.8V		34		dB
	f = 10kHz, I_{LDO_OUT} = 20mA, V_{LDO_OUT} = 1.8V		37		
	f = 2.25MHz, I_{LDO_OUT} = 20mA, V_{LDO_OUT} = 1.8V		7.1		
Supply Current per Output	Regulator Disabled		0		µA
Supply Current per Output	Regulator Enabled, No load		25		µA
Soft-Start Period	V_{LDO_OUT} = 1.8V Setting (10% to 90%) LDO SS_RAMP=00 LDO SS_RAMP=01 LDO SS_RAMP=10 LDO SS_RAMP=11		 110 110 165 215		µs
	V_{LDO_OUT} = 2.5V Setting (10% to 90%) LDO SS_RAMP=00 LDO SS_RAMP=01 LDO SS_RAMP=10 LDO SS_RAMP=11		 145 145 175 215		
	V_{LDO_OUT} = 3.3V Setting (10% to 90%) LDO SS_RAMP=00 LDO SS_RAMP=01 LDO SS_RAMP=10 LDO SS_RAMP=11		 200 200 210 235		
Power Good Threshold	V_{LDO_OUT} Rising	89	93	97	$\%V_{NOM}$
Power Good Hysteresis	V_{LDO_OUT} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{LDO_OUT} Rising	104	110	115	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{LDO_OUT} Falling		3		$\%V_{NOM}$
Discharge Resistance			1600		Ω
Dropout Voltage	I_{LDO_OUT} = 30mA		20	90	mV
Dropout Voltage	I_{LDO_OUT} = 50mA, LDO_ILIM=01		33	150	mV
Dropout Voltage	I_{LDO_OUT} = 100mA, LDO_ILIM=1x		68	310	mV

Dropout Voltage	I_{LDO_OUT} = 150mA V_{IN_LDO23} > 2.8 LDO_ILIM=11	103	500	mV
Output Current Limit	LDO_ILIM=00 LDO_ILIM=01 LDO_ILIM=10 LDO_ILIM=11	80 145 225 390		mA

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{IO_IN} = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low				0.35	V
SCL, SDA Input High	V_{IO_IN} = 1.8V	1.2			V
SDA Leakage Current	SDA = 5V			1	μA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		1000	kHz
SCL Low Period, t_{LOW}		0.5			μs
SCL High Period, t_{HIGH}		0.26			μs
SDA Data Setup Time, t_{SU}		50			ns
SDA Data Hold Time, t_{HD}	(Note1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns
Stop Setup Time, t_{SP}	For Stop Condition	260			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Rise Time SDA, Tr	Device requirement			120	ns
SDA Fall Time SDA, Tf	Device requirement			120	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns

Note1: Comply to I²C timings for 1MHz operation - “Fast Mode Plus”.

Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering UV/POR state.

Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the device.

Note4: The ACT85610 has two I²C addresses. Address 0x24h is for the PLP and address 0x25h is for the PMIC.

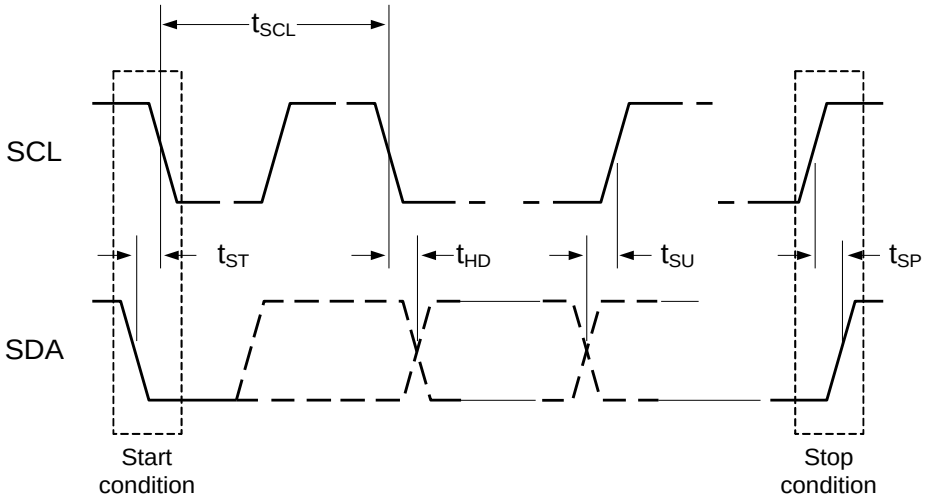


Figure 4: I²C Data Transfer

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

ACT85610 provides protection, control, and supplemental storage for power failure prevention systems. This functionality goes by many names: Power Loss Protection (PLP), Power Loss Imminent (PLI) and Power Failure Protection (PFP). It provides a system with additional run time after a power failure to all the system to save critical data before shutting down. Typical applications include solid state disk drives (SSD) and servers. In normal operation when input power is good, the IC connects the input to the output through the eFuse. This powers the system load from the system input power. If an input voltage fault occurs, the IC disconnects the input from the output and enters supplement mode, where output power comes from the high voltage storage capacitor power. The internal buck converter efficiently converts the storage voltage down to the regulated output voltage. All startup, storage capacitor charging, and switching between normal and supplement mode operation is autonomous and does not require user intervention.

During start up, the ACT85610 limits the output voltage dV/dt to minimize system level inrush currents. After soft start is complete, the IC charges the storage capacitors with the internal boost converter. The IC automatically recharges the storage capacitors as needed. The IC contains extensive protection circuitry to protect against input voltage overvoltage and under voltage, output voltage overload and short circuit, degraded storage capacitors, and thermal overload.

When ACT85610 detects input voltage drops below the programmed threshold, the eFuse is turned off and the supplement mode is activated to discharge the storage cap and provide power to the VBUS. The integrated buck converter works in synchronous mode and can provides up to 8A current.

The ACT85610 is highly integrated high voltage PMIC. There are four buck regulators and one boost regulator in the ACT85610. The four buck regulators are high voltage or “HV” buck regulators and can operate over a wide input voltage range of 2.7V to 14V.

The boost regulator can accept input voltages in the range of 2.5V to 14V also. The output voltage is configurable between 10.8V to 13.2V. The typical output voltage is in the 12.0V range for many SSD applications.

ACT85610 also has one mini buck and one mini LDO combined together to provide the power for internal blocks and gate driver. The best efficiency points for the PMIC in general are for input voltages higher than 5.0V as the gate drive to all switching regulators is the VCC output and the VCC output can regulate to 5.0V with input voltages higher than 5.0V. The target output voltage on the VCC output is 5.0V as the name implies. Driving the gate voltage of the internal power FETs in the switching regulators to the full 5.0V results in the best on-resistance possible for the power FETs in all of the internal regulators.

The IC communicates with the host processor via I2C and GPIOs. There are 6 available GPIO pins in ACT85610. These GPIOs allow a variety of functions to be implemented. They can be used as input type, open drain output type, or as analog input/output pins. The analog GPIOs also allow an analog comparator function where the input to the GPIO pin is compared against an internal reference voltage and the result can be output as an internal signal or can also be routed back through a second GPIO output pin.

In addition, the dedicated Power Loss Indicator (PLI) pin in ACT85610 automatically and immediately goes low to indicate a power loss condition. This gives the system advanced warning to complete all active tasks and shutdown. See the Pin Function section for additional PLI pin functionality.

These configurable options allow implementation of a variety of system functions and also allow flexibility of functions tied to each pin, thereby allowing pin changes and routing flexibility on the fly. Some examples of system functions that can be implemented are nRESET or Power Good (PG) output, interrupt request or interrupt pin (nIRQ), digital output controlled by the “power okay” (POK) signal from individual regulators, digital input to control power sequencing of internal regulators, digital

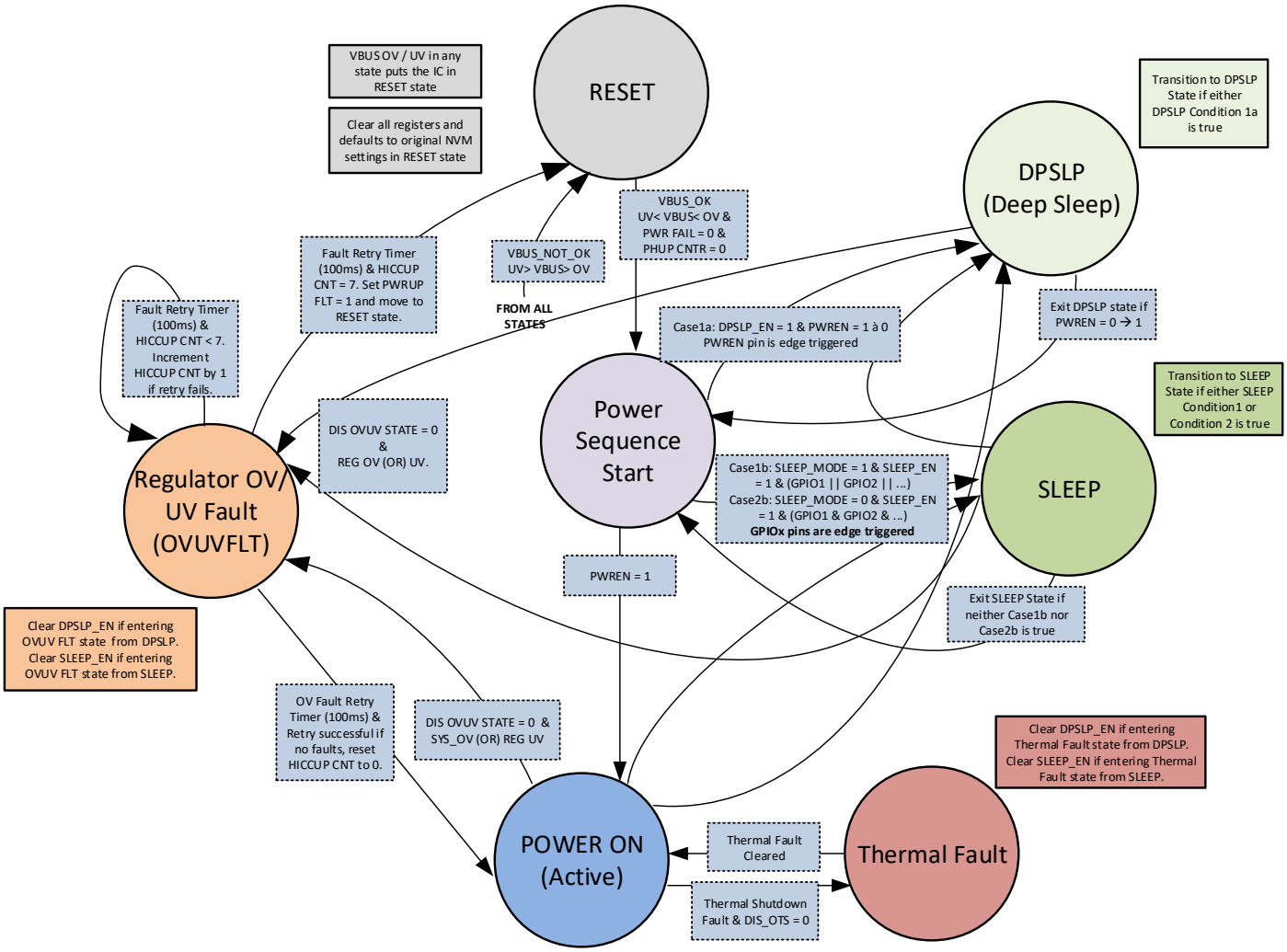
inputs/outputs to control external regulators, digital input used to enter or exit low power mode, input lines to monitor power good signals from external regulators, to control Dynamic Voltage Scaling (DVS) in BUCK regulators, and the ADC input.

The order of the regulator outputs turning ON or in other words - the “power on” sequence is fully configurable in the ACT85610. The same is true for the power OFF sequence. The dependency of each regulator output on other regulator outputs and the ON/OFF delays for each regulator can all be configured for each of the Buck regulators and the Boost regulator independently. The output voltages for each regulator is programmable via I^2C and the default value during power up can be changed by programming different settings during factory test – referred to as **CMI or Coding Matrix Index**. By changing the CMI program during factory testing, the default values during power up that control the power-on/off sequence, output voltage and current settings of regulators, fault detection settings, interrupt generation, GPIO functions and low power mode settings can all be factory programmed to specifically suit different applications. This allows tremendous flexibility to use the same device that can be configured differently in a variety of systems and applications. The PMIC can also control external regulators and can therefore seamlessly integrate and increase the number of power supplies. This can be done using the available GPIOs – the PMIC can therefore behave like a single but larger power management system by controlling both internal and external regulators and managing low power modes such as low power state and can thus eliminate the need for external logic or microcontrollers that may otherwise be needed for system power management or safety monitoring.

The default configuration values are also modifiable via I^2C commands and can therefore be altered by firmware at any time. As the PMIC is powering up, as soon as the external controller for the system powers up, I^2C access may be available and can be used to change the default power sequence or the default output voltages for the remaining regulators that are yet to turn on after the power supply for the main controller has been turned on. The power sequence after the main system controller has powered on can therefore be altered via firmware if required and this makes the system power management compatible to firmware upgrades. Firmware intervention or control is not necessary in most cases. This is especially true if the CMI is adjusted to the desired sequence and default settings during factory programming. Firmware overwrite and control is useful in cases where the unit cannot be re-programmed and adjustments / improvements can still be made with firmware updates.

In low power state, some or all of the regulator outputs can be turned OFF or change the voltage. The user has full control over which power supplies respond to the low power mode signal by using the LPM EN register bit that is available as a setting in each internal regulator of the ACT85610. The low power state should be viewed as configurable state that the user is allowed to configure. This state can be defined or altered each time before entering it or left unchanged from the default programmed state. If left unchanged, entering the state will result in the default behavior of the PMIC each time low power mode is activated. The default behavior for low power state is independently configurable and is usually different. Low power mode can also be configured differently before entering the state each time and this empowers the user to control and change the low power configuration by firmware in a variety of permutations and combinations. This gives the user immense control via firmware to configure the system low power state differently from the default configuration. The behavior can therefore be altered before each time one of these low power states is activated.

GPIO power sequencing (turning ON by GPIO input) shall have 0/2.5/5/10ms delay setting options. This fixed time delay, can be added to the rising edge transitions and can be added to each of GPIO outputs independently.



LEGEND

DPSLP_MODE: Factory NVM Register bit to choose AND/OR Function for DPSLP conditions.
SLEEP_MODE: Factory NVM Register bit to choose AND/OR Function for SLEEP conditions.
DPSLP_EN: Basic NVM Register bit that has to be factory programmed or set to 1 by I^2C to allow entry into DPSLP state.
SLEEP_EN: Basic NVM Register bit that has to be factory programmed or set to 1 by I^2C to allow entry into DPSLP state.
GPIO1,2,3...: One or more GPIO pins that are configured as control inputs for DPSLP or SLEEP states (single GPIO can control one of SLEEP or DPSLP states)

Figure 6: PMIC State Machine Diagram

STATE MACHINE DESCRIPTION

ACT85610 has several main states of operation, VIN UV/POR, eFuse Soft-start, eFuse Fully On, PMIC Sequence Start, Power On, Low Power Mode, PMIC Fault, Health Check and Supplement. And there are two fault shutdown states.

VIN UV/POR — this state is the first time power up, or when the input voltage is below the VIN_UV threshold. VIN_UV is set by register bits.

eFuse Soft-Start — this state is the eFuse in rush prevention turn on phase. It is using the VIN/VBUS and controlled by the SS capacitor.

eFuse Fully On — this state is when the PLP system is operating normally after powering up. The eFuse is fully on VBUS ≈ VIN during this state. The storage capacitor voltage is boosted to the set point if the charge Boost converter is programmed to operate after eFuse is fully on.

Health Check — this state is part of eFuse fully on state, it allows the storage cap to be regularly checked by build-in circuit.

Supplement — this state occurs when a fault condition is detect. Usually this is a power failure and the input voltage has dropped below the VIN_UV threshold. There are conditions that allow entry into this state.

1. VIN voltage below VIN_UV threshold
2. VIN voltage above the VIN_OV threshold which is set in register bits
3. Input voltage above the VIN_MAX threshold
4. eFuse current above the OC threshold
5. VIN – VBUS > 560mV
6. VBUS – VIN > 130mV

Supplement Disable — this state is when junction temperature is over 135°C, or abnormal on Boost cap charge regulator. The supplement function is disabled, IC will NOT provide power to VBUS if input is failed. The eFuse still stays on in this state.

PMIC Sequence Start — this state is when the eFuse is fully turned on, and there is no fault condition at the PLP stage, the PMIC start to power up with programmed sequence.

Power On — this state is when system is fully powered, all rails are on.

Low Power Mode — this state is when PMIC outputs turned off or changed voltage, which can be configured by GPIO or register bits.

PMIC Fault — this state is when PMIC outputs have OC/OV/UV conditions.

The eFuse, Boost converter, Buck convert, and ADC operation mode at each state are shown in below table.

Table 1: Operation States

Operation Conditions	eFuse	Blocking FET	PLP Boost	PLP Buck	PMIC	PLI	PG_STR	IC Action
Normal Operation	On	On	Enabled	Off	On	High	High	Boost Charges STR Cap as needed
Input OC Vin - Vbus< 560mV (t < 10us)	On	On	Enabled	Off	On	High	High	eFuse in LDO Mode
Input OC Vin - Vbus > 560mV	On → Off	On	Off	On	On	Low	High → Low	Enter Supplement Mode
VBUS Short	On → Off	On	Off	On → Off	Off	Low	High → Low	Enter Supplement Mode
Input Over Voltage	On → Off	On	Off	On	On	Low	High → Low	Enter Supplement Mode
Input Under Voltage	On → Off	On	Off	On	On	Low	High → Low	Enter Supplement Mode
Health Checking	On	On	Standby or turn of for recharge	Off	On	High	High	If failed, PS_STR and nIRQ go low
Low Power Mode	On	On	Enabled	Off	As configured	High	High	PMIC outputs are as programmed
120°C < Tj < 145 °C	On	On	Enabled	Off	On	High	High	Sends out thermal alert
145 °C < Tj < 155 °C	On	On	Off	Off	On	High	Depends on Vstr	PG_STG depends on Vstr
Tj > 155 °C	Off	Off	Off	Off	Off	Low	Low	IC is disabled

EFUSE

DESCRIPTION

The ACT85610 will perform as an eFuse for input transient voltage protector up to 20V. The internal eFuse FETs provides control for inrush current, protection for high input voltage transients, defense against short circuits, and blocks reverse current during power loss. This function is useful for hot-plugging environments when large transients occur due to the insertion and remove of large loads.

Input UV/OV

The ACT85610 senses VIN pin voltage to determine the IC on or off and enables supplement mode when input is failed. The internal precision comparator with hysteresis can be used to program a startup voltage higher than the normal UVLO value.

The ACT85610 has the hard coded UVLO voltage at 2.6V and OVLO at 14.4V. If the input voltage drops below 2.6V, IC will shut down. If the input voltage rises above 14.4V, IC will turn off eFuse and enter supplement mode.

The ACT85610 has the second programmable UV and OV threshold to determine when to turn on the device at start up and enter supplement mode if input voltage drops below UV threshold or too high that is over OV threshold.

The programmable separated VIN_UV_SEL [1:0] and VIN_OV_SEL [1:0] thresholds registers set the UV and OV reference voltage. The Actual UV and OV thresholds are the percentage of VIN_SEL as shown in the table below. Please note that the UV and OV can choose different value for better flexibility. For example,

the VIN_UV_SEL can be 7.5V and VIN_OV_SEL can be 12V.

Table 2: Input Voltage Selection

VIN_SEL [1:0]	Input Voltage
00	3.3V
01	5V
10	7.5V
11	12V

The VIN_UV threshold is the percentage of VIN_UV_SEL which is set by VIN_UV_2ND_PER [3:0] in register 0x2Dh [7:4] from range of 80% ~ 95% with 1% steps, as shown in table 3.

Table 3: Under Voltage Reference Settings

VIN_UV_2ND_PER [2:0]	UV Threshold (V)	
	VIN_UV_2ND_PER [3] = 0	VIN_UV_2ND_PER [3] = 1
000	80%	88%
001	81%	89%
010	82%	90%
011	83%	91%
100	84%	92%
101	85%	93%
110	86%	94%
111	87%	95%

The VIN_OV threshold is the percentage of VIN_OV_SEL which is set by VIN_OV_2ND_PER [3:0] in register 0x30h [7:4] from range of 106% ~ 120% with 1% steps, as shown in table 4.

Table 4: Over Voltage Reference Settings

VIN_OV_2ND_PER [2:0]	OV Threshold (V)	
	VIN_OV_2ND_PER [3] = 0	VIN_OV_2ND_PER [3] = 1
000	Disabled	113%
001	106%	114%
010	107%	115%
011	108%	116%
100	109%	117%
101	110%	118%
110	111%	119%
111	112%	120%

eFuse Current Limit Setting

ACT85610 eFuse function will limit the inrush current by setting the capacitance for the soft start time. It also has the maximum current limit function, the maximum current value and this limit is set by the ISET[3:0] register bits.

Table 5: eFuse Current Limit Settings

ISET [2:0]	ISET [3] = 0	ISET [3] = 1
000	1.5A	9A
001	2A	10A
010	3A	11A
011	4A	12A
100	5A	12A
101	6A	12A
110	7A	12A
111	8A	12A

When the eFuse current is over the ISET threshold, eFuse will work at linear mode to limit the current and the VBUS voltage drops. After 10us, the eFuse will turn off to avoid overheat. The eFuse will also turn off if the VIN to VBUS exceeds 560mV.

In the condition that the eFuse current rises fast such as VBUS short condition, eFuse needs to react quickly to turn off. A second level over current protection is implement as well. The OC thresholds are set by EFUSE_OC SETTING [1:0] in register 0x2Ch [3:2]. When eFuse current rises above the OC threshold, eFuse turns off immediately and enter supplement mode.

Table 6: eFuse Over Current Protection Threshold

EFUSE_OC SETTING [1:0]	OC Threshold
00	6.5A
01	10.5A
10	14.5A
11	18.5A

Soft-Start

The voltage on the SS pin controls the start-up of the eFuse output. This regulates the internal feedback voltage to the voltage on the SS pin. The SS pin can be used to program an external soft-start function or to allow output of the eFuse to track another supply during start-up. The device has an internal pull-up current source of 5μA (typical) that charges an external soft-start capacitor to provide a linear ramping voltage at the SS pin. Regulating the internal feedback voltage to the voltage on the SS pin, allows the output to rise smoothly from 0V to its final voltage. The soft-start capacitance can be calculated by below equation:

$$C_{SS}(nF) = \frac{65 \times T_{SS}(mS)}{V_{BUS}(V)} \qquad \text{Equation 1}$$

Where the T_{SS} is the soft-start time, and the VBUS is the output voltage.

SUPPLEMENT BUCK REGULATOR

Description

The supplement Buck regulator is voltage mode, synchronous PWM step-down converters that achieves peak efficiencies of up to 95%. The Buck minimizes noise in sensitive applications and allowing the use of small external components. Additionally, the buck is available with a variety of standard and custom output voltages and may be software-controlled via the I2C interface for systems that require advanced power management functions.

The Buck operation frequency can be factory-set from 562 kHz, 1.125 MHz, 1.5 MHz, and 2.25 MHz which allows the system to be optimized at different applications.

In supplement mode operation, the Buck can be disabled by set FORCE_PWROFF = 0.

Buck Output Voltage Range

Output voltage for the Buck regulator can be programmed by BK_VOUT_SET [6:0] in register 0xCBh [6:0] from 2.5V to 13.2V with 100mV step.

Table 7: Supplement Buck Output Voltage

VBUS [4:0]	ISET [6:5] =			
	00	01	10	11
00000	2.5	5.7	8.9	12.1
00001	2.6	5.8	9.0	12.2
00010	2.7	5.9	9.1	12.3
00011	2.8	6.0	9.2	12.4
00100	2.9	6.1	9.3	12.5
00101	3.0	6.2	9.4	12.6
00110	3.1	6.3	9.5	12.7
00111	3.2	6.4	9.6	12.8
01000	3.3	6.5	9.7	12.9
01001	3.4	6.6	9.8	13.0
01010	3.5	6.7	9.9	13.1
01011	3.6	6.8	10.0	13.2
01100	3.7	6.9	10.1	13.2
01101	3.8	7.0	10.2	13.2
01110	3.9	7.1	10.3	13.2
01111	4.0	7.2	10.4	13.2
10000	4.1	7.3	10.5	13.2
10001	4.2	7.4	10.6	13.2
10010	4.3	7.5	10.7	13.2
10011	4.4	7.6	10.8	13.2
10100	4.5	7.7	10.9	13.2
10101	4.6	7.8	11.0	13.2
10110	4.7	7.9	11.1	13.2
10111	4.8	8.0	11.2	13.2
11000	4.9	8.1	11.3	13.2
11001	5.0	8.2	11.4	13.2
11010	5.1	8.3	11.5	13.2
11011	5.2	8.4	11.6	13.2
11100	5.3	8.5	11.7	13.2
11101	5.4	8.6	11.8	13.2
11110	5.5	8.7	11.9	13.2
11111	5.6	8.8	12.0	13.2

Protection

The Buck converter has several protection mechanisms to insure safe operation. It stops operation when input voltage from storage cap reaches STR_UVLO (2.9V); or the output voltage drops below power good threshold; or the output voltage is above the over voltage threshold. The output under-voltage protection can be masked so Buck converter still can run at 100% duty cycle mode even the output voltage is lower than UV threshold.

A cycle by cycle current limit is also implemented in Buck converter. The current limit threshold ILIMSET can be factory-set from 3A to 10A. When the current is over the 22.5% of ILIMSET, the converter is shutdown.

Table 8: Factory-set Buck Current Limit

BK_CLIM[2:0]	ILIMSET (A)
000	3
001	4
010	5
011	6
100	7
101	8
110	9
111	10

100% Duty Cycle Operation

The Buck regulator is capable of operating at up to 100% duty cycle. During 100% duty cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage for applications.

The Buck should be able to operate in 100% duty cycle mode if the input voltage drops below set output voltage to full utilize the storage cap energy.

Compensation

The Buck regulator utilizes external compensation placed on the COMP pin. The compensation of the design is required; simply follow a few simple guidelines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A ceramic capacitor is recommended for the Buck regulator in most applications.

Output Capacitor Selection

The Buck regulator is designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR. The Buck regulator is designed to operate with 44uF output capacitor over most of their output voltage ranges, although more capacitance may be desired depending on the duty cycle and load step requirements.

Two of the most common dielectrics are Y5V and X5R. Whereas Y5V dielectrics are inexpensive and can provide high capacitance in small packages, their capacitance varies greatly over their voltage and temperature ranges and are not recommended for DC/DC applications. X5R and X7R dielectrics are more suitable for output capacitor applications.

Inductor Selection

The Buck regulator utilizes voltage-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with 1.5uH inductors at 1500kHz operation. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%.

Operation Frequency

The optional Buck operation frequency is selectable between 562 kHz, 1.125 MHz, 1.5 MHz, and 2.25 MHz by BK_FREQ [1:0] register, REG 0x10[7:6]. The frequency is also limited by the storage voltage, please see the below table.

Table 9: Recommended Supplement Buck Operation Frequency

STR voltage	Frequency max
<18V	2.2Mhz
18V-25V	1.5Mhz
25V-31V	1.125Mhz

STORAGE BOOST REGULATOR

General Description

The Storage regulator provides the ability to store charge on a bank of capacitors by boosting the voltage and has a programmable output voltage. This will maintain the storage voltage as long as the input supply is available. This regulator is an asynchronous boost regulator. When switched to supplemental mode the storage regulator is turned off. The boost output is set using internal registers.

Operating Mode

By default, the storage boost regulator operates in peak current mode, non-fixed frequency mode.

The peak switch current can be programed by register BST_ILIM [1:0] as shown in table below.

Table 10: Boost Peak Current Settings

BST_ILIM [1:0]	(mA)
00	250
01	500
10	950
11	1500

Set Storage Capacitor Voltage

The desired storage capacitor voltage can be set by BST_VSET [7:0] in register 0xCAh in the range of 5.5V ~ 31V with 100mV steps.

Table 11: Storage Cap Voltage Settings

BSTV_SET [4:0]	BST_VSET [7:5]							
	000	001	010	011	100	101	110	111
00000	5.5	8.7	11.9	15.1	18.3	21.5	24.7	27.9
00001	5.6	8.8	12.0	15.2	18.4	21.6	24.8	28.0
00010	5.7	8.9	12.1	15.3	18.5	21.7	24.9	28.1
00011	5.8	9.0	12.2	15.4	18.6	21.8	25.0	28.2
00100	5.9	9.1	12.3	15.5	18.7	21.9	25.1	28.3
00101	6.0	9.2	12.4	15.6	18.8	22.0	25.2	28.4
00110	6.1	9.3	12.5	15.7	18.9	22.1	25.3	28.5
00111	6.2	9.4	12.6	15.8	19.0	22.2	25.4	28.6
01000	6.3	9.5	12.7	15.9	19.1	22.3	25.5	28.7
01001	6.4	9.6	12.8	16.0	19.2	22.4	25.6	28.8
01010	6.5	9.7	12.9	16.1	19.3	22.5	25.7	28.9
01011	6.6	9.8	13.0	16.2	19.4	22.6	25.8	29.0
01100	6.7	9.9	13.1	16.3	19.5	22.7	25.9	29.1
01101	6.8	10.0	13.2	16.4	19.6	22.8	26.0	29.2
01110	6.9	10.1	13.3	16.5	19.7	22.9	26.1	29.3
01111	7.0	10.2	13.4	16.6	19.8	23.0	26.2	29.4
10000	7.1	10.3	13.5	16.7	19.9	23.1	26.3	29.5
10001	7.2	10.4	13.6	16.8	20.0	23.2	26.4	29.6
10010	7.3	10.5	13.7	16.9	20.1	23.3	26.5	29.7
10011	7.4	10.6	13.8	17.0	20.2	23.4	26.6	29.8
10100	7.5	10.7	13.9	17.1	20.3	23.5	26.7	29.9
10101	7.6	10.8	14.0	17.2	20.4	23.6	26.8	30.0
10110	7.7	10.9	14.1	17.3	20.5	23.7	26.9	30.1
10111	7.8	11.0	14.2	17.4	20.6	23.8	27.0	30.2
11000	7.9	11.1	14.3	17.5	20.7	23.9	27.1	30.3
11001	8.0	11.2	14.4	17.6	20.8	24.0	27.2	30.4
11010	8.1	11.3	14.5	17.7	20.9	24.1	27.3	30.5
11011	8.2	11.4	14.6	17.8	21.0	24.2	27.4	30.6
11100	8.3	11.5	14.7	17.9	21.1	24.3	27.5	30.7

11101	8.4	11.6	14.8	18.0	21.2	24.4	27.6	30.8
11110	8.5	11.7	14.9	18.1	21.3	24.5	27.7	30.9
11111	8.6	11.8	15.0	18.2	21.4	24.6	27.8	31.0

Output Capacitor Selection

The storage regulator is designed to take advantage of the benefits of both super capacitors or bulk capacitors. The storage capacitors can be electrolytic, polymer, Tantalum, ceramic, super capacitors, or a combination of these.

Output Power Good Selection

The storage capacitor power good signal indicates whether the capacitor voltage is over the threshold or not. This threshold can be programmed by register HMON_THR [3:0]. This threshold is also used for storage capacitor health checking.

Table 12: Storage Capacitor PG Threshold

HMON_THR[2:0]	**HMON_THR[3]**	
	0	**1**
000	90.5%	94.5%
001	91.0%	95.0%
010	91.5%	95.5%
011	92.0%	96.0%
100	92.5%	96.5%
101	93.0%	97.0%
110	93.5%	97.5%
111	94.0%	98.0%

Storage Cap Discharge

In order to discharge the storage residual energy in the evaluation test, when the VIN or VBUS power off, the internal 50mA sink current can be activated to discharge the storage cap until reaches storage UV. It is configurable in the NVM register whether the discharge is automatic every time or single shot.

When ACT85610 enters power loss protection mode, the supplement turns on to provide power for system. In proper design, the energy stored in the storage cap should be more than system back up needed. Therefore, when system back up is done, the Buck converter should still run and there's still energy in storage cap, the voltage on storage cap can be potential high as well. Since system will not draw high current anymore, it will take long time before storage cap or Buck reaches UV threshold. In order to speed up system re-startup process, ACT85610 has the storage cap and VBUS discharge function that can be activated through I2C command or GPIO so system activate the discharge process after back up is done.

The DISCHARGE_ALL in register 0xEBh [1] is used to activate the discharge process by I2C. The default value of this register bit is 0. Set this bit to 1 will put the IC in turn off sequence. If a GPIO is preferred, then the EN_GPIO_DISCHARGE_ALL in register 0xEBh [2] needs to be set to 1, pull the GPIO low will put the IC in the turn off sequence.

Below is a typical process for the discharge:

1. Buck starts for supplement
2. System back up is done in SSD drive
3. Write DISCHARGE_ALL =1 or pull one GPIO low with EN_GPIO_DISCHARGE_ALL = 1. The GPIO is configured as output discharge function.
4. Supplement Buck stop running and supplement mode ends
5. Boost is disabled
6. Blocking FET is off
7. VSTR and VBUS will be discharged by 50mA pull down.
8. When VSTR & VBUS voltage down to low level the discharge circuit have no voltage room to run, then the discharge current will reduce. DISCHARGE_DONE=1 when the current hits 10mA.

9. After discharge done, the register that store “DISCHARGE_ALL” command will be clear and IC come back VIN_UV_POR state.
10. Soft start starts again

Be noted that, once IC enter discharge all state then if we plug VIN then IC will continue discharge until DISCHARGE_DONE=1 and IC start up again.

Blocking FET

The blocking FET is an internal MOSFET that provides isolation between the system output voltage (VBUS) and the storage capacitors. It provides system level fault tolerance that allows the system to continue operating normally in the event of a storage capacitor failure. During the blocking FET soft start, the blocking FET provides constant current to charge the storage capacitors. This current is programmable between 150mA and 500mA, and it is valid when the storage capacitor voltage is lower than the VBUS voltage. The blocking FET stays in soft start until the voltage across it (VBUS-VSPL) approaches 0V. After soft start is complete, the blocking FET turns on fully and the current limit is automatically set to 2A.

During startup, the constant current source linearly charges up the storage capacitors. If the storage capacitors are not charged up to VIN within 250ms, the IC assumes there is a fault condition and turns the blocking FET off for 250ms. It then retries to startup. This hiccup mode minimizes power dissipation and IC temperature with very large storage capacitance or with fault conditions. The BFET_HIC_OPTION register sets the number of times the BFET retries to startup into a fault condition. When BFET_HIC_OPTION[]=1 (0x34[0]) the BFET only tries to startup one time. If unsuccessful, the IC moves to SHUTDOWN1 state. If BFET_HIC_OPTION = 0, the BFET continues to restart indefinitely. With extremely large storage capacitors such as supercapacitors and BFET_HIC_OPTION[]=0 the blocking FET will turn on and off at a 250ms period. This is expected functionality and minimizes the power dissipation in the IC.

In normal operation, when the blocking FET is fully turned on, it applies power to the boost converter, allowing the storage capacitors to charge up to their final value. When the IC enters supplement mode, the buck output power flows into the VSPL pin, through the blocking FET, and out of VBUS to the system.

The blocking FET limits a storage capacitor overload or short circuit condition to 2A. The blocking FET immediately turns off when its current reaches 2A. This causes the voltage at VSPL to drop and the IC generates a VSPL undervoltage fault and pulls nIRQ low. After 250ms, the blocking FET turns back on. If the fault has cleared, it enters softstart again. If the fault if still present, it immediately turns off again. Hiccup mode applies to both normal startup with very large storage capacitors and to short circuit conditions. Note that the IC enters the SUPPLEMENT-DISABLE state during both startup and short circuit conditions.

During this condition, the eFuse stays on and system continues to operate normally, even with a short circuit on VSPL or the storage capacitor.

The blocking FET can be manually turned on and off by the EN_BFET bit in register 0xEBh [0] with 0x34[1] = 1.

Note that disabling the blocking FET also disables the boost converter. This allows systems to startup faster by keeping the boost disabled until the system is up and running.

STORAGE CAP HEALTH MONITOR

GO/NO GO Test

The ACT85610 has an internal health monitor for the storage capacitors. It will apply a constant 10mA for a selected period then followed by 50mA current for 200us and monitor that the STR. If the voltage falls below a predetermined level (HMON_THR), a fault will be indicated on the PG_STR.

With MCU control using the I2C the parameters of the time the current source is applied can be adjust to account for different capacitors and the monitoring can be triggered on demand to avoid any critical system operations.

When the ACT85610 is in autonomous health checking mode, the boost is activated just before the health check to ensure the storage capacitor is topped off. Then when the current source is applied the boost will be

locked out. The HMON_THR is monitored only while the current source is on, and if the STR voltage falls below it, then a fault is latched and the PG_STR and nIRQ are set low. When the set time has expired, then the boost will be turned back on to replace the charge removed from the storage capacitor.

The routine health checking time is every 4 minutes. It can be factory-set to every 8 minutes or 16 minutes. Customer can also choose single shot test as needed.

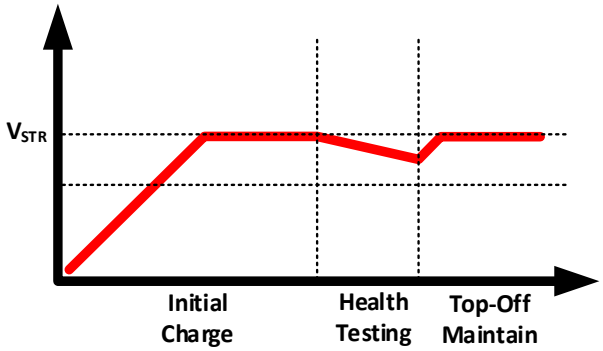


Figure 7: Storage Voltage at Different Stages

The health check discharge time can be set by register HMON_TSET [3:0], as shown in table 6. This also allows the use of the ADC to check the slope of the discharge and calculate the capacitance.

Table 13: Health Check Discharge Time

HMON_TSET[2:0]	HMON_TSET[3] (ms)	
	0	1
000	2	512
001	4	768
010	8	1024
011	16	1280
100	32	1536
101	64	1792
110	128	2048
111	256	2304

Storage Capacitance Read

ACT86510 also has the feature to read out the storage capacitance. Each time IC enter health check state, after finishing GO / NO GO health checking, IC will automatically measure storage capacitance. If the cap voltage after GO /NO GO checking is lower than HMON_THR threshold then the boost will activate to charge the cap voltage to STR_PG then start to capacitance read. If the GO / NO GO checking is passed and cap voltage is still higher HMON_THR threshold, then IC starts capacitance read without activating boost to charge the cap.

ACT85610 use the 10mA current sink to discharge the storage cap and monitoring the cap voltage until the delta voltage drops to 1V. Based on the discharge time, ACT85610 calculate the capacitance and store the value in CAP_VALUE [12:0] in register 0xE0h [7:3] and 0xE4h [7:0].

The maximum capacitance can be read is 8.191mF because of there are only 13 register bits. Any larger capacitance will return in 0x1FFF.

There's a 5s timer for the total time of GO / NO GO checking and capacitance read. If the timer expires, IC always jump back to NORMAL state.

HIGH VOLTAGE STEP-DOWN DC/DC REGULATORS

General Description

BUCK1,2,3,4 are high voltage regulators and use a proprietary topology based on a Constant ON Time (COT) architecture. They are synchronous step-down converters that use a hysteretic constant on time mode that allows it to achieve low quiescent current during stand-by operation. The regulators can achieve high peak efficiencies higher than 95% under some operating conditions. Typical efficiency depends on input and output voltage conditions and also on load current. The HV buck regulators are highly configurable with many configurable parameters including switching frequency. They allow the use of small external components while emulating a constant frequency PWM mode regulator during continuous current mode operation under high load current situations. Additionally, all regulators are

available with a variety of standard and custom output voltages and may be software-controlled via the I²C interface for systems that require advanced power management functions.

100% Duty Cycle Operation

The HV buck regulators are capable of operating at NEARLY 100% duty cycle but NOT fully 100% mode owing to the minimum off time needed for the Constant on Time hysteretic mode architecture. The maximum duty cycle limit is about 95% but is also a function of selected switching frequency and operating conditions such as input and output voltage and the load current. A minimum off time is needed for controlling and bounding the frequency of operation for the switching regulators. During high duty cycle operation, the high-side power MOSFETs are held on continuously for the majority of the time as the constant on-time scales according to the ratio of Vout/Vin. This prolongs the high-side on time for high duty cycle cases and keeps the high-side on for nearly 100% of the time, thus providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout. However, the HS switch will need to turn off for at least the minimum off time, every switching cycle and thereby limits the overall duty cycle to less than 100%.

Operating Mode

By default, the BUCK regulators operate in a pseudo fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary COT mode at light loads in order to improve efficiency at light loads.

Synchronous Rectification

Each BUCK regulator features an integrated synchronous rectifier (or LS FET), maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Soft-Start

The BUCK regulators include an internal soft-start ramp which limit the rate of change of the output voltage, minimizing input inrush current and ensuring that the output powers up in a monotonic manner that is independent of current load on the outputs. This circuitry is effective any time the regulator is enabled, as well as during retry after responding to a short-circuit or other fault condition and helps control the inrush current during power up.

Dynamic Voltage Scaling

Dynamic Voltage Scaling (DVS) is supported through the I²C interface. Two voltage settings are available for configuration in each Buck regulator. When DVS is enabled, the regulator transitions from VSET0 to the VSET1 setting and returns back to VSET0 during normal operation (DVS is off). During DVS, the regulator may be forced into a “forced PWM” mode in which the zero-cross comparator may be ignored. This is to ensure that the output reaches the new set point as quickly as possible when the output capacitor needs to be discharged. This helps in particular, when the new output voltage setting is lower than the previous setting and the output discharge rate depends on the output load current. In this case the output would otherwise drift down as the load discharges the output capacitor slowly instead of tracking the regulation point due to the forced PWM operation. When the output voltage register setting is changed via the I²C, the digital logic in the regulator will step the output setting through each step between the initial and final settings. When the register values in the VSET [] register bits (See Register Map for BUCK regulators) is changed, the control logic steps the code between the previous and current settings and while this transition occurs, the OV and UV of the regulators are ignored so as to avoid triggering any false OV or UV faults inadvertently.

Output Pull Down Resistor

Each output has two options of discharge resistance to discharge the output voltage when the Bucks are off. Host can select between 6Ω and 20Ω. The discharge function can be disabled as well.

Enable / Disable Control

During normal operation, each BUCK regulator may be enabled or disabled via the I²C interface by writing to the regulator's ON [ ] bit. With a discharge function, the output can be discharged when the regulator is disabled (discharge enabled) through an internal resistor or pull-down path.

POK [ ] and Output Fault Interrupt

Each regulator features a Power-OK (POK) status bit that can be read by the system microprocessor via the I²C interface. If an output voltage is lower than the power-OK threshold, typically ~10.0% below the programmed regulation voltage, that regulator's POK [ ] bit will be 0.

If a DC/DC's nFLTMSK [-] bit is set to 1, the ACT85610 will interrupt the processor if the DC/DC's output voltage falls below the Power-OK (POK) threshold. In this case, the nIRQ pin (interrupt request pin) will assert low and remain asserted until either the regulator is turned off or back in regulation, and the POK [ ] bit has been read via I2C. The POK interrupt will be cleared upon read, provided that the POK = 0 condition does not persist and a read operation is performed.

Compensation

The buck regulators utilize a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components such as the inductor and output capacitor. While selecting these external components, the peak inductor current ripple, input and output voltage conditions, efficiency requirements and expected load conditions must be considered.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 10µF ceramic capacitor is recommended for each regulator in most applications.

Output Capacitor Selection

The buck regulators were designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR capacitors. The buck regulators are designed to operate with 44uF output capacitor over most of their output voltage ranges, although more capacitance may be desired depending on the load current requirements of the regulator as well as the duty cycle, ripple and the desired load step response. In addition, low power mode behavior and discharge time of the output capacitors, when experiencing bursts of load current intermittently, are also important criteria that can determine the value of output capacitors selected. Voltage de-rating that is more common and significant in small package sizes such 0402 should be carefully considered when choosing output capacitors. This is especially true with higher output voltages in which case there is a larger voltage bias on the output capacitors.

Two of the most common dielectrics are Y5V and X5R. Whereas Y5V dielectrics are inexpensive and can provide high capacitance in small packages, their capacitance varies greatly over their voltage and temperature ranges and are not recommended for DC/DC applications. X5R and X7R dielectrics are more suitable for output capacitor applications.

Inductor Selection

All BUCK regulators utilize a Constant on Time and a hysteretic mode hybrid topology and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. The regulators in ACT85610 are optimized for operation with inductors in the 0.47uH to 2.2µH range. It is best to choose inductors with a low DC-resistance or DCR for higher efficiency and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum inductor peak current by at least 30%. Additionally, the inductor peak-to-peak current ripple must be carefully considered along with the selected switching frequency before selecting appropriate inductor values with adequate current rating.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Ground shielding the output or feedback traces to the PMIC is recommended. Care must be taken by kelvin (star) connecting the feedback points for precise voltage regulation. In general, the output capacitors should be placed closest to the

point of load and the feedback trace connected directly to the capacitors. High frequency bypass caps can be added to improve ripple and dynamic response to fast transients. Placing the inductor close to the PMIC is a good practice and minimizing currents in the ground plane that can cause ground current loops is important.

Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as close as possible to the IC while avoiding the use of vias as much as possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple via. The output node for each regulator should be connected to its corresponding feedback/output pin (on the PMIC) through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Shielding the feedback traces with ground traces can help as stated earlier. Finally, the exposed pad should be directly connected to the backside ground plane using multiple via to achieve low electrical and thermal resistance.

BUCK Output Voltage Range

Buck 1/2/3 output voltage for the internal buck regulators can be programmed in 20mV steps from 0.6V to 5.26V or 5mV steps from 0.6V to 1.875V.

Table 14: HV Buck Regulator Output Voltage Settings for BUCKS 1/2/3/4 with 20mV steps

BUCK_VSET [4:0]	BUCK_VSET [7:5]							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
0 0000	0.6	1.24	1.88	2.52	3.16	3.8	4.44	5.08
0 0001	0.62	1.26	1.9	2.54	3.18	3.82	4.46	5.1
0 0010	0.64	1.28	1.92	2.56	3.2	3.84	4.48	5.12
0 0011	0.66	1.3	1.94	2.58	3.22	3.86	4.5	5.14
0 0100	0.68	1.32	1.96	2.6	3.24	3.88	4.52	5.16
0 0101	0.7	1.34	1.98	2.62	3.26	3.9	4.54	5.18
0 0110	0.72	1.36	2	2.64	3.28	3.92	4.56	5.2
0 0111	0.74	1.38	2.02	2.66	3.3	3.94	4.58	5.22
0 1000	0.76	1.4	2.04	2.68	3.32	3.96	4.6	5.24
0 1001	0.78	1.42	2.06	2.7	3.34	3.98	4.62	5.26
0 1010	0.8	1.44	2.08	2.72	3.36	4	4.64	
0 1011	0.82	1.46	2.1	2.74	3.38	4.02	4.66	
0 1100	0.84	1.48	2.12	2.76	3.4	4.04	4.68	
0 1101	0.86	1.5	2.14	2.78	3.42	4.06	4.7	
0 1110	0.88	1.52	2.16	2.8	3.44	4.08	4.72	
0 1111	0.9	1.54	2.18	2.82	3.46	4.1	4.74	
1 0000	0.92	1.56	2.2	2.84	3.48	4.12	4.76	
1 0001	0.94	1.58	2.22	2.86	3.5	4.14	4.78	
1 0010	0.96	1.6	2.24	2.88	3.52	4.16	4.8	

1 0011	0.98	1.62	2.26	2.9	3.54	4.18	4.82	
1 0100	1	1.64	2.28	2.92	3.56	4.2	4.84	
1 0101	1.02	1.66	2.3	2.94	3.58	4.22	4.86	
1 0110	1.04	1.68	2.32	2.96	3.6	4.24	4.88	
1 0111	1.06	1.7	2.34	2.98	3.62	4.26	4.9	
1 1000	1.08	1.72	2.36	3	3.64	4.28	4.92	
1 1001	1.1	1.74	2.38	3.02	3.66	4.3	4.94	
1 1010	1.12	1.76	2.4	3.04	3.68	4.32	4.96	
1 1011	1.14	1.78	2.42	3.06	3.7	4.34	4.98	
1 1100	1.16	1.8	2.44	3.08	3.72	4.36	5	
1 1101	1.18	1.82	2.46	3.1	3.74	4.38	5.02	
1 1110	1.2	1.84	2.48	3.12	3.76	4.4	5.04	
1 1111	1.22	1.86	2.5	3.14	3.78	4.42	5.06	

Table 15: HV Buck Regulator Output Voltage Settings for BUCKS 1/2/3/4 with 5mV steps

BUCK_VSET [4:0]	BUCK_VSET [7:5]							
	000	001	010	011	100	101	110	111
0 0000	0.6	0.76	0.92	1.08	1.24	1.4	1.56	1.72
0 0001	0.605	0.765	0.925	1.085	1.245	1.405	1.565	1.725
0 0010	0.61	0.77	0.93	1.09	1.25	1.41	1.57	1.73
0 0011	0.615	0.775	0.935	1.095	1.255	1.415	1.575	1.735
0 0100	0.62	0.78	0.94	1.1	1.26	1.42	1.58	1.74
0 0101	0.625	0.785	0.945	1.105	1.265	1.425	1.585	1.745
0 0110	0.63	0.79	0.95	1.11	1.27	1.43	1.59	1.75
0 0111	0.635	0.795	0.955	1.115	1.275	1.435	1.595	1.755
0 1000	0.64	0.8	0.96	1.12	1.28	1.44	1.6	1.76
0 1001	0.645	0.805	0.965	1.125	1.285	1.445	1.605	1.765
0 1010	0.65	0.81	0.97	1.13	1.29	1.45	1.61	1.77
0 1011	0.655	0.815	0.975	1.135	1.295	1.455	1.615	1.775
0 1100	0.66	0.82	0.98	1.14	1.3	1.46	1.62	1.78
0 1101	0.665	0.825	0.985	1.145	1.305	1.465	1.625	1.785
0 1110	0.67	0.83	0.99	1.15	1.31	1.47	1.63	1.79
0 1111	0.675	0.835	0.995	1.155	1.315	1.475	1.635	1.795
1 0000	0.68	0.84	1	1.16	1.32	1.48	1.64	1.8
1 0001	0.685	0.845	1.005	1.165	1.325	1.485	1.645	1.805
1 0010	0.69	0.85	1.01	1.17	1.33	1.49	1.65	1.81
1 0011	0.695	0.855	1.015	1.175	1.335	1.495	1.655	1.815
1 0100	0.7	0.86	1.02	1.18	1.34	1.5	1.66	1.82
1 0101	0.705	0.865	1.025	1.185	1.345	1.505	1.665	1.825
1 0110	0.71	0.87	1.03	1.19	1.35	1.51	1.67	1.83
1 0111	0.715	0.875	1.035	1.195	1.355	1.515	1.675	1.835
1 1000	0.72	0.88	1.04	1.2	1.36	1.52	1.68	1.84
1 1001	0.725	0.885	1.045	1.205	1.365	1.525	1.685	1.845
1 1010	0.73	0.89	1.05	1.21	1.37	1.53	1.69	1.85
1 1011	0.735	0.895	1.055	1.215	1.375	1.535	1.695	1.855
1 1100	0.74	0.9	1.06	1.22	1.38	1.54	1.7	1.86
1 1101	0.745	0.905	1.065	1.225	1.385	1.545	1.705	1.865
1 1110	0.75	0.91	1.07	1.23	1.39	1.55	1.71	1.87
1 1111	0.755	0.915	1.075	1.235	1.395	1.555	1.715	1.875

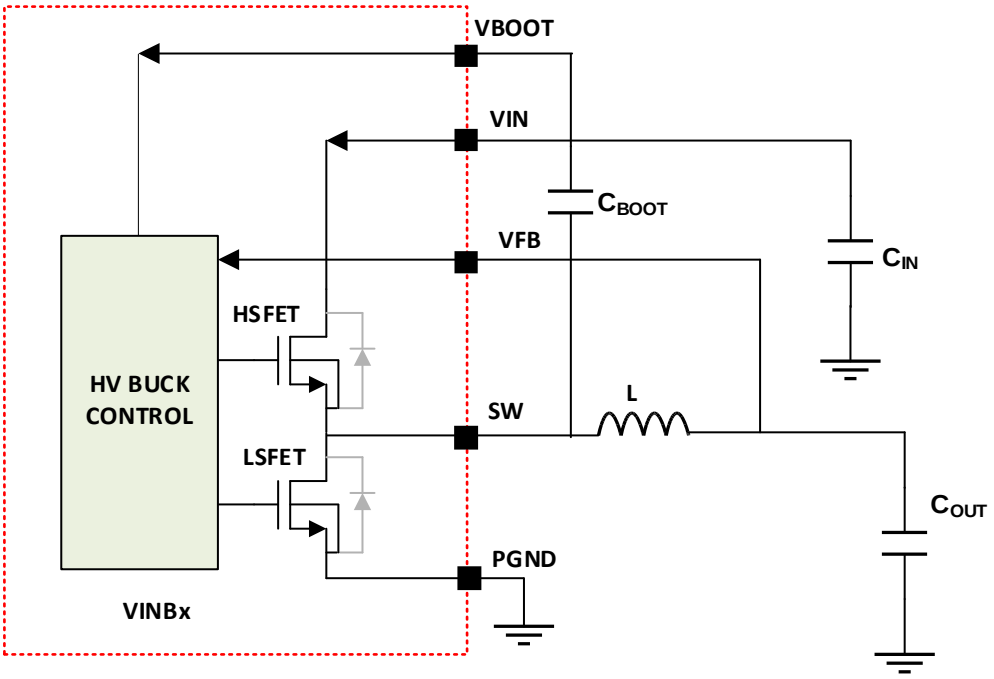


Figure 8: Buck Regulator Output Voltages

BOOST REGULATOR

General Description

The Boost regulator provides the ability to drive a high output voltage up to 13.2V and up to a maximum load current of 1.2A. The regulator is designed to use inductor values of 4.7uH or 6.8uH and has a switching frequency of 1125 kHz. By selecting a suitable value of inductor and an appropriate output capacitor, the regulator provides options to allow optimization of the regulator efficiency, output ripple and dynamic transient response under switched load conditions.

The output of the boost regulator can be set in the range of 10.8V to 13.2V. The output voltage can be configured in of 50mV steps. The Boost regulator has the cycle by cycle current limit on the lows side FET (LSFET) to prevent the over current condition.

Table 16: Boost Regulator Output Voltage Settings

Boost VSET [3:0]	Boost VSET [6:4]			
	000	001	010	011
0000	10.80	11.60	12.40	13.20
0001	10.85	11.65	12.45	
0010	10.90	11.70	12.50	
0011	10.95	11.75	12.55	
0100	11.00	11.80	12.60	
0101	11.05	11.85	12.65	
0110	11.10	11.90	12.70	
0111	11.15	11.95	12.75	
1000	11.20	12.00	12.80	
1001	11.25	12.05	12.85	
1010	11.30	12.10	12.90	
1011	11.35	12.15	12.95	
1100	11.40	12.20	13.00	
1101	11.45	12.25	13.05	
1110	11.50	12.30	13.10	
1111	11.55	12.35	13.15	

VCC Regulator

ACT85610 has the 5V output Buck VCC regulator to power the internal blocks and can provide 100mA max current for external circuit. VCC node is supplied by a mininBuck & mininLDO. miniBuck regulates at 5V while the miniLDO regulates at 4.5V. When VBUS >2V then miniLDO will turn on to pull VCC higher than VCC_UVLO (2.6V). At that time, if VBUS> 3.5V then miniBuck will also turn on parallelly with the miniLDO to stronger support VCC. In the case VBUS >5V then miniBuck will regulate VCC to 5V > miniLDO's regulation (4.5V) so the miniLDO will automatically no longer supply any curent to VCC. However if VCC down to 4.5V then miniLDO will work again to prevent VCC drop more. miniLDO always works but the miniBuck can be set off by set 0x34[4]=1. Once the bit set to 1, VCC will be regulated to 4.5V by the miniLDO.

VCC regulator It is also the input source for the LDO.

At 3.3V or 5V input, the output VCC pin is recommended to tie to VBUS. However if we hard connect VCC to VBUS, noise due to PMIC_BUCK running can also affect to VCC. It is better to turn off miniBuck and turn on miniLDO in this case or connect VBUS to VCC through 0.1Ohm. Pass device of miniLDO or 0.1Ohm combine with cap at VCC will make a low pass filter to limit high frequency noise at VBUS so keep VCC more clean.

For miniBuck, a 10uH inductor is recommended with over 500mA current rating.

LDO

ACT85610 has a built in LDO. When the input is 3.3V and VCC pin is connected to VBUS, the maximum output current is 300mA. When the Buck VCC is in switching mode, the maximum output current is 50mA.

The output range of LDO is from 0.6V to 3.75V with 50mV steps.

Table 17: LDO Output Voltage

LDOx_VSET[3:0]	LDOx_VSET[5:4]			
	00	01	10	11
0000	0.60	1.40	2.20	3.00
0001	0.65	1.45	2.25	3.05
0010	0.70	1.50	2.30	3.10
0011	0.75	1.55	2.35	3.15
0100	0.80	1.60	2.40	3.20
0101	0.85	1.65	2.45	3.25
0110	0.90	1.70	2.50	3.30
0111	0.95	1.75	2.55	3.35
1000	1.00	1.80	2.60	3.40
1001	1.05	1.85	2.65	3.45
1010	1.10	1.90	2.70	3.50
1011	1.15	1.95	2.75	3.55
1100	1.20	2.00	2.80	3.60
1101	1.25	2.05	2.85	3.65
1110	1.30	2.10	2.90	3.70
1111	1.35	2.15	2.95	3.75

ADC

General Description

The ACT85610 contains a built-in analog to digital converter, ADC, which can be used to monitor eight system level parameters. These include input voltage, VBUS voltage, storage capacitor voltage, eFuse current, Buck 1 output voltage, GPIO1&2 A2D inputs, and die temperature. It is a single 12 bit delta-sigma ADC that uses an analog input multiplexer to select one of eight channels for the A/D conversion. For better accuracy, the last 2 LSB are not used for calculation. The resulting digital results are stored in eight digital registers. An eight to one multiplexer connects one of the ADC output registers to the user accessible register map.

ADC Configuration

The ACT85610 ADC is configured through the I^2C interface. It is enabled and disabled by the EN_ADC register bit. The ADC has two conversion modes, manual single-shot conversion and automatic polling conversion.

Single-Channel Conversion

Configure the IC for single-channel conversion mode by setting the following I²C bits in register 0xE8h

ADC_ONE_SHOT = 1.

ADC_CH_SCAN = 0

EN_ADCBUF = 1

In single channel mode, the user defines the input channel to be converted and then manually initiates the ADC conversion. I²C bits ADC_CH_CONV [2:0] in register 0xE8h select the input channel to be converted. ADC_CH_READ [2:0] selects the ADC channel to be read. These should be set to the same channel. The user initiates an ADC read by writing a 1 into EN_ADC in register 0xE8h. When ADC conversion is complete, the ADC_DATA_READY bit (register 0xE7h [7]) is set to 1, nIRQ is asserted low, and EN_ADC automatically changes back to 0. The uP can then read the status bits to find that the ADC conversion is complete. The ADC data are stored in ADC_DOUT [13:6] in register 0xE5h for 8 MSB and in ADC_DOUT [5:0] in register 0xE6h for 6 LSB. The last 2 LSB data are not used for value calculation for better accuracy. nIRQ stays asserted low and the ADC_READY_BIT stays equal to 1 until the ADC data is read. Reading the ADC data automatically deasserts nIRQ. To initiate another ADC conversion for the same channel, set EN_ADC=1. To initiate an ADC conversion for another channel, change ADC_CH_CONV and ADC_CH_READ to the appropriate channel and then set EN_ADC=1.

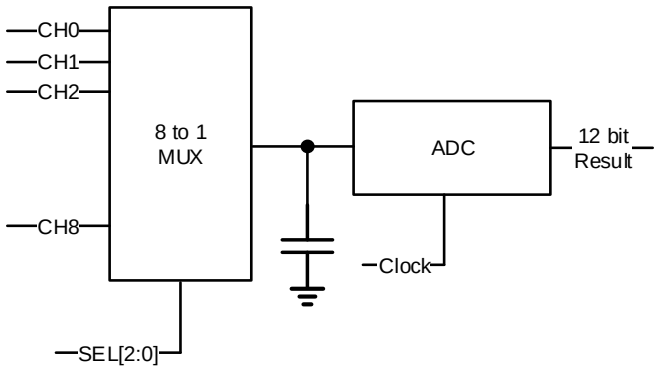


Figure 9: ADC Block Diagram

Multiple Channel Conversion

Configure the IC for multiple channel conversion by setting the following I²C bits in register 0xE8h

ADC_ONE_SHOT = 1

ADC_CH_SCAN = 1

EN_ADCBUF = 1

Start a conversion by changing EN_ADC to 1. This reads and stores the ADC results for all channels. After the conversion is complete, set ADC_CH_SCAN = 0. Define the channel to be read with the ADC_CH_CONV [2:0] bits in register 0xE8h and then read the ADC_DOUT values. Change ADC_CH_CONV to read additional channels.

ADC Value Calculation

Table 17 shows how to calculate the values of each channel with the 12-bit ADC data. Where for CH0 input current measurement, the V_Isense is the value that related with input current limit ISET [3:0]. Table 18 shows the setting. The DOUT_25 is the die temperature ADC value at 25C and stored at 0x23[3:0] as 4 MSB and 8 LSB at 0x24[7:0].

Table 18*: ADC Channel Value Calculation*

Channel	Channel Description	ADC_CH_CONV[2:0]	ADC_CH_READ[2:0]	Value
CH0	Input Current	000	000	IIN = (DOUT-2048)*1.531*1e-3/V_Isense (A)
CH1	Input Voltage (bit 0x32[5]=0)	001	001	VIN = (DOUT-2048)*0.0245 (V)

CH2	Storage Cap Voltage	010	010	VSTR = (DOUT-2048)* 0.0245 (V)
CH3	Output Voltage	011	011	VOUT = (DOUT-2048)* 0.0245 (V)
CH4	Die Temperature	100	100	Temp = (DOUT- DOUT_25)/(DOUT_25-2048)*298 +25 (C)
CH5	Buck 1 Output	101	101	VBK1 = (DOUT-2048)* 0.004593 (V)
CH6	A2D GPIO Input 1	110	110	VGPIO1 = (DOUT-2048)* 0.00153125 (V)
CH7	A2D GPIO Input 2	111	111	VGPIO2 = (DOUT-2048)* 0.00153125 (V)

ADC_offset = (-1)^Reg0x2E[7]*BIN (Reg0x2E[6:0])

Gain_Error = (-1)^Reg0x2F[5] * BIN (Reg0x2F[4:0])

Dout= 16 * BIN(Reg0xE5[7:0]) + BIN(Reg0xE6[5:2])

Dout_final = 2048 + (Dout - ADC_offset - 2048) * (1+Gain_Error/1000)

Table 19: V_Isense vs ISET

ISET[2:0]	V_Isense (V/A)	
	ISET[3] = 0	ISET[3] = 1
000	0.533	0.089
001	0.400	0.080
010	0.267	0.073
011	0.200	0.067
100	0.160	0.067
101	0.133	0.067
110	0.114	0.067
111	0.100	0.067

Input Power Monitoring

ACT85610 can monitoring the input power by measuring input voltage and current with the ADC. The resulting power calculation should be accurate to withing 5% with an input current of 1.5A.

For input power measurement, need to measure input current & VIN separately then calculate input power by multiple them together.

To achieve better accuracy, when measure the input power, the MSE_POWER bit in register 0x32h [5] needs to be set 1, the voltage divider for VIN is switched to trimmed divider. The divider is trimmed to compensate all error for input voltage and input current.

Set MSE_POWER = 0 when just measure VIN by ADC. No TRIM divider will be used in this case.

For furthermore accurate input power measurement, host can do input current conversion first, then followed by input voltage, and then the input current again. The two input current values can be averaged which will be very close to the instantaneous input current.

Anti-Aliasing Filter

In order to prevent the aliasing interference when measuring the input power. An anti-aliasing filter is added for input voltage and input current, and GPIO A2D inputs with bypass switch option so the AAF can be bypassed if not needed.

GPIO Configuration

ACT85610 has 6 GPIOs that can be used as digital/analog input and open-drain output. These GPIOs allow a variety of functions to be implemented. These configurable options allow implementation of a variety of system functions and also allow flexibility of functions tied to each pin, thereby allowing pin changes and routing flexibility on the fly. Some examples of system functions that can be implemented are regulator enable (PWREN), system reset signal output (nRESET) , Power Good (PG) output, interrupt request or interrupt pin (nIRQ), digital output controlled by the “power okay” (POK) signal from individual regulators, digital input to control power sequencing of internal regulators, digital inputs/outputs to control external regulators (EXT_EN),

input lines to monitor power good signals from external regulators (EXT_PG), to control Dynamic Voltage Scaling (DVS) in Buck regulators, enable signal for the storage cap Boost charger and blocking FET (ENB), open drain output for storage cap voltage power good (STR_PG) and VBUS (VB_PG), storage cap discharge enable, and the analog input for internal ADC (A2D), Buck output power good.

When configured as an input, each GPIO can be independently configured with 200kΩ pullup resistor to an internal 1.8V supply. Set I^2C register bit GPIOx_Pullup_Enable = 1 to enable the pullup resistor.

Regulators On/OFF Enable– PWREN

PWREN is a logic input that can be used to control the regulators power on/off and DVS. When PWREN pulled low, the configured rails can be turned off and some Buck rail will change the output voltage to different setting (DVS). It will be a convenience way to put the system in low power mode.

If PWREN pin pulls low, the configured rails will not turned on until the PWREN pin pulls high.

Alternately, an always-on mode is also possible with the ACT85610, where the PWREN input is not required to start the power-on sequence or to power up the system. After power up, PWREN can be used to put the IC in low power mode.

nIRQ

ACT85610 has the interrupt pin to inform the host any fault happens. In general anything with a status change the IRQ is inserted. The status changes can be masked by set the corresponding register bits. If the IRQ is set the fault must be read before it clears the IRQ. If the fault remains the IRQ will remain set.

The below status changes will set the IRQ:

- Input over-voltage, under-voltage
- Thermal warning, thermal shutdown
- eFuse VIN to VBUS over limits
- eFuse current warning and limit
- Storage capacitor over-voltage, under-voltage
- Supplemental mode active
- Buck operation faults
- Buck under-voltage shutdown
- VCC under-voltage
- ADC data is ready
- Any buck regulator exceeding peak current limit for 16 cycles after soft start or a UV/OV condition.
- Any regulator exceeding current limit for more than 20uS after soft start or a UV/OV condition.
- Watch Dog timer expiring.

If any of these status changes that is not desired to trigger the nIRQ, they can be masked in the register bit.

nRESET

The nRESET is an open drain 5V compatible output used to issue the main reset to the CPU/controller used in the system. The output monitors the input voltage and valid regulator outputs to trigger a reset if input or said regulator output voltage is not valid. The nRESET delay time is controlled by the TRST_DLY [1:0] control bits. Programmable delay time from 20ms, 40ms, 60ms, and 100ms. The nRESET is essentially also the same as a Power Good (PG) function but with a fixed delay after all the supply rails are up and settled to the correct level.

The nRESET output signal is typically tied to all regulators whose outputs are necessary for the system controller and I/Os to function properly. Configurable register bits in each regulator determine if the regulator's POK signal is allowed to control the nRESET output signal or not. In general, the behavior of the nRESET output is such that the nRESET output is low if any one of the Power Okay (POK) signals from the controlling regulators is low. In other words, if any one of the controlling regulator outputs is not okay, the nRESET output will be low and will not assert high. The POK signal for any regulator can be low only when the regulator is enabled and the output is not regulating at normal levels. Any regulator that is disabled will not affect the nRESET signal even if it's POK signal were configured to control the nRESET output. This is because, the POK signal from any regulator that is disabled is high and can only be low or "not okay" if the regulator is enabled but the output is not at the target regulation voltage. When a

regulator is enabled, it has a soft-start and it typically takes time as the output is ramped to the final regulation voltage. The POK signal is therefore typically low only from the time when a regulator is enabled (enable to the regulator goes high) to the time when the output ramps toward the final value and reaches 90% or higher of the final output voltage. The POK signal should go high if the output reaches a value greater than ~90% of the final value after it is enabled.

Besides of the PMIC output that trigger the RESET, the STR_PG is another signal that triggers. All the trigger signals need to be programmable to determine whether it is the gating item for RESET.

Enable

GPIO can be configured as Enable for the IC. When Enable pin is asserted, IC will back to POR state and stays there until it is de-asserted, even the VIN is valid. When this pin is de-asserted, IC states the soft start process, with optional 0 or 125ms delay time.

Another option when the Enable pin is asserted is that instead of enter POR state, IC can enter supplement mode state.

This pin is used to hard reset the IC back to the POR state and re-start up from whatever prior states. All the registers will be reset to default as well when this pin is asserted.

Ideally, the polarity of this pin can be configurable for active high or active low. When it is set at active high, it should be compatible with 1.8V or 3.3V voltage level.

OPERATION

Watch-Dog Supervision

The ACT85610 features a watchdog supervisory function. An internal watchdog timer of 4s is unmasked by setting either WDSREN [ ] or WDPCEN [ ] bit to one. WDSREN stands for Watch Dog Soft Reset Enable and WDPCEN stands for Watch Dog Power Cycle Enable. Once enabled, the watchdog timer is reset whenever there is I^2C activity for the PMIC. In the case where the system software stops responding and that there is no I^2C transactions for 8s, the watchdog timer expires. As a result, the PMIC either performs a soft-reset or power cycle, depending on whether WDSREN [ ] or WDPCEN [ ] bit is set. The watch dog timer can be enabled as necessary and is disabled by default.

Software-Initiated Power Cycle

ACT85610 supports software-initiated power cycle. Once the MR register bit is set in the Master Tile, the PMIC waits for 8ms and then initiate a power cycle to restart the system.

SDA & SCL

The input pins for the I2C are SDA and SCL. The SDA is an input and open drain output, and requires a pull-up resistor. That pull-up resistor is typically tied to the MCU IO voltage. The IO voltage can range from 1.8V to 5.0V. So care must be taken to make sure the input buffers can handle that range and not shoot-thru with current when being driven.

A lower voltage rail on the input buffers, or a comparator may be required to prevent the shoot-thru current from being a DC bias.

I2C Passcode

The IC implements a special register passcode that enables I2C write transactions. This prevents accidental register changes. Enable I2C write functionality by writing a value of 0xAAh to register 0x0Ah (Unlock Register Key). Change this register to any other value to prevent accidental changes to the I2C register values. Both PMIC and PLP has its passcode independently

Thermal Alert and Shutdown

The ACT85610 sets the THERMAL_ALERT register bit and asserts nIRQ when the temperature is over 120°C. If the die temperature is over 145°C, the Boost and Buck converters are disabled. THERMAL_PWRDWN register bit and nIRQ are asserted. If the die temperature is over 155°C, all circuits are disabled. THERMAL_SHUTDWN register bit and nIRQ are asserted. It resumes when the temperature has dropped by 15°C.

APPLICATION INFORMATION

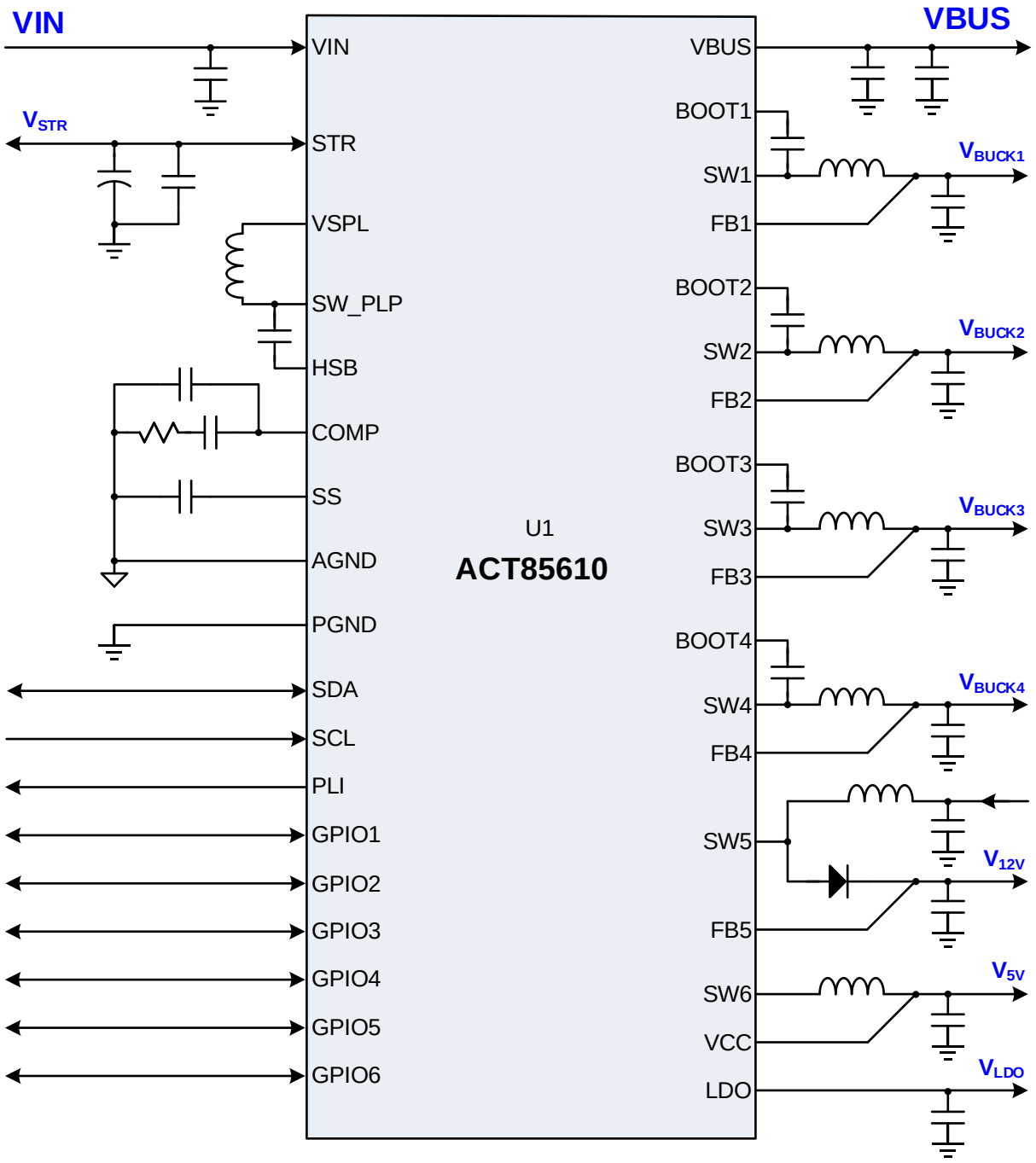


Figure10: Application Schematic (12V Input)

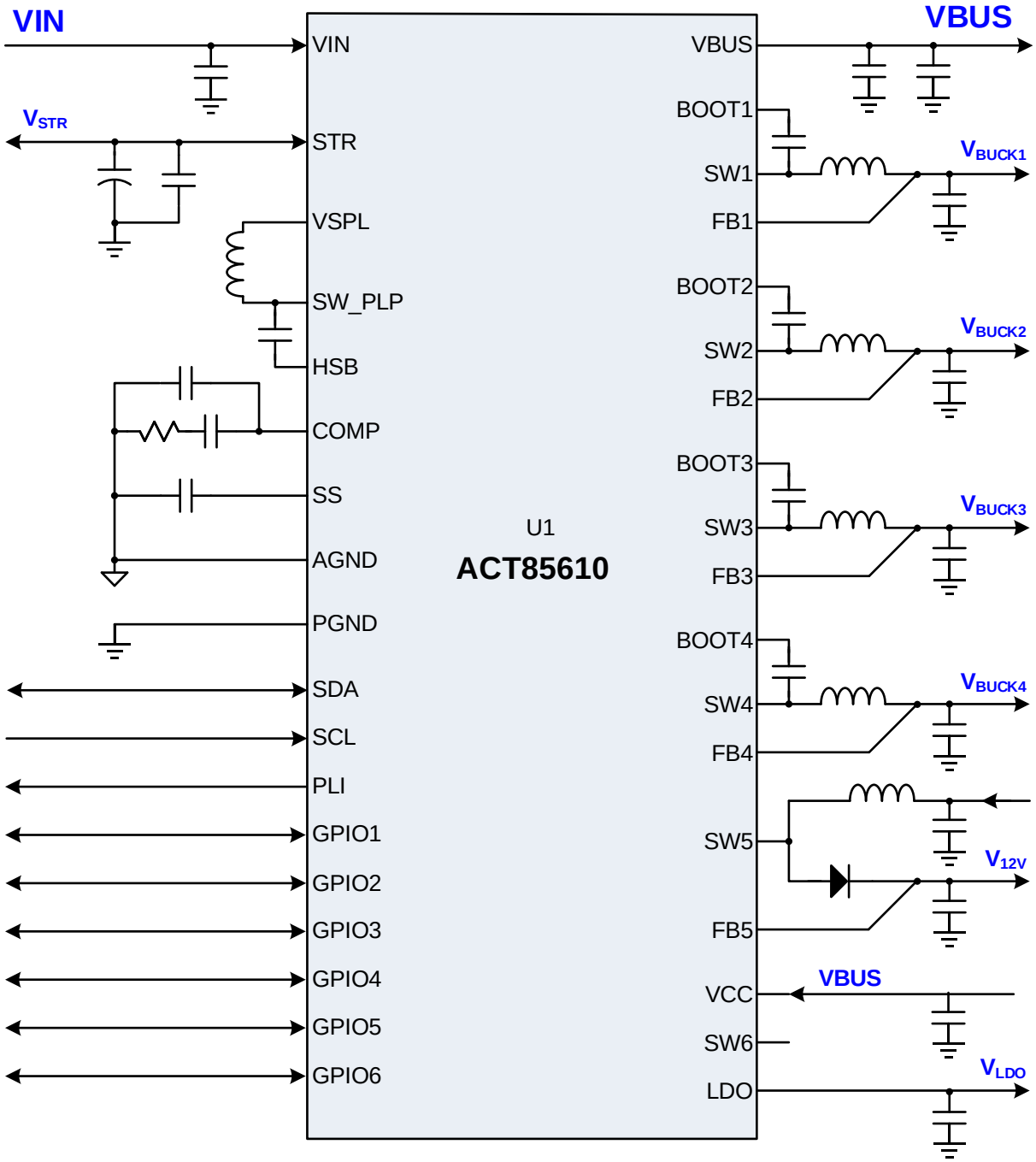


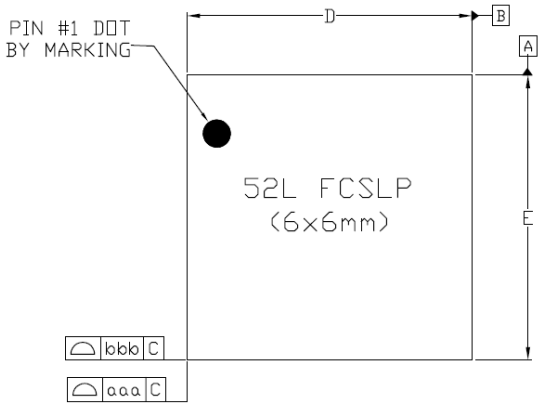
Figure 11: Application Schematic (3.3V and 5V Input)

LAYOUT RECOMMENDATION

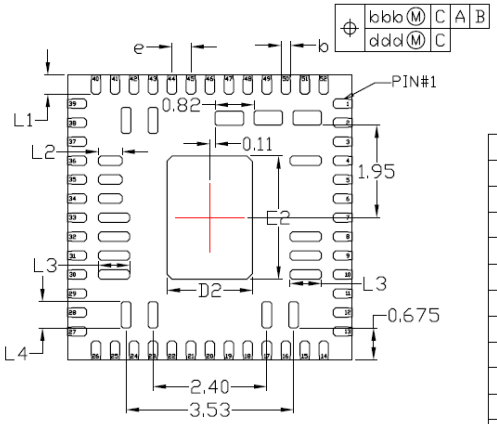
High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors.

Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as close as possible to the IC, and avoiding the use of via if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple via. The output node for each regulator should be connected to its corresponding FBx pin through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple via to achieve low electrical and thermal resistance.

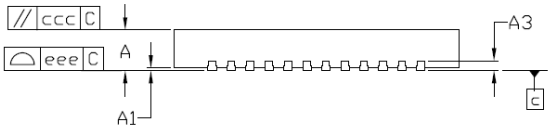
QFN-52 PACKAGE OUTLINE AND DIMENSIONS



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	---	---	0.050
A3	0.203 Ref.		
D	5.950	6.000	6.050
E	5.950	6.000	6.050
D2	1.750	1.800	1.850
E2	2.550	2.600	2.650
b	0.150	0.200	0.250
e	0.400 BSC		
L1	0.350	0.400	0.450
L2	0.450	0.500	0.550
L3	0.610	0.660	0.710
L4	0.500	0.550	0.600
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Notes

1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)