ACT8700

Rev PrA 08/2006

Advanced Product Information—All Information Subject to Change

FOUR CHANNEL INTEGRATED POWER MANAGEMENT IC FOR HANDHELD PORTABLE EQUIPMENT

FEATURES

- **Four Integrated Regulators**
  - **350mA PWM Step-Down DC/DC**
  - **500mA PWM Step-Down DC/DC**
  - **Step-Up DC/DC for WLED Bias**
  - **Complete Li+ Battery Charger**
- **Minimal External Components**
- **4x4mm, Thin-QFN44-24 (TQFN) Package**

APPLICATIONS

- **Portable Media Players**
- **Digital Camera Modules**
- **GPS Receivers**
- **PDAs**

ACT8700 contains circuitry with multiple patents pending.

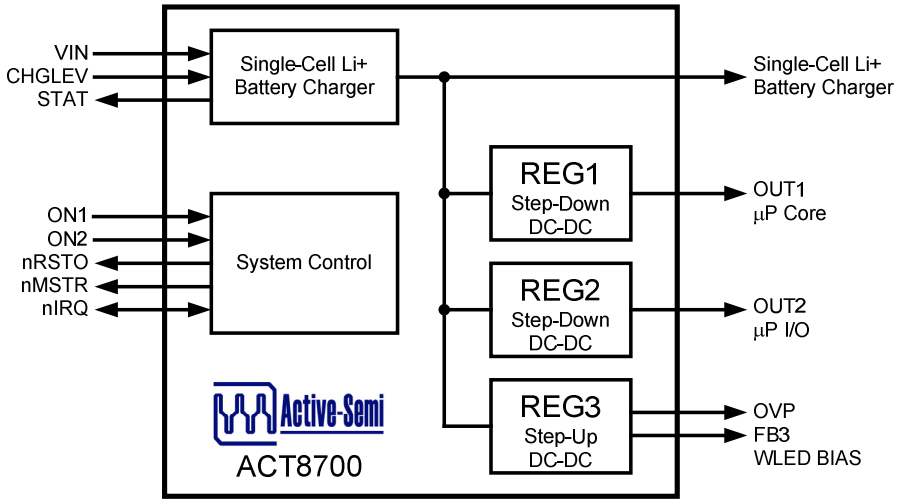
GENERAL DESCRIPTION

The ACT8700 is a complete, cost-effective *ActivePMU*™ power management solution with multiple patents pending for portable handheld equipment. This device integrates all four regulators required for small portable devices — two step-down DC/DCs for processor core and I/O power, a step-up DC/DC for WLED bias, and a complete, stand-alone Li+ battery charger — into a single, space-saving package.

REG1 and REG2 are fixed-frequency, current-mode PWM step-down DC/DC converters that are capable of supplying up to 350mA and 500mA, respectively. REG1 and REG2 are available with a variety of factory-preset output voltage combinations. REG3 is a fixed-frequency, step-up DC/DC converter that provides efficient display backlight bias to a string of up to six white-LEDs. Finally, the ACT8700 also contains a complete, thermally-regulated, stand-alone single-cell Li+ charger.

The ACT8700 is available in a tiny 4mm x 4mm 24-pin Thin-QFN package that is just 0.75mm thick.

SYSTEM BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS①

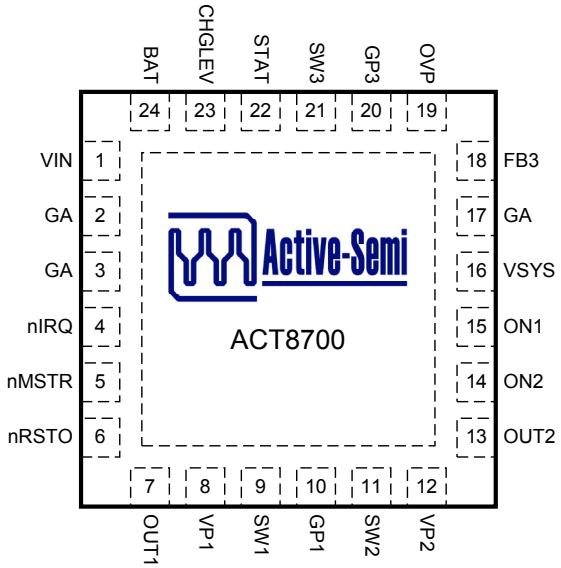
PARAMETER	VALUE
VP1, VP2 to GP1	-0.3V to +6.5V
VSYS, VIN, OUT1, OUT2, BAT to GA	-0.3V to +6.5V
OVP to GA	-0.3V to +30V
CHGLEV, STAT, ON1, ON2, nRSTO, nMSTR, nIRQ to GA	-0.3V to +6.5V
SW1 to GP1, SW2 to GP2, SW3 to GP3	-0.3V to +6.5V
SW1 to VP1, SW2 to VP2	-6.5V to +0.3V
GP1, GP2, GP3 to GA	-0.3V to +0.3V
RMS Power Dissipation (T_A=70ºC)②	TBDW
Operating Temperature Range	-40°C to 85°C
Junction Temperature	125°C
Storage Temperature	-55°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

②: Derate TBDmW/ºC above T_A=70ºC)

PIN CONFIGURATION

TOP VIEW



THIN QFN (TQFN)

ORDERING INFORMATION

PART NUMBER	V_{OUT1}	V_{OUT2}	PACKAGE	PINS	TEMPERATURE RANGE
ACT8700xxx-001	1.8V	3.0V	TQFN44	24	-40ºC to 85ºC
ACT8700xxx-002	1.5V	3.0V	TQFN44	24	-40ºC to 85ºC

Contact Active-Semi for custom REG1 and REG2 output voltage combinations.

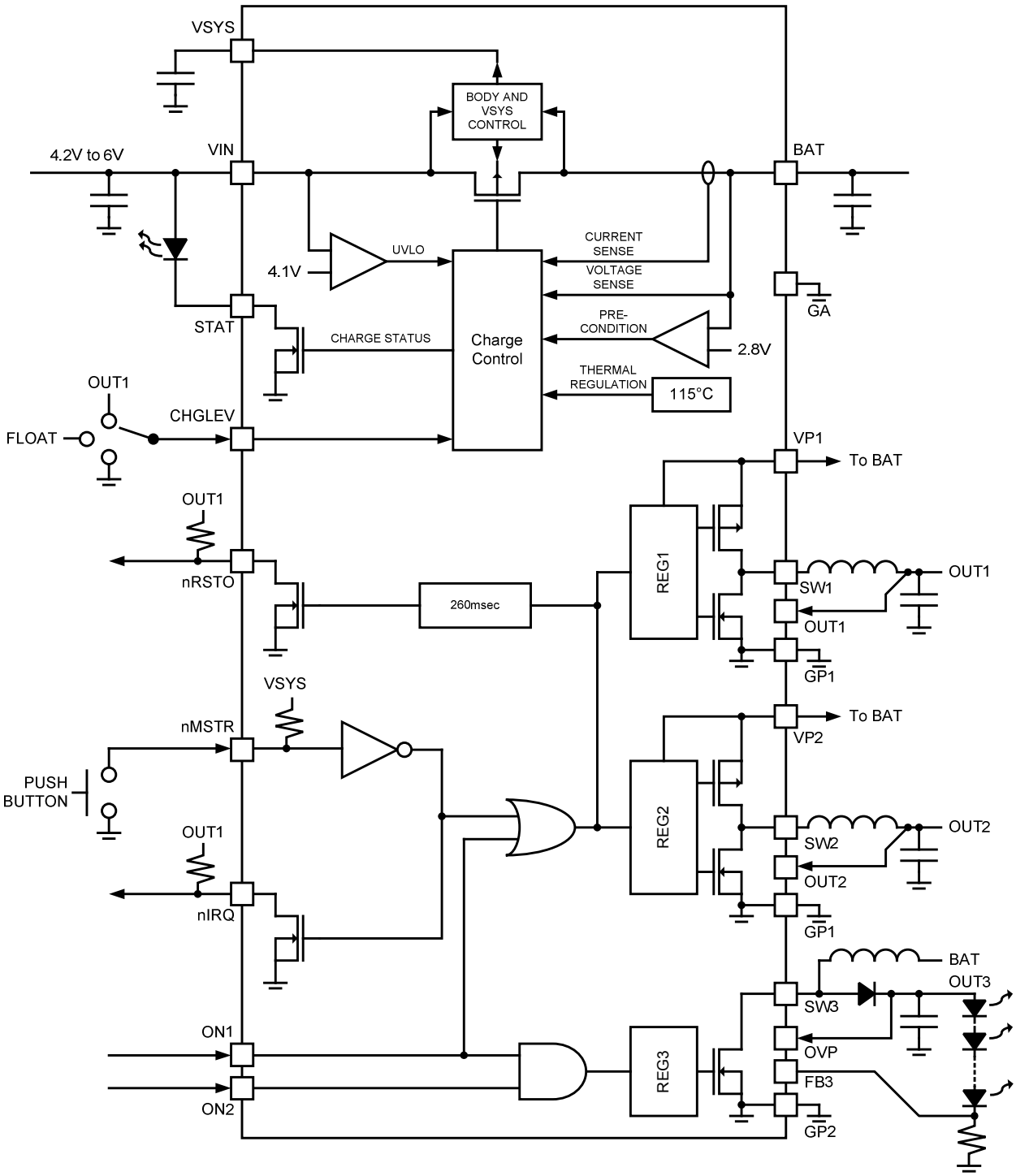
PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	VIN	Power Input for the Battery Charger. The Battery Charger is automatically enabled whenever a valid voltage is present on VIN. Bypass to GA with a high quality ceramic capacitor placed as close as possible to the IC.
4	nIRQ	Open-Drain Interrupt Output. nIRQ is an open-drain interrupt output which asserts when nMSTR is asserted. See the *System Startup & Shutdown* section for more information.
5	nMSTR	Master Enable Input. Drive nMSTR to GA or to a logic low to enable the ACT8700. Refer to the System Startup & Shutdown section for more information.
6	nRSTO	Open-Drain Push-Button Status Pin. nRSTO asserts low for the programmed reset timeout period of 260msec whenever the ACT8700 is enabled.
7	OUT1	Output Sense for REG1. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
8	VP1	Power Input for REG1. Bypass to PG1 with a high quality ceramic capacitor placed as closely as possible to the IC.
9	SW1	Switching Node Output for REG1. Connect this pin to the switching end of the inductor.
10	GP1	Power Ground for REG1 and REG2. Connect GA, GP1, and GP3 together at a single point as close to the IC as possible.
11	SW2	Switching Node Output for REG2. Connect this pin to the switching end of the inductor.
12	VP2	Power Input for REG2. Bypass to PG1 with a high quality ceramic capacitor placed as close as possible to the IC.
13	OUT2	Output Sense for REG2. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
14	ON2	Enable Control Input for REG3. ON2 is functional only when ON1 is driven high, ON2 has no affect when ON1 is driven low. Drive ON2 to VSYS or to a logic high for normal operation, drive to GA or a logic low to disable REG3. See the System Startup & Shutdown section for more information.
15	ON1	Enable Control Input for REG1 and REG2. Drive ON1 to VSYS or to a logic high for normal operation, drive to GA or a logic low to disable REG1 and REG2. Driving ON2 high also enables the ON2 input. See the System Startup & Shutdown section for more information.
16	VSYS	Power Input for System Management Circuitry. Bypass to GA with a high quality ceramic capacitor placed as close as possible to the IC.

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
2,3,17	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP1, and GP3 together at a single point as close to the IC as possible.
18	FB3	Feedback Sense for REG3. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
19	OVP	Overvoltage Protection Intput for REG3. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
20	GP3	Power Ground for REG3. Connect PG3 directly to a power ground plane. Connect GA, GP1, GP2, and GP3 together at a single point as close to the IC as possible.
21	SW3	Switching Node Output for REG3. Connect this pin to the switching end of the inductor.
22	STAT	Active-Low Open-Drain Charger Status Output. STAT sinks current when that charger is actively charging the battery, and goes high-Z whenever the charge is terminated. When active, STAT limits its sink current to 8mA (typ), allowing it to directly drive an indicator LED. To produce a logic-level output, connect STAT to VSYS through a resistor.
23	CHGLEV	Tri-State Charging State Select Input. Drive CHGLEV to VSYS or to a logic high for high-current charging (maximum charge current of 500mA), drive to GA or a logic low to for low-current charging (maximum charge current of 100mA). Allowing CHGLEV to float ($\|I_{CHGLEV}\|$ < 5μA) to disable the charger.
24	BAT	Output Sense for the Battery Charger. Connect this pin directly to the battery anode to connect the internal feedback network to the battery.
-	EP	Exposed Pad. Must be soldered to ground on PCB.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{SYS} = 3.6V, T_A = 25°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VSYS Operating Voltage Range	VSYS	2.6		5.5	V
VSYS UVLO Threshold	VSYS Voltage Rising	2.3	2.4	2.5	V
VSYS UVLO Hysteresis	VSYS Voltage Falling		100		mV
VSYS UVLO Delay	VSYS Rising		0.1		mV
	VSYS Falling		5		mV
Oscillator Frequency		1.4	1.7	2.0	MHz
VSYS Supply Current	ON1=ON2=GA, CHGLEV = floating		TBD		µA
Voltage Reference		1.24	1.25	1.26	V
Voltage Tracking Ramp Slew Rate			1		V/msec
Logic High Input Voltage	ON1, ON2			1.4	V
Logic Low Input Voltage	ON1, ON2	0.4			V
Logic Low Output Voltage	nIRQ, nRSTO, I_{SINK} = 10mA			0.3	V
Leakage Current	nIRQ, nRSTO, V = 4.2V			1	µA
nRSTO Delay		TBD	260		msec
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis	Temperature falling		20		°C

FUNCTIONAL DESCRIPTION

General Description

The ACT8700 offers a wide array of system management functions that allow it to be configured for optimal performance in a wide range of applications.

Master Clock Frequency

The ACT8700 utilizes a high-frequency 1.7MHz oscillator that is used by each of the regulators.

Enable / Disable Inputs (ON1 and ON2)

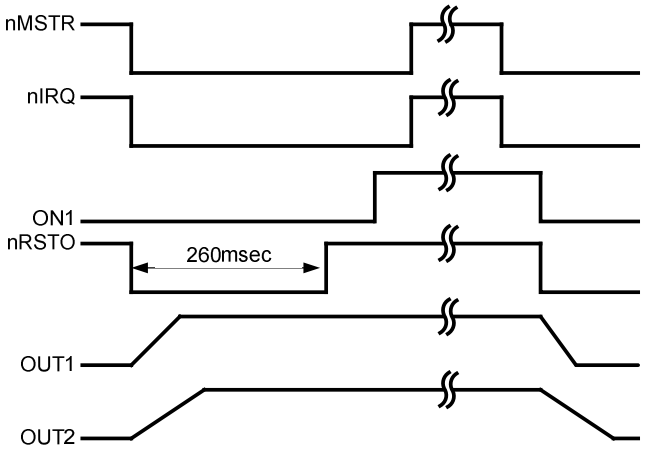
In order to support systems that utilize pin-controlled regulator enable / disable, the ACT8700 provides two manual enable / disable inputs (ON1 and ON2).

ON1 is the master enable, when driven high ON1 enables REG1 and REG2, as well as the ON2 input. Once ON1 is driven high, ON2 may be driven to manually control enable / disable of REG3.

Master Enable Input (nMSTR)

In most applications, connect nMSTR to a momentary-on push-button switch. To ensure a successful power-up sequence, this pin must be held low until the host microcontroller drives ON1 to indicate that the ACT8700 is to remain active. If a momentary-on switch is not used, drive nMSTR to a GA or to a logic low to initiate a startup sequence.

Figure TBD: Startup & Shutdown Timing Diagram



Power-On Reset Period (nRSTO)

The ACT8700 integrates a 260msec power-on reset output, reducing system size and cost. nRSTO is an open-drain output that asserts low upon startup and remains low until the 260msec reset-timeout period expires, at which point nRSTO goes high-Z.

Open-Drain Interrupt Output (nIRQ)

The ACT8700 provides an active-low, open-drain interrupt (nIRQ) that asserts whenever nMSTR is driven to a logic-low. Connect this pin to the interrupt input of the host processor, this output is useful in a variety of controlled startup / shutdown control routines. Refer to the *System Startup & Shutdown* section for more information.

System Startup & Shutdown

The ACT8700 features a flexible enable architecture that allows it to support a variety of push-button enable/disable schemes. Although other startup routines are possible, a typical startup and shutdown process would proceed as follows (referring to Figure TBD and Figure TBD): system startup is initiated when the user presses the push-button, asserting nMSTR. When this occurs, ACT8700 enables both REG1 and REG2 and asserts nRSTO to hold the microprocessor in RESET for 260msec. The ACT8700 deasserts nRSTO upon expiration of the reset timer so that the microprocessor can begin its power up sequence. Once the power-up routine is successfully completed, the microprocessor assumes control of ON1 so that the ACT8700 remains enabled after the push-button is released by the user. This start-up procedure requires that the push-button be held until the microprocessor assumes control of ON1, providing protection against accidental momentary assertions of the push-button. If desired, longer “push-and-hold” times can be easily implemented by simply adding an additional delay before assuming control of ON1. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button, then the ACT8700 will automatically shut down itself down. Once ON1 is driven high, ON2 may be used to manually enable and disable REG3.

FUNCTIONAL DESCRIPTION

Once a successful power-up routine is completed, the user can initiate a shutdown process by pressing the push-button a second time. Upon a second nMSTR assertion the ACT8700 interrupts the microprocessor by asserting nIRQ, initiating an interrupt service routine which will reveal that the user pressed the push-button. The microprocessor then initiates a power-down routine, the final step of which will be to deassert ON1, disabling REG1 and REG2.

Thermal Overload Protection

The ACT8700 integrates thermal overload protection circuitry to prevent damage resulting excessive thermal stress that may be encountered under fault conditions, for example. This circuitry disables all regulators if the ACT8700 die temperature exceeds 160°C, and prevents the regulators from being enabled until the die temperature drops by 20°C (typ), after which a normal startup routine may commence.

ELECTRICAL CHARACTERISTICS (REG1)

V_{VP1} = 3.6V, T_A = 25°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VP1 Input Voltage Range		3.1		5.5	V
VP1 UVLO Threshold	Voltage Rising	2.9	3	3.1	V
VP1 UVLO Hysteresis	Voltage Falling		100		mV
Standby Supply Current			24	35	µA
Shutdown Supply Current	ON1 = GA, V_{VP1} = 4.2V		0.1	1	µA
Output Voltage Accuracy	I_{OUT} = 10mA	-1.5%	1.8	1.5%	V
	I_{OUT} = 10mA	-1.5%	1.5	1.5%	
Line Regulation	V_{VP1} = 3.2V to 5.5V		0.04	0.4	%/V
Load Regulation	I_{OUT} = 10mA to 350mA		0.5		%/mA
Current Limit		0.5	0.6		A
Oscillator Frequency		1.4	1.7	2.0	MHz
	$V_{OUT1\_}$ = 0.5V or V_{OUT} = 80%		360		kHz
PMOS On Resistance	I_{SW1} = -100mA		0.69	TBD	Ω
NMOS On Resistance	I_{SW1} = -100mA		0.47	TBD	Ω
SW Leakage Current	V_{VP1} = V_{SW1} = 5.5V or 0V			1	µA
Minimum On-Time			TBD		nsec

ELECTRICAL CHARACTERISTICS (REG2)

V_{VP2} = 3.6V, T_A = 25°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VP2 Input Voltage Range		3.1		5.5	V
VP2 UVLO Threshold	Voltage Rising	2.9	3	3.1	V
VP2 UVLO Hysteresis	Voltage Falling		100		mV
Standby Supply Current			24	35	µA
Shutdown Supply Current	ON1 = GA, V_{VP2} = 4.2V		0.1	1	µA
Output Voltage Accuracy	I_{OUT} = 10mA	-1.5%	3.3	1.5%	V
Line Regulation	V_{VP2} = 3.2V to 5.5V		0.04	0.4	%/V
Load Regulation	I_{OUT} = 10mA to 500mA		0.5		%/mA
Current Limit		0.7	0.9		A
Oscillator Frequency		1.4	1.7	2.0	MHz
	$V_{OUT2\_}$ = 0.5V or V_{OUT} = 80%		360		kHz
PMOS On Resistance	I_{SW2} = -100mA		0.47	TBD	Ω
NMOS On Resistance	I_{SW2} = -100mA		0.29	TBD	Ω
SW Leakage Current	V_{VP2} = V_{SW2} = 5.5V or 0V			1	µA
Minimum On-Time			TBD		nsec

FUNCTIONAL DESCRIPTION

General Description

REG1 and REG2 are fixed-frequency current-mode synchronous PWM step down converters that achieve peak efficiency of over 95%. REG1 is capable of supplying up to 350mA of output current, while REG2 supports up to 500mA. Under light load conditions, these regulators utilize a proprietary pulse skipping control scheme that consumes just 24µA of supply current, maximizing battery life and making them ideal for portable applications. These regulators operate with a fixed frequency of 1.7MHz, minimizing noise in sensitive applications and allowing the use of small external components.

REG1 and REG2 operate out of phase to minimize both the size and cost of the required input capacitor.

The ACT8700 is available with a variety of standard REG1 and REG2 output voltages. Contact the factory for other available voltage options or to inquire about custom output voltage requirements.

100% Duty Cycle Operation

Although REG1 and REG2 have been optimized to maximize efficiency in lower output voltage applications, both regulators are capable of operating at up to 100% duty cycle to ensure the lowest possible dropout voltage.

Synchronous Rectification

In order to maximize efficiency and minimize the total solution size and cost, REG1 and REG2 both feature integrated synchronous rectifiers that eliminate the need for an external rectifier.

REG1 and REG2 feature adaptive reverse current limit circuitry that engages during PWM operation to maintain regulation with a constant switching frequency without the need for a minimum load.

Operating Modes

In order to maximize efficiency over the full load current range, REG1 and REG2 operate with fixed-frequency PWM operation under medium to high load conditions, and utilize a proprietary and patent-pending control scheme at light loads to reduce quiescent supply current to just 24µA to ensure the highest possible light-load efficiency. This combination of control schemes maximizes efficiency over the full load current range while avoiding the high output voltage ripple caused by “pulse-grouping” behavior of competing light-load control schemes.

Enabling and Disabling REG1 and REG2

REG1 and REG2 are automatically enabled whenever 1) an input supply is present on VIN, 2) nMSTR is driven low, or 3) ON1 is driven high. When disabled, each regulator's quiescent supply current drops to just 1µA.

Enable/disable functionality is typically implemented as part of a controlled enable/disable scheme utilizing nMSTR and other features of the ACT8700 system controller. See the *System Startup & Shutdown* section for more information.

APPLICATIONS INFORMATION

REG1 and REG2 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. REG1 and REG2 operate 180° out of phase in order to minimize the RMS input ripple current, allowing a lower total input bypass capacitance to support both regulators while providing adequate filtering. A 4.7µF ceramic capacitor for each of REG1 and REG2 is recommended for most applications.

Output Capacitor Selection

Although the ACT8700 was designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR, low-ESR tantalum capacitors are acceptable as well. When selecting an output capacitor, the output ripple voltage as a function of the ESR and capacitance of the output capacitor should be considered, and is approximated by the equation:

$$\Delta V_{OUT} \approx \Delta IL \bullet \left(ESR_{COUT} + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

More capacitance may be required depending on the duty cycle and load step requirements, but this approximation generally provides a good starting point for the design process.

Ceramic Capacitor Considerations

Despite the advantages of ceramic capacitors, there can be some disadvantageous if care is not taken during the selection and design process to ensure stable operation over the full operating voltage and temperature range. It is important to understand that ceramic capacitors are available in a variety of dielectrics each of which exhibiting different characteristics that can greatly affect performance over their temperature and voltage ranges.

The most common dielectrics are Y5V, and X5R, and their characteristics over their operating voltage and temperature ranges are shown in Figure TBD and TBD, respectively. Whereas Y5V dielectrics are inexpensive and can provide high capacitance in small packages, their capacitance varies greatly over their voltage and temperature ranges and are not recommended for DC/DC applications. X5R dielectrics are more suitable for output capacitor applications, as their characteristics are more stable over their operating ranges, and are highly-recommended.

Inductor Selection

Figure TBD: Typical MLCC Temperature Characteristics

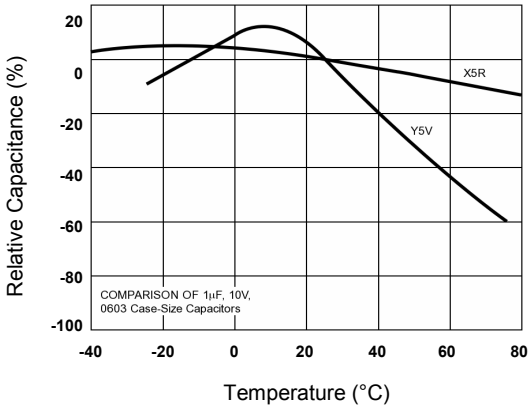
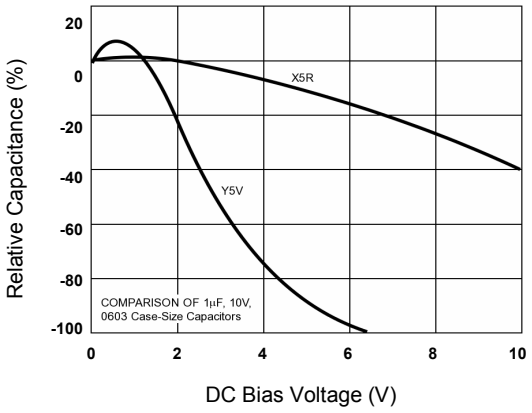


Figure TBD: Typical MLCC Voltage Characteristics



APPLICATIONS INFORMATION

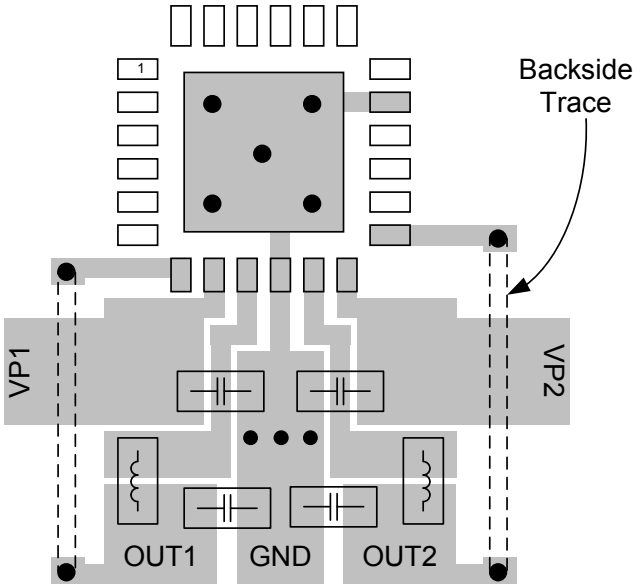
REG1 and REG2 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with TBDµH inductors, although inductors in the TBDµH to TBDµH range can be used.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors.

Figure TBD shows the recommended layout for REG1 and REG2. Step-down DC-DCs exhibit discontinuous input current, so the input capacitors as placed as close to the IC as possible, avoiding the use of vias. The inductor, input filter capacitor, and output filter capacitor are connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop are connected at a single point in a star-ground configuration, and this point is connected to the backside ground plane with vias. GA and GP1 are connected as close together as possible with a direct connection to the exposed pad. The output node for each regulator is connected the its OUT_ pin through the shortest possible route while keeping sufficient distance to prevent noise injection from the SW_ nodes. Finally, the exposed pad is directly connected to the backside ground plane using multiple vias to achieve low thermal resistance.

Figure TBD: Recommended PCB Layout for REG1 and REG2



ELECTRICAL CHARACTERISTICS

V_{BAT} = 3.6V, T_A = 25°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VSYS Input Voltage Range		3.1		6	V
VSYS UVLO Voltage Threshold	VSYS Voltage Rising	2.9	3	3.1	V
VSYS UVLO Voltage Hysteresis	VSYS Voltage Falling		100		mV
Supply Current	ON2 = IN, V_{FB3} = 0.3V		0.7	1.5	mA
	ON2 = GA, I_{OUT} = 0mA		0	1	µA
FB3 Feedback Voltage		TBD	250	TBD	mV
FB3 Input Current			50		nA
Minimum On-Time			TBD	TBD	nsec
Maximum Duty Cycle		TBD	TBD		%
Switch Current Limit		TBD	300		mA
Switch On Resistance	I_{SW3} = 100mA		1	TBD	Ω
Switch Leakage Current	V_{SW3} = 30V, ON = GA			10	µA
Power Good Threshold	V_{FB3} - V_{REF}	-9	-7	-5	%
Over Voltage Threshold	OVP	27	28	29	V

FUNCTIONAL DESCRIPTION

General Description

REG3 is a highly efficient step-up DC/DC converter that employs a fixed frequency, current-mode, PWM architecture. This regulator is optimized for white-LED bias applications consisting of up to six white-LEDs.

Setting the Maximum LED Bias Current

In current regulation mode, the maximum LED bias current is set by a resistor placed from FB3 to GA, with the resistor required to provide the desired maximum LED current given by:

$$R = \frac{0.25\ V}{I_{LED,MAX}}$$

LED current can be adjusted from the maximum value by utilizing any of a variety of methods, several of which are described in the *Adjusting the LED Bias Current* section.

Adjusting the LED Bias Current

Once the maximum LED current is set as described in the *Setting the Maximum LED Bias Current* section, the LED current can be adjusted using any one of a variety of standard methods.

To ease implementation of backlight dimming and to eliminate external components, REG3 has been designed to accept a 1kHz to 10kHz PWM signal driven to the ON2 pin. The average LED current is equal to:

$$I_{LED} = I_{LED,MAX} \cdot D$$

where $I_{LED,MAX}$ is the maximum LED current and D is the duty ratio of the PWM signal.

Over-Voltage Protection

REG3 integrates internal over-voltage protection (OVP) in order to protect itself from open-circuit fault conditions in the white-LED feedback loop. The ACT8700's OVP threshold is set at 28V, and ensures that the voltage at the top of the LED string never exceeds this voltage. If the voltage at the top of the LED string ever exceeds the OVP threshold, REG3 regulates the voltage at the top of the LED string to the OVP threshold.

Enabling and Disabling REG3

REG3 enable/disable control is supported via the combination of the ON1 and ON2 pins. Driving ON1 to a logic high enables REG1 and REG2 as well as the ON2 input. Once ON1 is driven high, drive ON2 to VSYS or to a logic high to enable REG3, drive ON2 to GA or to a logic low to disable REG3. Gating ON2 with ON1 ensures that REG3 is enabled only when REG1 and REG2 are enabled.

When disabled, REG3's quiescent supply current drops to just 1µA. As with all non-synchronous step-up DC/DC converters, REG3's application circuit produces a DC current path between the input and the output in shutdown mode. Although the forward drop of the WLEDs will make this leakage current very small in most applications, it is important to consider the effect that this may have in your application particularly when using fewer than three WLEDs.

The ACT8700 supports a simple means of providing true shutdown. A small MOSFET may be connected from the bottom of the current sense resistor and ground. Connecting the gate of this MOSFET to ON2 disconnects. Note that this circuit prevents the use of “PWMing” ON2 for WLED dimming. In such cases, REG3 is compatible with many other industry-standard methods of dimming WLEDs.

Compensation and Stability

REG3 utilizes current-mode control to optimize transient performance, ease compensation, and improve stability. This converter utilizes an internal compensation network that optimizes its performance under most operating conditions. Good stability performance is obtained through proper selection of the inductor and output capacitor. See the *Inductor Selection* and *Input and Output Capacitor Selection* sections for more information.

Inductor Selection

REG3 utilizes current-mode control, making its stability relatively insensitive to inductor selection. Select the inductor to balance the transient response and

APPLICATIONS INFORMATION

output voltage ripple requirements of your application.

A 22µH inductor is recommended for most applications. Ensure that the peak inductor current at maximum load current and the inductor saturation current are less than the current limit, typically 300mA.

Input and Output Capacitor Selection

REG3 requires just 1µF input and output capacitors for most applications. Ceramic capacitors are recommended for most applications, please refer to the *Ceramic Capacitor Considerations* section for more information about choosing a ceramic capacitor.

Rectifier Selection

REG3 requires a Schottky diode to rectify the inductor current. Select a low forward voltage drop Schottky diode with a forward current (I_F) rating that is sufficient to support the maximum switch current of 400mA (typ) and a sufficient peak repetitive reverse voltage (V_{RRM}) to support the output voltage.

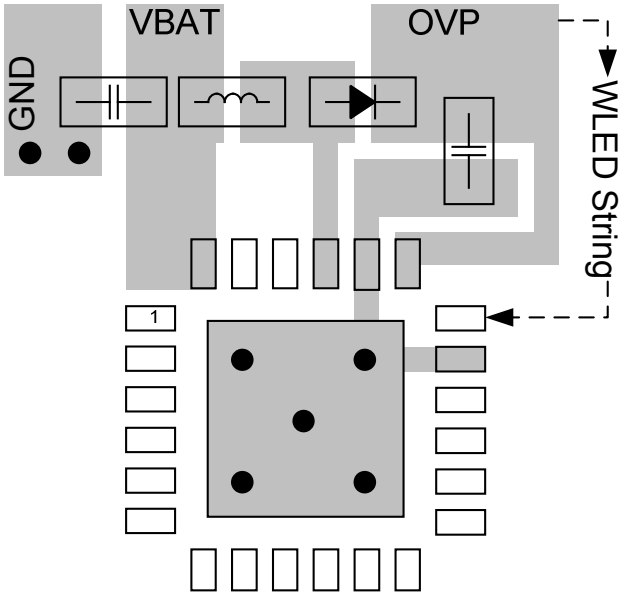
PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors.

Figure TBD shows the recommended layout for REG3. Step-up DC-DCs exhibit continuous input current, so there is some amount of flexibility in placing vias in the input capacitor circuit. The inductor, input filter capacitor, rectifier, and output filter capacitor are connected as close together as possible, with short, direct, and wide traces. GA and GP3 are connected as close together as possible with a direct connection to the exposed pad. Finally, the exposed pad is directly connected to the backside ground plane using multiple vias to achieve low thermal resistance.

Note that the LED string is a low-current, DC current path and does not generally require special layout consideration.

Figure TBD: Recommended PCB Layout for REG3



ELECTRICAL CHARACTERISTICS

V_{VIN} = 5V, T_A = 25˚C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VIN Operating Voltage Range		4.2		6	V
UVLO Threshold	VIN Voltage Rising	3.9	4	4.1	V
UVLO Hysteresis	VIN Voltage Falling		500		mV
On-Resistance			TBD	TBD	Ω
Battery Regulation Voltage	V_{VIN} = 4.5V to 5.5V, T_A = 0°C to +70°C	4.079	4.10	4.121	V
Line Regulation	V_{VIN} = 4.5V to 5.5V, I_{BAT} = 10mA		0.025	0.03	%/V
Load Regulation	I_{BAT} = 50mA to 500mA		TBD	TBD	%/mA
Charge Current	V_{BAT} = 4V, CHGLEV = GA		90	100	mA
	V_{BAT} = 4V, CHGLEV = VSYS		450	500	mA
Precondition Charge Current	V_{BAT} = 4V, CHGLEV = VSYS	TBD	45	TBD	mA
Precondition Threshold Voltage	V_{BAT} Voltage Rising	2.7	2.8	2.9	V
Precondition Threshold Hysteresis	V_{BAT} Voltage Falling		100		mV
End-of-Charge Current Threshold	V_{BAT} = 4.1V, CHGLEV = VSYS	TBD	45	TBD	mA
Thermal Regulation Threshold			115		°C
BAT Reverse Leakage Current	V_{BAT} = 4.2V, VIN = GA or BAT		50	70	µA
VIN Supply Current	SLEEP, SUSPEND, or TIMER-FAULT state		50	70	µA
	PRECONDITION, FAST-CHARGE, or TOP-OFF state		TBD	500	µA
STAT Sink current		6	8	10	mA
STAT Output Low Voltage	I_{STAT}=1mA			0.8	V
STAT Leakage Current	V_{STAT}=6V			1	µA
Charge Timeout Period			90		min
CHGLEV Logic High Input Voltage				1.4	V
CHGLEV Tri-state Input Current		-35	0	35	µA
CHGLEV Logic Low Input Voltage		0.4			V

FUNCTIONAL DESCRIPTION

General Description

The ACT8700's internal battery charger is an intelligent, stand-alone CC/CV (constant-current/constant-voltage), linear-mode single-cell charger for Lithium-based cell-chemistries. This device incorporates current and voltage sense circuitry, an internal power MOSFET, a complete state-machine to implement charge safety features, and circuitry that eliminates the reverse-blocking diode required by conventional charger designs. The ACT8700 battery charger operates independently of the regulators, and is automatically enabled whenever a valid input supply is available.

The ACT8700's battery charger features an accurate charge termination voltage, pin-programmable fast-charge current, and a 90-minute charge safety timeout period. Other features include a current-limited STAT output that can directly drive an LED indicator or provide a logic-level status signal to the host microprocessor.

The ACT8700's charger also features a thermal-regulation circuitry that protects it against excessive junction temperature, as well as proprietary input protection circuitry that makes the charger robust against input voltage transients that can damage other chargers.

The battery charger, along with REG1 and REG2, is enabled and initiates a charging cycle whenever an input supply is present.

CC/CV Regulation Loop

At the core of the ACT8700's battery charger is a CC/CV regulation loop, which regulates either current or voltage as necessary to ensure fast and safe charging of the battery.

In a normal charge cycle, this loop regulates the current to the value set by the CHGLEV pin. Charging continues at this current until the battery cell voltage reaches the charge termination voltage. At this point the CV loop takes over, and charge current is allowed to decrease as necessary to maintain charging at the termination voltage.

Charge Current Programming

To simplify current programming, the ACT8700 features pin-selectable charge current selection via the tri-state CHGLEV input. This multi-function input provides charge-current selection of either 100mA or 500mA, as well as a charge suspend function. Drive CHGLEV LOW to set the charge current to 100mA max, drive CHGLEV HIGH to set the charge current to 500mA max. To suspend charging, float CHGLEV ($|I_{CHGLEV}| < 35\mu A$).

Note that the actual charging current may be limited to a current that is lower than the programmed fast-charge current due to the ACT8700's internal thermal-regulation loop. See the *Thermal Regulation* section for more information.

Thermal Regulation

The ACT8700 features an internal thermal feedback loop that reduces the charging current as necessary to ensure that the die temperature does not rise beyond the thermal regulation threshold of 115°C. This feature protects the ACT8700 against excessive junction temperature and makes the ACT8700 more rugged to aggressive thermal designs without risk of damage. Note, however, that attention to good thermal design is required to achieve the fastest possible charge time.

CHGR State-Machine

PRECONDITION State

A new charging cycle begins with the PRECONDITION state. In this state, the cell is charged at a reduced current of 10% of the selected maximum fast-charge current. During a normal charge cycle, charging continues at this rate until V_{BAT} reaches the Precondition Threshold Voltage of 2.8V (typ), at which point the charging state machine jumps to its FAST-CHARGE state. If V_{BAT} does not reach the Precondition Threshold Voltage before the 90-minute charge timeout period expires, then a damaged cell is detected and the state machine jumps to the TIME-OUT-FAULT State.

FAST-CHARGE State

In FAST-CHARGE mode, the charger operates in constant-current (CC) mode and charges the cell at

FUNCTIONAL DESCRIPTION

the current programmed by CHGLEV. During a normal charge cycle fast-charge continues until V_{BAT} reaches the 4.2V termination voltage, at which point the state machine jumps to the TOPOFF state.

TOP-OFF State

In the TOP-OFF state, the cell is charged in constant-voltage (CV) mode. With the charge current limited by the internal chemistry of the cell, decreasing as charging continues. During a normal charging cycle charging proceeds until the charge current decreases beyond the End-Of Charge (EOC) threshold, defined as 10% of the selected maximum charge current. When this happens, the state machine terminates the charge cycle and jumps to the SLEEP state.

SLEEP State

In SLEEP mode the ACT8700 presents a high-impedance to the battery, allowing the cell to "relax" and minimizing battery leakage current. The ACT8700 continues to monitor the cell voltage, however, so that it can reinitiate charging cycles as necessary to ensure that the cell remains fully charged. Under normal operation, the state machine initiates a new charging cycle by jumping to the FAST-CHARGE state when V_{BAT} drops below the Charge Termination Threshold (4.2V) by more than the Charge Restart Threshold of 200mV (typ).

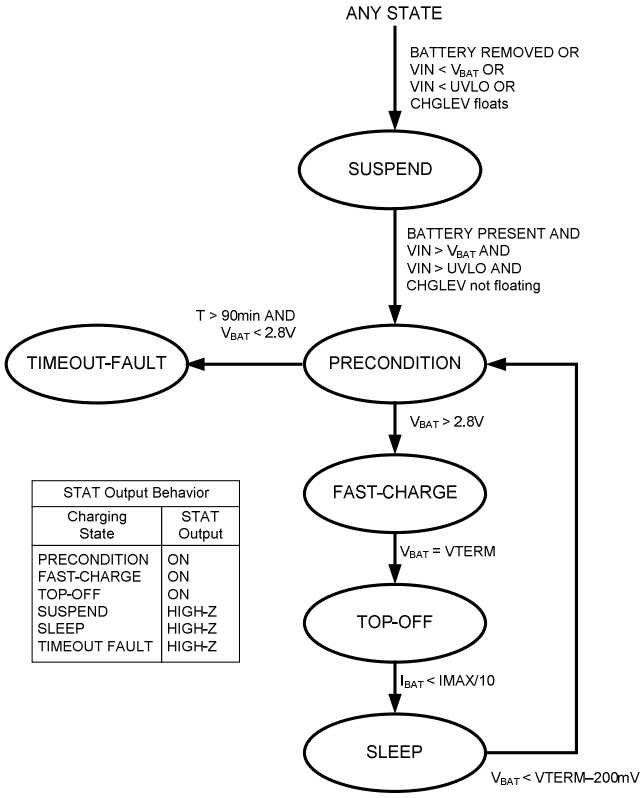
SUSPEND State

The ACT8700 features a user-selectable suspend-charge mode, which disables the charger but keeps other circuitry functional. Put the charger in suspend mode by floating CHGLEV. Upon exiting the SUSPEND state, typically when CHGLEV is driven high or low, the charge timer is reset and the state machine jumps to the PRECHARGE state.

TIMEOUT-FAULT State

In order to prevent continued operation with a damaged cell, there is no direct path to resume charging once a Timeout Fault occurs. In order to resume charging, the state machine must jump to the SUSPEND state as a result of any of the following events: 1) CHGLEV is floated, 2) the input supply is removed

Figure TBD: Charger State Diagram



STAT Output Behavior	
Charging State	STAT Output
PRECONDITION	ON
FAST-CHARGE	ON
TOP-OFF	ON
SUSPEND	HIGH-Z
SLEEP	HIGH-Z
TIMEOUT FAULT	HIGH-Z

or the input supply voltage drops below the UVLO threshold (4V), or 3) the battery is removed. Once any of these events occur, the state machine jumps to the SUSPEND state and charging can resume as defined by Figure TBD. See the SUSPEND State section for more information.

Charge Restart

After a charge cycle successfully terminates, the ACT8700 jumps to its SLEEP state to minimize battery drain, but continues to monitor the cell voltage. When the cell voltage drops by 200mV(typ), the ACT8700 reinitiates a charge cycle to keep the cell topped up.

This charge restart process prevents cell cycle-life degradation by allowing the cell to "relax" between charges, while ensuring that the equipment maintains a fully-charged battery.

FUNCTIONAL DESCRIPTION

Charge Status Output (STAT)

STAT is an open-drain output that sinks current whenever the cell is being charged, and is high-Z whenever charging is suspended, terminated, or when a fault occurs. For more information regarding the state of STAT throughout the entire charging cycle, refer to the *Charger State Diagram*.

STAT has an internal 8mA current limit, and is capable of directly driving LEDs, without the need of current-limiting resistors or other external circuitry, for a visual charge-status indication. To drive an LED, simply connect the LED between an appropriate supply, typically VIN, and STAT.

When a logic-level charge status indicator is desired, simply connect a pull-up resistor of 10kΩ or more from STAT to OUT2 or another suitable supply.

Reverse Leakage Current

The ACT8700 includes internal circuitry that eliminates the need for series blocking diodes, reducing solution size and cost as well as dropout voltage relative to conventional battery chargers. When the input supply is removed, when VIN goes below the ACT8700's undervoltage-lockout (UVLO) voltage, or when VIN drops below V_{BAT}, the ACT8700 automatically goes into SUSPEND mode and reconfigures its power switch to minimize current drain from the battery.

Input and Output Capacitor Selection

When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.