ACT8712

Rev0, 25-Feb-08

Advanced Product Information—All Information Subject to Change

Four Channel Integrated Power Management IC for Handheld Portable Equipment

FEATURES

- **Multiple Patents Pending**
- **Li+ Battery Charger with Integrated MOSFET**
  - **Programmable Charge Current up to 1A**
  - **ON/OFF Control and Status Indication**
- **Three Integrated Regulators**
  - **550mA Step-Down DC/DC**
  - **750mA Step-Down DC/DC**
  - **Step-Up DC/DC with OVP for WLED Bias**
- **I²C™ Compatible Serial Interface**
  - **Programmable Output Voltages**
  - **Configurable Operating Modes**
- **Minimal External Components**
- **4x4mm, Thin-QFN (TQFN44-24) Package**
  - **Only 0.75mm Height**
  - **RoHS Compliant**

APPLICATIONS

- **Portable Devices and PDAs**
- **Digital Media Players**
- **Battery Operated Devices**
- **GPS Receivers, etc.**

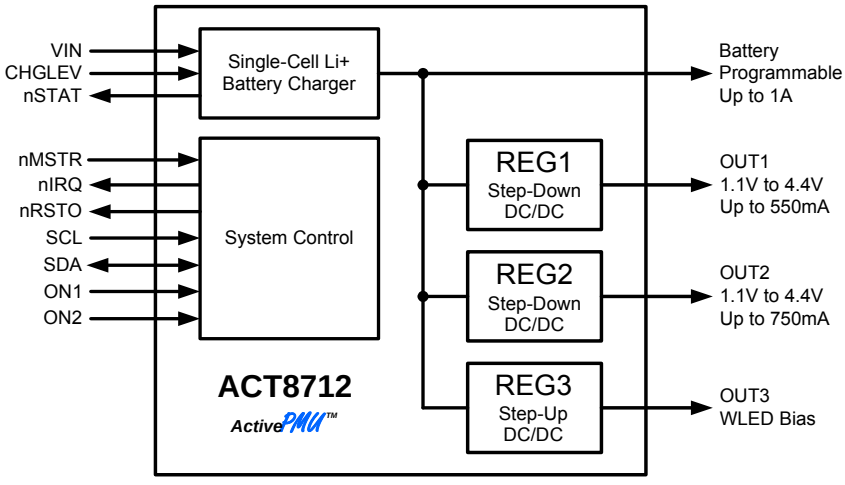
GENERAL DESCRIPTION

The patent-pending ACT8712 is a complete, cost effective, highly efficient *ActivePMU™* power management solution that is ideal for a wide range of portable handheld equipment. This device integrates two PWM step-down DC/DC converters, one PWM step-up DC/DC converter with over-voltage protection (OVP) and a full-featured linear-mode Li+ battery charger into a single, thin, space-saving package. An I²C Serial Interface provides programmability for the DC/DC converters and battery charger.

REG1 and REG2 are fixed-frequency, current-mode PWM step-down DC/DC converters that are optimized for high efficiency and are capable of supplying up to 550mA and 750mA, respectively. REG3 is a fixed-frequency PWM step-up converter that safely and efficiently biases a string of up to seven white-LEDs for backlighting. The battery charger incorporates an internal power MOSFET for constant-current/constant-voltage, thermally regulated charging of a single-cell Li+ battery. All DC/DC converters' output voltage are programmable and controllable via the I²C interface.

The ACT8712 is available in a tiny 4mm x 4mm 24-pin Thin-QFN package that is just 0.75mm thin.

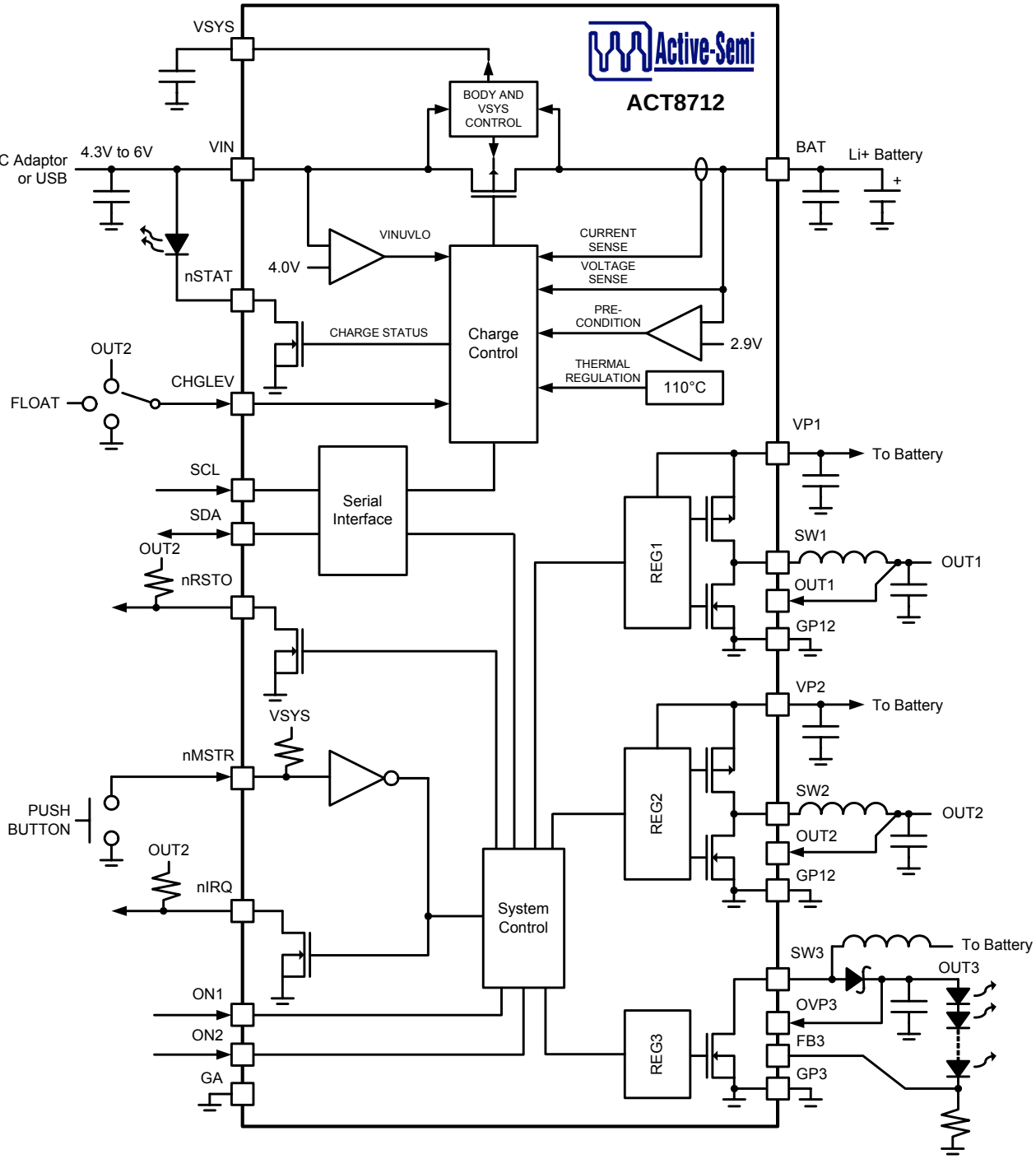
SYSTEM BLOCK DIAGRAM



Pb-free

TABLE OF CONTENTS

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①②

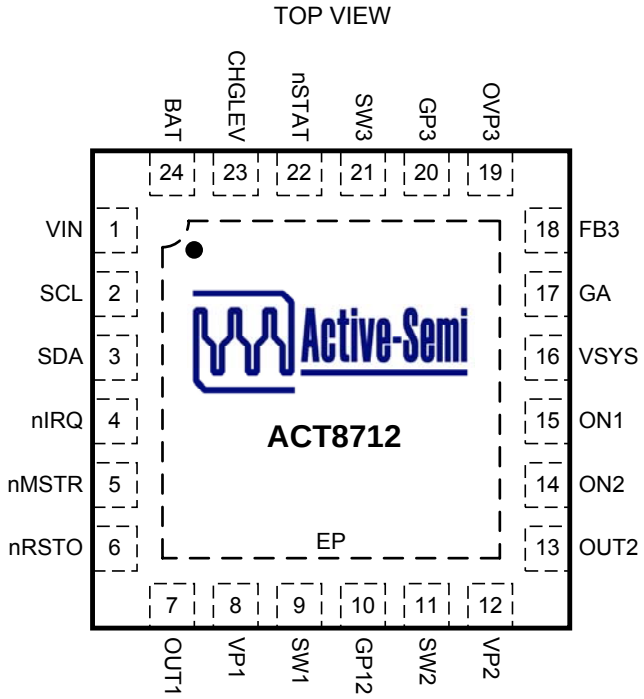
PART NUMBER	V_{OUT1}	V_{OUT2}	PACKAGE	PINS	TEMPERATURE RANGE
ACT8712QLCHA-T	1.2V	3.3V	TQFN44-24	24	-40°C to +85°C
ACT8712QLEHA-T	1.8V	3.3V	TQFN44-24	24	-40°C to +85°C

OUTPUT VOLTAGE CODES					
C	D	E	F	G	H
1.2V	1.5V	1.8V	2.5V	3.0V	3.3V

①: Output voltage options detailed in this table represent standard voltage options, and are available for samples or production orders. Additional output voltage options, as detailed in the *Output Voltage Codes* table, are available for production subject to minimum order quantities. Contact Active-Semi for more information regarding semi-custom output voltage combinations.

②: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

PIN CONFIGURATION



Thin - QFN (TQFN44-24)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	VIN	Power Input for the Battery Charger. Bypass VIN to GA with a capacitor placed as close to the IC as possible. The battery charger and both step-down DC/DCs (REG1 and REG2) are automatically enabled when a valid voltage is present on VIN.
2	SCL	Clock Input for I^2C Serial Interface. Data is read on the rising edge of the clock.
3	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of the clock.
4	nIRQ	Open-Drain Push-Button Status Output. nIRQ is an open-drain output which sinks current when nMSTR is asserted.
5	nMSTR	Master Enable Input. Drive nMSTR to GA or to a logic low to enable IC.
6	nRSTO	Open-Drain Reset Output. nRSTO asserts low for the reset timeout period of 300ms whenever the IC is enabled.
7	OUT1	Output Feedback Sense for REG1. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
8	VP1	Power Input for REG1. Bypass to GP12 with a high quality ceramic capacitor placed as close as possible to the IC.
9	SW1	Switching Node Output for REG1. Connect this pin to the switching end of the inductor.
10	GP12	Power Ground for REG1 and REG2. Connect GA, GP12, and GP3 together at a single point as close to the IC as possible.
11	SW2	Switching Node Output for REG2. Connect this pin to the switching end of the inductor.
12	VP2	Power Input for REG2. Bypass to GP12 with a high quality ceramic capacitor placed as close as possible to the IC.
13	OUT2	Output Feedback Sense for REG2. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
14	ON2	Enable Control Input for REG3. ON2 is functional only when ON1 is driven high, nMSTR is driven low, or when a valid supply voltage is present on VIN. Drive ON2 to VSYS or to a logic high for normal operation, drive to GA or a logic low to disable REG3.
15	ON1	Enable Control Input for REG1 and REG2. Drive ON1 to VSYS or to a logic high for normal operation, drive to GA or to a logic low to disable REG1 and REG2.
16	VSYS	Power Bypass for System Management Circuitry. Bypass to GA with a high quality ceramic capacitor placed as close as possible to the IC. VSYS is internally connected to the higher voltage of either V_{VIN} or V_{BAT}. Do not load VSYS with more than 100µA.

PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
17	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP12, and GP3 together at a single point as close to the IC as possible.
18	FB3	Feedback Sense for REG3. Connect this pin to the LED string current sense resistor to sense the LED current.
19	OVP3	Over-Voltage Protection Input for REG3. Connect this pin directly to the output node to sense and prevent over-voltage conditions.
20	GP3	Power Ground for REG3. Connect GP3 directly to a power ground plane. Connect GA, GP12, and GP3 together at a single point as close to the IC as possible.
21	SW3	Switching Node Output for REG3. Connect this pin to the switching end of the inductor.
22	nSTAT	Active-Low Open-Drain Charger Status Output. nSTAT sinks current whenever the charger is charging the battery, and is high-Z otherwise. nSTAT has a 6mA (typ) current limit, allowing it to directly drive an indicator LED without additional external components. To generate a logic-level output, connect nSTAT to an appropriate supply voltage (typically OUT2) through a 10kΩ or greater pull-up resistor.
23	CHGLEV	Tri-State Charging State Select Input. When ISET1[ ] = [0000], drive CHGLEV to VSYS or to a logic high for high-current charging mode (maximum charge current of 500mA), and drive to GA or a logic low for low-current charging mode (maximum charge current of 100mA). Allow CHGLEV to float ($\|I_{CHGLEV}\| < 2\mu A$) to disable the charger.
24	BAT	Battery Charger Output. Connect this pin directly to the battery anode (+ terminal) to sense the battery voltage.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VP1, SW1, VP2, SW2 to GP12, VSYS, OUT1, OUT2, FB3, BAT, CHGLEV, nSTAT, ON1, ON2, nRSTO, nMSTR, nIRQ, SCL, SDA to GA	-0.3 to +6	V
OVP3, SW3 to GP3	-0.3 to +30	V
SW1 to VP1, SW2 to VP2	-6 to +0.3	V
VIN to GA t <1ms and duty cycle <1% Steady State	 -0.3 to +7 -0.3 to +6	 V V
GP12, GP3 to GA	-0.3 to +0.3	V
RMS Power Dissipation (T_A = 70°C)	1.8	W
Operating Temperature Range	-40 to 85	°C
Junction Temperature	125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

REGISTER DESCRIPTIONS

Table 1:

Global Register Map

OUTPUT	ADDRESS									DATA (DEFAULT VALUE)							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
CHGR	08h	0	0	0	0	1	0	0	0	0	0	0	0	R	R	R	R
CHGR	09h	0	0	0	0	1	0	0	1	0	1	R	R	R	R	R	R
CHGR	0Ah	0	0	0	0	1	0	1	0	0	0	0	0	R	R	R	R
CHGR	0Bh	0	0	0	0	1	0	1	1	R	R	R	R	0	0	R	0
REG1	10h	0	0	0	1	0	0	0	0	R	V	V	V	V	V	V	V
REG1	11h	0	0	0	1	0	0	0	1	R	R	R	R	R	R	R	0
REG1	12h	0	0	0	1	0	0	1	0	0	0	R	R	R	R	R	R
REG1	13h	0	0	0	1	0	0	1	1	R	R	R	0	R	0	R	1
REG2	20h	0	0	1	0	0	0	0	0	R	V	V	V	V	V	V	V
REG2	21h	0	0	1	0	0	0	0	1	R	R	R	R	R	R	R	0
REG2	22h	0	0	1	0	0	0	1	0	0	1	R	R	R	R	R	R
REG2	23h	0	0	1	0	0	0	1	1	R	R	R	0	R	0	R	1
REG3	30h	0	0	1	1	0	0	0	0	R	R	1	1	1	1	1	1
REG3	31h	0	0	1	1	0	0	0	1	R	R	R	R	R	R	R	0
REG3	32h	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
REG3	33h	0	0	1	1	0	0	1	1	0	0	0	R	R	0	R	0

KEY:

R: Read-Only bit. No Default Assigned.

V: Default Values Depend on Voltage Option. Default Values May Vary.

Note: Addresses other than those specified in Table 1 may be used for factory settings. Do not access any registers other than those specified in Table 1.

ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

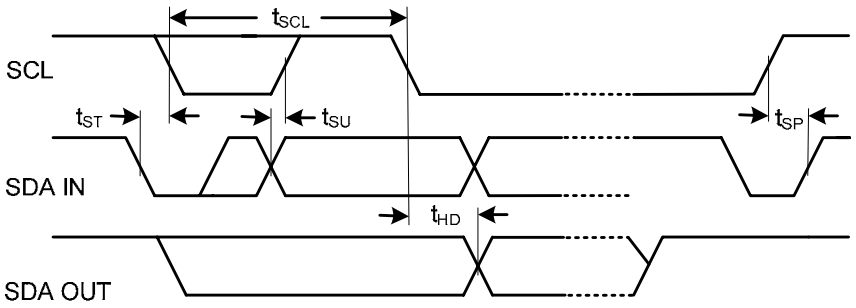
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSYS Operating Voltage Range		2.6		5.5	V
VSYS UVLO Threshold	VSYS Voltage Rising	2.25	2.4	2.55	V
VSYS UVLO Hysteresis	VSYS Voltage Falling		80		mV
VSYS Output Resistance			10		Ω
Oscillator Frequency		1.35	1.6	1.85	MHz
VSYS Supply Current	ON1 = ON2 = GA, CHGLEV = floating		1.5		μA
nMSTR Internal Pull-Up Resistance		250	500		kΩ
Logic High Input Voltage	ON1, ON2, nMSTR	1.4			V
Logic Low Input Voltage	ON1, ON2, nMSTR			0.4	V
Logic Low Output Voltage	nIRQ, nRSTO, I_{SINK} = 5mA			0.3	V
Leakage Current	nIRQ, nRSTO, V_{nIRQ} = V_{nRSTO} = 4.2V			1	μA
nRSTO Delay		240	300	360	ms
Thermal Shutdown Temperature	Temperature Rising		160		°C
Thermal Shutdown Hysteresis	Temperature Falling		20		°C

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Low Input Voltage				0.4	V
SCL, SDA High Input Voltage		1.4			V
SCL, SDA Leakage Current				1	µA
SDA Low Output Voltage	I_{OL} = 5mA			0.3	V
SCL Clock Period, t_{SCL}	f_{SCL} clock freq = 400kHz	2.5			µs
SDA Data In Setup Time to SCL High, t_{SU}		100			ns
SDA Data Out Hold Time after SCL Low, t_{HD}		300			ns
SDA Data Low Setup Time to SCL Low, t_{ST}	Start Condition	100			ns
SDA Data High Hold Time after Clock High, t_{SP}	Stop Condition	100			ns

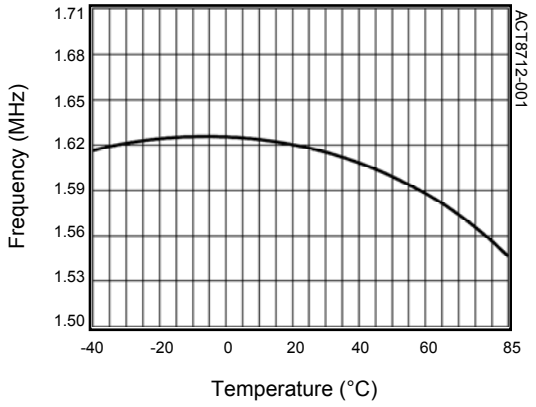
Figure 1:
I²C Serial Bus Timing



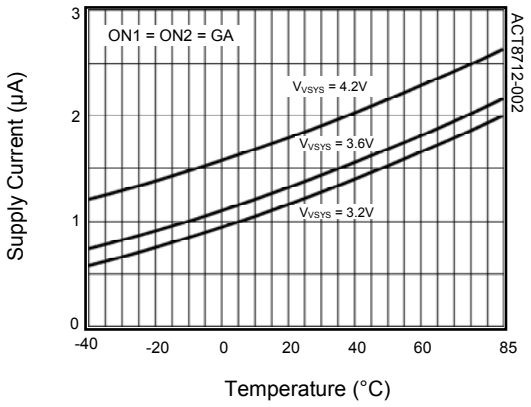
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

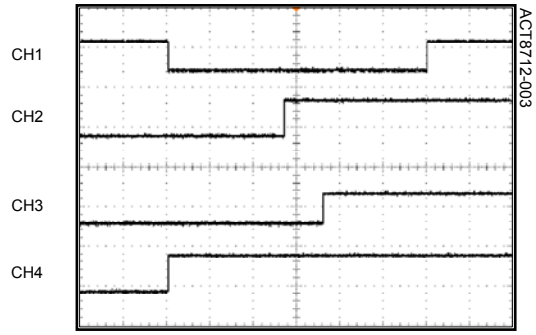
Oscillator Frequency vs. Temperature



VSYS Current vs. Temperature

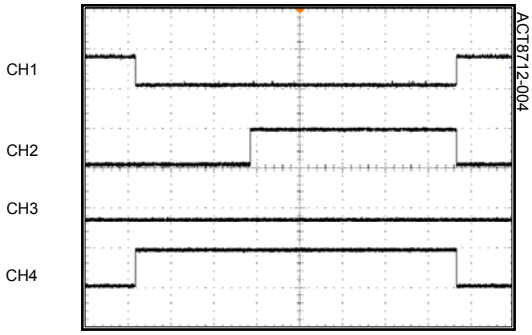


Startup Sequence



CH1: V_{nMSTR}, 5V/div
CH2: V_{nRSTO}, 2V/div
CH3: V_{ON1}, 5V/div
CH4: V_{OUT1}, 2V/div
TIME: 100ms/div

Shutdown Sequence



CH1: V_{nMSTR}, 5V/div
CH2: V_{nRSTO}, 2V/div
CH3: V_{ON1}, 5V/div
CH4: V_{OUT1}, 2V/div
TIME: 100ms/div

FUNCTIONAL DESCRIPTION

General Description

The ACT8712 offers an array of system management functions that allow it to provide optimal performance in a wide range of applications.

I²C Serial Interface

At the core of the ACT8712's flexible architecture is an I²C interface that permits optional programming capability to enhance overall system performance.

To ensure compatibility with a wide range of system processors, the ACT8712 uses standard I²C commands; I²C write-byte commands are used to program the ACT8712, and I²C read-byte commands are used to read the ACT8712's internal registers. The ACT8712 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1010 011x].

SDA is a bi-directional data line and SCL is a clock input. The master initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an "Acknowledge" (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I²C 2-wire serial interface, go to the NXP website: http://www.nxp.com

System Startup and Shutdown

The ACT8712 features a flexible control architecture that supports a variety of software-controlled enable/disable functions that make it a simple yet flexible and highly configurable solution.

The ACT8712 is automatically enabled when any of the following conditions exists:

1) A valid supply voltage is present at VIN,

2) nMSTR is asserted low, or

3) ON1 is asserted high.

If any of these conditions is true, the ACT8712 enables REG1 and REG2, powering up the system processor so that the startup and shutdown sequences may be controlled via software. Each of these startup conditions are described in detail below.

Automatic Enable Due to Valid VIN Supply

The ACT8712 battery charger and step-down DC/DC converters (REG1 and REG2) are automatically enabled when a valid input supply is applied to VIN. Automatically enabling these functions simplifies system design and eliminates the need for external input supply-detection circuitry.

Manual Enable Due to Asserting nMSTR Low

System startup is initiated when the user presses the push-button, asserting nMSTR low. When this occurs, both REG1 and REG2 are enabled and nRSTO is asserted low to hold the microprocessor in RESET for 260ms. nRSTO goes high-Z upon expiration of the reset timer, de-asserting the processor's reset input and allowing the microprocessor to initiate its power up sequence. Once the power-up routine is successfully completed, the microprocessor must assert ON1 so that the ACT8712 remains enabled after the push-button is released by the user. Upon completion of the start-up sequence the processor assumes control of the power system and all further operation is software-controlled.

Manual Enable Due to Asserting ON1 High

The ACT8712 is compatible with applications that do not utilize it's push-button control function, and may be enabled by simply driving ON1 to a logic-high. In this case, the signal driving ON1 controls enable/disable timing, although software-controlled enable/disable sequences are still supported if the processor assumes control of the power system once the startup sequence is completed.

Shutdown Sequence

Once a successful power-up routine is completed, the system processor controls the operation of the power system, including the system shutdown timing and sequence. The ACT8712 asserts nIRQ low when nMSTR is asserted low, providing a simple means of alerting the system processor when the user wishes to shut the system down. Asserting nIRQ interrupts the system processor, initiating an interrupt service routine in the processor which will reveal that the user pressed the push-button. The microprocessor may validate the input, such as by ensuring that the push-button is asserted for a minimum amount of time, then initiates a software-controlled power-down routine, the final step of which is to de-assert the ON1 input, disabling REG1 and REG2 and shutting the system down.

nMSTR Enable Input

In most applications, connect nMSTR to an active low, momentary push-button switch to utilize the ACT8712's closed-loop enable/disable functionality. If a momentary-on switch is not used, drive nMSTR to GA or to a logic low to initiate a startup sequence.

Enable/Disable Inputs (ON1 and ON2)

The ACT8712 provides two manual enable/disable inputs, ON1 and ON2. ON1 is the master enable input. When driven high, ON1 enables REG1 and REG2. ON2 is the enable input for REG3. ON2 is used to enable REG3 when any of the following conditions exists:

1) A valid supply voltage is present at VIN,

2) nMSTR is asserted low, or

3) ON1 is asserted high.

Power-On Reset Output

The ACT8712 integrates a 260ms power-on reset generator, reducing system size and cost. nRSTO is an open-drain output. Connect a 10kΩ or greater pull-up resistor from nRSTO to an appropriate voltage supply, typically OUT2. nRSTO asserts low upon startup and remains low until the reset-timeout period expires, at which point nRSTO goes high-Z.

nIRQ Output

The ACT8712 provides an active-low, open-drain push-button status output that sinks current when nMSTR is driven to a logic-low. Connect a pull-up resistor from nIRQ to an appropriate voltage supply. nIRQ is typically used to drive the interrupt input of the system processor, and is useful in a variety of software-controlled enable/disable control routines.

Thermal Shutdown

The ACT8712 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions. This circuitry disables all regulators if the ACT8712 die temperature exceeds 160°C, and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

ELECTRICAL CHARACTERISTICS

(V_{VP1} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP1 Operating Voltage Range		3.1		5.5	V
VP1 UVLO Threshold	Input Voltage Rising	2.9	3	3.1	V
VP1 UVLO Hysteresis	Input Voltage Falling		80		mV
Standby Supply Current			130	200	µA
Shutdown Supply Current	ON1 = GA, V_{VP1} = 4.2V		0.1	1	µA
Output Voltage Regulation Accuracy	V_{NOM1} < 1.3V, I_{OUT1} = 10mA	-2.4%	V_{NOM1}①	+1.8%	V
	V_{NOM1} ≥ 1.3V, I_{OUT1} = 10mA	-1.2%	V_{NOM1}	+1.8%	
Line Regulation	V_{VP1} = Max(V_{NOM1} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT1} = 10mA to 550mA		0.0017		%/mA
Current Limit		0.65	0.85		A
Oscillator Frequency	V_{OUT1} ≥ 20% of V_{NOM1}	1.35	1.6	1.85	MHz
	V_{OUT1} = 0V		530		kHz
PMOS On-Resistance	I_{SW1} = -100mA		0.35	0.60	Ω
NMOS On-Resistance	I_{SW1} = 100mA		0.23	0.40	Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM1}
Minimum On-Time			70		ns

①: V_{NOM1} refers to the nominal output voltage level for V_{OUT1} as defined by the *Ordering Information* section.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 2:

REG1 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
10h	R	VRANGE	VSET					
11h	R	R	R	R	R	R	R	MODE
12h	W/E	W/E	R	R	R	R	R	R
13h	R	R	R	W/E	R	W/E	OK	W/E

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1.

Table 3:

REG1 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
10h	VSET	[5:0]	R/W	REG1 Output Voltage Selection	See Table 4	
10h	VRANGE	[6]	R/W	REG1 Reference Voltage Selection	0	Min V_{OUT} = 1.1V
					1	Min V_{OUT} = 1.25V
10h		[7]	R		READ ONLY	
11h	MODE	[0]	R/W	Mode Selection	0	PFM/PWM
					1	Forced PWM
11h		[7:1]	R		READ ONLY	
12h		[5:0]	R		READ ONLY	
12h		[7:6]	W/E		WRITE-EXACT	
13h		[0]	W/E		WRITE-EXACT	
13h	OK	[1]	R	REG1 Power-OK	0	Output is not OK
					1	Output is OK
13h		[2]	W/E		WRITE-EXACT	
13h		[3]	R		READ ONLY	
13h		[4]	W/E		WRITE-EXACT	
13h		[7:5]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 4:

REG1/VSET[ ] Output Voltage Setting

REG1/VSET [3:0]	REG1/VSET[5:4]							
	REG1/VRANGE = [0]				REG1/VRANGE = [1]			
	00	01	10	11	00	01	10	11
0000	N/A	N/A	1.455	1.860	1.250	2.050	2.850	3.650
0001	N/A	N/A	1.480	1.890	1.300	2.100	2.900	3.700
0010	N/A	1.100	1.505	1.915	1.350	2.150	2.950	3.750
0011	N/A	1.125	1.530	1.940	1.400	2.200	3.000	3.800
0100	N/A	1.150	1.555	1.965	1.450	2.250	3.050	3.850
0101	N/A	1.175	1.585	1.990	1.500	2.300	3.100	3.900
0110	N/A	1.200	1.610	2.015	1.550	2.350	3.150	3.950
0111	N/A	1.225	1.635	2.040	1.600	2.400	3.200	4.000
1000	N/A	1.255	1.660	2.065	1.650	2.450	3.250	4.050
1001	N/A	1.280	1.685	2.090	1.700	2.500	3.300	4.100
1010	N/A	1.305	1.710	2.115	1.750	2.550	3.350	4.150
1011	N/A	1.330	1.735	2.140	1.800	2.600	3.400	4.200
1100	N/A	1.355	1.760	2.165	1.850	2.650	3.450	4.250
1101	N/A	1.380	1.785	2.190	1.900	2.700	3.500	4.300
1110	N/A	1.405	1.810	2.200	1.950	2.750	3.550	4.350
1111	N/A	1.430	1.835	2.245	2.000	2.800	3.600	4.400

(N/A): Not Available

ELECTRICAL CHARACTERISTICS

(V_{VP2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP2 Operating Voltage Range		3.1		5.5	V
VP2 UVLO Threshold	Input Voltage Rising	2.9	3	3.1	V
VP2 UVLO Hysteresis	Input Voltage Falling		80		mV
Standby Supply Current			130	200	µA
Shutdown Supply Current	ON1 = GA, V_{VP2} = 4.2V		0.1	1	µA
Output Voltage Regulation Accuracy	V_{NOM2} < 1.3V, I_{OUT2} = 10mA	-2.4%	V_{NOM2}①	+1.8%	V
	V_{NOM2} ≥ 1.3V, I_{OUT2} = 10mA	-1.2%	V_{NOM2}	+1.8%	
Line Regulation	V_{VP2} = Max(V_{NOM2} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT2} = 10mA to 750mA		0.0017		%/mA
Current Limit		0.85	1.1		A
Oscillator Frequency	V_{OUT2} ≥ 20% of V_{NOM2}	1.35	1.6	1.85	MHz
	V_{OUT2} = 0V		530		kHz
PMOS On-Resistance	I_{SW2} = -100mA		0.28	0.50	Ω
NMOS On-Resistance	I_{SW2} = 100mA		0.20	0.35	Ω
SW2 Leakage Current	V_{VP2} = 5.5V, V_{SW2} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM2}
Minimum On-Time			70		ns

①: V_{NOM2} refers to the nominal output voltage level for V_{OUT2} as defined by the *Ordering Information* section.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 5:

REG2 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
20h	R	VRANGE	VSET					
21h	R	R	R	R	R	R	R	MODE
22h	W/E	W/E	R	R	R	R	R	R
23h	R	R	R	W/E	R	W/E	OK	W/E

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1.

Table 6:

REG2 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
20h	VSET	[5:0]	R/W	REG2 Output Voltage Selection	See Table 7	
20h	VRANGE	[6]	R/W	REG2 Reference Voltage Selection	0	Min V_{OUT} = 1.1V
					1	Min V_{OUT} = 1.25V
20h		[7]	R		READ ONLY	
21h	MODE	[0]	R/W	Mode Selection	0	PFM/PWM
					1	Forced PWM
21h		[7:1]	R		READ ONLY	
22h		[5:0]	R		READ ONLY	
22h		[7:6]	W/E		WRITE-EXACT	
23h		[0]	W/E		WRITE-EXACT	
23h	OK	[1]	R	REG2 Power-OK	0	Output is not OK
					1	Output is OK
23h		[2]	W/E		WRITE-EXACT	
23h		[3]	R		READ ONLY	
23h		[4]	W/E		WRITE-EXACT	
23h		[7:5]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 7:

REG2/VSET[ ] Output Voltage Setting

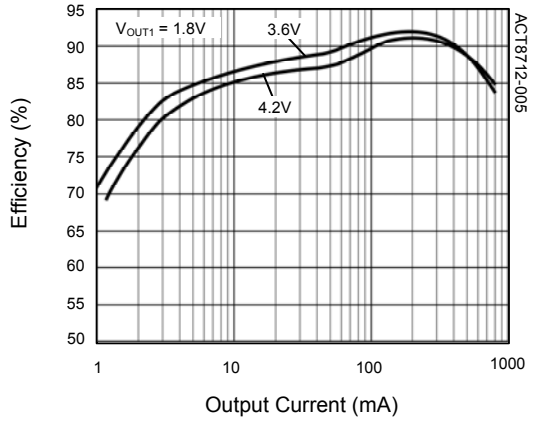
REG2/VSET [3:0]	REG2/VSET[5:4]							
	REG2/VRANGE = [0]				REG2/VRANGE = [1]			
	00	01	10	11	00	01	10	11
0000	N/A	N/A	1.455	1.860	1.250	2.050	2.850	3.650
0001	N/A	N/A	1.480	1.890	1.300	2.100	2.900	3.700
0010	N/A	1.100	1.505	1.915	1.350	2.150	2.950	3.750
0011	N/A	1.125	1.530	1.940	1.400	2.200	3.000	3.800
0100	N/A	1.150	1.555	1.965	1.450	2.250	3.050	3.850
0101	N/A	1.175	1.585	1.990	1.500	2.300	3.100	3.900
0110	N/A	1.200	1.610	2.015	1.550	2.350	3.150	3.950
0111	N/A	1.225	1.635	2.040	1.600	2.400	3.200	4.000
1000	N/A	1.255	1.660	2.065	1.650	2.450	3.250	4.050
1001	N/A	1.280	1.685	2.090	1.700	2.500	3.300	4.100
1010	N/A	1.305	1.710	2.115	1.750	2.550	3.350	4.150
1011	N/A	1.330	1.735	2.140	1.800	2.600	3.400	4.200
1100	N/A	1.355	1.760	2.165	1.850	2.650	3.450	4.250
1101	N/A	1.380	1.785	2.190	1.900	2.700	3.500	4.300
1110	N/A	1.405	1.810	2.200	1.950	2.750	3.550	4.350
1111	N/A	1.430	1.835	2.245	2.000	2.800	3.600	4.400

(N/A): Not Available

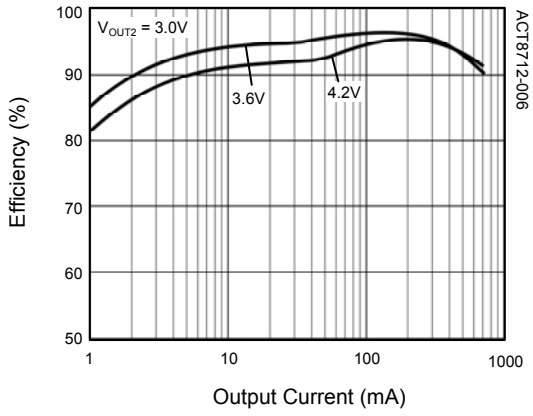
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8712QLEHA, V_{VP1} = V_{VP2} = 3.6V, L = 3.3μH, C_{VP1} = C_{VP2} = 2.2μF, C_{OUT1} = C_{OUT2} = 10μF, T_A = 25°C, unless otherwise specified.)

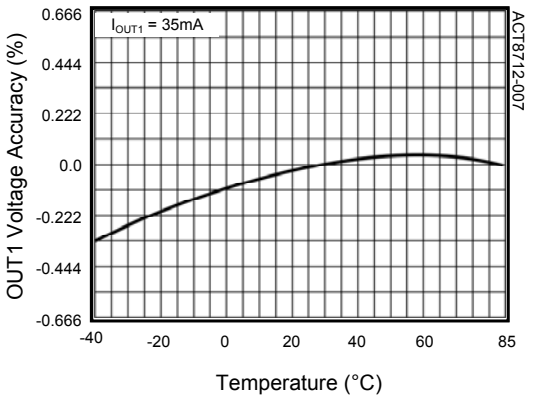
REG1 Efficiency vs. Load Current



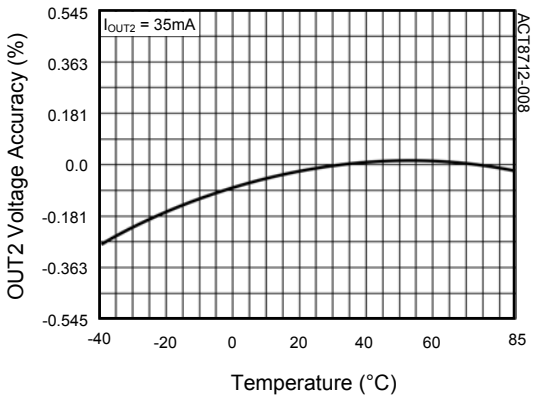
REG2 Efficiency vs. Load Current



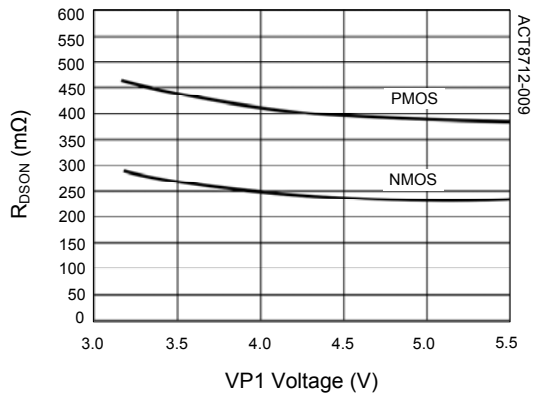
OUT1 Regulation Voltage



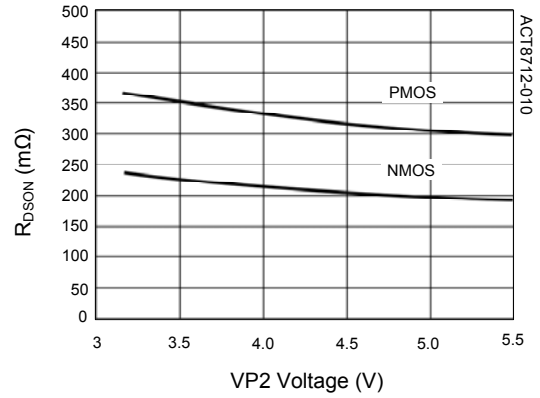
OUT2 Regulation Voltage



REG1 MOSFET Resistance



REG2 MOSFET Resistance



FUNCTIONAL DESCRIPTION

General Description

REG1 and REG2 are fixed-frequency, current-mode, synchronous PWM step down converters that achieve peak efficiencies of up to 97%. REG1 is capable of supplying up to 550mA of output current, while REG2 supports up to 750mA. These regulators operate with a fixed frequency of 1.6MHz, minimizing noise in sensitive applications and allowing the use of small external components. REG1 and REG2 are available with a variety of standard and custom output voltages, as described in the Ordering Information section of this datasheet. REG1 and REG2 also take advantage of the I^2C interface, and may be software-controlled in systems that require advanced power management functions.

100% Duty Cycle Operation

Both REG1 and REG2 are capable of operating at up to 100% duty cycle. During 100% duty-cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery-powered applications.

Synchronous Rectification

REG1 and REG2 both feature integrated n-channel synchronous rectifiers, maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Enabling and Disabling REG1 and REG2

Enable/disable functionality is typically implemented as part of a controlled enable/disable scheme utilizing nMSTR and other system control features of the ACT8712. REG1 and REG2 are automatically enabled whenever any of the following conditions are met:

1) A valid input voltage is present at VIN,

2) nMSTR is driven low, or

3) ON1 is asserted high.

When none of these conditions are true, REG1 and REG2 are disabled, and each regulator's quiescent supply current drops to less than 1µA.

Programming the Output Voltage

By default, REG1 and REG2 each power up and regulate to their default output voltage. Once the system is enabled, each regulator's output voltage may be independently programmed to a different value, typically in order to reduce the power consumption of a microprocessor in standby mode. Program the output voltages via the I2C serial interface by writing to the REGx/VSETx[ ] and REGx/VRANGE[ ] registers.

Programmable Operating Mode

By default, REG1 and REG2 operate in fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power. In applications where low noise is critical, force fixed-frequency PWM operation across the entire load current range, at the expense of light-load efficiency, by setting the REGx/MODE[ ] bit to [1].

Power-OK

REG1 and REG2 each feature a variety of status bits that can be read by the system microprocessor. If either output voltage is lower than the power-OK threshold, typically 6% below the programmed regulation voltage, REGx/OK[ ] will clear to 0.

Soft-Start

REG1 and REG2 each include matched soft-start circuitry. When enabled, the output voltages track the internal 80µs soft-start ramp and both power up in a monotonic manner that is independent of loading on either output. This circuitry ensures that both outputs power up in a controlled manner, greatly simplifying power sequencing design considerations.

Compensation

REG1 and REG2 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 2.2µF ceramic capacitor for each of REG1 and REG2 is recommended for most applications.

Output Capacitor Selection

For most applications, 10µF ceramic output capacitors are recommended for both REG1 and REG2. Although the these regulators were designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR, low-ESR tantalum capacitors can provide acceptable results as well.

Inductor Selection

REG1 and REG2 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with 3.3µH inductors, although inductors in the 2.2µH to 4.7µH range can be used. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current of the application by at least 30%.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as close as possible to the IC, and avoiding the use of vias if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple vias. The output node for each regulator should be connected to its corresponding OUTx pin through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple vias to achieve low electrical and thermal resistance.

ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range①		2		5.5	V
UVLO Voltage Threshold	VSYS Voltage Rising	2.9	3	3.1	V
UVLO Voltage Hysteresis	VSYS Voltage Falling		80		mV
Supply Current	ON2 = VIN, V_{FB3} = 0.3V		75	150	μA
	ON2 = GA, I_{LOAD} = 0mA		0.1	1	μA
FB3 Feedback Voltage		235	255	275	mV
FB3 Input Current			50		nA
Oscillator Frequency		1.35	1.6	1.85	MHz
Minimum On-Time			100		ns
Maximum Duty Cycle		87	92		%
Switch Current Limit	Duty = 83%, L = 22μH, C_{OUT3} = 4.7μF	500	750		mA
Switch On-Resistance	I_{SW3} = 100mA		0.67	1.1	Ω
Switch Leakage Current	V_{SW3} = 30V, ON2 = GA			10	μA
Over-Voltage Threshold	REG3/VSET[ ] = [111111]	27.5	28.5	29.5	V

①: As long as VSYS is within the VSYS operating range, this spec refers to the voltage range of the input that the inductor is connected to.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 8:

REG3 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
30h	R	R	VSET					
31h	R	R	R	R	R	R	R	W/E
32h	W/E	W/E	W/E	W/E	W/E	W/E	W/E	W/E
33h	W/E	W/E	W/E	R	R	W/E	OK	ON

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1.

Table 9:

REG3 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
30h	VSET	[5:0]	R/W	REG3 Over Voltage Threshold Selection	See Table 10	
30h		[7:6]	R		READ ONLY	
31h		[0]	W/E		WRITE-EXACT	
31h		[7:1]	R		READ ONLY	
32h		[7:0]	W/E		WRITE-EXACT	
33h	ON	[0]	R/W	REG3 Enable	0	REG3 Disable
					1	REG3 Enable
33h	OK	[1]	R	REG3 Power-OK	0	Output is not OK
					1	Output is OK
33h		[2]	W/E		WRITE-EXACT	
33h		[4:3]	R		READ ONLY	
33h		[7:5]	W/E		WRITE-EXACT	

REGISTER DESCRIPTIONS CONT'D

Table 10:

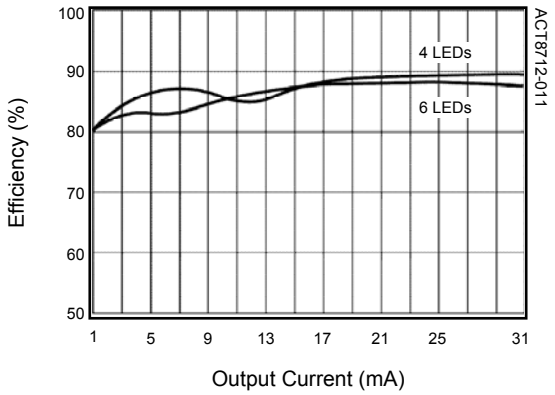
REG3/VSET[ ] Output Voltage Setting

REG3/VSET [2:0]	REG3/VSET[4:3]							
	REG3/VSET[5] = [0]				REG3/VSET[5] = [1]			
	00	01	10	11	00	01	10	11
000	5.00	7.00	9.00	11.00	13.00	17.00	21.00	25.00
001	5.25	7.25	9.25	11.25	13.50	17.50	21.50	25.50
010	5.50	7.50	9.50	11.50	14.00	18.00	22.00	26.00
011	5.75	7.75	9.75	11.75	14.50	18.50	22.50	26.50
100	6.00	8.00	10.00	12.00	15.00	19.00	23.00	27.00
101	6.25	8.25	10.25	12.25	15.50	19.50	23.50	27.50
110	6.50	8.50	10.50	12.50	16.00	20.00	24.00	28.00
111	6.75	8.75	10.75	12.75	16.50	20.50	24.50	28.50

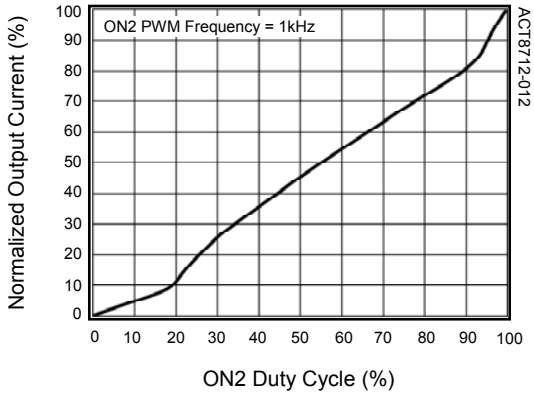
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8712QLEHA, V_{VSYS} = 3.6V, L = 22µH, C_{VP1} = C_{VP2} = 2.2µF, C_{OUT} = 2.2µF, T_A = 25°C, unless otherwise specified.)

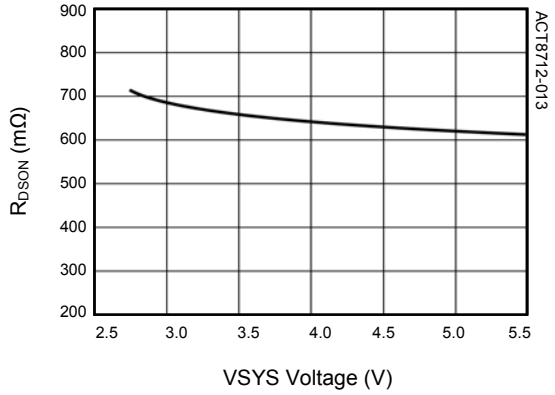
REG3 Efficiency vs. Output Current



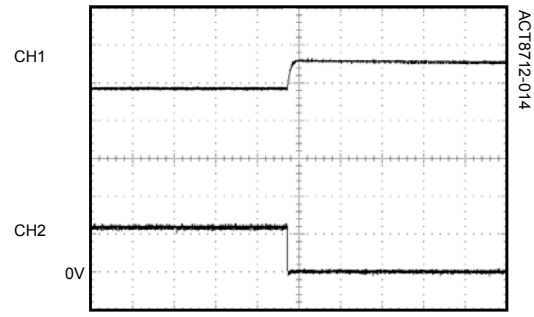
PWM Output Current Adjustment



REG3 R_{DSON}

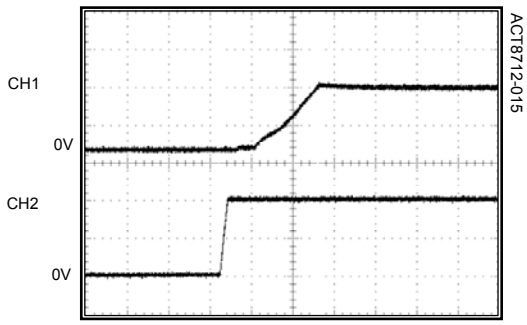


REG3 Over-Voltage Protection



CH1: V_{OUT3}, 10V/div
CH2: V_{FB3}, 200mV/div
TIME: 2ms/div

REG3 Startup Waveform



CH1: V_{OUT3}, 10V/div
CH2: V_{ON2}, 1V/div
TIME: 100µs/div

FUNCTIONAL DESCRIPTION

General Description

REG3 is a highly efficient step-up DC/DC converter that employs a fixed frequency, current-mode, PWM architecture. This regulator is optimized for white-LED bias applications consisting of up to seven white-LEDs.

Enabling and Disabling REG3

Enable/disable control of REG3 is done through a combination of the ACT8712's system control circuitry, the ON2 pin, and the REG3/ON[ ] bit. REG3 may be enabled when at least one of the following conditions exists:

1) A valid supply voltage is present at VIN
2) nMSTR is asserted low, or
3) ON1 is asserted high.

When any of these conditions exist, REG3 may be enabled by either of the following conditions:

1) ON2 is asserted high, or
2) REG3/ON[ ] is set to [1].

When disabled, REG3's quiescent supply current drops to just 1µA.

As with all non-synchronous step-up DC/DC converters, REG3's application circuit produces a DC current path between the input and the output in shutdown mode. Although the forward drop of the WLEDs makes this leakage current very small in most applications, it is important to consider the effect that this may have in your application particularly when using fewer than three WLEDs.

Over-Voltage Protection

REG3 features internal over-voltage protection (OVP) circuitry which protects the system from LED open-circuit fault conditions. If the voltage at OV ever reaches the over-voltage threshold, REG3 will regulate the top of the LED strong to the OVP threshold voltage. By default, the ACT8712's OVP threshold is set at 28.5V, although it may be programmed to a lower value by writing to the REG3/VSET[ ] register.

Power-OK Bit

REG3 feature a variety of status bits that can be read by the system microprocessor. If the voltage at OV is greater than the OVP threshold, REG3/OK[ ] will clear to 0.

Compensation and Stability

REG3 utilizes current-mode control and an internal compensation network to optimize transient performance, ease compensation, and improve stability over a wide range of operating conditions. REG3 is a flexible regulator, and its external components can be chosen to achieve the smallest possible footprint or to achieve the highest possible efficiency.

Inductor Selection

REG3 was designed to provide excellent performance across a wide range of applications, but was optimized for operation with inductors in the 10µH to 22µH range, although larger inductor values of up to 68µH can be used to achieve the highest possible efficiency.

Optimizing for Smallest Footprint

REG3 is capable of operating with very low inductor values in order to achieve the smallest possible footprint. When solution size is of primary concern, best results are achieved when using an inductor that ensures discontinuous conduction mode (DCM) operation over the full load current range.

Optimizing for Highest Efficiency

REG3 achieves excellent efficiency in applications that demand the longest possible battery life. When efficiency is the primary design consideration, best results are achieved when using an inductor that results in continuous conduction mode (CCM) operation and achieves very small inductor ripple current.

Output Capacitor Selection

REG3 was designed to operate with output capacitors ranging from 0.47µF to 10µF, providing design flexibility. A 1µF output capacitor is suitable for most

applications, although larger output capacitors may be used to minimize output voltage ripple, if needed. Ceramic capacitors are recommended for most applications.

Rectifier Selection

REG3 requires a Schottky diode to rectify the inductor current. Select a low forward voltage drop Schottky diode with a forward current (I_F) rating that is sufficient to support the maximum switch current and a sufficient peak repetitive reverse voltage (V_{RRM}) to support the output voltage.

Setting the LED Bias Current

The LED bias current is set by a resistor connected from FB3 and ground, and the regulator is satisfied when the LED current is sufficient to generate 250mV across this resistor. Once the bias current is programmed, the LED current can be adjusted using the ACT8712's Direct-PWM feature. REG3 is also compatible with a variety of well-known LED dimming circuits, such as with a DC control voltage and a filtered PWM signal.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout a very important part of the design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Step-up DC/DCs exhibit continuous input current, so there is some amount of flexibility in placing vias in the input capacitor circuit. The inductor, input filter capacitor, rectifier, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. Connect the ground nodes together in a star configuration, with a direct connection to the exposed pad. Finally, the exposed pad should be directly connected to the backside ground plane using multiple vias to achieve low electrical and thermal resistance. Note that since the LED string is a low, DC-current path, it does not generally require special layout consideration.

ELECTRICAL CHARACTERISTICS

(V_{VIN} = 5V, V_{BAT} = 3.6V, ISET[ ] = [0101], T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN Operating Voltage Range		4.3		6	V
VIN UVLO Threshold	V_{VIN} Voltage Rising	3.75	4	4.25	V
VIN UVLO Hysteresis	V_{VIN} Voltage Falling		500		mV
On-Resistance			300	500	mΩ
Battery Termination Voltage	T_A = 25°C	4.179	4.200	4.221	V
	V_{VIN} = 4.5V to 5.5V, T_A = 0°C to 85°C	4.158	4.200	4.242	
Line Regulation	V_{VIN} = 4.5V to 5.5V, I_{BAT} = 10mA		0.2		%/V
Load Regulation	I_{BAT} = 50mA to 500mA		0.001		%/mA
Charge Current	V_{BAT} = 4V, CHGLEV = GA		90	100	mA
	V_{BAT} = 4V, CHGLEV = VSYS	400	450	500	mA
Precondition Charge Current	V_{BAT} = 2.7V, CHGLEV = VSYS or GA	30	45	60	mA
Precondition Threshold Voltage	V_{BAT} Voltage Rising	2.75	2.9	3.05	V
Precondition Threshold Hysteresis	V_{BAT} Voltage Falling		150		mV
End-of-Charge Current Threshold	V_{BAT} = 4.2V, CHGLEV = VSYS	31	47	63	mA
End-of-Charge Delay			4		min
Charge Restart Threshold	VSET[ ] -V_{BAT}, V_{BAT} falling		200		mV
Thermal Regulation Threshold			110		°C
BAT Reverse Leakage Current	V_{BAT} = 4.2V, VIN = GA or BAT		0.4	2	μA
VIN Supply Current	V_{VIN} < UVLO Voltage		50		μA
	SLEEP, SUSPEND, or TIMER-FAULT state		200		
	PRECONDITION, FAST-CHARGE, or TOP-OFF state		700		
Precondition Timeout Period	TIMOSET[ ] = [01]		90		min
nSTAT Sink current	V_{nSTAT} = 2V	4	8	12	mA
nSTAT Output Low Voltage	I_{nSTAT} = 1mA			0.4	V
nSTAT Leakage Current	V_{nSTAT} = 6V			1	μA
CHGLEV Logic Low Input Voltage	I_{CHGLEV} ≤ -15μA			0.4	V
CHGLEV Tri-state Current Threshold①		-2		2	μA
CHGLEV Logic High Input Voltage	I_{CHGLEV} ≥ 15μA	1.4			V

①: Charger is suspended when CHGLEV pin current is within this range

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 11:

Battery Charger (CHGR) Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
08h	ISET1				R	R	R	R
09h	TIMOSET		R	BATFLT	TIMOFLT	TEMPFLT	CHGRSTAT	VINPOK
0Ah	ISET2				R	R	R	R
0Bh	R	R	R	R	W/E	ICHGSET	CHGROK	SUSCHG

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1.

Table 12:

Battery Charger (CHGR) Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
08h		[3:0]	R		READ ONLY	
08h	ISET1	[7:4]	R/W	ISET1 Charger Current Selection	See Tables 13 and 14	
09h	VINPOK	[0]	R	Input Supply Power-OK	0	Input Power is not OK
					1	Input Power is OK
09h	CHGRSTAT	[1]	R	Charging Status	0	Not Charging
					1	Charging
09h	TEMPFLT	[2]	R	Temperature Status	0	Temperature Fault
					1	No Timeout Fault
09h	TIMOFLT	[3]	R	Timeout Fault	0	No Timeout Fault
					1	Timeout Fault
09h	BATFLT	[4]	R	Battery Removed Fault	0	Battery Not Removed
					1	Battery Removed
09h		[5]	R		READ ONLY	
09h	TIMOSET	[7:6]	R/W	Charge Timeout Select	00	60mins
					01	90mins
					10	120mins
					11	No Timeout
0Ah		[3:0]	R		READ ONLY	
0Ah	ISET2	[7:4]	R/W	ISET2 Charger Current Selection	See Tables 13 and 14	

REGISTER DESCRIPTIONS CONT'D

Table 12:

Battery Charger (CHGR) Control Register Bit Descriptions (Cont'd)

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
0Bh	SUSCHG	[0]	R/W	Suspend Charging	0	Charging Enable
					1	Charging Disable
0Bh	CHGROK	[1]	R	Charge Status	0	Charging Error Occurred
					1	Charging OK
0Bh	ICHGSET	[2]	R/W	Charge Current Selection①	0	90mA
					1	450mA
0Bh		[3]	W/E		WRITE-EXACT	
0Bh		[7:4]	R		READ ONLY	

①: ICHGSET only has affect when CHGLEV = 0 and ISET2[3:0] = [0000]

Table 13:

Charge Current Setting for CHGLEV = 0

CHGLEV = 0		
ISET1[3:0]	ISET2[3:0]	CURRENT(mA)
Any Value	0000	90 if ICHGSET = 0
		450 if ICHGSET = 1
	0001	300
	0010	350
	0011	400
	0100	450
	0101	500
	0110	550
	0111	600
	1000	650
	1001	700
	1010	750
	1011	800
	1100	850
	1101	900
	1110	950
	1111	1000

Table 14:

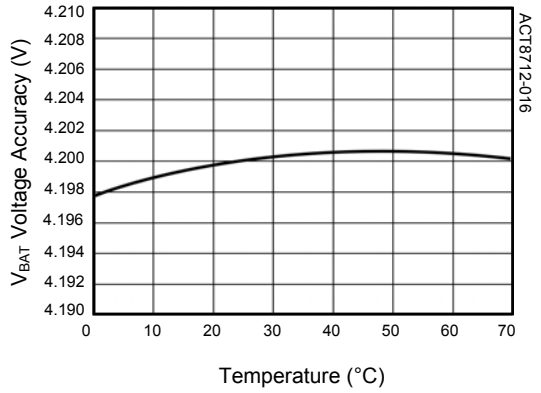
Charge Current Setting for CHGLEV = 1

CHGLEV = 1		
ISET1[3:0]	ISET2[3:0]	CURRENT(mA)
0000	Any Value	450
0001		300
0010		350
0011		400
0100		450
0101		500
0110		550
0111		600
1000		650
1001		700
1010		750
1011		800
1100		850
1101		900
1110		950
1111		1000

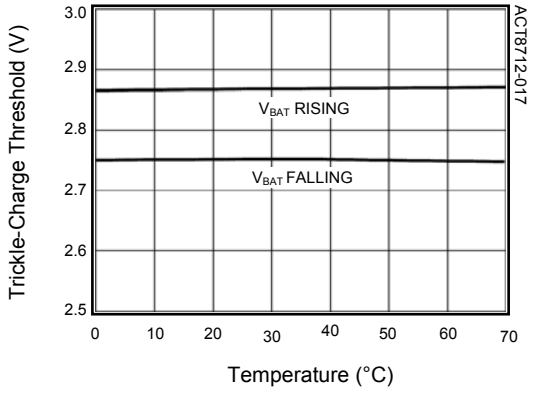
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8712QLEHA, V_{VIN} = 5V, T_A = 25°C, unless otherwise specified.)

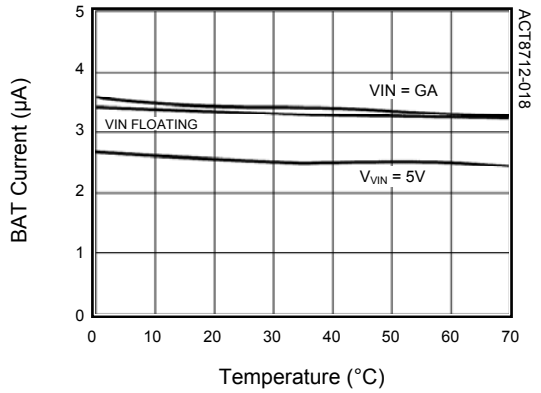
Charge Termination Voltage



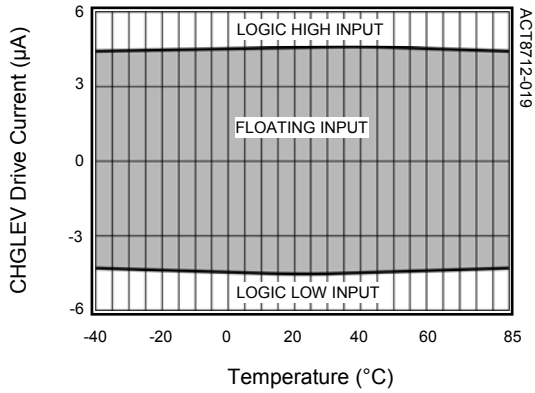
Trickle-Charge Threshold



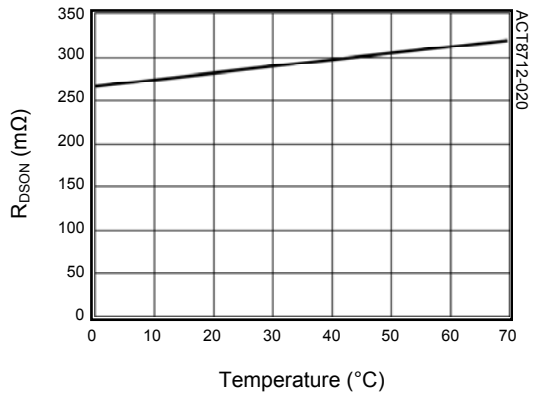
SUSPEND Mode Battery Current



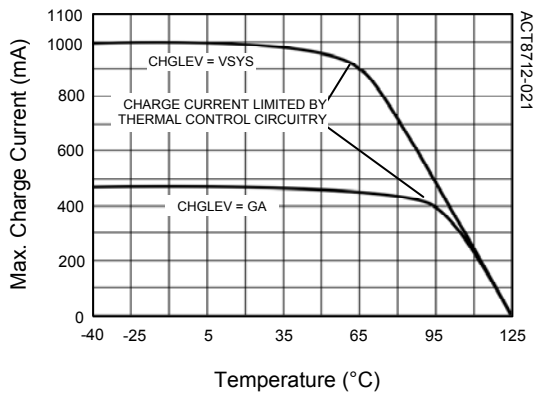
CHGLEV Drive Current Threshold



MOSFET Resistance



Maximum Charge Current



FUNCTIONAL DESCRIPTION

General Description

The ACT8712's internal battery charger is a full-featured, intelligent, linear-mode, single-cell charger for Lithium-based cells. This charger provides a complete selection of advanced functions and requires minimum system design effort.

The core of the charger is a CC/CV (Constant- Current/Constant-Voltage), linear-mode charge controller with a highly-accurate charge termination threshold. This controller incorporates current and voltage sense circuitry, an internal power MOSFET, a full-featured state-machine that implements charge control and safety features, and circuitry that eliminates the reverse-blocking diode required by conventional charger designs. The ACT8712's charger also features thermal-regulation circuitry that protects it against excessive junction temperature, allowing the fastest possible charging times, as well as proprietary input protection circuitry that makes the charger robust against input voltage transients that can damage other chargers.

CC/CV Regulation Loop

At the core of the ACT8712's battery charger is a CC/CV regulation loop, which regulates either current or voltage as necessary to ensure fast and safe charging of the battery. In a normal charge cycle, this loop regulates the charge current to the programmed charge current level and continues charging at this current until the battery cell voltage reaches the charge termination voltage. Once the cell reaches the Charge-Termination Threshold Voltage, the CV loop takes over and charge current is allowed to decrease as necessary to keep the cell voltage at the charge termination voltage.

Charger Enable/Disable

When a valid input voltage is applied to VIN, the battery charger is automatically enabled in order to simplify system design and eliminate the need for external input supply detection circuitry.

Once the charger is enabled, a charge cycle automatically begins unless CHGLEV is floating, CHGR/SUSCHG[ ] is set to [1], or a fault condition has occurred.

Charger Status

During normal operation, the processor can read the status of the input supply by reading CHGR/VINPOK[ ], which is set to [1] when the following conditions are true:

1) The voltage at VIN is greater than the voltage at BAT, and
2) The voltage at VIN is greater than the VIN UVLO threshold.

Alternatively, the processor can read the status of the charger by reading the CHGR/CHGROK[ ] bit, which is set to [1] when the following conditions are true:

1) The voltage at VIN is greater than the voltage at BAT, and
2) The voltage at VIN is greater than the VIN UVLO threshold, and
3) No fault has occurred.

Finally, the status of a charge cycle can be determine by reading the CHGR/CHGSTAT[ ] bit or by evaluating the state of the nSTAT output. nSTAT is an open-drain output that has an internal 8mA current limit, and is capable of directly driving LEDs for a visual charge-status indication without the need of current-limiting resistors or other external circuitry. To drive an LED, simply connect the LED between an appropriate supply, typically VIN, and nSTAT. When a logic-level charge status indicator is desired, simply connect a pull-up resistor of 10kΩ or more from nSTAT to OUT2 or another suitable supply.

CHGR/CHGSTAT[ ] is set to [1] and nSTAT sinks current when any of the following conditions are true:

1) The charger is operating in the PRECONDITION state, or
2) The charger is operating in the FAST-CHARGE state, or
3) The charger is operating in the TOP-OFF state.

When none of these conditions are true, CHGR/CHGSTAT[ ] is cleared to [0] and nSTAT goes into a high-Z state.

Input Capacitor Selection

VIN is the power input pin for the ACT8712 battery charger. The battery charger is automatically enabled whenever a valid voltage is present on VIN. In most applications, VIN is connected to either a wall adapter or a USB port. Under normal operation, the input of the charger will often be "hot-plugged" directly to a powered USB or a wall adapter cable, and supply voltage ringing and overshoot may appear at the VIN pin and can potentially be large enough to damage the charger input. In most applications, a capacitor connected from VIN to GA, placed as close as possible to the IC, is sufficient to absorb the energy. The VIN pin is designed for enhanced robustness and has an absolute maximum transient voltage rating of +7V, and attention must be given to bypass techniques to ensure operation within this limit.

Charge Current Programming

Charge current programming is performed using a combination of the ACT8712's CHGR/ISET1[ ] and CHGR/ISET2[ ] registers and the multifunction CHGLEV input. The multi-function CHGLEV input provides charge-current selection between the current setting defined by CHGR/ISET1[ ] and the current setting programmed by CHGR/ISET2[ ], as well as a charge suspend function. Drive CHGLEV to a logic-low to select the current programmed by CHGR/ISET1[ ]. In order to reduce the number of GPIOs required to interface with the ACT8712, the CHGR/ICHGSET[ ] bit may be used instead of the CHGLEV pin to achieve identical functionality.

By default, the ACT8712's CHGR/ISET1[ ] and CHGR/ISET2[ ] registers are programmed to provide a charge current of 90mA when CHGLEV is driven low, and 450mA when CHGLEV is driven high, so that the ACT8712 is compatible with system that utilize lower-current input supplies, such as a USB port. To achieve a different charge current, program the CHGR/ISET1[ ] and/or CHGR/ISET2[ ] registers accordingly.

Charge Safety Timer

The ACT8712 features a programmable charge safety timer that is utilized during operation in the PRECONDITION state. The safety timer has a default timeout period of 60 minutes, although it may be programmed to either 90 minutes or 120 minutes by writing to the CHGR/TIMOSET[ ] register. This register also provides a timer-disable function, for applications that do not require a charge safety timer function.

Thermal Regulation

The ACT8712 features an internal thermal feedback loop that reduces the charging current as necessary to ensure that the die temperature does not exceed the thermal regulation threshold of 110°C. This feature protects the ACT8712 against excessive junction temperature and makes the ACT8712 more accommodating of aggressive thermal designs without risk of damage. Note, however, that attention to good thermal design is required to achieve the shortest possible charge time.

Charge Status Bits

The ACT8712 charger provides a variety of read-only charge status bits that can be read by the host processor as needed to make intelligent power management decisions. Five charge status bits are available:

Input Voltage Status

The CHGR/VINPOK[ ] bit is set to [1] when a valid input supply is connected to VIN. A valid input supply is defined as one that :

1) is greater than the voltage at BAT, and

2) is greater than the VIN UVLO threshold.

Charger Status

There are two bits available that describe the current status of the charger itself.

The CHGR/CHGSTAT[ ] bit is set to [1] when the charger is actively charging the battery, and is cleared to [0] when a charge cycle terminates or is suspended.

The CHGR/CHGROK[ ] bit is set to [1] when TBD, and is cleared otherwise.

Timeout Fault

The CHGR/TIMOFLT[ ] bit is set to [1] when a timeout fault occurs, and remains cleared otherwise. Once set to [1], it is automatically cleared to [0] when TBD.

Battery Removed Fault

The CHGR/BATFLT[ ] bit is set to [1] when there is no battery connected, and remains cleared otherwise.

Reverse Leakage Current

The ACT8712 includes internal circuitry that eliminates the need for series blocking diodes, reducing solution size and cost as well as dropout voltage relative to conventional battery chargers. When the input supply is removed, when V_{VIN} goes below its under-voltage-lockout (UVLO) voltage, or when V_{VIN} drops below V_{BAT}, the ACT8712 automatically goes into SUSPEND mode and reconfigures its power switch to minimize current drain from the battery.

Charger State Machine

PRECONDITION State

A new charging cycle begins in the PRECONDITION state. In this state, the cell is charged at a reduced current of either 45mA or 10% of the selected maximum fast-charge current, whichever is greater. During a normal charge cycle, charging continues at this rate until V_{BAT} reaches the Precondition Threshold Voltage, at which point the state machine jumps to the FAST-CHARGE state. If V_{BAT} does not reach the Precondition Threshold Voltage before the Precondition Charge Timeout period expires, then a damaged cell is detected and the state machine jumps to the TIMEOUT-FAULT state.

FAST-CHARGE State

In the FAST-CHARGE state the charger operates in Constant-Current (CC) mode and charges the cell at the programmed charge current. During a normal charge cycle, constant-current charging continues until V_{BAT} reaches the charge termination voltage, at which point the state machine jumps to the TOP-OFF state.

TOP-OFF State

In the TOP-OFF state the cell is charged in Constant-Voltage (CV) mode with the charge current limited by the internal chemistry of the cell, decreasing as the cell charges. A normal charging cycle continues until the charge current decreases to below the End-Of-Charge (EOC) threshold. In order to improve immunity to conditions that can result in false-EOC detection, the charging continues until the EOC condition persists for 4 consecutive minutes. Once this condition is met, the charge cycle is terminated and the state machine jumps to the SLEEP state.

SLEEP State

In the SLEEP state the ACT8712 presents a high-impedance to the battery, allowing the cell to “relax” and minimizing battery leakage current. The ACT8712 continues to monitor the cell voltage, however, so that it can reinitiate a charging cycle as necessary to ensure that the cell remains fully charged.

Charge Restart

After a charge cycle successfully terminates, the ACT8712 jumps to its SLEEP state to minimize battery drain, but continues to actively monitor the cell voltage. A new charging cycle begins when the cell voltage has dropped by 200mV (typ), keeping the cell fully charged. This charge restart process minimizes cycle-life degradation of the cell by allowing it to “relax” between charges, while ensuring that the cell remains fully-charged while connected to a power source.

SUSPEND State

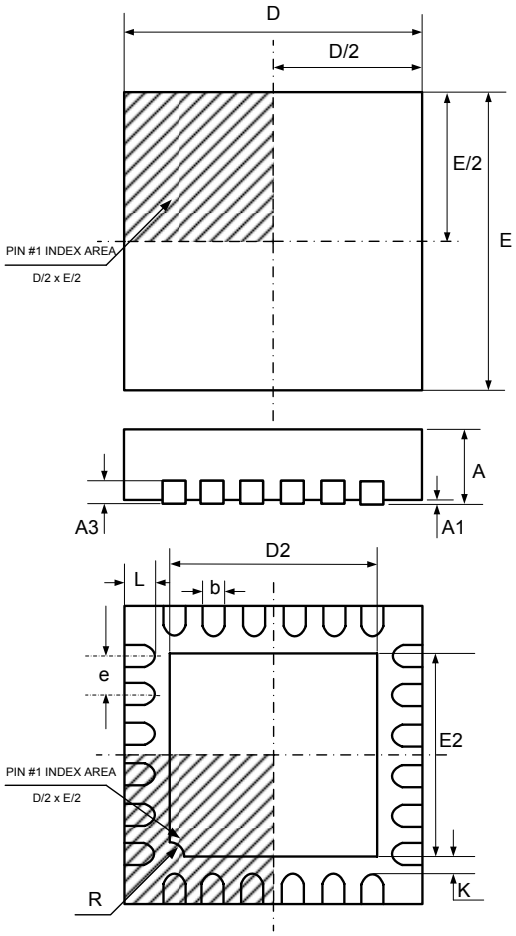
When in the SUSPEND state, the charger is disabled and the charger presents a high-impedance to the battery, but the charge-control circuitry remains functional. When exiting the SUSPEND state, the charge timer is reset and the state machine jumps to the PRECONDITION state.

TIMEOUT-FAULT State

When a TIMEOUT-FAULT occurs, charging is suspended, CHGR/TIMOFLT[ ] is set to [1], and the charger presents a high-impedance to the battery. To maximize safety, there is no direct path to resume charging from the TIMEOUT-FAULT state. A new charging cycle may only be initiated if the state machine first jumps to the SUSPEND state then each of the conditions necessary to enter the PRECONDITION state are satisfied.

PACKAGE OUTLINE

TQFN44-24 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.200 REF		0.008 REF	
b	0.180	0.300	0.007	0.012
D	3.850	4.150	0.152	0.163
E	3.850	4.150	0.152	0.163
D2	2.500	2.800	0.098	0.110
E2	2.500	2.800	0.098	0.110
e	0.500 BSC		0.020 BSC	
L	0.350	0.450	0.014	0.018
R	0.200 TYP		0.008 TYP	
K	0.200	---	0.008	---

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