ACT8796

Rev1, 10-Oct-08

Six Channel Integrated Power Management IC for Handheld Portable Equipment

FEATURES

- **Multiple Patents Pending**
- **Six Integrated Regulators**
  - **750mA PWM Step-Down DC/DC**
  - **750mA PWM Step-Down DC/DC**
  - **550mA PWM Step-Down DC/DC**
  - **250mA Low Noise LDO**
  - **250mA Low Noise LDO**
  - **250mA Low Noise LDO**
- **I²C™ Compatible Serial Interface**
  - **Programmable Output Voltages**
  - **Configurable Operating Modes**
- **Minimal External Components**
- **4x4mm, Thin-QFN (TQFN44-24) Package**
  - **Only 0.75mm Height**
  - **RoHS Compliant**

APPLICATIONS

- **Portable Devices and PDAs**
- **Wireless Handhelds**
- **DMB Enabled Devices**
- **GPS Receivers, etc.**

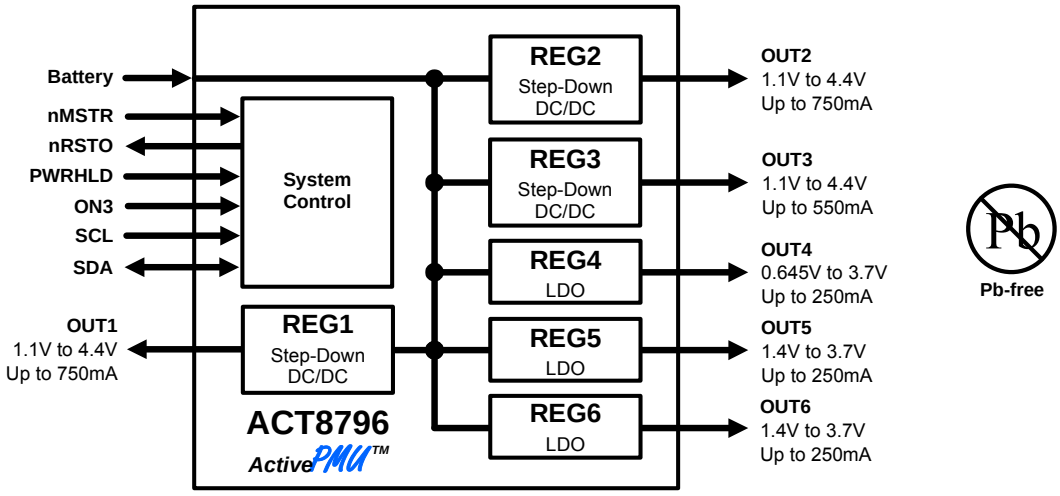
GENERAL DESCRIPTION

The patent-pending ACT8796 is a complete, cost-effective, highly-efficient *ActivePMU™* power management solution that is ideal for a wide range of portable handheld equipment. This device integrates three step-down DC/DC converters and three low dropout linear regulators (LDOs) into a single, thin, space-saving package. An I²C Serial Interface provides programmability for the DC/DC converters and LDOs.

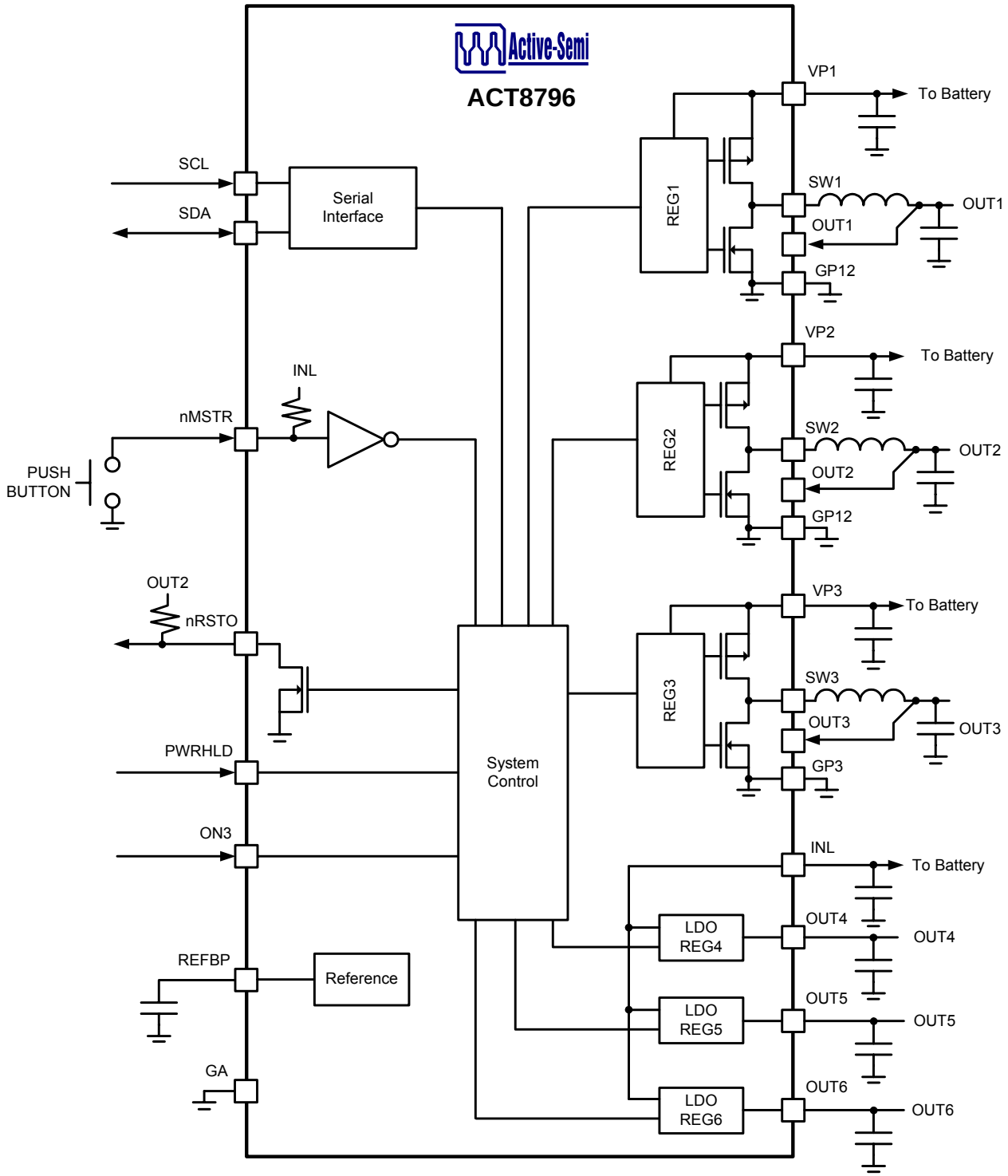
REG1, REG2 and REG3 are fixed-frequency, current-mode PWM step-down DC/DC converters that are optimized for high efficiency and are capable of supplying up to 750mA, 750mA and 550mA, respectively. REG4, REG5 and REG6 are low noise, high PSRR linear regulators that are capable of supplying up to 250mA each.

The ACT8796 is available in a tiny 4mm x 4mm 24-pin Thin-QFN package that is just 0.75mm thin.

SYSTEM BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①②

PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	PACKAGE	PINS	TEMPERATURE RANGE
ACT8796QLGHW-T	3.0V	3.3V	1.35V	1.35V	2.8V	1.8V	TQFN44-24	24	-40°C to +85°C

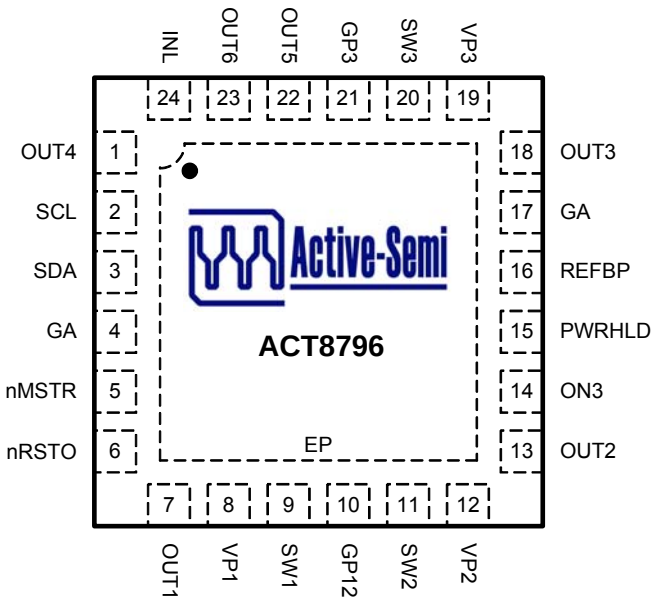
OUTPUT VOLTAGE CODES (V_{OUT1} AND V_{OUT2})						
C	D	E	F	G	H	I
1.2V	1.5V	1.8V	2.5V	3.0V	3.3V	2.8V

①: Output voltage options detailed in this table represent standard voltage options, and are available for samples or production orders. Additional output voltage options, as detailed in the *Output Voltage Codes* table, are available for production subject to minimum order quantities. Contact Active-Semi for more information regarding semi-custom output voltage combinations.

②: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

PIN CONFIGURATION

TOP VIEW



Thin - QFN (TQFN44-24)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	OUT4	Output Voltage for REG4. Capable of delivering up to 250mA of output current. The output is discharged to G with 650Ω load when disabled.
2	SCL	Clock Input for I^{2}C Serial Interface. Data is read on the rising edge of the clock.
3	SDA	Data Input for I^{2}C Serial Interface. Data is read on the rising edge of the clock.
4, 17	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP12, and GP3 together at a single point as close to the IC as possible.
5	nMSTR	Master Enable Input. Drive nMSTR to GA or to a logic low to enable the IC. REG1, REG2, and REG3 are enabled while nMSTR is asserted.
6	nRSTO	Open-Drain Reset Output. nRSTO asserts low for the reset timeout period of 300ms whenever the IC is enabled.
7	OUT1	Output Feedback Sense for REG1. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
8	VP1	Power Input for REG1. Bypass to GP12 with a high quality ceramic capacitor placed as close as possible to the IC.
9	SW1	Switching Node Output for REG1. Connect this pin to the switching end of the inductor.
10	GP12	Power Ground for REG1 and REG2. Connect GA, GP12, and GP3 together at a single point as close to the IC as possible.
11	SW2	Switching Node Output for REG2. Connect this pin to the switching end of the inductor.
12	VP2	Power Input for REG2. Bypass to GP12 with a high quality ceramic capacitor placed as close as possible to the IC.
13	OUT2	Output Feedback Sense for REG2. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
14	ON3	Enable Input for REG3, ON3 is functional only when PWRHLD is driven high. Drive ON3 to a logic high to turn on the REG3. Drive ON3 to a logic low to turn off the REG3.
15	PWRHLD	Power Hold Input. Drive PWRHLD to logic high to enable the IC. Drive PWRHLD to a logic low to disable all regulators.
16	REFBP	Reference Noise Bypass. Connect a 0.01µF ceramic capacitor from REFBP to GA. This pin is discharged to GA in shutdown.
18	OUT3	Output Feedback Sense for REG3. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
19	VP3	Power Input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close as possible to the IC.
20	SW3	Switching Node Output for REG3. Connect this pin to the switching end of the inductor.
21	GP3	Power Ground for REG3. Connect GA, GP12, and GP3 together at a single point as close to the IC as possible.
22	OUT5	Output Voltage for REG5. Capable of delivering up to 250mA of output current. The output is discharged to G with 650Ω load when disabled.
23	OUT6	Output Voltage for REG6. Capable of delivering up to 250mA of output current. The output is discharged to G with 650Ω load when disabled.
24	INL	Power Input for REG4, REG5 and REG6. Bypass to GA with a high quality ceramic capacitor placed as close as possible to the IC.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VP1, VP2, SW1, SW2 to GP12 VP3, SW3 to GP3 SCL, SDA, INL, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, ON3, REFBP, nRSTO, PWRHLD, nMSTR to GA	-0.3 to +6	V
SW1 to VP1 SW2 to VP2 SW3 to VP3	-6 to +0.3	V
GP12, GP3 to GA	-0.3 to +0.3	V
Junction to Ambient Thermal Resistance (θ_{JA})	30	°C/W
RMS Power Dissipation (T_A = 70°C)	1.8	W
Operating Temperature Range	-40 to 85	°C
Junction Temperature	125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

REGISTER DESCRIPTIONS

Table 1:

Global Register Map

OUTPUT	ADDRESS									DATA (DEFAULT VALUE)							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
REG1	10h	0	0	0	1	0	0	0	0	R	V	V	V	V	V	V	V
REG1	11h	0	0	0	1	0	0	0	1	R	R	R	R	R	R	R	0
REG1	12h	0	0	0	1	0	0	1	0	R	R	R	R	R	R	R	R
REG1	13h	0	0	0	1	0	0	1	1	R	R	R	R	R	0	R	1
REG2	20h	0	0	1	0	0	0	0	0	R	V	V	V	V	V	V	V
REG2	21h	0	0	1	0	0	0	0	1	R	R	R	R	R	R	R	0
REG2	22h	0	0	1	0	0	0	1	0	R	R	R	R	R	R	R	R
REG2	23h	0	0	1	0	0	0	1	1	R	R	R	R	R	0	R	1
REG3	30h	0	0	1	1	0	0	0	0	R	V	V	V	V	V	V	V
REG3	31h	0	0	1	1	0	0	0	1	R	R	R	R	R	R	R	0
REG3	32h	0	0	1	1	0	0	1	0	R	R	R	R	R	R	R	R
REG3	33h	0	0	1	1	0	0	1	1	R	R	R	R	R	0	R	1
REG4	03h	0	0	0	0	0	0	1	1	R	V	V	V	V	V	V	V
REG4	40h	0	1	0	0	0	0	0	0	R	R	0	R	R	R	R	R
REG5	41h	0	1	0	0	0	0	0	1	R	R	0	V	V	V	V	V
REG6	42h	0	1	0	0	0	0	1	0	R	R	0	V	V	V	V	V
REG456CFG	43h	0	1	0	0	0	0	1	1	R	R	R	1	1	1	0	R

KEY:

R: Read-Only bits. No Default Assigned.

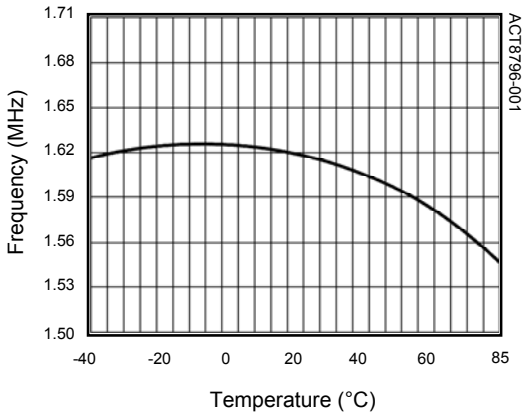
V: Default Values Depend on Voltage Option. Default Values May Vary.

Note: Addresses other than those specified in Table 1 may be used for factory settings. Do not access any registers other than those specified in Table 1.

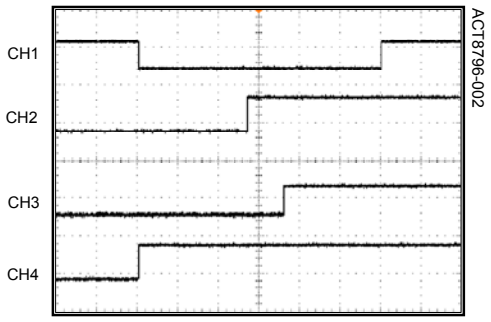
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

Oscillator Frequency vs. Temperature



Startup Sequence



CH1: V_{nMSTR}, 5V/div
CH2: V_{nRSTO}, 2V/div
CH3: V_{PWRHLD}, 5V/div
CH4: V_{OUT1}, 2V/div
TIME: 100ms/div

ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, T_A = 25°C, unless otherwise specified.)

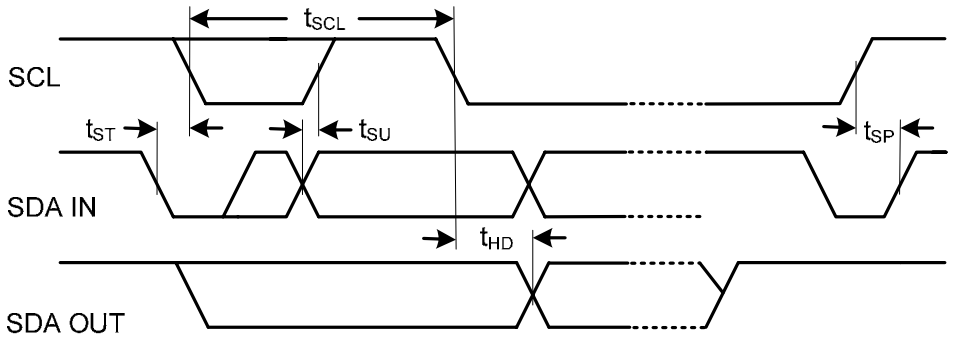
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL Operating Voltage Range		2.6		5.5	V
INL UVLO Threshold	INL Voltage Rising	2.25	2.4	2.55	V
INL UVLO Hysteresis	INL Voltage Falling		80		mV
Oscillator Frequency		1.35	1.6	1.85	MHz
INL Supply Current	PWRHLD = ON3 = GA		1.5		µA
nMSTR Internal Pull-Up Resistance		250	500		kΩ
Logic High Input Voltage	PWRHLD, ON3, nMSTR	1.4			V
Logic Low Input Voltage	PWRHLD, ON3, nMSTR			0.4	V
Logic Low Output Voltage	I_{SINK} = 5mA			0.3	V
Leakage Current	nRSTO, V_{nRSTO} = 4.2V			1	µA
nRSTO Delay		240	300	360	ms
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis	Temperature falling		20		°C

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Low Input Voltage				0.4	V
SCL, SDA High Input Voltage		1.4			V
SCL, SDA Leakage Current				1	µA
SDA Low Output Voltage	I_{OL} = 5mA			0.3	V
SCL Clock Period, t_{SCL}	f_{SCL} clock freq = 400kHz	2.5			µs
SDA Data In Setup Time to SCL High, t_{SU}		100			ns
SDA Data Out Hold Time after SCL Low, t_{HD}		300			ns
SDA Data Low Setup Time to SCL Low, t_{ST}	Start Condition	100			ns
SDA Data High Hold Time after Clock High, t_{HP}	Stop Condition	100			ns

Figure 1:
I²C Serial Bus Timing



FUNCTIONAL DESCRIPTION

General Description

The ACT8796 offers an array of system management functions that allow it to provide optimal performance in a wide range of applications.

I²C Serial Interface

At the core of the ACT8796's flexible architecture is an I²C interface that permits optional programming capability to enhance overall system performance.

To ensure compatibility with a wide range of system processors, the ACT8796 uses standard I²C commands; I²C write-byte commands are used to program the ACT8796, and I²C read-byte commands are used to read the ACT8796's internal registers. The ACT8796 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011011x].

SDA is a bi-directional data line and SCL is a clock input. The master initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an Acknowledge (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I²C 2-wire serial interface, go to the NXP website: http://www.nxp.com

System Startup and Shutdown

The ACT8796 features a flexible control architecture that supports a variety of software-controlled enable/disable functions that make it a simple yet flexible and highly configurable solution. The ACT8796 is automatically enabled when either of the following conditions exists:

1) nMSTR is asserted low, or

2) PWRHLD is asserted high.

If either of these conditions is true, the ACT8796 enables REG1, REG2, REG4, and may be REG3 powering up the system processor so that the startup and shutdown sequences may be controlled via software. These startup conditions are described in detail below.

Manual Enable Due to Asserting nMSTR Low

System startup is initiated when the user presses the push-button, asserting nMSTR low. When this occurs, REG1, REG2, REG3, and REG4 are enabled and nRSTO is asserted low to hold the microprocessor in RESET for 260ms. nRSTO goes high-Z upon expiration of the reset timer, de-asserting the processor's reset input and allowing the microprocessor to initiate its power up sequence. Once the power-up routine is successfully completed, the microprocessor must assert PWRHLD so that the ACT8796 remains enabled after the push-button is released by the user. Upon completion of the start-up sequence the processor assumes control of the power system and all further operation is software-controlled.

Manual Enable Due to Asserting PWRHLD High

The ACT8796 is compatible with applications that do not utilize its push-button control function, and may be enabled by simply driving PWRHLD to a logic-high to enable REG1, REG2, and REG4. In this case, the signal driving PWRHLD controls enable/disable timing, although software-controlled enable/disable sequences are still supported if the processor assumes control of the power system once the startup sequence is completed.

Shutdown Sequence

Once a successful power-up routine is completed, the system processor controls the operation of the power system, including the system shutdown timing and sequence. When using the application circuits shown in Figure 2, the nIRQ signal is asserted when nMSTR is asserted low, providing a simple means of alerting the system processor when the user wishes to shut the system down. Asserting nIRQ interrupts the system processor, initiating an interrupt service routine in the processor which will reveal that the user pressed the push-button. The microprocessor may validate the input, such as by ensuring that the push-button is asserted for a minimum amount of time, then initiates a software controlled power-down routine, the final step of which is to de-assert the PWRHLD input, disabling the regulators and shutting the system down.

FUNCTIONAL DESCRIPTION (CONT'D)

nMSTR Enable Input

In most applications, connect nMSTR to an active low, momentary push-button switch to utilize the ACT8796's closed-loop enable/disable functionality. If a momentary-on switch is not used, drive nMSTR to GA or to a logic low to initiate a startup sequence.

Enable/Disable Inputs

The ACT8796 provides two manual enable/disable inputs, PWRHLD and ON3. PWRHLD is the master enable input. When driven high, PWRHLD enables REG1, REG2, and REG4, and also activates the enable/disable control logic for the other regulators. ON3 is the enable input for REG3, and is active when either of the following conditions exists:

1) nMSTR is asserted low, or

2) PWRHLD is asserted high.

Power-On Reset Output

The ACT8796 integrates a 260ms power-on reset generator, reducing system size and cost. nRSTO is an open-drain output. Connect a 10kΩ or greater pull-up resistor from nRSTO to an appropriate voltage supply. nRSTO asserts low upon startup and remains low until the reset-timeout period expires, at which point nRSTO goes high-Z.

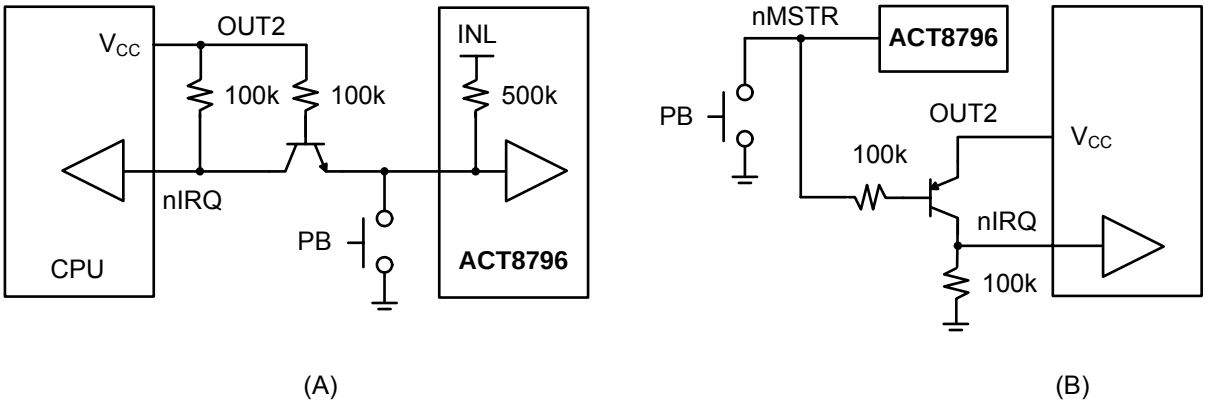
nIRQ Output

Figure 2 shows two simple circuits that can be used to generate nIRQ, a processor interrupt signal, which can be used as part of the ACT8796's push-button control logic. This signal is typically used to drive the interrupt input of the system processor, and is useful in a variety of software-controlled enable/disable control routines. Figure 2A provides an active-low, open-collector push-button status output that sinks current when nMSTR is driven to a logic-low. Figure 2B provides an active-high, open-collector push-button status output that sources current when nMSTR is driven to a logic-low.

Thermal Shutdown

The ACT8796 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions. This circuitry disables all regulators if the ACT8796 die temperature exceeds 160°C, and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

Figure 2:
Simple Circuits



(A) (B)

ELECTRICAL CHARACTERISTICS (REG1)

(V_{VP1} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP1 Operating Voltage Range		3.1		5.5	V
VP1 UVLO Threshold	Input Voltage Rising	2.9	3	3.1	V
VP1 UVLO Hysteresis	Input Voltage Falling		80		mV
Standby Supply Current			130	200	µA
Shutdown Supply Current	REG1 is disabled, V_{VP1} = 4.2V		0.1	1	µA
Output Voltage Regulation Accuracy	V_{NOM1} < 1.3V, I_{OUT1} = 10mA	-2.4%	V_{NOM1}①	+1.8%	V
	V_{NOM1} ≥ 1.3V, I_{OUT1} = 10mA	-1.2%	V_{NOM1}	+1.8%	
Line Regulation	V_{VP1} = Max(V_{NOM1} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT1} = 10mA to 750mA		0.0017		%/mA
Current Limit		0.85	1.1		A
Oscillator Frequency	V_{OUT1} ≥ 20% of V_{NOM1}	1.35	1.6	1.85	MHz
	V_{OUT1} = 0V		530		kHz
PMOS On-Resistance	I_{SW1} = -100mA		0.28	0.50	Ω
NMOS On-Resistance	I_{SW1} = 100mA		0.20	0.35	Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM1}
Minimum On-Time			70		ns

①: V_{NOM1} refers to the nominal output voltage level for V_{OUT1} as defined by the *Ordering Information* section.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 2:

REG1 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
10h	R	VRANGE	VSET					
11h	R	R	R	R	R	R	R	MODE
12h	R	R	R	R	R	R	R	R
13h	R	R	R	R	R	W/E	OK	ON

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1

Table 3:

REG1 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
10h	VSET	[5:0]	R/W	REG1 Output Voltage Selection	See Table 4	
10h	VRANGE	[6]	R/W	REG1 Voltage Range Selection	0	Min V_{OUT} = 1.1V
					1	Min V_{OUT} = 1.25V
10h		[7]	R		READ ONLY	
11h	MODE	[0]	R/W	Mode Selection	0	PWM/PFM
					1	Forced PWM
11h		[7:1]	R		READ ONLY	
12h		[7:0]	R		READ ONLY	
13h	ON	[0]	R/W	REG1 Enable	0	REG1 Disable
					1	REG1 Enable
13h	OK	[1]	R	REG1 Power-OK	0	Output is not OK
					1	Output is OK
13h		[2]	W/E		WRITE-EXACT	
13h		[7:3]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 4:
REG1/VSET[ ] Output Voltage Setting

REG1/VSET[3:0]	REG1/VSET[5:4]							
	REG1/VRANGE[ ] = [0]				REG1/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	N/A	N/A	1.455	1.860	1.250	2.050	2.850	3.650
0001	N/A	N/A	1.480	1.890	1.300	2.100	2.900	3.700
0010	N/A	1.100	1.505	1.915	1.350	2.150	2.950	3.750
0011	N/A	1.125	1.530	1.940	1.400	2.200	3.000	3.800
0100	N/A	1.150	1.555	1.965	1.450	2.250	3.050	3.850
0101	N/A	1.175	1.585	1.990	1.500	2.300	3.100	3.900
0110	N/A	1.200	1.610	2.015	1.550	2.350	3.150	3.950
0111	N/A	1.225	1.635	2.040	1.600	2.400	3.200	4.000
1000	N/A	1.255	1.660	2.065	1.650	2.450	3.250	4.050
1001	N/A	1.280	1.685	2.090	1.700	2.500	3.300	4.100
1010	N/A	1.305	1.710	2.115	1.750	2.550	3.350	4.150
1011	N/A	1.330	1.735	2.140	1.800	2.600	3.400	4.200
1100	N/A	1.355	1.760	2.165	1.850	2.650	3.450	4.250
1101	N/A	1.380	1.785	2.190	1.900	2.700	3.500	4.300
1110	N/A	1.405	1.810	2.200	1.950	2.750	3.550	4.350
1111	N/A	1.430	1.835	2.245	2.000	2.800	3.600	4.400

(N/A): Not Available

ELECTRICAL CHARACTERISTICS (REG2)

(V_{VP2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP2 Operating Voltage Range		3.1		5.5	V
VP2 UVLO Threshold	Input Voltage Rising	2.9	3	3.1	V
VP2 UVLO Hysteresis	Input Voltage Falling		80		mV
Standby Supply Current			130	200	µA
Shutdown Supply Current	REG2 Disabled, V_{VP2} = 4.2V		0.1	1	µA
Output Voltage Regulation Accuracy	V_{NOM2} < 1.3V, I_{OUT2} = 10mA	-2.4%	V_{NOM2}①	+1.8%	V
	V_{NOM2} ≥ 1.3V, I_{OUT2} = 10mA	-1.2%	V_{NOM2}	+1.8%	
Line Regulation	V_{VP2} = Max(V_{NOM2} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT2} = 10mA to 750mA		0.0017		%/mA
Current Limit		0.85	1.1		A
Oscillator Frequency	V_{OUT2} ≥ 20% of V_{NOM2}	1.35	1.6	1.85	MHz
	V_{OUT2} = 0V		530		kHz
PMOS On-Resistance	I_{SW2} = -100mA		0.28	0.50	Ω
NMOS On-Resistance	I_{SW2} = 100mA		0.20	0.35	Ω
SW2 Leakage Current	V_{VP2} = 5.5V, V_{SW2} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM2}
Minimum On-Time			70		ns

①: V_{NOM2} refers to the nominal output voltage level for V_{OUT2} as defined by the *Ordering Information* section.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 5:

REG2 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
20h	R	VRANGE	VSET					
21h	R	R	R	R	R	R	R	MODE
22h	R	R	R	R	R	R	R	R
23h	R	R	R	R	R	W/E	OK	ON

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1

Table 6:

REG2 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
20h	VSET	[5:0]	R/W	REG2 Output Voltage Selection	See Table 7	
20h	VRANGE	[6]	R/W	REG2 Voltage Range Selection	0	Min V_{OUT} = 1.1V
					1	Min V_{OUT} = 1.25V
20h		[7]	R		READ ONLY	
21h	MODE	[0]	R/W	Mode Selection	0	PWM/PFM
					1	Forced PWM
21h		[7:1]	R		READ ONLY	
22h		[7:0]	R		READ ONLY	
23h	ON	[0]	R/W	REG2 Enable	0	REG2 Disable
					1	REG2 Enable
23h	OK	[1]	R	REG2 Power-OK	0	Output is not OK
					1	Output is OK
23h		[2]	W/E		WRITE-EXACT	
23h		[7:3]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 7:

REG2/VSET[ ] Output Voltage Setting

REG2/VSET[3:0]	REG2/VSET[5:4]							
	REG2/VRANGE[ ] = [0]				REG2/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	N/A	N/A	1.455	1.860	1.250	2.050	2.850	3.650
0001	N/A	N/A	1.480	1.890	1.300	2.100	2.900	3.700
0010	N/A	1.100	1.505	1.915	1.350	2.150	2.950	3.750
0011	N/A	1.125	1.530	1.940	1.400	2.200	3.000	3.800
0100	N/A	1.150	1.555	1.965	1.450	2.250	3.050	3.850
0101	N/A	1.175	1.585	1.990	1.500	2.300	3.100	3.900
0110	N/A	1.200	1.610	2.015	1.550	2.350	3.150	3.950
0111	N/A	1.225	1.635	2.040	1.600	2.400	3.200	4.000
1000	N/A	1.255	1.660	2.065	1.650	2.450	3.250	4.050
1001	N/A	1.280	1.685	2.090	1.700	2.500	3.300	4.100
1010	N/A	1.305	1.710	2.115	1.750	2.550	3.350	4.150
1011	N/A	1.330	1.735	2.140	1.800	2.600	3.400	4.200
1100	N/A	1.355	1.760	2.165	1.850	2.650	3.450	4.250
1101	N/A	1.380	1.785	2.190	1.900	2.700	3.500	4.300
1110	N/A	1.405	1.810	2.200	1.950	2.750	3.550	4.350
1111	N/A	1.430	1.835	2.245	2.000	2.800	3.600	4.400

(N/A): Not Available

ELECTRICAL CHARACTERISTICS (REG3)

(V_{VP3} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP3 Operating Voltage Range		3.1		5.5	V
VP3 UVLO Threshold	Input Voltage Rising	2.9	3	3.1	V
VP3 UVLO Hysteresis	Input Voltage Falling		80		mV
Standby Supply Current			130	200	µA
Shutdown Supply Current	REG3 Disabled, V_{VP3} = 4.2V		0.1	1	µA
Output Voltage Regulation Accuracy	V_{NOM3} < 1.3V, I_{OUT3} = 10mA	-2.4%	V_{NOM3}①	+1.8%	V
	V_{NOM3} ≥ 1.3V, I_{OUT3} = 10mA	-1.2%	V_{NOM3}	+1.8%	
Line Regulation	V_{VP3} = Max(V_{NOM3} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT3} = 10mA to 550mA		0.0017		%/mA
Current Limit		0.65	0.85		A
Oscillator Frequency	V_{OUT3} ≥ 20% of V_{NOM3}	1.35	1.6	1.85	MHz
	V_{OUT3} = 0V		530		kHz
PMOS On-Resistance	I_{SW3} = -100mA		0.35	0.60	Ω
NMOS On-Resistance	I_{SW3} = 100mA		0.23	0.40	Ω
SW3 Leakage Current	V_{VP3} = 5.5V, V_{SW3} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM3}
Minimum On-Time			70		ns

①: V_{NOM3} refers to the nominal output voltage level for V_{OUT3} as defined by the *Ordering Information* section.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 8:

REG3 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
30h	R	VRANGE	VSET					
31h	R	R	R	R	R	R	R	MODE
32h	R	R	R	R	R	R	R	R
33h	R	R	R	R	R	W/E	OK	ON

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1

Table 9:

REG3 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
30h	VSET	[5:0]	R/W	REG3 Output Voltage Selection	See Table 10	
30h	VRANGE	[6]	R/W	REG3 Voltage Range Selection	0	Min V_{OUT} = 1.1V
					1	Min V_{OUT} = 1.25V
30h		[7]	R		READ ONLY	
31h	MODE	[0]	R/W	Mode Selection	0	PWM/PFM
					1	Forced PWM
31h		[7:1]	R		READ ONLY	
32h		[7:0]	R		READ ONLY	
33h	ON	[0]	R/W	REG3 Enable	0	REG3 Disable
					1	REG3 Enable
33h	OK	[1]	R	REG3 Power-OK	0	Output is not OK
					1	Output is OK
33h		[2]	W/E		WRITE-EXACT	
33h		[7:3]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 10:
REG3/VSET[ ] Output Voltage Setting

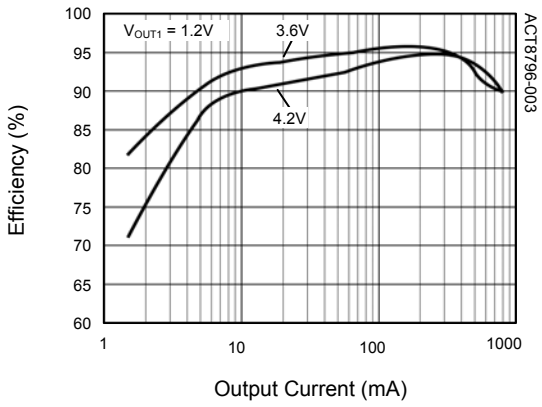
REG3/VSET[3:0]	REG3/VSET[5:4]							
	REG3/VRANGE[ ] = [0]				REG3/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	N/A	N/A	1.455	1.860	1.250	2.050	2.850	3.650
0001	N/A	N/A	1.480	1.890	1.300	2.100	2.900	3.700
0010	N/A	1.100	1.505	1.915	1.350	2.150	2.950	3.750
0011	N/A	1.125	1.530	1.940	1.400	2.200	3.000	3.800
0100	N/A	1.150	1.555	1.965	1.450	2.250	3.050	3.850
0101	N/A	1.175	1.585	1.990	1.500	2.300	3.100	3.900
0110	N/A	1.200	1.610	2.015	1.550	2.350	3.150	3.950
0111	N/A	1.225	1.635	2.040	1.600	2.400	3.200	4.000
1000	N/A	1.255	1.660	2.065	1.650	2.450	3.250	4.050
1001	N/A	1.280	1.685	2.090	1.700	2.500	3.300	4.100
1010	N/A	1.305	1.710	2.115	1.750	2.550	3.350	4.150
1011	N/A	1.330	1.735	2.140	1.800	2.600	3.400	4.200
1100	N/A	1.355	1.760	2.165	1.850	2.650	3.450	4.250
1101	N/A	1.380	1.785	2.190	1.900	2.700	3.500	4.300
1110	N/A	1.405	1.810	2.200	1.950	2.750	3.550	4.350
1111	N/A	1.430	1.835	2.245	2.000	2.800	3.600	4.400

(N/A): Not Available

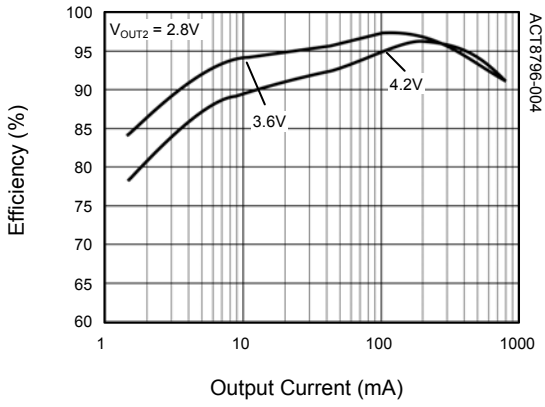
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8796QLCIA, V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, L = 3.3µH, C_{VP1} = C_{VP2} = C_{VP3} = 2.2µF, C_{OUT1} = C_{OUT2} = C_{OUT3} = 10µF, T_A = 25°C, unless otherwise specified.)

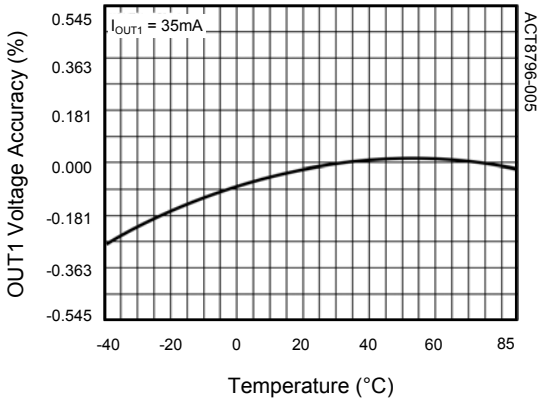
REG1 Efficiency vs. Load Current



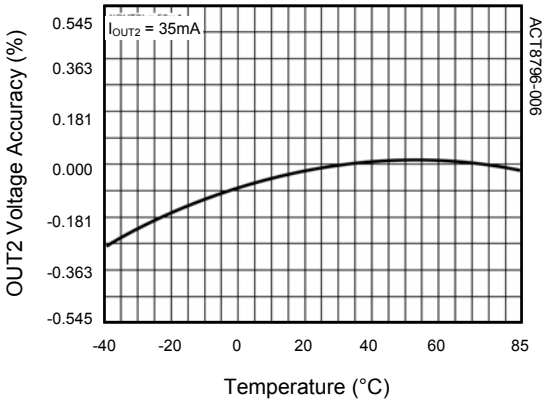
REG2 Efficiency vs. Load Current



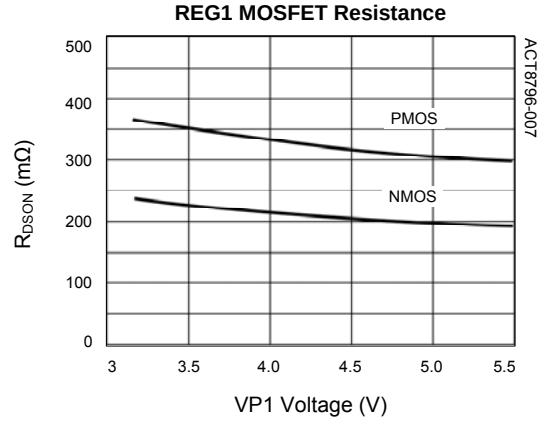
OUT1 Regulation Voltage



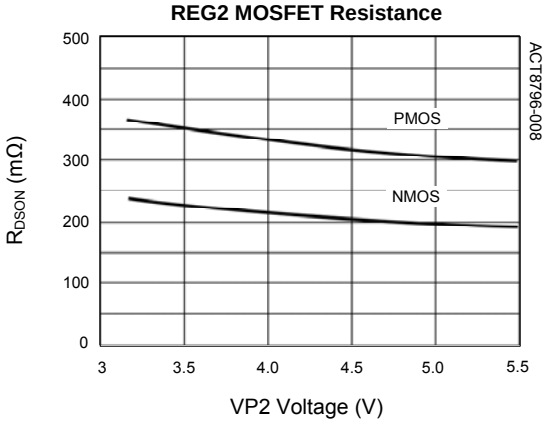
OUT2 Regulation Voltage



REG1 MOSFET Resistance



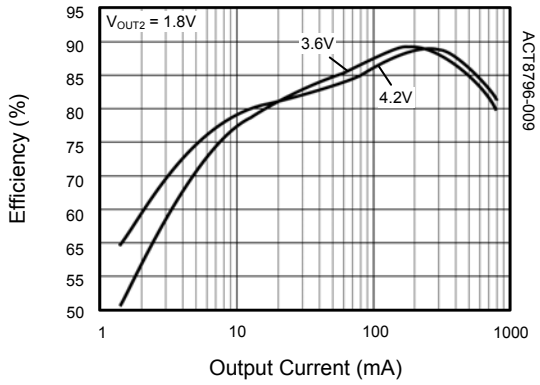
REG2 MOSFET Resistance



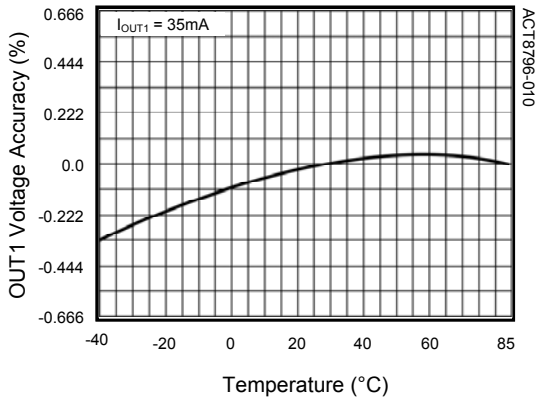
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8796QLCIA, V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, L = 3.3µH, C_{VP1} = C_{VP2} = C_{VP3} = 2.2µF, C_{OUT1} = C_{OUT2} = C_{OUT3} = 10µF, T_A = 25°C, unless otherwise specified.)

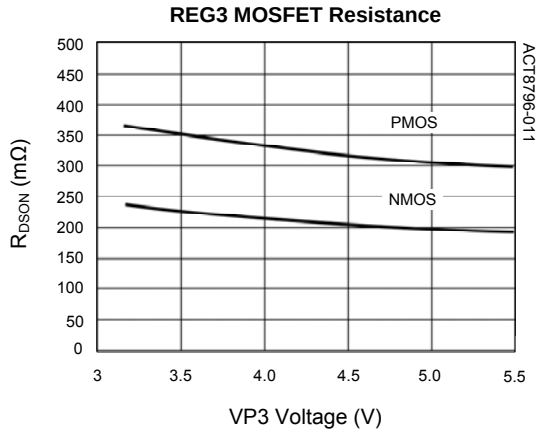
REG3 Efficiency vs. Load Current



OUT3 Regulation Voltage



REG3 MOSFET Resistance



FUNCTIONAL DESCRIPTION

General Description

REG1, REG2, and REG3 are fixed-frequency, current-mode, synchronous PWM step down converters that achieve peak efficiencies of up to 97%. REG1 and REG2 are capable of supplying up to 750mA of output current, while REG3 supports up to 550mA. These regulators operate with a fixed frequency of 1.6MHz, minimizing noise in sensitive applications and allowing the use of small external components. Each of the step-down DC/DCs are available with a variety of standard and custom output voltages, and each may be software-controlled via the I^2C interface by systems that require advanced power management functions.

100% Duty Cycle Operation

REG1, REG2, and REG3 are each capable of operating at up to 100% duty cycle. During 100% duty-cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

Synchronous Rectification

REG1, REG2, and REG3 each feature integrated n-channel synchronous rectifiers, maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Enabling and Disabling REG1, REG2, and REG3

Enable/disable functionality is typically implemented as part of a controlled enable/disable scheme utilizing nMSTR and other system control features of the ACT8796. REG1 and REG2 are automatically enabled whenever either of the following conditions re met:

1) nMSTR is driven low, or

2) PWRHLD is asserted high.

When none of these conditions are true, or if a regulator's ON[ ] bit is set to [0], REG1 and REG2 are disabled, and each regulator's quiescent supply current drops to less than 1µA.

REG3 is enabled whenever ON3 is asserted high, and is disabled whenever ON is asserted low or if the REG3/ON[ ] bit is set to [0].

Programming the Output Voltage

By default, REG1, REG2, and REG3 each power up and regulate to their default output voltage. Once the system is enabled, each regulator's output voltage may be independently programmed to a different value, typically in order to reduce the power consumption of a microprocessor in standby mode. Program the output voltages via the I^2C serial interface by writing to the REGx/VSETx[ ] and REGx/VRANGE[ ] registers.

Programmable Operating Mode

By default, REG1, REG2 ,and REG3 each operate in fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power. In applications where low noise is critical, force fixed-frequency PWM operation across the entire load current range, at the expense of light-load efficiency, by setting the REGx/MODE[ ] bit to [1].

Power-OK

REG1, REG2, and REG3 each feature a variety of status bits that can be read by the system microprocessor. If either output voltage is lower than the power-OK threshold, typically 6% below the programmed regulation voltage, REGx/OK[ ] will clear to 0.

Soft-Start

REG1, REG2, and REG3 each include matched soft-start circuitry. When enabled, the output voltages track the internal 80µs soft-start ramp and both power up in a monotonic manner that is independent of loading on either output. This circuitry ensures that each output powers up in a controlled manner, greatly simplifying power sequencing design considerations.

Compensation

REG1, REG2, and REG3 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components.

FUNCTIONAL DESCRIPTION (CONT'D)

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 2.2µF ceramic capacitor for each of REG1, REG2, and REG3 is recommended for most applications.

Output Capacitor Selection

For most applications, 10µF ceramic output capacitors are recommended for REG1, REG2, and REG3. Although the these regulators were designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR, low-ESR tantalum capacitors can provide acceptable results as well.

Inductor Selection

REG1, REG2, and REG3 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with 3.3µH inductors, although inductors in the 2.2µH to 4.7µH range can be used. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current of the application by at least 30%.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as close as possible to the IC, and avoiding the use of via if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple via. The output node for each regulator should be connected to its corresponding OUTx pin through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple via to achieve low electrical and thermal resistance.

ELECTRICAL CHARACTERISTICS (REG4)

(V_{INL} = 3.6V, C_{OUT4} = 1μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL Operating Voltage Range		3.1		5.5	V
INL UVLO Threshold	V_{INL} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{INL} Input Falling		0.1		V
Output Voltage Accuracy	V_{NOM4} < 1.3V, I_{OUT4} = 10mA	-2.4%	V_{NOM4}①	+1.8%	V
	V_{NOM4} ≥ 1.3V, I_{OUT4} = 10mA	-1.2%	V_{NOM4}	+1.8%	
Line Regulation Error	V_{INL} = Max(V_{OUT4} + 0.5V, 3.6V) to 5.5V		0		mV
Load Regulation Error	I_{OUT4} = 1mA to 250mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT4} = 250mA, C_{OUT4} = 1μF		60		dB
	f = 10kHz, I_{OUT4} = 250mA, C_{OUT4} = 1μF		50		
Supply Current per Output	Regulator Enabled		40		μA
	Regulator Disabled		0		
Dropout Voltage②	I_{OUT4} = 120mA, V_{OUT4} > 3.1V		100	200	mV
Output Current				250	mA
Current Limit③	V_{OUT4} = 95% of regulation voltage	280			
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT4}, hysteresis = -4%		89		%
Output Noise	C_{OUT4} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT4} Range		1		20	μF
Discharge Resistor in Shutdown	LDO Disabled, DIS4[ ] = [1]		650		Ω

①: V_{NOM4} refers to the nominal output voltage level for V_{OUT4} as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage (for 2.8V output voltage or higher)

③: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 30% (typ)

ELECTRICAL CHARACTERISTICS (REG5)

(V_{INL} = 3.6V, C_{OUT5} = 1μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL Operating Voltage Range		3.1		5.5	V
INL UVLO Threshold	V_{INL} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{INL} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	V_{NOM5}①	+2	%
	T_A = -40°C to 85°C	-2.5	V_{NOM5}	+3	
Line Regulation Error	V_{INL} = Max(V_{OUT5} + 0.5V, 3.6V) to 5.5V		0		mV
Load Regulation Error	I_{OUT5} = 1mA to 250mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT5} = 250mA, C_{OUT5} = 1μF		70		dB
	f = 10kHz, I_{OUT5} = 250mA, C_{OUT5} = 1μF		60		
Supply Current per Output	Regulator Enabled		40		μA
	Regulator Disabled		0		
Dropout Voltage②	I_{OUT5} = 120mA, V_{OUT5} > 3.1V		100	200	mV
Output Current				250	mA
Current Limit③	V_{OUT5} = 95% of regulation voltage	280			mA
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT5}, hysteresis = -4%		89		%
Output Noise	C_{OUT5} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT5} Range		1		20	μF
Discharge Resistor in Shutdown	LDO Disabled, DIS5[ ] = [1]		650		Ω

①: V_{NOM5} refers to the nominal output voltage level for V_{OUT5} as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage (for 2.8V output voltage or higher)

③: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 30% (typ)

ELECTRICAL CHARACTERISTICS (REG6)

(V_{INL} = 3.6V, C_{OUT6} = 1μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL Operating Voltage Range		3.1		5.5	V
INL UVLO Threshold	V_{INL} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{INL} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	V_{NOM6}①	+2	%
	T_A = -40°C to 85°C	-2.5	V_{NOM6}	+3	
Line Regulation Error	V_{INL} = Max(V_{OUT6} + 0.5V, 3.6V) to 5.5V		0		mV
Load Regulation Error	I_{OUT6} = 1mA to 250mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT6} = 250mA, C_{OUT6} = 1μF		70		dB
	f = 10kHz, I_{OUT6} = 250mA, C_{OUT6} = 1μF		60		
Supply Current per Output	Regulator Enabled		40		μA
	Regulator Disabled		0		
Dropout Voltage②	I_{OUT6} = 120mA, V_{OUT6} > 3.1V		100	200	mV
Output Current				250	mA
Current Limit③	V_{OUT6} = 95% of regulation voltage	280			mA
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT6}, hysteresis = -4%		89		%
Output Noise	C_{OUT6} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT6} Range		1		20	μF
Discharge Resistor in Shutdown	LDO Disabled, DIS6[ ] = [1]		650		Ω

①: V_{NOM6} refers to the nominal output voltage level for V_{OUT6} as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage (for 2.8V output voltage or higher)

③: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 30% (typ)

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 11:

Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
03h	R	VRANGE	VSET4					
40h	R	R	W/E	R	R	R	R	R
41h	R	R	ON5	VSET5				
42h	R	R	ON6	VSET6				
43h	OK6	OK5	OK4	DIS6	DIS5	DIS4	W/E	R

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1.

Table 12:

REG56 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
03h	VSET4	[5:0]	R/W	REG4 Output Voltage Selection	See Table 14	
03h	VRANGE	[6]	R/W	REG4 Output Voltage Selection	0	Min VOUT = 0.645V
					1	Min VOUT = 1.25V
03h		[7]	R		READ ONLY	
40h		[4:0]	R		READ ONLY	
40h		[5]	W/E		WRITE-EXACT	
40h		[7:6]	R		READ ONLY	
41h	VSET5	[4:0]	R/W	REG5 Output Voltage Selection	See Table 13	
41h	ON5	[5]	R/W	REG5 Enable	0	REG5 Disable
					1	REG5 Enable
41h		[7:6]	R		READ ONLY	
42h	VSET6	[4:0]	R/W	REG6 Output Voltage Selection	See Table 13	
42h	ON6	[5]	R/W	REG6 Enable	0	REG6 Disable
					1	REG6 Enable
42h		[7:6]	R		READ ONLY	
43h		[0]	R		READ ONLY	
43h		[1]	W/E		WRITE-EXACT	

REGISTER DESCRIPTIONS CONT'D

Table 12:
Control Register Bit Descriptions (Cont'd)

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
43h	DIS4	[2]	R/W	REG4 Discharge Enable	0	Discharge Disable
					1	Discharge Enable
43h	DIS5	[3]	R/W	REG5 Discharge Enable	0	Discharge Disable
					1	Discharge Enable
43h	DIS6	[4]	R/W	REG6 Discharge Enable	0	Discharge Disable
					1	Discharge Enable
43h	OK4	[5]	R	REG4 Power-OK	0	Output is not OK
					1	Output is OK
43h	OK5	[6]	R	REG5 Power-OK	0	Output is not OK
					1	Output is OK
43h	OK6	[7]	R	REG6 Power-OK	0	Output is not OK
					1	Output is OK

Table 13:
REG56/VSETx[ ] Output Voltage Setting

REG56CFG/VSETx[2:0]	REG56CFG/VSETx[4:3]			
	00	01	10	11
000	1.4	2.15	2.55	3.0
001	1.5	2.20	2.60	3.1
010	1.6	2.25	2.65	3.2
011	1.7	2.30	2.70	3.3
100	1.8	2.35	2.75	3.4
101	1.9	2.40	2.80	3.5
110	2.0	2.45	2.85	3.6
111	2.1	2.50	2.90	3.7

REGISTER DESCRIPTIONS CONT'D

Table 14:

REG4/VRANGE[ ] Output Voltage Setting

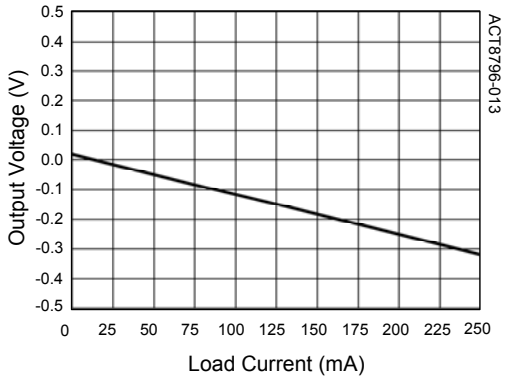
REG4/VSET[3:0]	REG4/VSET[5:4]							
	REG4/VRANGE[ ] = [0]				REG4/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	0.645	1.050	1.455	1.860	1.250	2.050	2.850	3.650
0001	0.670	1.075	1.480	1.890	1.300	2.100	2.900	3.700
0010	0.695	1.100	1.505	1.915	1.350	2.150	2.950	N/A
0011	0.720	1.125	1.530	1.940	1.400	2.200	3.000	N/A
0100	0.745	1.150	1.555	1.965	1.450	2.250	3.050	N/A
0101	0.770	1.175	1.585	1.990	1.500	2.300	3.100	N/A
0110	0.795	1.200	1.610	2.015	1.550	2.350	3.150	N/A
0111	0.820	1.225	1.635	2.040	1.600	2.400	3.200	N/A
1000	0.845	1.255	1.660	2.065	1.650	2.450	3.250	N/A
1001	0.870	1.280	1.685	2.090	1.700	2.500	3.300	N/A
1010	0.895	1.305	1.710	2.115	1.750	2.550	3.350	N/A
1011	0.920	1.330	1.735	2.140	1.800	2.600	3.400	N/A
1100	0.950	1.355	1.760	2.165	1.850	2.650	3.450	N/A
1101	0.975	1.380	1.785	2.190	1.900	2.700	3.500	N/A
1110	1.000	1.405	1.810	2.200	1.950	2.750	3.550	N/A
1111	1.025	1.430	1.835	2.245	2.000	2.800	3.600	N/A

(N/A): Not Available

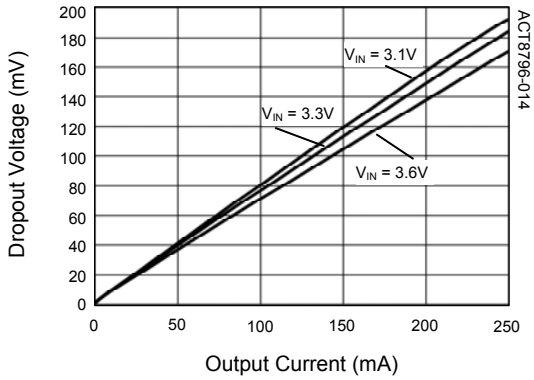
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8796QLCIA, V_{VIN} = 5V, T_A = 25°C, unless otherwise specified.)

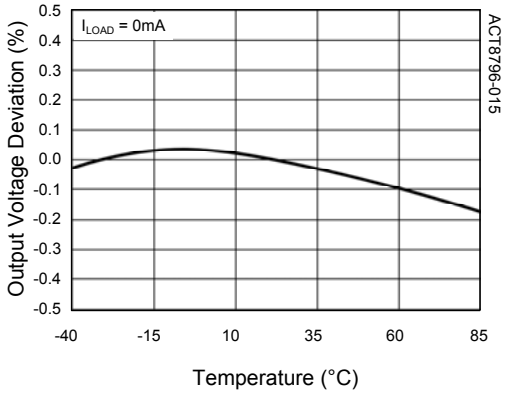
Load Regulation



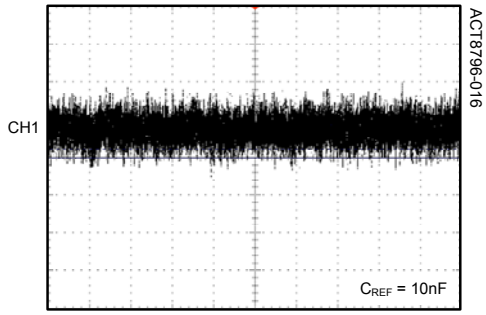
Dropout Voltage vs. Output Current



Output Voltage Deviation vs. Temperature

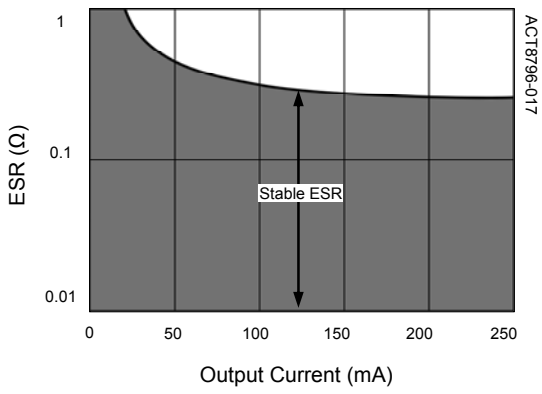


LDO Output Voltage Noise



CH1: V_{OUTx}, 200µV/div (AC COUPLED)
TIME: 200ms/div

Region of Stable C_{OUT} ESR vs. Output Current



FUNCTIONAL DESCRIPTION

General Description

REG4, REG5, and REG6 are low-noise, low-dropout linear regulators (LDOs) that are optimized for low noise and high-PSRR operation, achieving more than 60dB PSRR at frequencies up to 10kHz.

LDO Output Voltage Programming

All LDOs feature independently-programmable output voltages that are set via the I^{2}C serial interface, increasing the ACT8796's flexibility while reducing total solution size and cost. Set the output voltage by writing to the REG456CFG/VSETx[ ] registers.

Output Current Capability

REG4, REG5, and REG6 each supply an output current of 250mA. Excellent performance is achieved over this load current range.

Output Current Limit

In order to ensure safe operation under over-load conditions, each LDO features current-limit circuitry with current fold-back. The current-limit circuitry limits the current that can be drawn from the output, providing protection in over-load conditions. For additional protection under extreme over current conditions, current-fold-back protection reduces the current-limit by approximately 30% under extreme overload conditions.

Enabling and Disabling the LDOs

REG4 is enabled whenever either of the following conditions are met:

1) nMSTR is driven low, or

2) PWRHLD is asserted high.

Furthermore, once these conditions are met REG5 and REG6 maybe independently enabled or disabled via the I^{2}C serial interface by writing the appropriate REG56/ONx[ ] bit.

Power-OK

Each of the LDOs features power-OK status bit that can be read by the system microprocessor via the I^{2}C interface. If an output voltage is lower than the power-OK threshold, typically 6% below the programmed regulation voltage, the corresponding REG456CFG/OKx[ ] will clear to 0.

Reference Bypass Pin

The ACT8796 contains a reference bypass pin which filters noise from the reference, providing a low noise voltage reference to the LDOs. Bypass REF to G with a 0.01µF ceramic capacitor.

Optional LDO Output Discharge

Each of the ACT8796's LDOs features an optional, independent output voltage discharge feature. When this feature is enabled, the LDO output is discharged to ground through a 1kΩ resistance when the LDO is shutdown. This feature may be enabled or disabled via the I^{2}C interface by writing to the REG456CFG/DISx[ ] bits.

Output Capacitor Selection

REG4, REG5, and REG6 each require only a small ceramic capacitor for stability. For best performance, each output capacitor should be connected directly between the OUTx and G pins as possible, with a short and direct connection. To ensure best performance for the device, the output capacitor should have a minimum capacitance of 1µF, and ESR value between 10mΩ and 200mΩ. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

FUNCTIONAL DESCRIPTION (CONT'D)

PCB Layout Considerations

PCB Layout Considerations The ACT8796's LDOs provide good DC, AC, and noise performance over a wide range of operating conditions, and are relatively insensitive to layout considerations. When designing a PCB, however, careful layout is necessary to prevent other circuitry from degrading LDO performance.

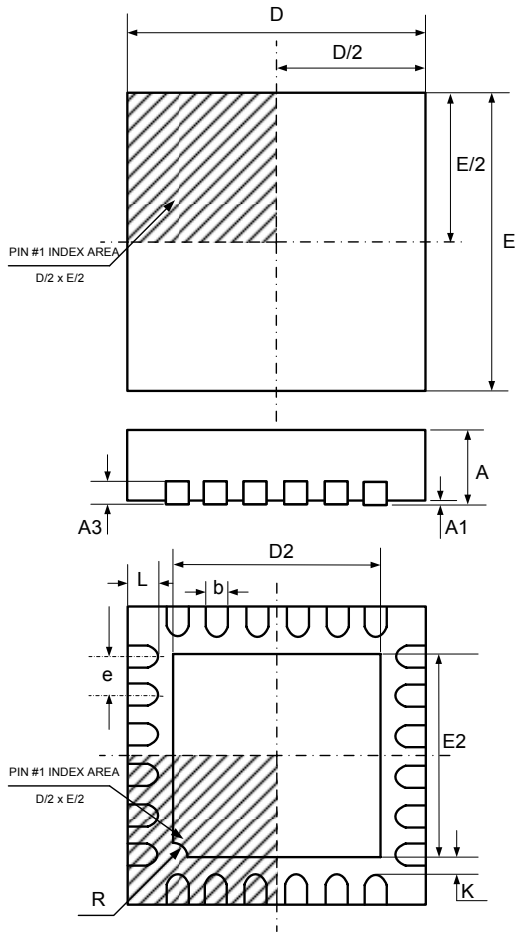
A good design places input and output capacitors as close to the LDO inputs and output as possible, and utilizes a star-ground configuration for all regulators to prevent noise-coupling through ground. Output traces should be routed to avoid close proximity to noisy nodes, particularly the SW nodes of the DC/DCs.

REFBP is a filtered reference noise, and internally has a direct connection to the linear regulator controller. Any noise injected onto REFBP will directly affect the outputs of the linear regulators, and therefore special care should be taken to ensure that no noise is injected to the outputs via REFBP. As with the LDO output capacitors, the REFBP bypass capacitor should be placed as close to the IC as possible, with short, direct connections to the star-ground. Avoid the use of via whenever possible. Noisy nodes, such as from the DC/DCs, should be routed as far away from REFBP as possible.

PACKAGE OUTLINE AND DIMENSIONS

PACKAGE OUTLINE

TQFN44-24 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.200 REF		0.008 REF	
b	0.180	0.300	0.007	0.012
D	3.850	4.150	0.152	0.163
E	3.850	4.150	0.152	0.163
D2	2.500	2.800	0.098	0.110
E2	2.500	2.800	0.098	0.110
e	0.500 BSC		0.020 BSC	
L	0.350	0.450	0.014	0.018
R	0.200 TYP		0.008 TYP	
K	0.200	---	0.008	---