ACT8810

Rev 4, 01-Oct-09

Eight Channel *ActivePath*™ Power Management IC

FEATURES

- ***ActivePath***™ **Li+ Charger with System Power Selection**
- **Six Integrated Regulators**
  - **1.3A High Efficiency Step-Down DC/DC**
  - **1.0A High Efficiency Step-Down DC/DC**
  - **0.55A High Efficiency Step-Down DC/DC**
  - **2×360mA Low Noise, High PSRR LDOs**
  - **30mA RTC LDO / Backup Battery Charger**
- **I²C™ Serial Interface**
- **Minimal External Components**
- **Compatible with USB or AC-Adapter Charging**
- **5mm × 5mm, Thin-QFN (TQFN55-40) Package**
  - **Only 0.75mm Height**
  - **RoHS Compliant**

APPLICATIONS

- **Personal Navigation Devices**
- **Portable Media Players**
- **Smart Phones**

GENERAL DESCRIPTION

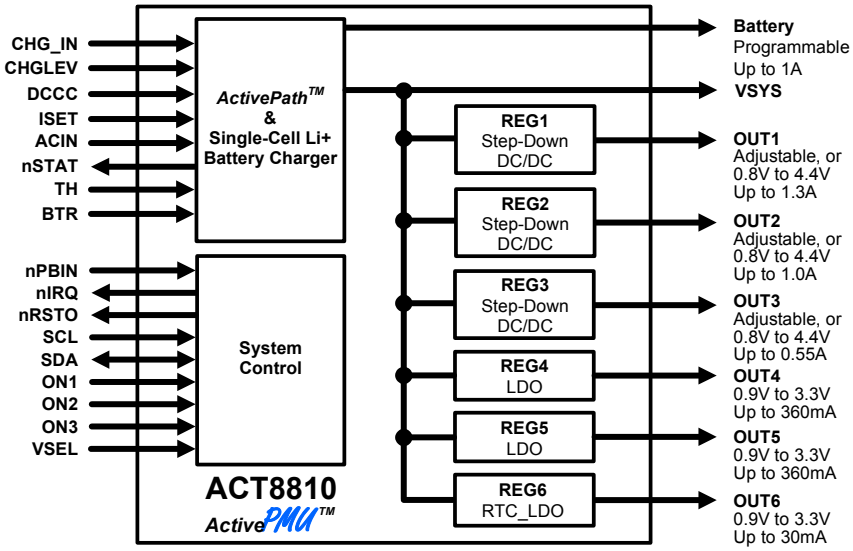
The patent-pending ACT8810 is a complete, cost effective, highly-efficient *ActivePMU*™ power management solution that is ideal for a wide range of high performance portable handheld applications such as personal navigation devices (PNDs). This device integrates the *ActivePath*™ complete battery charging and management system with six power supply channels.

The *ActivePath* architecture automatically selects the best available input supply for the system. If the external input source is not present or the system load current is more than the input source can provide, the *ActivePath* supplies additional current from the battery to the system. The charger is a complete, thermally-regulated, stand-alone single-cell linear Li+ charger that incorporates an internal power MOSFET.

REG1, REG2, and REG3 are three independent, fixed-frequency, current-mode step-down DC/DC converters that output 1.3A, 1.0A, and 0.55A, respectively. REG4 and REG5 are high performance, low-noise, low-dropout linear regulators that output up to 360mA each. REG6 is a RTC LDO that outputs up to 30mA for a real time clock. Finally, an I²C serial interface provides programmability for the DC/DC converters and LDOs.

The ACT8810 is available in a tiny 5mm x 5mm 40-pin Thin-QFN package that is just 0.75mm thin.

SYSTEM BLOCK DIAGRAM



Pb-free

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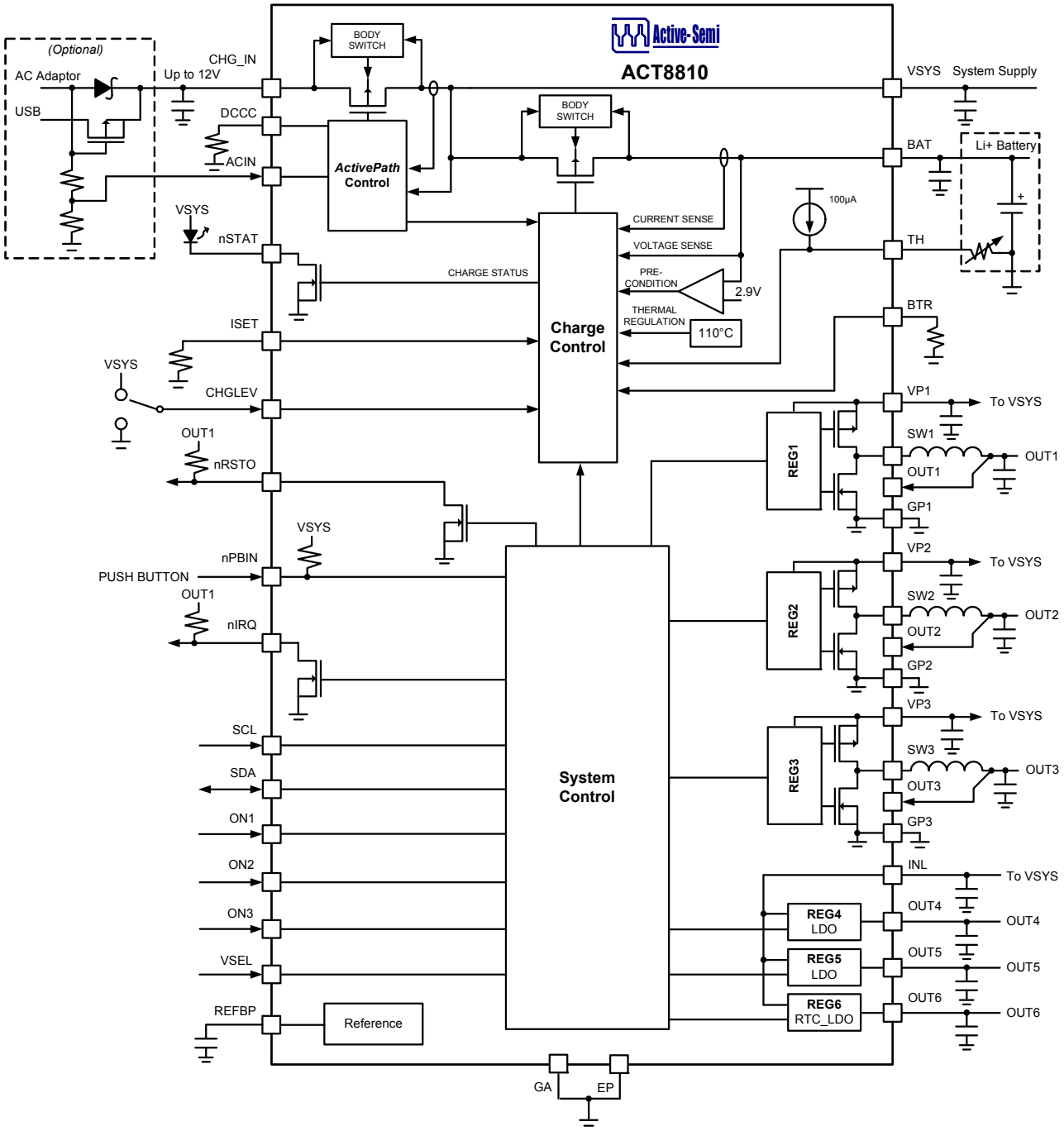
FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①

PART NUMBER	V_{OUT1}/V_{STBY1}②	V_{OUT2}/V_{STBY2}	V_{OUT3}/V_{STBY3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	CONTROL SEQUENCE③
ACT8810QJ1C1-T	3.3V/3.3V	1.1V/1.2V	1.2V/1.2V	1.2V	2.8V	3.3V	Sequence A
ACT8810QJ213-T	1.2V/1.2V	1.8V/1.8V	1.0V/1.0V	3.3V	1.2V	3.0V	Sequence B
ACT8810QJ3EB-T	3.3V/3.3V	1.2V/1.2V	1.8V/1.8V	1.5V	2.8V	3.3V	Sequence C
ACT8810QJ45D-T	3.3V/3.3V	1.8V/1.8V	1.3V/1.3V	1.2V	3.3V	3.3V	Sequence D
ACT8810QJ50F-T	1.2V/1.2V	3.3V/3.3V	1.8V/1.8V	3.3V	1.8V	3.0V	Sequence E

PACKAGING DETAILS	PACKAGE	PINS	TEMPERATURE RANGE	PACKING
ACT8810QJ###-T	TQFN55-40	40	-40°C to +85°C	TAPE & REEL

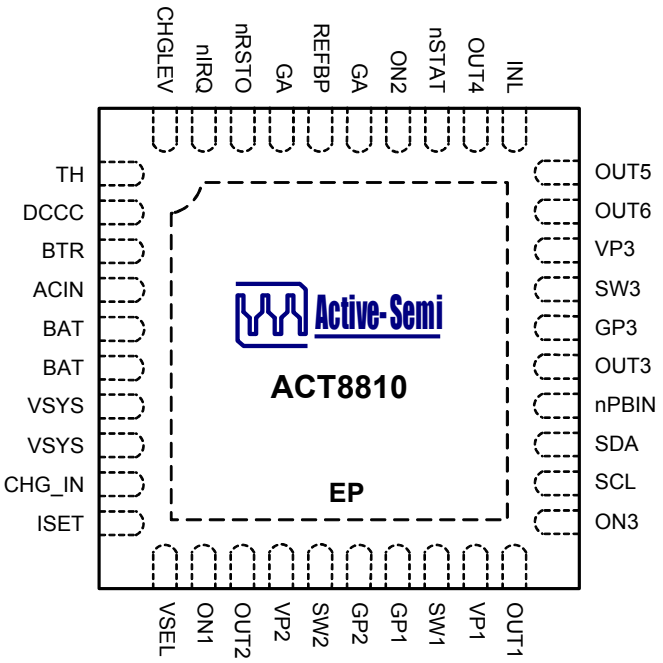
①: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

②: To select V_{STBYx} as a output regulation voltage of REGx, tie VSEL to VSYS or a logic high.

③: Refer to the Control Sequence section for more information.

PIN CONFIGURATION

TOP VIEW



Thin - QFN (TQFN55-40)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	TH	Temperature Sensing Input. Connect to battery thermistor. TH is pulled up with a 100µA current internally. See the *Battery Temperature Monitoring* section for more information.
2	DCCC	Dynamic Charging Current Control. Connect a resistor to set the dynamic charging current control point. A internal 100µA current source sets up a voltage that is used to compare with VSYS and dynamically scale the charging current to maintain VSYS regulation. See the *Dynamic Charge Current Control* section for more information.
3	BTR	Safety Timer Program Pin. The resistance between this pin and GA determines the timers timeout values. See the *Charging Safety Timers* section for more information.
4	ACIN	AC Adaptor Detect. Detects presence of a wall adaptor and automatically adjusts the charge current to the maximum charge current level. Do not leave ACIN floating.
5, 6	BAT	Battery Charger Output. Connect this pin directly to the battery anode (+ terminal)
7, 8	VSYS	System Output Pin. Bypass to GA with a 10µF or larger ceramic capacitor.
9	CHG_IN	Power Input for the Battery Charger. Bypass CHG_IN to GA with a capacitor placed as close to the IC as possible. The battery charger are automatically enabled when a valid voltage is present on CHG_IN. See the *CHG_IN Bypass Capacitor Selection* section for more information.
10	ISET	Charge Current Set. Program the maximum charge current by connecting a resistor (R_{ISET}) between ISET and GA. See the *Charger Current Programming* section for more information.
11	VSEL	Step-Down DC/DCs Output Voltage Selection. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage. See the *Output Voltage Selection Pin* section for more information.
12	ON1	Independent Enable Control Input for REG1. Drive ON1 to VSYS or to a logic high for normal operation, drive to GA or a logic low to disable REG1. Do not leave ON1 floating.
13	OUT2	Output Feedback Sense for REG2. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
14	VP2	Power Input for REG2. Bypass to GP2 with a high quality ceramic capacitor placed as close as possible to the IC.
15	SW2	Switching Node Output for REG2. Connect this pin to the switching end of the inductor.
16	GP2	Power Ground for REG2. Connect GA, GP1, GP2 and GP3 together at a single point as close to the IC as possible.
17	GP1	Power Ground for REG1. Connect GA, GP1, GP2 and GP3 together at a single point as close to the IC as possible.
18	SW1	Switching Node Output for REG1. Connect this pin to the switching end of the inductor.
19	VP1	Power Input for REG1. Bypass to GP1 with a high quality ceramic capacitor placed as close as possible to the IC.
20	OUT1	Output Feedback Sense for REG1. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
21	ON3	Enable Control Input for REG3. Drive ON3 to a logic high for normal operation, drive to GA or a logic low to disable REG3. Do not leave ON3 floating.
22	SCL	Clock Input for I^2C Serial Interface.
23	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of SCL.

PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
24	nPBIN	Master Enable Input. Drive nPBIN to GA through a 100kΩ resistor to enable the IC, drive nPBIN directly to GA to assert a Hard-Reset condition. Refer to the *System Startup & Shutdown and Control Sequence* sections for more information. nPBIN is internally pulled up to VSYS through a 50kΩ resistor.
25	OUT3	Output Feedback Sense for REG3. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
26	GP3	Power Ground for REG3. Connect GA, GP1, GP2, and GP3 together at a single point as close to the IC as possible.
27	SW3	Switching Node Output for REG3. Connect this pin to the switching end of the inductor.
28	VP3	Power Input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close as possible to the IC.
29	OUT6	RTC LDO Output Voltage. Capable of delivering up to 30mA of output current.
30	OUT5	Output Voltage for REG5. Capable of delivering up to 360mA of output current. The output is discharged to GA with 1kΩ when disabled.
31	INL	Power Input for REG4, REG5, and REG6. Bypass to GA with a high quality ceramic capacitor placed as close as possible to the IC.
32	OUT4	Output Voltage for REG4. Capable of delivering up to 360mA of output current. The output is discharged to GA with 1kΩ when disabled.
33	nSTAT	Active-Low Open-Drain Charger Status Output. nSTAT has a 5mA (typ) current limit, allowing it to directly drive an indicator LED without additional external components. To generate a logic-level output, connect nSTAT to an appropriate supply voltage (typically VSYS) through a 10kΩ or greater pull-up resistor. See the *Charge Status Indication* section for more information.
34	ON2	Independent Enable Control Input for REG2. Drive ON2 to a logic high for normal operation, drive to GA or a logic low to disable REG2. Do not leave ON2 floating.
35, 37	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP1, GP2, and GP3 together at a single point as close to the IC as possible.
36	REFBP	Reference Noise Bypass. Connect a 0.01µF ceramic capacitor from REFBP to GA. This pin is discharged to GA in shutdown.
38	nRSTO	Open-Drain Reset Output. nRSTO asserts low whenever REG1 is out of regulation, and remains low for 260ms (typ) after REG1 reaches regulation.
39	nIRQ	Open-Drain Interrupt Output. nIRQ asserts any time nPBIN is asserted or an unmasked fault condition exists. See the *nIRQ Output* section for more information.
40	CHGLEV	Charging State Select Input. When ACIN = 0 charge current is internally set; Drive CHGLEV to a logic-high for high-current USB charging mode (maximum charge current is 500mA), drive CHGLEV to a logic-low for low-current USB charging mode (maximum charge current is 100mA). When ACIN = 1 charge current is externally set by R_{ISET}; Drive CHGLEV to a logic-high to for high-current charging mode (I_{CHG} = K × 1000/R_{ISET} (mA) where K = 640), drive CHGLEV to a logic-low for low-current charging mode (I_{CHG} = K × 500/R_{ISET} (mA) where K = 640). Do not leave CHGLEV floating.
EP	EP	Exposed Pad. Must be soldered to ground on the PCB.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
CHG_IN to GA t < 1ms and duty cycle <1% Steady State	 -0.3 to +18 -0.3 to +14	 V V
VP1 to GP1, VP2 to GP2, VP3 to GP3	-0.3 to +6	V
BAT, VSYS, INL to GA	-0.3 to +6	V
SW1, OUT1 to GP1	-0.3 to (V_{VP1} +0.3)	V
SW2, OUT2 to GP2	-0.3 to (V_{VP2} +0.3)	V
SW3, OUT3 to GP3	-0.3 to (V_{VP3} +0.3)	V
ON1, ON2, ON3, ISET, ACIN, VSEL, DCCC, CHGLEV, TH, SCL, SDA, REFBP, nIRQ, nRSTO, nSTAT, BTR, nPBIN to GA	-0.3 to +6	V
OUT4, OUT5, OUT6 to GA	-0.3 to (V_{INL} +0.3)	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	125	°C
Maximum Power Dissipation TQFN55-40 (Thermal Resistance θ_{JA} = 30°C/W)	2.7	W
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

REGISTER DESCRIPTIONS

Table 1:
Global Register Map

OUTPUT	ADDRESS									DATA (DEFAULT VALUE)							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
SYS	06h	0	0	0	0	0	1	1	0	R	R	R	0	R	R	1	R
REG1	10h	0	0	0	1	0	0	0	0	R	R	V	V	V	V	V	V
REG1	11h	0	0	0	1	0	0	0	1	R	R	R	R	R	R	R	R
REG1	12h	0	0	0	1	0	0	1	0	R	R	R	R	R	0	R	1
REG1	13h	0	0	0	1	0	0	1	1	R	V	V	V	V	V	V	V
REG2	20h	0	0	1	0	0	0	0	0	R	R	V	V	V	V	V	V
REG2	21h	0	0	1	0	0	0	0	1	R	R	R	R	R	R	R	R
REG2	22h	0	0	1	0	0	0	1	0	R	R	R	R	R	0	R	1
REG2	23h	0	0	1	0	0	0	1	1	R	V	V	V	V	V	V	V
REG3	30h	0	0	1	1	0	0	0	0	R	R	V	V	V	V	V	V
REG3	31h	0	0	1	1	0	0	0	1	R	R	R	R	R	R	R	R
REG3	32h	0	0	1	1	0	0	1	0	R	R	R	R	R	0	R	1
REG3	33h	0	0	1	1	0	0	1	1	R	V	V	V	V	V	V	V
REG4	40h	0	1	0	0	0	0	0	0	1	R	1	V	V	V	V	V
REG4	43h	0	1	0	0	0	0	1	1	R	R	R	R	R	R	0	R
REG5	41h	0	1	0	0	0	0	0	1	1	R	1	V	V	V	V	V
REG6	42h	0	1	0	0	0	0	1	0	R	R	R	V	V	V	V	V

KEY:

R: Read-Only bits. No Default Assigned.

V: Default Values Depend on Voltage Option. Default Values May Vary.

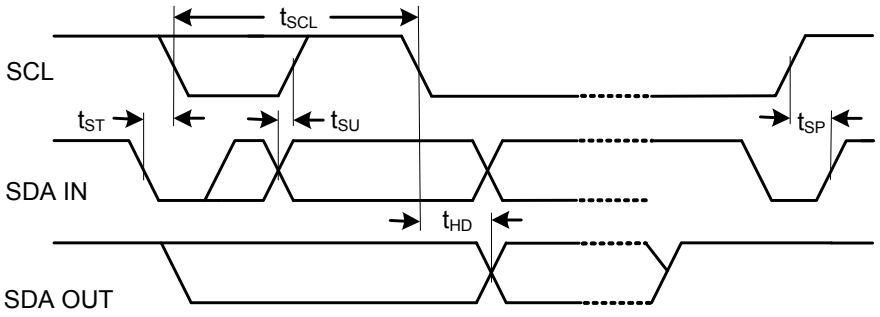
Note: Addresses other than those specified in Table 1 may be used for factory settings. Do not access any registers other than those specified in Table 1.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Low Input Voltage	V_{VSYS} = 2.6V to 5.5V, T_A = -40ºC to 85ºC			0.35	V
SCL, SDA High Input Voltage	V_{VSYS} = 2.6V to 5.5V, T_A = -40ºC to 85ºC	1.55			V
SCL, SDA Leakage Current				1	µA
SDA Low Output Voltage	I_{OL} = 5mA			0.3	V
SCL Clock Period, t_{SCL}		2.5			µs
SDA Data In Setup Time to SCL High, t_{SU}		100			ns
SDA Data Out Hold Time after SCL Low, t_{HD}		300			ns
SDA Data Low Setup Time to SCL Low, t_{ST}	Start Condition	100			ns
SDA Data High Hold Time after Clock High, t_{SP}	Stop Condition	100			ns

Figure 1:
I²C Serial Bus Timing



ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		2.6		5.5	V
UVLO Threshold Voltage	VSYS Rising	2.35	2.5	2.6	V
UVLO Hysteresis	VSYS Falling		100		mV
VSYS Supply Current	ONx = VSYS		70		µA
VSYS Shutdown Current	ONx = GA, Not Charging		30		µA
Voltage Reference		1.24	1.25	1.26	V
Oscillator Frequency		1.35	1.6	1.85	MHz
Logic High Input Voltage	ON1, ON2, ON3, VSEL	1.4			V
Logic Low Input Voltage	ON1, ON2, ON3, VSEL			0.4	V
Leakage Current	$V_{ON1} = V_{ON2} = V_{ON3} = V_{VSEL} = V_{nIRQ} = V_{nRSTO}$ = 4V			1	µA
nPBIN Internal Pull-up Resistance			50		kΩ
Low Level Output Voltage	nIRQ, nRSTO. Sinking 10mA		0.3		V
nRSTO Delay			260		ms
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis	Temperature decreasing		20		°C

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 2:

Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
06h	R	R	R	W/E	R	R	nPBMASK	PBSTAT

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1.

Table 3:

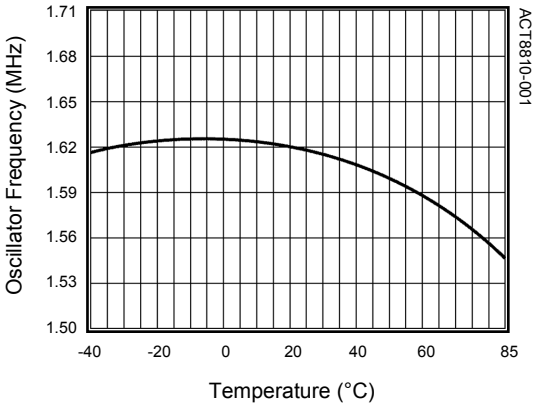
Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
06h	PBSTAT	[0]	R/W	Push Button Status	0	De-assert
					1	Asserted
06h	nPBMASK	[1]	R/W	Push Button Interrupt Mask Option	0	Masked
					1	Not Mask
06h		[3:2]	R		READ ONLY	
06h		[4]	W/E		WRITE-EXACT	
06h		[7:5]	R		READ ONLY	

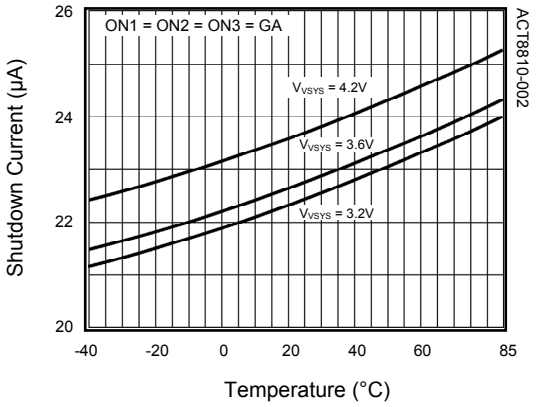
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

Oscillator Frequency vs. Temperature



Shutdown Current vs. Temperature



FUNCTIONAL DESCRIPTION

General Description

The ACT8810 offers a wide array of system management functions that allow it to be configured for optimal performance in a wide range of applications.

I²C Serial Interface

At the core of the ACT8810's flexible architecture is an I²C interface that permits optional programming capability to enhance overall system performance.

To ensure compatibility with a wide range of system processors, the ACT8810 uses standard I²C commands; I²C write-byte commands are used to program the ACT8810, and I²C read-byte commands are used to read the ACT8810's internal registers. The ACT8810 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011010x].

SDA is a bi-directional data line and SCL is a clock input. The master initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an "Acknowledge" (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I²C 2-wire serial interface, go to the NXP website: http://www.nxp.com

System Startup and Shutdown

Startup Sequence

The ACT8810 features a flexible enable architecture that allows it to support a variety of push-button enable/disable schemes. Although other startup routines are possible, ACT8810 provides three typical startup and shutdown processes proceed as shown in *Control Sequence* section.

Shutdown Sequence

Once a successful power-up routine is completed, a shutdown process may be initiated by asserting nPBIN a second time, typically as the result of pressing the push-button. Although the shutdown process is completely software-controlled, a typical shutdown sequence proceeds as follows: The second assertion of nPBIN asserts nPBIN and interrupts the microprocessor, which then initiates an interrupt service routine to reveal that nPBIN has been asserted. If there is no input to the charger, then the microprocessor disables each regulator according to the sequencing requirements of the system, then the system will finally be disabled when each of ON1, ON2, and ON3 have been de-asserted.

nPBIN Input

ACT8810's nPBIN pin is a dual-function pin, combining system enable/disable control with a hardware reset function. Refering to Figure 2, the two pin functions are obtained by asserting this pin low, either through a direct connection or through a 100kΩ resistor, as described below.

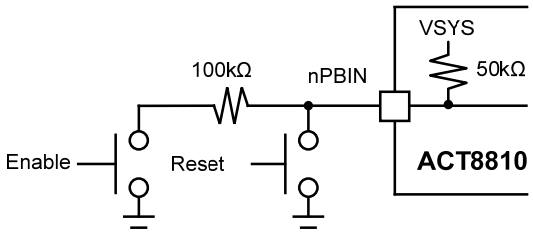
In most applications, nPBIN will be driven through a 100kΩ resistor. When driven in this way, nPBIN initiates system startup or shutdown, as described in the System Startup and Shutdown section.

When a hardware-reset function is desired, nPBIN may also be driven directly to GA. In this case, nRSTO is immediately asserted low and remains low until nPBIN is de-asserted and the reset timeout period expires. This provides a hardware-reset function, allowing the system to be manually reset if the system processor locks up.

Although a typical application will use momentary switches to drive nPBIN, as shown in Figure 2, nPBIN may also be driven by other sources, such as a GPIO or other logic output.

Figure 2:

nPBIN Input



Enable/Disable Inputs (ON1, ON2 and ON3)

The ACT8810 provides three manual enable/disable inputs, ON1, ON2 and ON3, which

FUNCTIONAL DESCRIPTION CONT'D

enable and disable REG1, REG2, and REG3, respectively. Once the system is enabled, the system will remain enabled until all of ON1, ON2, and ON3 have been de-asserted. See the *Control Sequence* section for more information.

Power-On Reset Output

nRSTO is an open-drain output which asserts low upon startup or when nPBIN is driven directly to GA, and remains asserted low until the 260ms (default) power-on reset timer has expired. Connect a 10kΩ or greater pull-up resistor from nRSTO to an appropriate voltage supply.

nIRQ Output

nIRQ is an open-drain output that asserts low any time startup or an unmasked fault condition exists. When asserted, nIRQ remains low until the microprocessor polls the ACT8810's I^2C interface. The ACT8810 supports a variety of other fault conditions, which may each be optionally unmasked via the I^2C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet.

Connect a pull-up resistor from nIRQ to an appropriate voltage supply. nIRQ is typically used to drive the interrupt input of the system processor, and is useful in a variety of software-controlled enable/disable control routines.

Thermal Shutdown

The ACT8810 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions. This circuitry disables all regulators if the ACT8810 die temperature exceeds 160°C, and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

Control Sequence

Sequence A

The ACT8810QJ1## which is set with "sequence A", has a system startup is initiated whenever the following conditions occurs:

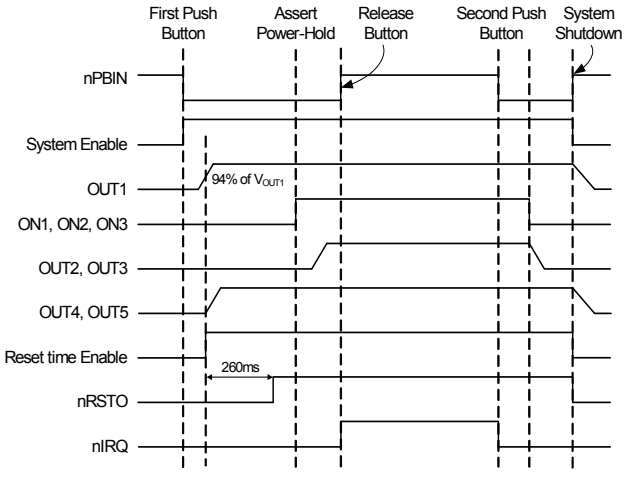
1) nPBIN is pushed low via 100kΩ resistance,

When ever this condition exists, the ACT8810QJ1## begins its system startup procedure by enabling REG1. When REG1 reaches 94% of its final regulation voltage, ACT8810QJ1## automatically turns on REG4 and REG5 and nRSTO is asserted low, holding the microprocessor in reset for a user-selectable reset period of 260ms. If V_{OUT1} is within 6% of its regulation voltage when the reset timer expires, the nRSTO is de-asserted, and the microprocessor can begin its power-up sequence. Once the power-up routine is successfully completed, the system remains enabled after the push-button is released as long as the microprocessor asserts any one of ON1, ON2 or ON3, and REG4, REG5 may be enabled or disabled via the I^2C interface.

This start-up procedure requires that the pushbutton be held until the microprocessor assumes control (by asserting any one of ON1, ON2, and ON3), providing protection against inadvertent momentary assertions of the pushbutton. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional time delay before asserting ON1, ON2, or ON3. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button, the ACT8810QJ1## automatically shuts itself down.

Figure 3:

Sequence A



Sequence B

The ACT8810QJ2## which is set with "sequence B", has a system startup is initiated whenever the following conditions occurs:

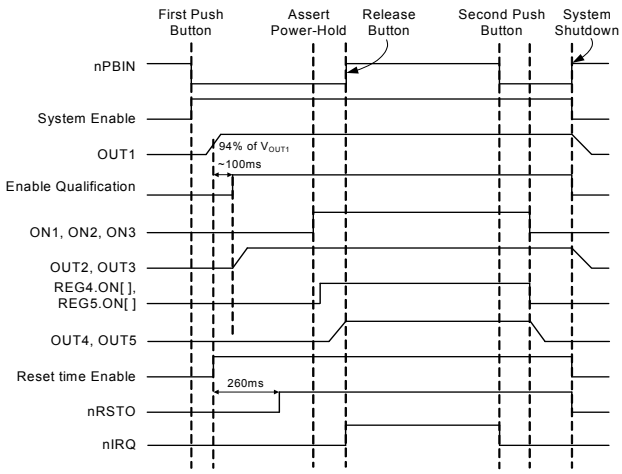
1) nPBIN is pushed low via 100kΩ resistance,

When ever this condition exists, the ACT8810QJ2## begins its system startup procedure by enabling REG1. When REG1 reaches 94% of its final regulation voltage, ACT8810QJ2## automatically turns on REG2 and REG3 and nRSTO is asserted low, holding the microprocessor in reset for a user-selectable reset period of 260ms. If V_{OUT1} is within 6% of its regulation voltage when the reset timer expires, the nRSTO is de-asserted, and the microprocessor can begin its power-up sequence. Once the power-up routine is successfully completed, the system remains enabled after the push-button is released as long as the microprocessor asserts any one of ON1, ON2 or ON3. REG4 and REG5 may be enabled if the microprocessor sets REG4.ON[] and REG5.ON[] to 1 via the I^2C interface. In other case, REG4 and REG5 are disable.

This start-up procedure requires that the pushbutton be held until the microprocessor assumes control (by asserting any one of ON1, ON2, and ON3), providing protection against inadvertent momentary assertions of the pushbutton. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional time delay before asserting ON1, ON2, or ON3. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button, the ACT8810QJ2## automatically shuts itself down.

Figure 4:

Sequence B



Sequence C

The ACT8810QJ3## which is set with "sequence C", has a system startup is initiated whenever the following conditions occurs:

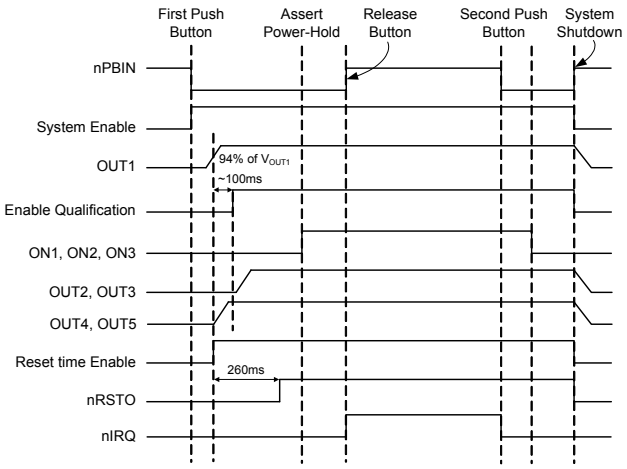
1) nPBIN is pushed low via 100kΩ resistance,

When ever this condition exists, the ACT8810QJ3## begins its system startup procedure by enabling REG1. When REG1 reaches 94% of its final regulation voltage, ACT8810QJ3## automatically turns on REG2, REG3, REG4, REG5 and nRSTO is asserted low, holding the microprocessor in reset for a user-selectable reset period of 260ms. If V_{OUT1} is within 6% of its regulation voltage when the reset timer expires, the nRSTO is de-asserted, and the microprocessor can begin its power-up sequence. Once the power-up routine is successfully completed, the system remains enabled after the push-button is released as long as the microprocessor asserts any one of ON1, ON2 or ON3, and REG4, REG5 may be enabled or disabled via the I^2C interface.

This start-up procedure requires that the pushbutton be held until the microprocessor assumes control (by asserting any one of ON1, ON2, and ON3), providing protection against inadvertent momentary assertions of the pushbutton. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional time delay before asserting ON1, ON2, or ON3. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button, the ACT8810QJ3## automatically shuts itself down.

Figure 5:

Sequence C



Sequence D

The ACT8810QJ4## which is set with "sequence D", has a system startup is initiated whenever the following conditions occurs:

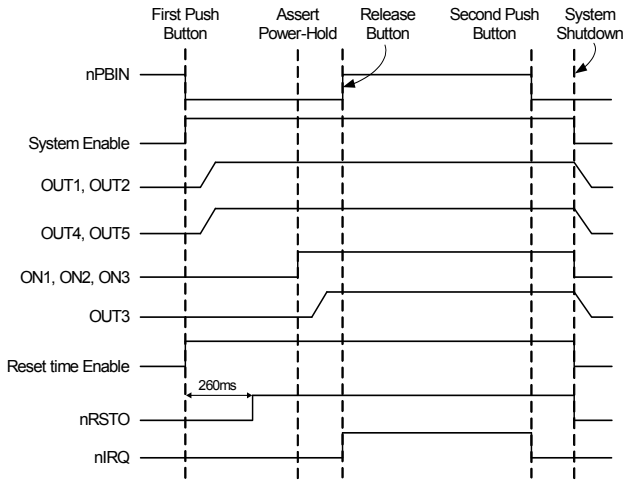
1) nPBIN is pushed low via 100kΩ resistance,

When ever this condition exists, the ACT8810QJ4## begins its system startup procedure by enabling REG1, REG2, REG4, and REG5. When ACT8810QJ4## in the first enable, nRSTO is asserted low, holding the microprocessor in reset for a user-selectable reset period of 260ms. when the reset timer expires, the nRSTO is de-asserted, and the microprocessor can begin its power-up sequence. Once the power-up routine is successfully completed, the system remains enabled after the push-button is released as long as the microprocessor asserts any one of ON1, ON2 or ON3, holding REG1, REG2, REG4, REG5, and enabling REG3. And any regulators could be enabled or disabled via the I^2C interface.

This start-up procedure requires that the pushbutton be held until the microprocessor assumes control (by asserting any one of ON1, ON2, and ON3), providing protection against inadvertent momentary assertions of the pushbutton. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional time delay before asserting ON1, ON2, or ON3. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button, the ACT8810QJ4## automatically shuts itself down.

Figure 6:

Sequence D



Sequence E

The ACT8810QJ5## which is set with "sequence E", has a system startup is initiated whenever the following conditions occurs:

1) A valid input voltage is present at VIN, or

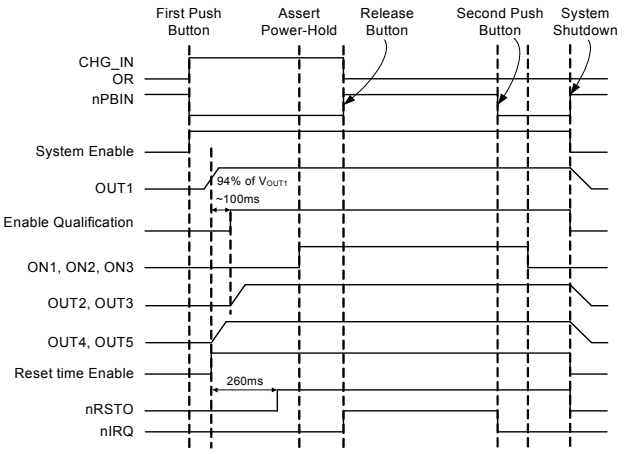
2) nPBIN is pushed low via 100kΩ resistance,

When ever this condition exists, the ACT8810QJ5## begins its system startup procedure by enabling REG1. When REG1 reaches 94% of its final regulation voltage, ACT8810QJ5## automatically turns on REG2, REG3, REG4, REG5 and nRSTO is asserted low, holding the microprocessor in reset for a user-selectable reset period of 260ms. If V_{OUT1} is within 6% of its regulation voltage when the reset timer expires, the nRSTO is de-asserted, and the microprocessor can begin its power-up sequence. Once the power-up routine is successfully completed, the system remains enabled after the push-button is released as long as the microprocessor asserts any one of ON1, ON2 or ON3, and REG4, REG5 may be enabled or disabled via the I^2C interface.

This start-up procedure requires that the pushbutton be held until the microprocessor assumes control (by asserting any one of ON1, ON2, and ON3), providing protection against inadvertent momentary assertions of the pushbutton. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional time delay before asserting ON1, ON2, or ON3. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button or un-plug charger input, the ACT8810QJ5## automatically shuts itself down.

Figure 7:

Sequence E



ELECTRICAL CHARACTERISTICS (REG1)

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP1 Operating Voltage Range		2.9		5.5	V
VP1 UVLO Threshold	Input Voltage Rising	2.7	2.8	2.9	V
VP1 UVLO Hysteresis	Input Voltage Falling		85		mV
Quiescent Supply Current			130	200	µA
Shutdown Supply Current	REG1 is disabled, V_{VP1} = 4.2V		0.1	1	µA
Output Voltage Accuracy	V_{NOM1} < 1.5V, I_{OUT1} = 10mA	-2.1%	V_{NOM1}①	+2.1%	V
	V_{NOM1} ≥ 1.5V, I_{OUT1} = 10mA	-1.5%	V_{NOM1}	+1.5%	
Line Regulation	V_{VP1} = Max(V_{NOM1} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT1} = 10mA to 1.3A		0.0017		%/mA
Current Limit		1.4	1.8		A
Oscillator Frequency	V_{OUT1} ≥ 20% of V_{NOM1}	1.35	1.6	1.85	MHz
	V_{OUT1} = 0V		540		kHz
PMOS On-Resistance	I_{SW1} = -100mA		0.16	0.24	Ω
NMOS On-Resistance	I_{SW1} = 100mA		0.16	0.24	Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM1}
Minimum On-Time			60		ns

①: V_{NOM1} refers to the nominal output voltage level for V_{OUT1} as defined by the *Ordering Information* section.

ELECTRICAL CHARACTERISTICS (REG2)

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP2 Operating Voltage Range		2.9		5.5	V
VP2 UVLO Threshold	Input Voltage Rising	2.7	2.8	2.9	V
VP2 UVLO Hysteresis	Input Voltage Falling		85		mV
Quiescent Supply Current			130	200	µA
Shutdown Supply Current	REG2 Disabled, V_{VP2} = 4.2V		0.1	1	µA
Output Voltage Regulation Accuracy	V_{NOM2} < 1.5V, I_{OUT2} = 10mA	-2.1%	V_{NOM2}①	+2.1%	V
	V_{NOM2} ≥ 1.5V, I_{OUT2} = 10mA	-1.5%	V_{NOM2}	+1.5%	
Line Regulation	V_{VP2} = Max(V_{NOM2} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT2} = 10mA to 1.0A		0.0017		%/mA
Current Limit		1.15	1.45		A
Oscillator Frequency	V_{OUT2} ≥ 20% of V_{NOM2}	1.35	1.6	1.85	MHz
	V_{OUT2} = 0V		540		kHz
PMOS On-Resistance	I_{SW2} = -100mA		0.25	0.38	Ω
NMOS On-Resistance	I_{SW2} = 100mA		0.17	0.26	Ω
SW2 Leakage Current	V_{VP2} = 5.5V, V_{SW2} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM2}
Minimum On-Time			60		ns

①: V_{NOM2} refers to the nominal output voltage level for V_{OUT2} as defined by the *Ordering Information* section.

ELECTRICAL CHARACTERISTICS (REG3)

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

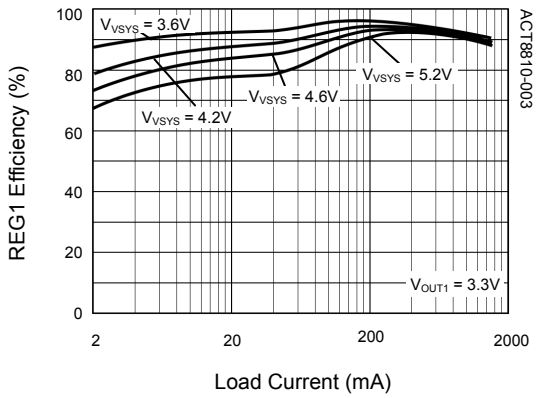
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP3 Operating Voltage Range		2.9		5.5	V
VP3 UVLO Threshold	Input Voltage Rising	2.7	2.8	2.9	V
VP3 UVLO Hysteresis	Input Voltage Falling		85		mV
Quiescent Supply Current			130	200	µA
Shutdown Supply Current	REG3 Disabled, V_{VP3} = 4.2V		0.1	1	µA
Output Voltage Regulation Accuracy	V_{NOM3} < 1.5V, I_{OUT3} = 10mA	-2.1%	V_{NOM3}①	+2.1%	V
	V_{NOM3} ≥ 1.5V, I_{OUT3} = 10mA	-1.5%	V_{NOM3}	+1.5%	
Line Regulation	V_{VP3} = Max(V_{NOM3} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT3} = 10mA to 550mA		0.0017		%/mA
Current Limit		0.55	0.7		A
Oscillator Frequency	V_{OUT3} ≥ 20% of V_{NOM3}	1.35	1.6	1.85	MHz
	V_{OUT3} = 0V		540		kHz
PMOS On-Resistance	I_{SW3} = -100mA		0.46	0.69	Ω
NMOS On-Resistance	I_{SW3} = 100mA		0.3	0.45	Ω
SW3 Leakage Current	V_{VP3} = 5.5V, V_{SW3} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM3}
Minimum On-Time			60		ns

①: V_{NOM3} refers to the nominal output voltage level for V_{OUT3} as defined by the *Ordering Information* section.

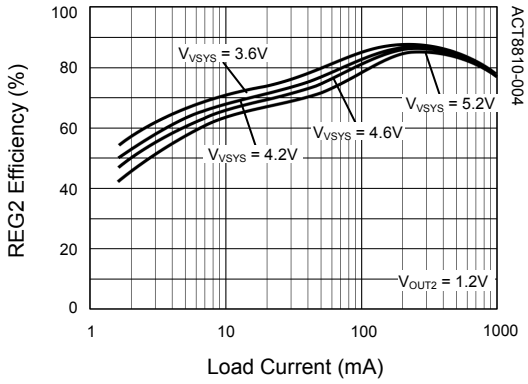
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8810QJ343, $V_{VP1} = V_{VP2} = 3.6V$, L = 3.3µH, $C_{VP1} = C_{VP2} = 4.7µF$, $C_{OUT1} = 22µF$, $C_{OUT2} = 10µF$, $T_A = 25°C$, unless otherwise specified.)

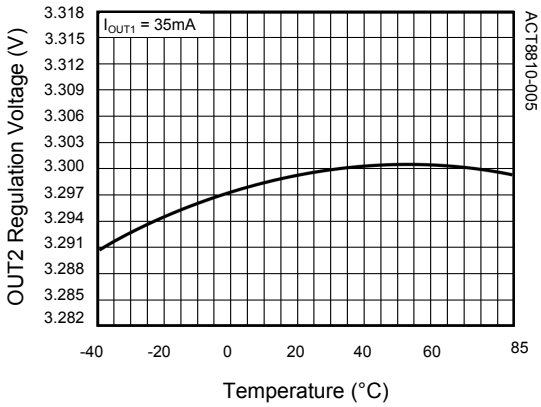
REG1 Efficiency vs. Load Current



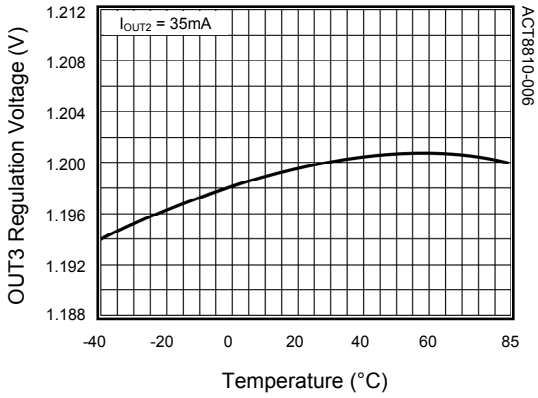
REG2 Efficiency vs. Load Current



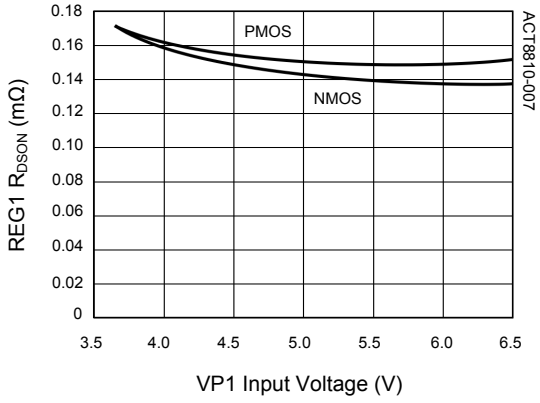
OUT1 Regulation Voltage vs. Temperature



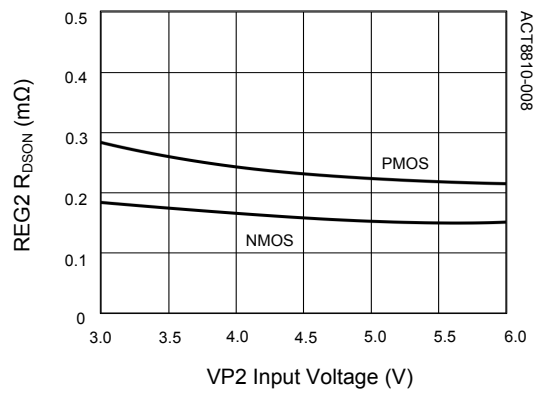
OUT2 Regulation Voltage vs. Temperature



REG1 R_{DSON} vs. VP1 Input Voltage



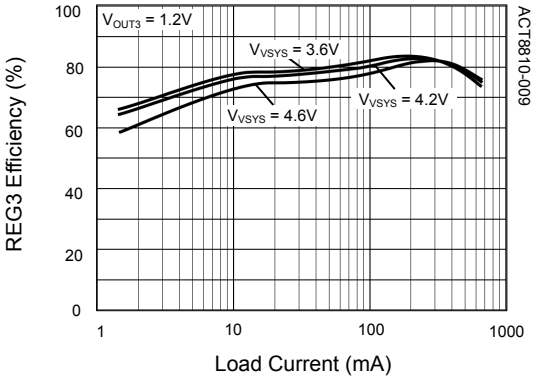
REG2 R_{DSON} vs. VP2 Input Voltage



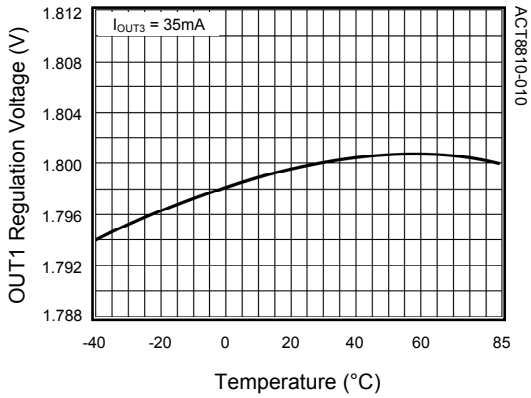
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(ACT8810QJ343, V_{VP3} = 3.6V, L = 3.3µH, C_{VP3} = 4.7µF, C_{OUT3} = 10µF, T_A = 25°C, unless otherwise specified.)

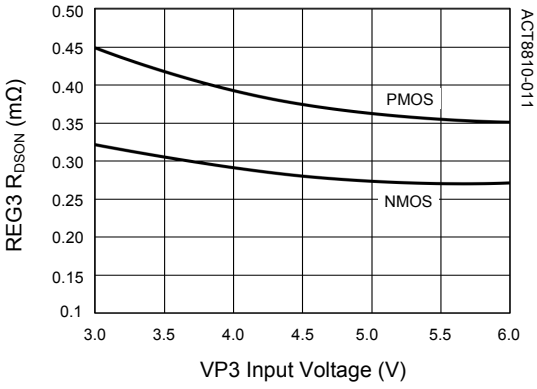
REG3 Efficiency vs. Load Current



OUT3 Regulation Voltage vs. Tempera-



REG3 R_{DSON} vs. VP3 Input Voltage



REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 4:

REG1 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
10h	R	R	VSET1					
11h	R	R	R	R	R	R	R	R
12h	R	R	R	R	R	nFLTMSK	OK	ON
13h	R	VRANGE	VSET0					

R: Read-Only bits. Default Values May Vary.

Table 5:

REG1 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
10h	VSET1	[5:0]	R/W	REG1 Standby Output Voltage Selection	See Table 4	
10h		[7:6]	R		READ ONLY	
11h		[7:0]	R		READ ONLY	
12h	ON	[0]	R/W	REG1 Enable	0	REG1 Disable
					1	REG1 Enable
12h	OK	[1]	R	REG1 Power-OK	0	Output is not OK
					1	Output is OK
12h	nFLTMSK	[2]	R/W	REG1 Output Voltage Fault Mask Option	0	Masked
					1	Not Mask
12h		[7:3]	R		READ ONLY	
13h	VSET0	[5:0]	R/W	REG1 Output Voltage Selection	See Table 4	
13h	VRANGE	[6]	R/W	REG1 Voltage Range	0	Min V_{OUT} = 0.8V
					1	Min V_{OUT} = 1.25V
13h		[7]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 6:

REG1/VSETx[ ] Output Voltage Setting

REG1/VSETx[3:0]	REG1/VSETx[5:4]							
	REG1/VRANGE[ ] = [0]①				REG1/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	Adjustable②	1.025	1.425	1.825	Adjustable	2.050	2.850	3.650
0001	0.800	1.050	1.450	1.850	1.300	2.100	2.900	3.700
0010	0.800	1.075	1.480	1.875	1.350	2.150	2.950	3.750
0011	0.800	1.100	1.500	1.900	1.400	2.200	3.000	3.800
0100	0.800	1.125	1.525	1.925	1.450	2.250	3.050	3.850
0101	0.800	1.150	1.550	1.950	1.500	2.300	3.100	3.900
0110	0.800	1.175	1.575	1.975	1.550	2.350	3.150	3.950
0111	0.800	1.200	1.600	2.000	1.600	2.400	3.200	4.000
1000	0.825	1.225	1.625	2.025	1.650	2.450	3.250	4.050
1001	0.850	1.250	1.650	2.050	1.700	2.500	3.300	4.100
1010	0.875	1.275	1.675	2.075	1.750	2.550	3.350	4.150
1011	0.900	1.300	1.700	2.100	1.800	2.600	3.400	4.200
1100	0.925	1.325	1.725	2.125	1.850	2.650	3.450	4.250
1101	0.950	1.350	1.750	2.150	1.900	2.700	3.500	4.300
1110	0.975	1.375	1.775	2.175	1.950	2.750	3.550	4.350
1111	1.000	1.400	1.800	2.200	2.000	2.800	3.600	4.400

①: Care must be taken when adjusting the VRANGE[ ] selection at address 13h bit-6 to avoid undesired output voltage selections. The VRANGE bit allows selection of the two output voltage ranges available for REG1, REG2 and REG3 (VRANGE = 0 – V_{OUT} range 0.8V to 2.2V, VRANGE = 1 – V_{OUT} range 1.3V to 4.4V). It is recommended that the user first establishes if the new V_{OUT} voltage is within the current selected voltage range (selected by VRANGE) prior to changing the value of the VRANGE bit.

②: Refer to the *Output Voltage Programming* section for more information.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 7:

REG2 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
20h	R	R	VSET1					
21h	R	R	R	R	R	R	R	R
22h	R	R	R	R	R	nFLTMSK	OK	ON
23h	R	VRANGE	VSET0					

R: Read-Only bits. Default Values May Vary.

Table 8:

REG2 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
20h	VSET1	[5:0]	R/W	REG2 Standby Output Voltage Selection	See Table 7	
20h		[7:6]	R		READ ONLY	
21h		[7:0]	R		READ ONLY	
22h	ON	[0]	R/W	REG2 Enable	0	REG2 Disable
					1	REG2 Enable
22h	OK	[1]	R	REG2 Power-OK	0	Output is not OK
					1	Output is OK
22h	nFLTMSK	[2]	R/W	REG2 Output Voltage Fault Mask Option	0	Masked
					1	Not Mask
22h		[7:3]	R		READ ONLY	
23h	VSET0	[5:0]	R/W	REG2 Output Voltage Selection	See Table 7	
23h	VRANGE	[6]	R/W	REG2 Voltage Range	0	Min V_{OUT} = 0.8V
					1	Min V_{OUT} = 1.25V
23h		[7]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 9:

REG2/VSETx[ ] Output Voltage Setting

REG2/VSETx[3:0]	REG2/VSETx[5:4]							
	REG2/VRANGE[ ] = [0]①				REG2/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	Adjustable②	1.025	1.425	1.825	Adjustable	2.050	2.850	3.650
0001	0.800	1.050	1.450	1.850	1.300	2.100	2.900	3.700
0010	0.800	1.075	1.480	1.875	1.350	2.150	2.950	3.750
0011	0.800	1.100	1.500	1.900	1.400	2.200	3.000	3.800
0100	0.800	1.125	1.525	1.925	1.450	2.250	3.050	3.850
0101	0.800	1.150	1.550	1.950	1.500	2.300	3.100	3.900
0110	0.800	1.175	1.575	1.975	1.550	2.350	3.150	3.950
0111	0.800	1.200	1.600	2.000	1.600	2.400	3.200	4.000
1000	0.825	1.225	1.625	2.025	1.650	2.450	3.250	4.050
1001	0.850	1.250	1.650	2.050	1.700	2.500	3.300	4.100
1010	0.875	1.275	1.675	2.075	1.750	2.550	3.350	4.150
1011	0.900	1.300	1.700	2.100	1.800	2.600	3.400	4.200
1100	0.925	1.325	1.725	2.125	1.850	2.650	3.450	4.250
1101	0.950	1.350	1.750	2.150	1.900	2.700	3.500	4.300
1110	0.975	1.375	1.775	2.175	1.950	2.750	3.550	4.350
1111	1.000	1.400	1.800	2.200	2.000	2.800	3.600	4.400

①: Care must be taken when adjusting the VRANGE[ ] selection at address 23h bit-6 to avoid undesired output voltage selections. The VRANGE bit allows selection of the two output voltage ranges available for REG1, REG2 and REG3 (VRANGE = 0 – V_{OUT} range 0.8V to 2.2V, VRANGE = 1 – V_{OUT} range 1.3V to 4.4V). It is recommended that the user first establishes if the new V_{OUT} voltage is within the current selected voltage range (selected by VRANGE) prior to changing the value of the VRANGE bit.

②: Refer to the *Output Voltage Programming* section for more information.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 10:

REG3 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
30h	R	R	VSET1					
31h	R	R	R	R	R	R	R	R
32h	R	R	R	R	R	nFLTMSK	OK	ON
33h	R	VRANGE	VSET0					

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1

Table 11:

REG3 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
30h	VSET1	[5:0]	R/W	REG3 Standby Output Voltage Selection	See Table 10	
30h		[7:6]	R		READ ONLY	
31h		[7:0]	R		READ ONLY	
32h	ON	[0]	R/W	REG3 Enable	0	REG3 Disable
					1	REG3 Enable
32h	OK	[1]	R	REG3 Power-OK	0	Output is not OK
					1	Output is OK
32h	nFLTMSK	[2]	R/W	REG3 Output Voltage Fault Mask Option	0	Masked
					1	Not Mask
32h		[7:3]	R		READ ONLY	
33h	VSET0	[5:0]	R/W	REG3 Output Voltage Selection	See Table 10	
33h	VRANGE	[6]	R/W	REG3 Voltage Range	0	Min V_{OUT} = 0.8V
					1	Min V_{OUT} = 1.25V
33h		[7]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 12:
REG3/VSETx[ ] Output Voltage Setting

REG3/VSETx[3:0]	REG3/VSETx[5:4]							
	REG3/VRANGE[ ] = [0]①				REG3/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	Adjustable②	1.025	1.425	1.825	Adjustable	2.050	2.850	3.650
0001	0.800	1.050	1.450	1.850	1.300	2.100	2.900	3.700
0010	0.800	1.075	1.480	1.875	1.350	2.150	2.950	3.750
0011	0.800	1.100	1.500	1.900	1.400	2.200	3.000	3.800
0100	0.800	1.125	1.525	1.925	1.450	2.250	3.050	3.850
0101	0.800	1.150	1.550	1.950	1.500	2.300	3.100	3.900
0110	0.800	1.175	1.575	1.975	1.550	2.350	3.150	3.950
0111	0.800	1.200	1.600	2.000	1.600	2.400	3.200	4.000
1000	0.825	1.225	1.625	2.025	1.650	2.450	3.250	4.050
1001	0.850	1.250	1.650	2.050	1.700	2.500	3.300	4.100
1010	0.875	1.275	1.675	2.075	1.750	2.550	3.350	4.150
1011	0.900	1.300	1.700	2.100	1.800	2.600	3.400	4.200
1100	0.925	1.325	1.725	2.125	1.850	2.650	3.450	4.250
1101	0.950	1.350	1.750	2.150	1.900	2.700	3.500	4.300
1110	0.975	1.375	1.775	2.175	1.950	2.750	3.550	4.350
1111	1.000	1.400	1.800	2.200	2.000	2.800	3.600	4.400

①: Care must be taken when adjusting the VRANGE[ ] selection at address 33h bit-6 to avoid undesired output voltage selections. The VRANGE bit allows selection of the two output voltage ranges available for REG1, REG2 and REG3 (VRANGE = 0 – V_{OUT} range 0.8V to 2.2V, VRANGE = 1 – V_{OUT} range 1.3V to 4.4V). It is recommended that the user first establishes if the new V_{OUT} voltage is within the current selected voltage range (selected by VRANGE) prior to changing the value of the VRANGE bit.

②: Refer to the *Output Voltage Programming* section for more information.

FUNCTIONAL DESCRIPTION

General Description

REG1, REG2, and REG3 are fixed-frequency, current-mode, synchronous PWM step-down converters that are capable of supplying up to 1.3A, 1.0A, and 0.55A of output current, respectively. These regulators operate with a fixed frequency of 1.6MHz, minimizing noise in sensitive applications and allowing the use of small external components, and achieve peak efficiencies of up to 97%.

Each step-down DC/DC is available with a variety of standard and custom output voltages, which may be software-controlled by systems requiring advanced power management functions, via the I^2C interface.

Buck Regulator PFM/PWM Operating Modes

The buck converters offer PFM/PWM operating modes to maximize efficiency under both light and full load conditions. The device will automatically transition from fixed frequency PWM mode to PFM mode when the output current is approximately 100mA. In PFM mode, the device maintains output voltage regulation by adjusting the switching frequency. The device transitions into fixed frequency PWM mode when the output current reaches approximately 100mA.

100% Duty Cycle Operation

REG1, REG2 and REG3 are each capable of operating at up to 100% duty cycle. During 100% duty-cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

Synchronous Rectification

REG1, REG2 and REG3 each feature integrated channel synchronous rectifiers, maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Enabling and Disabling REG1, REG2 and REG3

REG1, REG2, and REG3 are typically enabled and disabled using the ACT8810's closed-loop enable/disable control scheme, including the nPBIN input. Refer to the *System Startup and Shutdown* section for more information about this function.

Each regulator is enabled when the following conditions are met:

1) ONx is asserted high to enable REGx,
2) REGx/ONx[ ] is set to 1 when ONx is high

In addition REG1, REG2, or REG3 may be enabled when nPBIN is pushed low via 100kΩ resistance. It depends on sequence is set. See the *Control Sequence* section for more information.

When none of these conditions are true, REG1, REG2 and REG3 are disabled, and each regulator's quiescent supply current drops to less than 1μA.

Power-OK

REG1, REG2 and REG3 each feature a variety of status bits that can be read by the system microprocessor. If any output falls below its power-OK threshold, typically 6% below the programmed regulation voltage, REGx/OK[ ] is cleared to 0.

Soft-Start

REG1, REG2 and REG3 each include matched soft-start circuitry. When enabled, the output voltages track the internal 80μs soft-start ramp and both power up in a monotonic manner that is independent of loading on either output. This circuitry ensures that each output powers up in a controlled manner, greatly simplifying power sequencing design considerations.

Compensation

REG1, REG2 and REG3 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guide lines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 4.7μF ceramic capacitor for each of REG1, REG2 and REG3 is recommended for most applications.

Output Capacitor Selection

For most applications, 22μF ceramic output capacitors are recommended for REG1 and 10μF ceramic output capacitors are recommended for REG2, REG3. Although the these regulators were designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR, low-ESR tantalum capacitors can provide acceptable results as well.

FUNCTIONAL DESCRIPTION CONT'D

Inductor Selection

REG1, REG2 and REG3 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range.

REG1, REG2 and REG3 of the device were optimized for operation with and 3.3µH inductor, although inductors in the 2.2µH to 4.7µH range can be used.

Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current of the application by at least 30%.

Output Voltage Programming

By default, REG1, REG2 and REG3 each power up and regulate to their default output voltage, as defined in the *Ordering Information* section. Once the system is enabled, each regulator's output voltage may be modified through either the I^2C interface or the Voltage Selection (VSEL) pin.

Programming via the I^2C Interface

Following startup, REG1, REG2, and REG3 may be independently programmed to different values by writing to the REGx/VSETx[ ] and REGx/VRANGE[ ] registers via the I^2C interface. To program each regulator, first select the desired output voltage range via the REGx/VRANGE[ ] bit. Each regulator supports two overlapping ranges; set REGx/VRANGE[ ] to 0 for voltages below 2.245V, set REGx/VRANGE[ ] to 1 for voltages above 1.25V.

Once the desired range has been selected, program the output to a voltage within that range by setting the REGx/VSETx bits. For more information about the output voltage setting options, refer to Tables 4, 7, and 10, for REG1, REG2, and REG3, respectively.

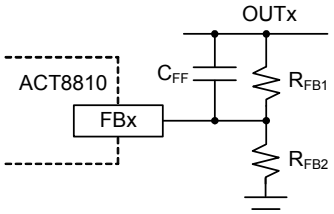
Programming with Adjustable Option

Figure 8 shows the feedback network necessary to set the output voltage when using the adjustable output voltage option. Select components as follows: Set R_{FB2} = 51kΩ, then calculate R_{FB1} using the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUTx}}{V_{FBx}} - 1\right) \qquad (1)$$

Where V_{FBx} is 0.625V when REGx × VRANGE[ ] = 0 and 1.25V when REGx × VRANGE[ ] = 1

Figure 8:
Output Voltage Programming



Finally choose C_{FF} using the following equation:

$$C_{FF} = \frac{2.2 \times 10^{-6}}{R_{FB1}} \qquad (2)$$

Where R_{FB1} = 47kΩ, use 47pF.

When using Adjustable Option, OUTx pins works as FBx function.

Output Voltage Selection Pin (VSEL)

ACT8810's VSEL pin provides a simple means of alternating between two preset output voltage settings, such as may be needed for dynamic voltage selection (DVS). The operation of this pin is as follows: when VSEL is driven to GA or a logic low, the output voltages of REG1, REG2, and REG3 are each defined by their VSET0[ ] register. when VSEL is driven to VSYS or a logic high, the output voltages of REG1, REG2, and REG3 are each defined by their VSET1[ ] register.

By default, each regulator's VSET0[ ] and VSET1[ ] registers are both programmed to the same voltage, as defined in the Ordering Information section. As a result, toggling VSET under default conditions has no affect. However, by re-programming one or more regulator's VSET0[ ] and/or VSET1[ ] registers, one can easily toggle these regulators' output voltages between two sets of voltages, such as to implement 'normal' and 'standby' modes in a system utilizing the ACT8810 to implement an advanced power management architecture.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors.

Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as

FUNCTIONAL DESCRIPTION CONT'D

close as possible to the IC, and avoiding the use of vias if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple vias. The output node for each regulator should be connected to its corresponding OUTx pin through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple vias to achieve low electrical and thermal resistance.

ELECTRICAL CHARACTERISTICS (REG4)

(V_{INL} = 3.6V, C_{OUT4} = 1µF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL Operating Voltage Range		2.6		5.5	V
INL UVLO Threshold	V_{INL} Input Rising	2.4	2.5	2.6	V
UVLO Hysteresis	V_{INL} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-2%	V_{NOM4}①	+2%	V
	T_A = -40°C to 85°C	-3%	V_{NOM4}	+3%	
Line Regulation Error	V_{INL} = Max(V_{OUT5} + 0.5V, 3.6V) to 5.5V		0		%/V
Load Regulation Error	I_{OUT5} = 1mA to 360mA		-0.006		%/mA
Power Supply Rejection Ratio②	f = 1kHz, I_{OUT4} = 360mA, C_{OUT4} = 1µF		70		dB
	f = 10kHz, I_{OUT4} = 360mA, C_{OUT4} = 1µF		60		
Supply Current per Output	Regulator Enabled		35		µA
	Regulator Disabled		0		
Dropout Voltage③	I_{OUT4} = 160mA, V_{OUT4} > 3.1V		100	200	mV
Output Current				360	mA
Current Limit④	V_{OUT4} = 95% of regulation voltage	400			
Internal Soft-Start			100		µs
Power Good Flag High Threshold	V_{OUT4}, hysteresis = -2%		88		%
Output Noise	C_{OUT4} = 10µF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT4} Range		1		20	µF
Discharge Resistor in Shutdown	LDO Disabled, DIS4[ ] = [1]		1000		Ω

①: V_{NOM4} refers to the nominal output voltage level for V_{OUT4} as defined by the *Ordering Information* section.

②: PSRR is lower with V_{SET} < 1.25V

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage (for 2.8V output voltage or higher)

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 40% (typ)

ELECTRICAL CHARACTERISTICS (REG5)

(V_{INL} = 3.6V, C_{OUT5} = 1μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL Operating Voltage Range		2.6		5.5	V
INL UVLO Threshold	V_{INL} Input Rising	2.4	2.5	2.6	V
UVLO Hysteresis	V_{INL} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-2%	V_{NOM5}①	+2%	V
	T_A = -40°C to 85°C	-3%	V_{NOM5}	+3%	
Line Regulation Error	V_{INL} = Max(V_{OUT5} + 0.5V, 3.6V) to 5.5V		0		%/V
Load Regulation Error	I_{OUT5} = 1mA to 360mA		-0.006		%/mA
Power Supply Rejection Ratio②	f = 1kHz, I_{OUT5} = 360mA, C_{OUT5} = 1μF		70		dB
	f = 10kHz, I_{OUT5} = 360mA, C_{OUT5} = 1μF		60		
Supply Current per Output	Regulator Enabled		35		μA
	Regulator Disabled		0		
Dropout Voltage③	I_{OUT5} = 160mA, V_{OUT5} > 3.1V		100	200	mV
Output Current				360	mA
Current Limit④	V_{OUT5} = 95% of regulation voltage	400			mA
Internal Soft-Start			100		μs
Output Noise	C_{OUT5} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT5} Range		1		20	μF
Discharge Resistor in Shutdown	LDO Disabled, DIS5[ ] = [1]		1000		Ω

①: V_{NOM5} refers to the nominal output voltage level for V_{OUT5} as defined by the *Ordering Information* section.

②: PSRR is lower with V_{SET} < 1.25V

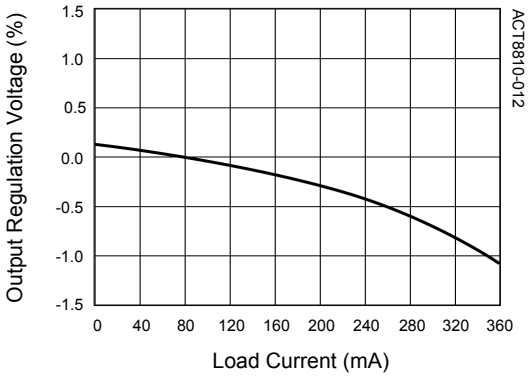
③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage (for 2.8V output voltage or higher)

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 40% (typ)

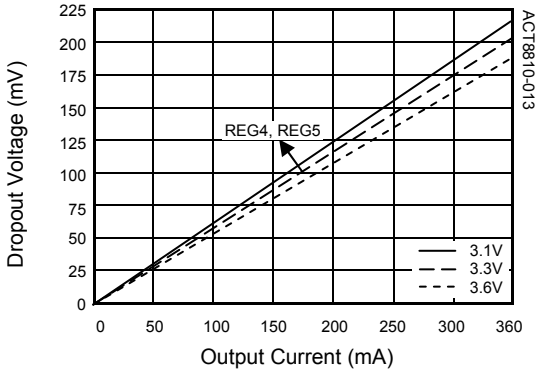
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8810QJ343, V_{VSYS} = 5V, T_A = 25°C, unless otherwise specified.)

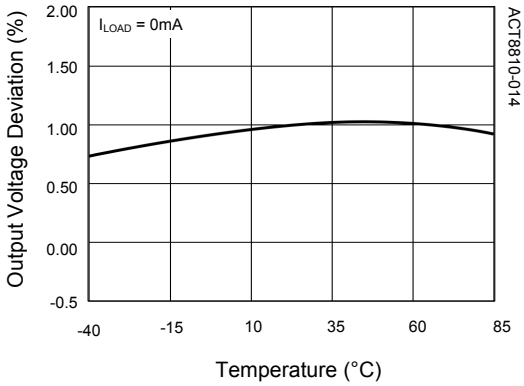
Output Regulation Voltage vs. Load Current



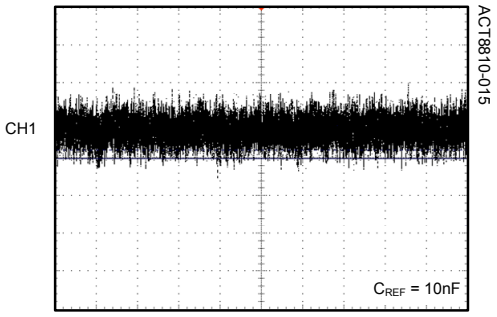
Dropout Voltage vs. Output Current



Output Voltage Deviation vs. Temperature

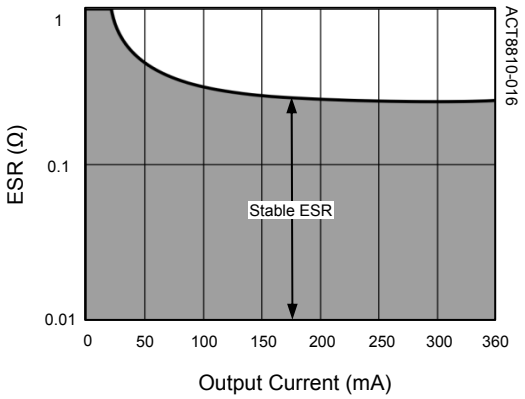


LDO Output Voltage Noise



CH1: V_{OUTx}, 200μV/div (AC COUPLED)
TIME: 200ms/div

Region of Stable C_{OUT} ESR vs. Output Current



REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 13:

REG45 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
40h	DIS4	R	ON4	VSET4				
41h	DIS5	R	ON5	VSET5				
43h	R	R	R	R	R	R	nFLTMSK	OK

R: Read-Only bits. Default Values May Vary.

Table 14:

REG45 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
40h	VSET4	[4:0]	R/W	REG4 Output Voltage Selection	See Table 15	
40h	ON4	[5]	R/W	REG4 Enable	0	REG4 Disable
					1	REG4 Enable
40h		[6]	R		READ ONLY	
40h	DIS4	[7]	R/W	REG4 Discharge Enable	0	Discharge Disable
					1	Discharge Enable
41h	VSET5	[4:0]	R/W	REG5 Output Voltage Selection	See Table 15	
41h	ON5	[5]	R/W	REG5 Enable	0	REG5 Disable
					1	REG5 Enable
41h		[6]	R		READ ONLY	
41h	DIS5	[7]	R/W	REG5 Discharge Enable	0	Discharge Disable
					1	Discharge Enable
43h	OK	[0]	R	REG4 Power-OK	0	Output is not OK
					1	Output is OK
43h	nFLTMSK	[1]	R/W	REG4 Output Voltage Fault Mask Option	0	Masked
					1	Not Mask
43h		[7:2]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 15:
REG45/VSETx[ ] Output Voltage Setting

REG45CFG/VSETx[2:0]	REG45CFG/VSETx[4:3]			
	00	**01**	**10**	**11**
000	0.90	1.45	1.90	2.75
001	1.00	1.50	2.00	2.80
010	1.10	1.55	2.10	2.85
011	1.20	1.60	2.20	2.90
100	1.25	1.70	2.40	3.00
101	1.30	1.75	2.50	3.10
110	1.35	1.80	2.60	3.20
111	1.40	1.85	2.70	3.30

FUNCTIONAL DESCRIPTION

General Description

REG4 and REG5 are low-noise, low-dropout linear regulators (LDOs) that are optimized for low noise and high-PSRR operation, achieving more than 60dB PSRR at frequencies up to 10kHz.

LDO Output Voltage Programming

All LDOs feature independently-programmable output voltages that are set via the I^2C serial interface, increasing the ACT8810's flexibility while reducing total solution size and cost. Set the output voltage by writing to the REG45CFG/VSETx[ ] registers.

Output Current Capability

REG4 and REG5 each supply an output current of 360mA. Excellent performance is achieved over this load current range.

Output Current Limit

In order to ensure safe operation under over-load conditions, each LDO features current-limit circuitry with current fold-back. The current-limit circuitry limits the current that can be drawn from the output, providing protection in over-load conditions. For additional protection under extreme over current conditions, current-fold-back protection reduces the current-limit by approximately 40% under extreme overload conditions.

Enabling and Disabling the LDOs

All LDOs feature independent enable/disable control via the I^2C serial interface. Independently enable or disable each output by writing to the appropriate REG45CFG/ONx[ ] bit.

In addition REG4 or REG5 may be enable when nPBIN is pushed low via 100kΩ resistance. It depends on sequence is set. See the *Control Sequence* section for more information.

Power-OK

REG4 features power-OK status bit that can be read by the system microprocessor via the I^2C interface. If an output voltage is lower than the power-OK threshold, typically 12% below the programmed regulation voltage, the corresponding REG45CFG/OK[ ] will clear to 0.

Reference Bypass Pin

The ACT8810 contains a reference bypass pin which filters noise from the reference, providing a low noise voltage reference to the LDOs. Bypass REFBP to GA with a 0.01µF ceramic capacitor.

Optional LDO Output Discharge

Each of the ACT8810's LDOs features an optional, independent output voltage discharge feature. When this feature is enabled, the LDO output is discharged to ground through a 1kΩ resistance when the LDO is shutdown. This feature may be enabled or disabled via the I^2C interface by writing to the REG45CFG/DISx[ ] bits.

Output Capacitor Selection

REG4 and REG5 each require only a small ceramic capacitor for stability. For best performance, each output capacitor should be connected directly between the OUTx and GA pins as possible, with a short and direct connection. To ensure best performance for the device, the output capacitor should have a minimum capacitance of 1µF, and ESR value between 10mΩ and 200mΩ. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

PCB Layout Considerations

The ACT8810's LDOs provide good DC, AC, and noise performance over a wide range of operating conditions, and are relatively insensitive to layout considerations. When designing a PCB, however, careful layout is necessary to prevent other circuitry from degrading LDO performance. A good design places input and output capacitors as close to the LDO inputs and output as possible, and utilizes a star-ground configuration for all regulators to prevent noise-coupling through ground. Output traces should be routed to avoid close proximity to noisy nodes, particularly the SW nodes of the DC/DCs. REFBP is a filtered reference noise, and internally has a direct connection to the linear regulator controller. Any noise injected onto REFBP will directly affect the outputs of the linear regulators, and therefore special care should be taken to ensure that no noise is injected to the outputs via REFBP. As with the LDO output capacitors, the REFBP bypass capacitor should be placed as close to the IC as possible, with short, direct connections to the star-ground. Avoid the use of vias whenever possible. Noisy nodes, such as from the DC/DCs, should be routed as far away from REFBP as possible.

ELECTRICAL CHARACTERISTICS (REG6)

(T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range		2.6		5.5	V
Output Voltage Accuracy	T_A = 25°C	-2%	V_{NOM6}①	+2%	V
	T_A = -40°C to 85°C	-3%	V_{NOM6}	+3%	
Line Regulation Error	V_{INL} = V_{OUT6} + 0.5V to V_{INL} = 5.5V		0.1		%/V
Load Regulation Error	I_{OUT6} = 0mA to 30mA		-0.01		%/mA
Input Supply Current	ON1 = ON2 = ON3 = GA		6	12	µA
Dropout Voltage②	I_{OUT6} = 10mA		35	70	mV
Output Current				30	mA
Current Limit③	V_{OUT6} = 95% of regulation voltage	45			mA
Stable C_{OUT6} Range		1		20	µF

①: V_{NOM6} refers to the nominal output voltage level for V_{OUT6} as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage (for 2.8V output voltage or higher)

③: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 16:

REG6 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
42h	R	R	R	VSET6				

R: Read-Only bits. Default Values May Vary.

Table 17:

REG6 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION
42h	VSET6	[4:0]	R/W	REG6 Output Voltage Selection	See Table 18
42h		[7:5]	R		READ ONLY

Table 18:

REG6/VSETx[ ] Output Voltage Setting

REG6CFG/VSETx[2:0]	REG6CFG/VSETx[4:3]			
	00	01	10	11
000	0.90	1.45	1.90	2.75
001	1.00	1.50	2.00	2.80
010	1.10	1.55	2.10	2.85
011	1.20	1.60	2.20	2.90
100	1.25	1.70	2.40	3.00
101	1.30	1.75	2.50	3.10
110	1.35	1.80	2.60	3.20
111	1.40	1.85	2.70	3.30

FUNCTIONAL DESCRIPTION

General Description

REG6 is an always-on, low-dropout linear regulator (LDO) that is optimized for RTC and backup-battery applications. REG6 features low-quiescent supply current, current-limit protection, and reverse-current protection, and is ideally suited for always-on power supply applications, such as for a real-time clock, or as a backup-battery or super-cap charger.

Output Voltage

By default, REG6's output voltage is as defined in the Ordering Information section. However, this voltage may be programmed by writing to the REG6CFG/VSETx[ ] register via the I^2C interface.

Reverse-Current Protection

REG6 features internal circuitry that limits the reverse supply current to less than 1µA when the input voltage falls below the output voltage, as can be encountered in backup-battery charging applications. REG6's internal circuitry monitors the input and the output, and disconnects internal circuitry and parasitic diodes when the input voltage falls below the output voltage, greatly minimizing backup battery discharge.

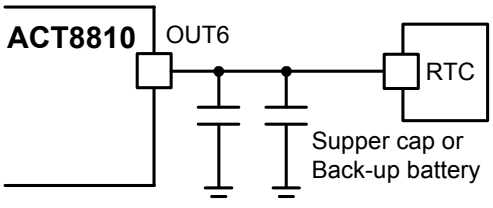
Typical Application

Voltage Regulators

REG6 is ideally suited for always-on voltage-regulation applications, such as for real-time clock and memory keep-alive applications. This regulator requires only a small ceramic capacitor with a minimum capacitance of 1µF for stability. For best performance, the output capacitor should be connected directly between the output and GA, with a short and direct connection.

Figure 9:

Typical Application of RTC LDO



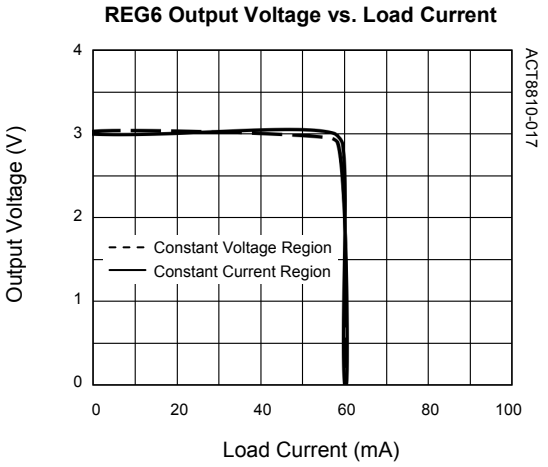
Backup Battery Charging

REG6 features a constant current-limit, which protects the IC under output short-circuit conditions as well as provides a constant charge current, when operating as a backup battery charger.

As shown in Figure 10, REG6 features a CC/CV output characteristic, regulating its output voltage for load currents up to 30mA, and regulating output current when the load exceeds (typically) 60mA.

Figure 10:

REG6 Output Voltage



ELECTRICAL CHARACTERISTICS

(V_{CHG_IN} = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ActivePath					
CHG_IN Operating Voltage Range		4.35		12	V
CHG_IN UVLO Threshold	CHG_IN Voltage Rising	3.6	3.8	4.0	V
CHG_IN UVLO Hysteresis	CHG_IN Voltage Falling		0.8		V
CHG_IN OVP Threshold	CHG_IN Voltage Rising		6.8		V
CHG_IN OVP Hysteresis	CHG_IN Voltage Falling		350		mV
CHG_IN Supply Current	V_{CHG_IN} < V_{UVLO}		20		µA
	V_{CHG_IN} < V_{BAT} + 120mV , V_{CHG_IN} > V_{UVLO}	50	120	200	µA
	V_{CHG_IN} > V_{BAT} + 120mV , V_{CHG_IN} > V_{UVLO} Charger disabled, I_{SYS} = 0mA		1.8		mA
CHG_IN to VSYS On-Resistance	I_{VSYS} = 100mA		0.4	0.6	Ω
CHG_IN to VSYS Current Limit	ACIN = VSYS	1.5	2	3	A
	ACIN = GA, CHGLEV = GA	85	95	105	mA
	ACIN = GA, CHGLEV = VSYS	400	450	500	
VSYS AND DCCC REGULATION					
VSYS Regulated Voltage	I_{VSYS} = 10mA	4.4	4.6	4.8	V
DCCC Pull-Up Current	V_{CHG_IN} > V_{BAT} + 120mV, Hysteresis = 50mV	92	100	108	µA
nSTAT OUTPUT					
nSTAT Sink current	V_{nSTAT} = 2V	3	5	7	mA
nSTAT Output Low Voltage	I_{nSTAT} = 1mA			0.4	V
nSTAT Leakage Current	V_{nSTAT} = 4.2V			1	µA
ACIN AND CHGLEV INPUTS					
CHGLEV Logic High Input Voltage		1.4			V
CHGLEV Logic Low Input Voltage				0.4	V
CHGLEV Leakage Current	V_{CHGLEV} = 4.2V			1	µA
ACIN Logic High Input Voltage		1.4			V
ACIN Logic Low Input Voltage				0.4	V
ACIN Leakage Current	V_{ACIN} = 4.2V			1	µA
TEMPERATURE SENSE COMPARATOR					
TH Pull-Up Current	V_{CHG_IN} > V_{BAT} + 120mV, Hysteresis = 50mV	92	100	108	µA
V_{TH} Upper Temperature Voltage Threshold (V_{THH})	Hot Detect NTC Thermistor	0.485	0.500	0.525	V
V_{TH} Lower Temperature Voltage Threshold (V_{THL})	Cold Detect NTC Thermistor	2.47	2.52	2.57	V
V_{TH} Hysteresis	Upper and Lower		30		mV

ELECTRICAL CHARACTERISTICS CONT'D

(V_{CHG_IN} = 5V, T_A = 25°C, unless otherwise specified.)

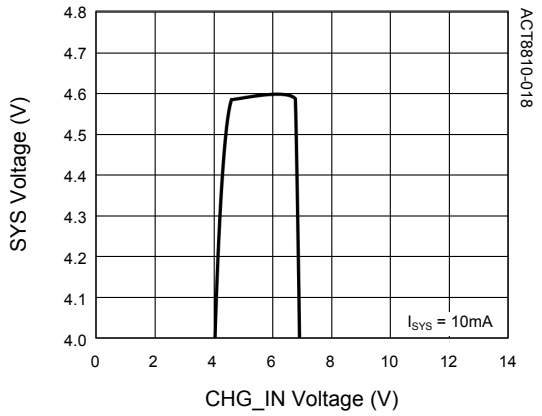
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CHARGER						
BAT Reverse Leakage Current	V_{CHG_IN} = 0V, V_{BAT} = 4.2V, I_{VSYS} = 0mA			5		μA
BAT to VSYS On-Resistance				80		mΩ
ISET Pin Voltage	Fast Charge			1.02		V
	Precondition			0.12		
Battery Regulation Voltage	T_A = -20°C to 70°C		4.179	4.2	4.221	V
	T_A = -40°C to 85°C		4.170		4.230	
Charge Current	V_{BAT} = 3.5V	ACIN = VSYS, CHGLEV = VSYS	-10%	ISET①	+10%	mA
		ACIN = VSYS, CHGLEV = GA	-16%	50%ISET	+16%	
		ACIN = GA, CHGLEV = VSYS	-10%	Smallest (450mA or ISET)	+10%	
		ACIN = GA, CHGLEV = GA	-10%	Smallest (90mA or ISET)	+10%	
Precondition Charge Current	V_{BAT} = 2.5V	ACIN = VSYS, CHGLEV = VSYS		12%ISET		mA
		ACIN = VSYS, CHGLEV = GA		12%ISET		
		ACIN = GA, CHGLEV = VSYS		12%ISET		
		ACIN = GA, CHGLEV = GA		Smallest (90mA or 12%ISET)		
Precondition Threshold Voltage	V_{BAT} Voltage Rising		2.75	2.85	2.95	V
Precondition Threshold Hysteresis	V_{BAT} Voltage Falling			100		mV
End-of-Charge Current Threshold	V_{BAT} = 4.2V	ACIN = VSYS, CHGLEV = VSYS	-10%	10%ISET	+10%	mA
		ACIN = VSYS, CHGLEV = GA	-10%	10%ISET	+10%	
		ACIN = GA, CHGLEV = VSYS	-10%	5%ISET	+10%	
		ACIN = GA, CHGLEV = GA	-10%	5%ISET	+10%	
Charge Restart Threshold	V_{SET} - V_{BAT}, V_{BAT} Falling		150	170	190	mV
BTR Scale Factor				0.24		s/Ω
Precondition Safety Timer	R_{BTR} = 47kΩ, t_{PRCHG} = 0.24 × R_{BTR}(Ω)/180(min)			1		hr
Fast Charge Safety Timer	R_{BTR} = 47kΩ, t_{CHG} = 0.24 × R_{BTR}(Ω)/60(min)			3		hr
THERMAL REGULATION						
Thermal Regulation Threshold			100		145	°C

①: ISET = 640 × (1V/R_{ISET})

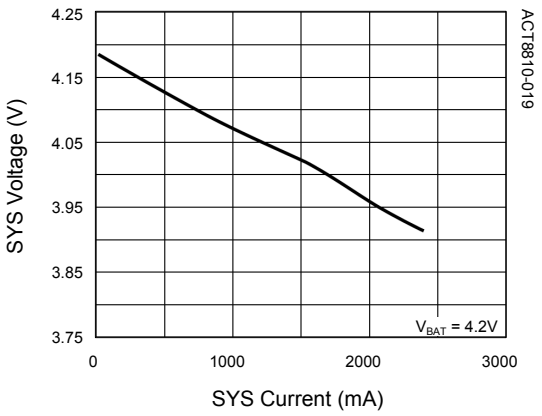
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{CHG_IN} = 5V, R_{DCCC} = 20k, R_{ISET} = 680Ω, T_A = 25°C, unless otherwise specified.)

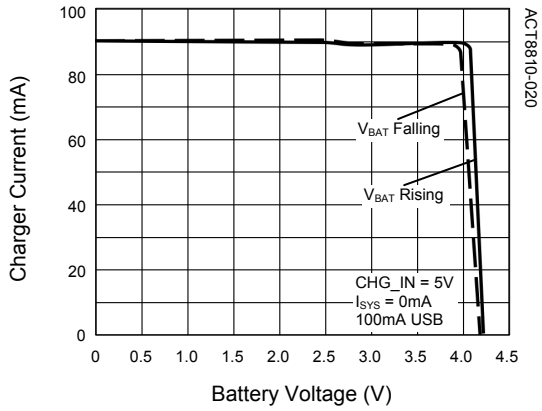
SYS Output Voltage vs. DC Voltage



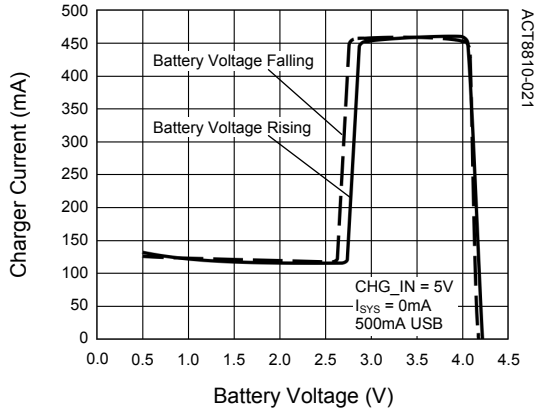
SYS Voltage vs. SYS Current



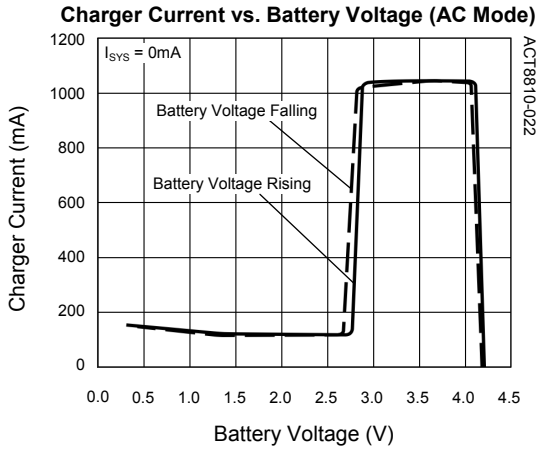
Charger Current vs. Battery Voltage (USB Mode)



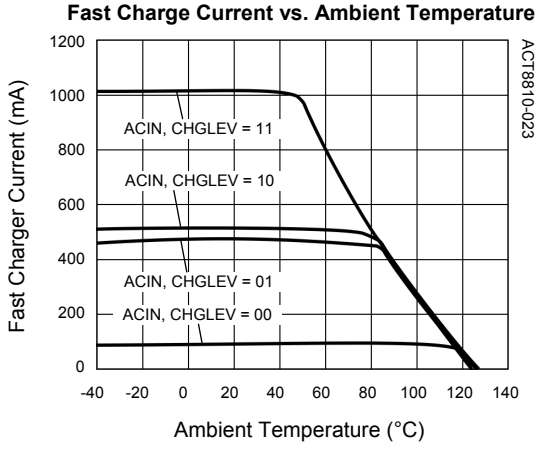
Charger Current vs. Battery Voltage (USB Mode)



Charger Current vs. Battery Voltage (AC Mode)



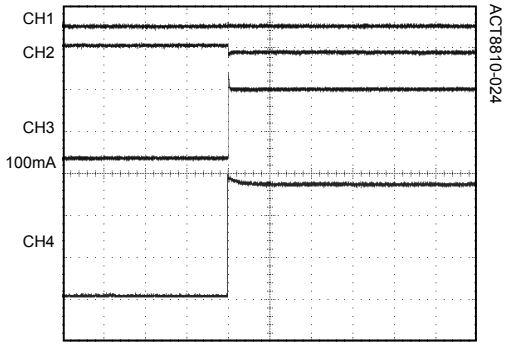
Fast Charge Current vs. Ambient Temperature



TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

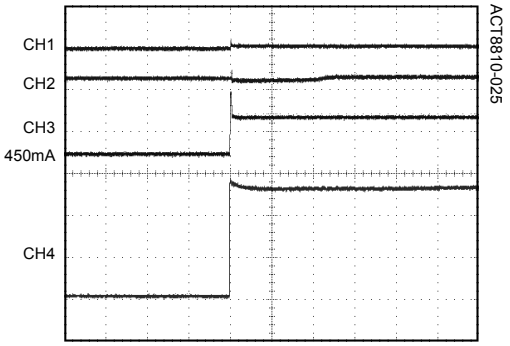
(V_{CHG_IN} = 5V, R_{DCCC} = 20k, R_{ISET} = 680Ω, T_A = 25°C, unless otherwise specified.)

VAC Applied, CHGLEV = LOW



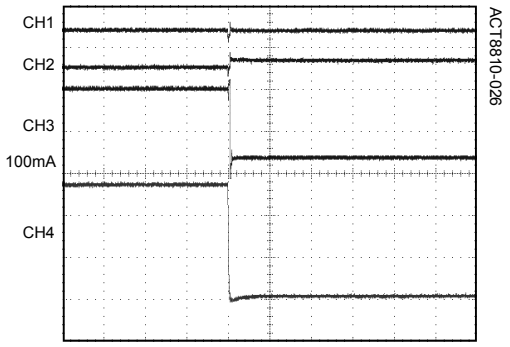
CH1: V_{USB}, 2.00V/div
CH2: V_{CHG_IN}, 2.00V/div
CH3: I_{BAT}, 500mA/div
CH4: V_{VAC}, 2.00V/div
TIME: 400µs/div

VAC Applied, CHGLEV = HIGH



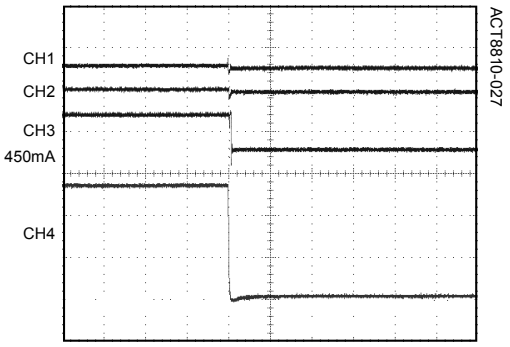
CH1: V_{USB}, 2.00V/div
CH2: V_{CHG_IN}, 2.00V/div
CH3: I_{BAT}, 500mA/div
CH4: V_{VAC}, 2.00V/div
TIME: 400µs/div

VAC Removed, CHGLEV = LOW



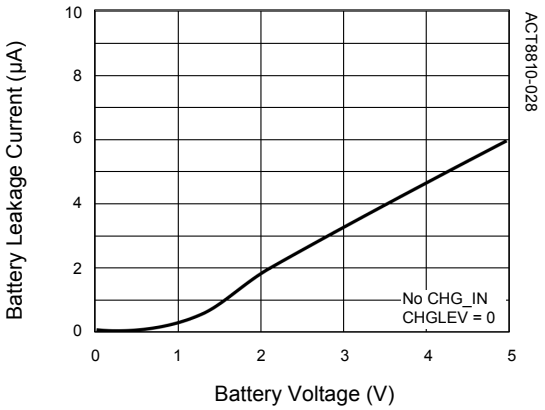
CH1: V_{USB}, 2.00V/div
CH2: V_{CHG_IN}, 2.00V/div
CH3: I_{BAT}, 500mA/div
CH4: V_{VAC}, 2.00V/div
TIME: 400µs/div

VAC Removed, CHGLEV = HIGH



CH1: V_{USB}, 2.00V/div
CH2: V_{CHG_IN}, 2.00V/div
CH3: I_{BAT}, 500mA/div
CH4: V_{VAC}, 2.00V/div
TIME: 400µs/div

Battery Leakage Current vs. Battery Voltage



FUNCTIONAL DESCRIPTION

General Description

The ACT8810 incorporates Active-Semi's patent-pending *ActivePath* architecture. *ActivePath* is a complete battery-charging and system power-management solution for portable hand-held equipment. This circuitry performs a variety of advanced battery-management functions, including automatic selection of the best available input supply, current-management to ensure system power availability, and a complete, high-accuracy (±0.5%), thermally regulated, full-featured single-cell linear Li+ charger with an integrated 12V power MOSFET.

ActivePath Architecture

Active-semi's patent-pending *ActivePath* architecture performs three important functions:

1) Input Protection,
2) System Configuration Optimization, and
3) Battery-Management

Input Protection

At the input of the ACT8810's *ActivePath* circuit is an internal, low-dropout linear regulator (LDO) that regulates the system voltage (VSYS). This LDO features a 12V power MOSFET, allowing the *ActivePath* system to withstand input voltages of up to 12V, and additionally includes a variety of other protection features, including current limit protection and input over-voltage protection.

The *ActivePath* circuitry provides a very simple means of implementing a solution that safely operates within the current-capability limitations of a USB port while taking advantage of the high output-current capability of an AC adapter, when available.

ActivePath limits the total current drawn from the input supply to a value set by the ACIN input; when ACIN is driven to a logic-low *ActivePath* operates in “USB Mode” and limits the current to either 500mA (when CHGLEV is driven to a logic-high) or to 100mA (when CHGLEV is driven to a logic-low), and when ACIN is driven to a logic-high *ActivePath* operates in “AC-Mode” and limits the input current to 2A. In either case, *ActivePath's* DCCC circuitry, described below, allows the input overload protection to be adjusted to accommodate a wide range of input supplies.

System Configuration Optimization

ActivePath circuitry automatically detects the state of the input supply, the battery, and the system, and automatically reconfigures itself to optimize the power system. If the input supply is present, *ActivePath* powers the system in parallel with charging the battery, so that system power and charge current can be independently managed to satisfy all system power requirements. This allows the battery to charge as quickly as possible, while ensuring that the total system current does not exceed the capability of the input supply. If the input supply is not present, however, then *ActivePath* automatically configures the system to draw power from the battery. Finally, if the input is present and the system current requirement exceeds the capability of the input supply, such as under momentary peak-power consumption conditions, *ActivePath* automatically configures itself for maximum power capability by drawing system power from both the battery and the input supply.

Battery Management

ActivePath includes a full-featured battery charger for single-cell Li-based batteries. This charger is a full-featured, intelligent, linear-mode, single-cell charger for Lithium-based cells, and was designed specifically to provide a complete charging solution with minimum system design effort.

The core of the *ActivePath's* charger is a CC/CV (Constant-Current/Constant-Voltage), linear-mode charge controller. This controller incorporates current and voltage sense circuitry, an internal 80mΩ power MOSFET, a full-featured state-machine that implements charge control and safety features, and circuitry that eliminates the reverse-blocking diode required by conventional charger designs.

This charger also features thermal-regulation circuitry that protects it against excessive junction temperature, allowing the fastest possible charging times, as well as proprietary input protection circuitry that makes the charger robust against input voltage transients that can damage other chargers.

The charge termination voltage is highly accurate (±0.5%), and features a selection of charge safety timeout periods that protect the system from operation with damaged cells. Other features include pin-programmable fast-charge current and

FUNCTIONAL DESCRIPTION CONT'D

two current-limited nSTAT outputs that can directly drive LED indicators or provide a logic-level status signal to the host microprocessor.

Dynamic Charge Current Control (DCCC)

The ACT8810's *ActivePath* charger features Dynamic Charge Current Control (DCCC) circuitry, which continuously monitors the input supply and prevents input overload conditions by dynamically adjusting the charge current to keep the input voltage from dropping below the DCCC voltage threshold.

By default, the DCCC voltage threshold is set to 4.4V, but it may also be programmed by connecting a resistor from DCCC to GA, where the resistor has value given by the following equation:

$$V_{DCCC} = 2 \times (I_{DCCC} \times R_{DCCC}) \quad (2)$$

Where R_{DCCC} is the value of the external resistor, and I_{DCCC} is the value of the current sourced from DCCC, typically 100µA.

Charger Current Programming

The ACT8810's *ActivePath* charger features a flexible charge current-programming scheme that combines the convenience of internal charge current programming with the flexibility of resistor based charge current programming. Current limits and charge current programming are managed as a function of the ACIN and CHGLEV pins, in combination with R_{ISET}, the resistance connected to the ISET pin.

ACIN and CHGLEV Inputs

ACIN is a logic input that configures the current-limit of *ActivePath's* linear regulator as well as that of the battery charger. ACIN features a precise 1.25V logic threshold, so that the input voltage detection threshold may be adjusted with a simple resistive voltage divider. This input also allows a simple, low-cost dual-input charger switch to be implemented with just a few, low-cost components.

When ACIN is driven to a logic high, the *ActivePath* operates in "AC-Mode" and the charger charges at the current programmed by R_{ISET},

$$I_{CHG} = 1V/R_{ISET} \times K_{ISET} \quad (3)$$

where K_{ISET} = 640 when CHGLEV is driven to a logic high, and K = 320 when CHGLEV is driven to a logic low.

When ACIN is driven to a logic-low, the *ActivePath* circuitry operates in "USB-Mode", which enforces a maximum charge current setting of 500mA, if CHGLEV is driven to a logic-high, or 100mA, if CHGLEV is driven to a logic-low.

The ACT8810's charge current settings are summarized in the table below:

Table 19:

ACIN and CHGLEV Inputs Table

ACIN	CHGLEV	CHARGE CURRENT I_{CHG} (mA)	PRECONDITION CHARGE CURRENT I_{CHG} (mA)
0	0	90mA or ISET (Smallest one)	90mA or 12%ISET (Smallest one)
0	1	450mA or ISET (Smallest one)	12% × ISET
1	0	50% × ISET	12% × ISET
1	1	ISET	12% × ISET

Note that the actual charging current may be limited to a current that is lower than the programmed fast charge current due to the ACT8810's internal thermal regulation loop. See the *Thermal Regulation* and *Protection* section for more information.

Battery Temperature Monitoring

The ACT8810 continuously monitors the temperature of the battery pack by sensing the resistance of its thermistor, and suspends charging if the temperature of the battery pack exceeds the safety limits.

In a typical application, shown in Figure 11, the TH pin is connected to the battery pack's thermistor input. The ACT8810 injects a 100µA current out of the TH pin into the thermistor, so that the thermistor resistance is monitored by comparing the voltage at TH to the internal V_{THH} and V_{THL} thresholds of 0.5V and 2.5V, respectively. When $V_{TH} > V_{THL}$ or $V_{TH} < V_{THH}$ charging and the charge timers are suspended. When V_{TH} returns to the normal range, charging and the charge timers resume.

The net resistance from TH to G required to cross the threshold is given by:

$100\mu A \times R_{NOM} \times k_{HOT} = 0.5V \rightarrow R_{NOM} \times k_{HOT} = 5k\Omega$

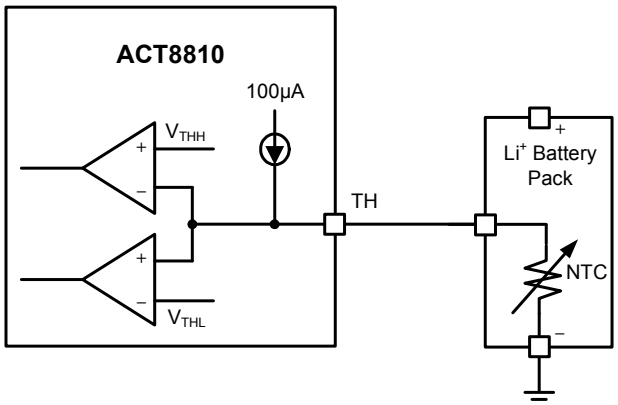
$100\mu A \times R_{NOM} \times k_{COLD} = 2.5V \rightarrow R_{NOM} \times k_{COLD} = 25k\Omega$

FUNCTIONAL DESCRIPTION CONT'D

where R_{NOM} is the nominal thermistor resistance at room temperature, and k_{HOT} and k_{COLD} are the ratios of the thermistor's resistance at the desired hot and cold thresholds, respectively.

Figure 11:

Simple Configuration



Design Procedure

When designing with thermistors it is important to keep in mind that their nonlinear behavior typically allows one to directly control no more than one threshold at a time. As a result, the design procedure can change depending on which threshold is most critical for a given application.

Most application requirements can be solved using one of three cases,

1) Simple solution
2) Fix V_{THH}, accept the resulting V_{THL}
3) Fix V_{THL}, accept the resulting V_{THH}

The ACT8810 was designed to achieve an operating temperature range that is suitable for most applications with very little design effort. The simple solution is often found to provide reasonable results and should always be used first, then the design procedure may proceed to one of the other solutions if necessary.

In each design example, we refer to the Vishay NTHS series of NTCs, and more specifically those which follow a "curve 2" characteristic. For more information on these NTCs, as well as access to the resistance/temperature characteristic tables referred to in the example, please refer to the Vishay website at http://www.vishay.com/thermistors.

Simple Solution

The ACT8810 was designed to accommodate most requirements with very little design effort, but also provides flexibility when additional control over a design is required. Initial thermistor selection is accomplished by choosing one that best meets the following requirements:

$R_{NOM} = 5k\Omega/k_{HOT}$, and

$R_{NOM} = 25k\Omega/k_{COLD}$

where k_{HOT} and k_{COLD} for a given thermistor can be found on its characteristic tables.

Taking a 0°C to 40°C application using a "curve 2" NTC for this example, from the characteristic tables one finds that k_{HOT} and k_{COLD} are 0.5758 and 2.816, respectively, and the R_{NOM} that most closely satisfies these requirements is therefore around 8.8kΩ. Selecting 10kΩ as the nearest standard value, calculate k_{COLD} and k_{HOT} as:

$k_{COLD} = V_{THL}/(I_{TH} \times R_{NOM}) = 2.5V/(100\mu A \times 10k\Omega) = 2.5$

$k_{HOT} = V_{THH}/(I_{TH} \times R_{NOM}) = 0.5V/(100\mu A \times 10k\Omega) = 0.5$

Identifying these values on the curve 2 characteristic tables indicates that the resulting operating temperature range is 2°C to 44°C, vs. the design goal of 0°C to 40°C. This example demonstrates that one can satisfy common operating temperature ranges with very little design effort.

Fix V_{THH}

For demonstration purposes, supposing that we had selected the next closest standard thermistor value of 6.8kΩ in the example above, we would have obtained the following results:

$k_{COLD} = V_{THL}/(I_{TH} \times R_{NOM}) = 2.5V/(100\mu A \times 6.8k\Omega) = 3.67$

$k_{HOT} = V_{THH}/(I_{TH} \times R_{NOM}) = 0.5V/(100\mu A \times 6.8k\Omega) = 0.74$

which, according to the characteristic tables would have resulted in an operating temperature range of -6°C to 33°C vs. the design goal of 0°C to 40°C.

In this case, one can add resistance in series with the thermistor to shift the range upwards, using the following equation:

$(V_{THH}/I_{TH}) = k_{HOT}(@40°C) \times R_{NOM} + R$

$R = (V_{THH}/I_{TH}) - k_{HOT}(@40°C) \times R_{NOM}$

$R = (2.5V/100\mu A) - 0.5758 \times 6.8k\Omega$

FUNCTIONAL DESCRIPTION CONT'D

Finally,

$R = 5k\Omega - 3.9k\Omega = 1.1k\Omega$

This result shows that adding 1.1kΩ in series with the thermistor sets the net resistance from TH to G to be 0.5V at 40°C, satisfying V_{THH} at the correct temperature. Adding this resistance, however, also impacts the lower temperature limit as follows:

$V_{THL}/I_{TH} = k_{COLD}(@TC) \times R_{NOM} + R$

$k_{COLD}(@TC) = (V_{THL}/I_{TH}) - R)/R_{NOM}$

Finally,

$k_{COLD}(@TC) = (25k\Omega - 1.1k\Omega)/6.8k\Omega = 3.51$

Reviewing the characteristic curves, the lower threshold is found to move to -5°C, a change of only 1°C. As a result, the system satisfies the upper threshold of 40°C with an operating temperature range of -5°C to 40°C, vs. our design target of 0°C to 40°C. It is informative to highlight that due to the NTC behavior of the thermistor, the relative impact on the lower threshold is significantly smaller than the impact on the upper threshold.

Fix V_{THL}

Following the same example as above, the "unadjusted" results yield an operating temperature range of -6°C to 33°C vs. the design goal of 0°C to 40°C. In applications that favor V_{THL} over V_{THH}, however, one can control the voltage present at TH at low temperatures by connecting a resistor in parallel with I_{TH}. The desired resistance can be found using the following equation:

$(I_{TH} + (V_{CHG\_IN} - V_{THL})/R) \times k_{COLD}(@0°C) \times R_{NOM} = V_{THL}$

Rearranging yields

$R = (V_{CHG\_IN} - V_{THL})/(V_{THL}/(k_{COLD}(@0°C) \times R_{NOM}) - I_{TH})$

$R = (5V - 2.5V)/(2.5V/(2.816 \times 6.8k\Omega) - 100\mu A)$

$R = 82k\Omega$

Adding 82kΩ in parallel with the current source increases the net current flowing into the thermistor, thus increasing the voltage at TH. Adding this resistance, however, also impacts the upper temperature limit:

$V_{THH} = (I_{TH} + (V_{CHG\_IN} - V_{THH})/R) \times k_{HOT}(@40°C) \times R_{NOM}$

Rearranging yields,

$k_{HOT}(@TC) = V_{THH}/(R_{NOM} \times (I_{TH} + (V_{CHG\_IN} - V_{THH})/R))$

$k_{HOT}(@TC) = 0.5V/(6.8k\Omega \times (100\mu A + (5V - 0.5V)/82k\Omega)) = 0.4748$

Reviewing the characteristic curves, the upper threshold is found to move to 45°C, a change of about 14°C. Adding the parallel resistance has allowed us to achieve our desired lower threshold of 0°C with an operating temperature range of 0°C to 45°C, vs. our design target of 0°C to 40°C.

Figure 12:
Fix V_{THH} Configuration

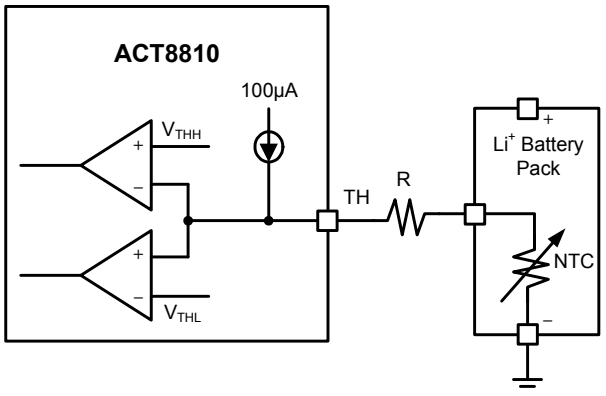
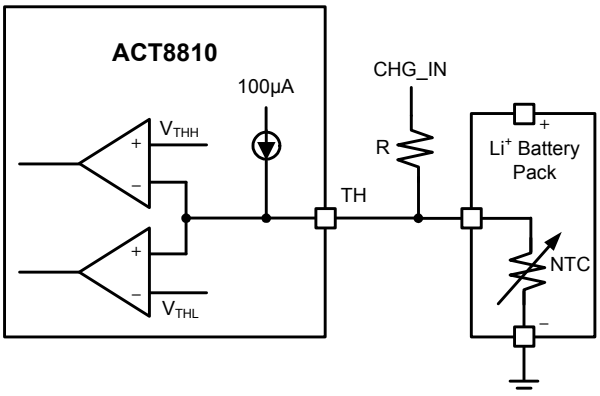


Figure 13:
Fix V_{THL} Configuration



FUNCTIONAL DESCRIPTION CONT'D

Thermal Regulation

The ACT8810's *ActivePath* charger features an internal thermal regulation loop that reduces the charging current as necessary to ensure that the die temperature does not rise beyond the thermal regulation threshold of 110°C. This feature protects the against excessive junction temperature and makes the device more accommodating to aggressive thermal designs. Note, however, that attention to good thermal designs is required to achieve the fastest possible charge time by maximizing charge current.

In order to account for the reduced charge current resulting from operation in thermal regulation mode, the charge timeout periods are extended proportionally to the reduction in charge current.

Charging Safety Timers

The ACT8810 features a safety timer that is programmable via an external resistor (R_{BTR}) connected from BTR to GA. The timeout period is calculated as a function of this resistor by the following equation:

$t_{CHG} = K_{BTR} \times R_{BTR}$, where $K_{BTR} = 0.24s/\Omega$.

If the timeout period expires prior to charge termination, the charger is disabled and the nSTAT pin signal a fault condition. If the ACT8810 detects that the charger remains in precondition for longer than the precondition time out period (which determined as $t_{CHG}/3$), the ACT8810 turns off the charger and generate a FAULT to ensure prevent charging a bad cell.

Charging Status Indication

The ACT8810 provides one charge-status output, nSTAT which indicates charge status as defined in Table 20. nSTAT is open-drain output with internal 5mA current limits, which sinks current when asserted and are high-Z otherwise, and is capable of directly driving LED without the need of current-limiting resistor or other external circuitry. To drive an LED, simply connect the LED between nSTAT pin and an appropriate supply (typically VSYS). For a logic level indication, simply connect a resistor from nSTAT to a appropriate voltage supply.

Table 20:

Charging Status Indication Table

STATE	nSTAT
Charging	ON
Discharging	OFF
Charging Complete	OFF
Input Floating	OFF
Fault	OFF

Input Supply Detection

The ACT8810's *ActivePath* charger is capable of withstanding voltages of up to 12V, protecting the system from fault conditions such as input voltage transients or application of an incorrect input supply. Although the ACT8810 can withstand a wide range of input voltages, valid input voltages for charging must be greater than the under-voltage lockout voltage (UVLO) and the over-voltage protection (OVP) thresholds, as described below.

Under Voltage Lock Output (UVLO)

Whenever the input voltage applied to CHG_IN falls below 3.0V (typ), an input under-voltage condition is detected and the charger is disabled. Once an input under-voltage condition is detected, the input must exceed the under-voltage threshold by at least 800mV for charging to resume.

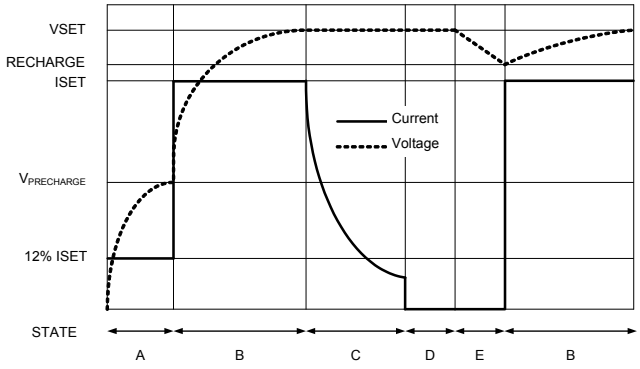
Over Voltage Protection (OVP)

If the charger detects that the voltage applied to CHG_IN exceeds 6.8V (typ), an over-voltage condition is detected and the charger is disabled. Once an input over-voltage condition is detected, the input must fall below the OVP threshold by at least 350mV for charging to resume.

Reverse Leakage Current

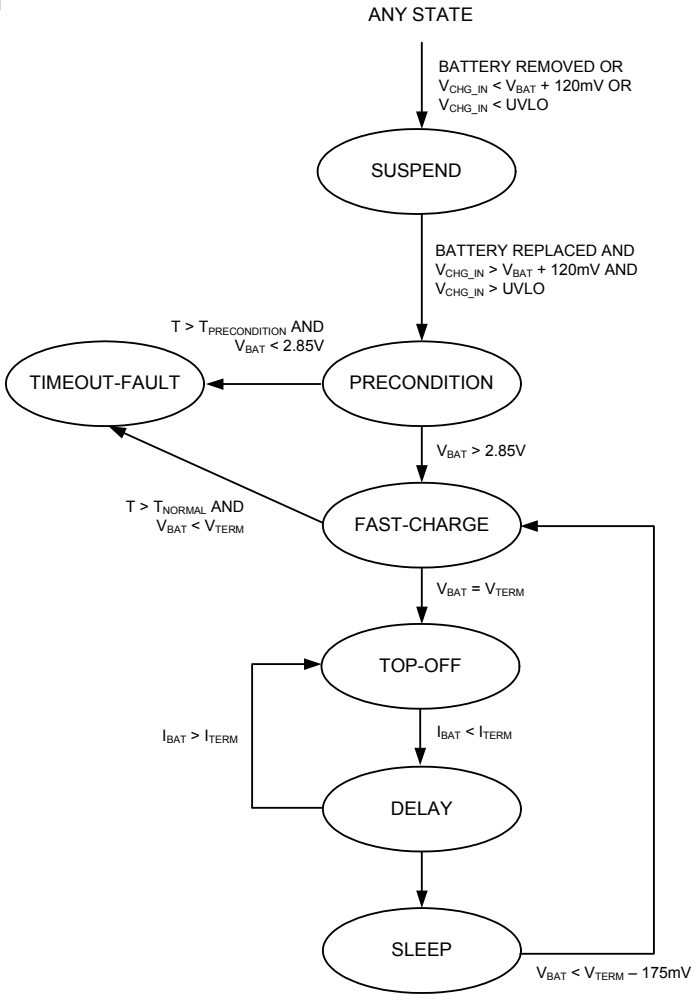
The ACT8810's *ActivePath* charger includes internal circuitry that eliminates the need for blocking diodes, reducing solution size and cost as well as dropout voltage relative to conventional battery chargers. When the voltage at CHG_IN falls below V_{BAT}, the charger automatically reconfigures its power switch to minimize current drain from the battery.

Figure 14:
Typical Li+ charge profile and ACT8810 charge states



A: PRECONDITION State
B: FAST-CHARGE State
C: TOP-OFF State
D: SLEEP State
E: DISCHARGE State

Figure 15:
Charger State Diagram



FUNCTIONAL DESCRIPTION CONT'D

Charger State-Machine

PRECONDITION State

A new charging cycle begins with the PRECONDITION state, and operation continues in this state until V_{BAT} exceeds the Precondition Threshold Voltage of 2.85V (typ). When operating in PRECONDITION state, the cell is charged at a reduced current, 12% of the programmed maximum fast-charge constant current, ISET. Once V_{BAT} reaches the Precondition Threshold Voltage the state machine jumps to the NORMAL state. If V_{BAT} does not reach the Precondition Threshold Voltage before the Precondition Timeout period $t_{PRECONDITION}$ expires, then a damaged cell is detected and the state machine jumps to the TIMEOUT-FAULT State. For the Precondition Timeout period, see the *Charging Safety Timers section* for more information.

FAST CHARGE State

Normal state is made up of two operating modes, fast charge Constant-Current (CC) and Constant-Voltage (CV). In CC mode, the ACT8810 charges at the current programmed by R_{ISET} (see the *Current Limits* and *Charge Current Programming* section for more information). During a normal charge cycle fast-charge continues in CC mode until V_{BAT} reaches the charge termination voltage (V_{TERM}), at which point the ACT8810 charges in CV mode. Charging continues in CV mode until the charge current drops to 10% (ACIN = 1) or 5% (ACIN = 0) of the programmed maximum charge current, at which point the state machine jumps to the TOP-OFF state. If V_{BAT} does not proceed out of the NORMAL state before the Normal Timeout period (T_{NORMAL}) expires, then a damaged cell is detected and the state machine jumps to the TIMEOUT-FAULT State. See the *Charging Safety Times* section for more information.

TOP-OFF State

In the TOP-OFF state, the cell is charged in constant-voltage (CV) mode. Charge current decreases as charging continues. During a normal charging cycle charging proceeds until the charge current decreases below the End-Of-Charge (EOC) threshold, defined as 10% of ISET (ACIN = 1) or 5% of ISET (ACIN = 0) . When this happens, the state machine terminates the charge cycle and jumps to the SLEEP state.

End of Charge State

In the End-of-Charge (EOC) state, the ACT8810 presents a high-impedance to the battery, allowing the cell to "relax" and minimizes battery leakage current. The ACT8810 continues to monitor the cell voltage, however, so that it can re-initiate charging cycles as necessary to ensure that the cell remains fully charged.

SUSPEND State

The ACT8810 features an user-selectable suspend-charge mode, which disables the charger but keeps other circuiting functional. The charger can be put into suspend mode by driving EN to logic low. Upon exiting the SUSPEND State, the charge timer is reset and the state machine jumps to PRECONDITION state.

SLEEP State

In SLEEP mode the ACT8810 presents a high-impedance to the battery, allowing the cell to "relax" and minimizes battery leakage current. The ACT8810 continues to monitor the cell voltage, however, so that it can re-initiate charging as necessary to ensure that the cell remains fully charged. Under normal operation, the state machine initiates a new charging cycle by jumping to the FAST-CHARGE state when V_{BAT} drops below the Charge Termination Threshold.

CHG_IN Bypass Capacitor Selection

CHG_IN is the power input for the ACT8810 battery charger. The battery charger is automatically enabled whenever a valid voltage is present on CHG_IN. In most applications, CHG_IN is connected to either a wall adapter or USB port. Under normal operation, the input of the charger will often be "hot-plugged" directly to a powered USB or wall adapter cable, and supply voltage ringing and overshoot may appear at the CHG_IN pin.

In most applications a high quality capacitor connected from CHG_IN to GA, placed as close as possible to the IC, is sufficient to absorb the energy. Wall-adapter powered applications provide flexibility in input capacitor selection, but the USB specification presents limitations to input capacitance selection. In order to meet both the USB 2.0 and USB OTG (On The Go) specifications while avoiding USB supply under-voltage conditions

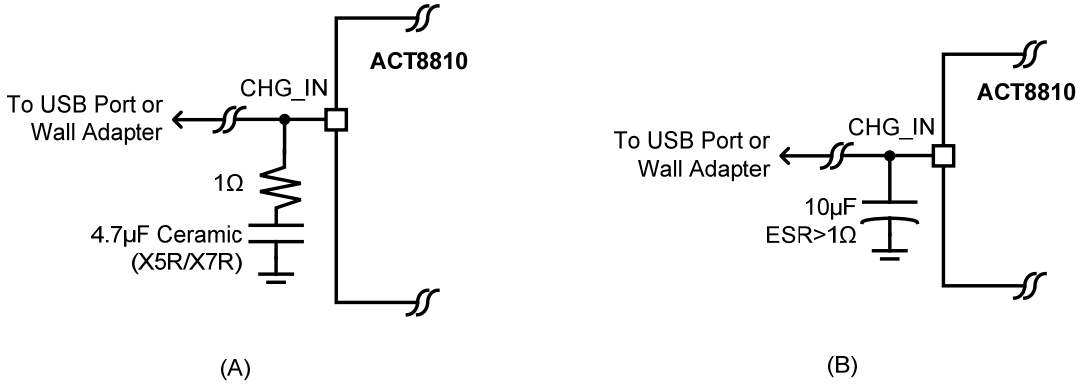
FUNCTIONAL DESCRIPTION CONT'D

resulting from the current limit slew rate (100mA/µS) limitations of the USB bus, the CHG_IN bypass capacitance value must to be between 4.7µF and 10µF for the ACT8810.

Ceramic capacitors are often preferred for bypassing applications due to their small size and good surge current ratings, but care must be taken in applications that can encounter hot plug conditions as their very low ESR, in combination with the inductance of the cable, can create a high-Q filter that induces excessive ringing at the CHG_IN pin. This ringing can couple to the output and be mistaken as loop instability, or the ringing may be large enough to damage the input itself. Although the CHG_IN pin is designed for maximum robustness and an absolute maximum voltage rating of 14V for transients, attention must be given to bypass techniques to ensure safe operation.

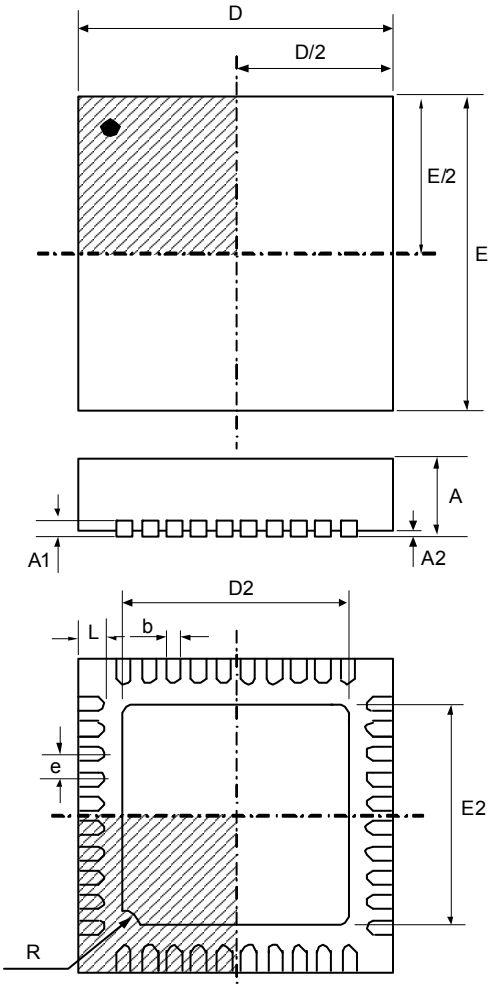
As a result, design of the CHG_IN bypass must take care to "de-Q" the filter. This can be accomplished by connecting a 1Ω resistor in series with a ceramic capacitor (as shown in Figure 16), or by using a tantalum or electrolytic capacitor to utilize it's higher ESR to dampen the ringing. For additional protection in extreme situations, Zener diodes with 12V clamp voltages may also be used. In any case, it is always critical to evaluate voltage transients at the ACT8810 CHG_IN pin with an oscilloscope to ensure safe operation.

Figure 16:
CHG_IN Bypass Options for USB or Wall Adaptor Supplies



PACKAGE OUTLINE

TQFN55-40 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.200 REF		0.008 REF	
A2	0.000	0.050	0.000	0.002
b	0.150	0.250	0.006	0.010
D	4.900	5.100	0.193	0.201
E	4.900	5.100	0.193	0.201
D2	3.450	3.750	0.136	0.148
E2	3.450	3.750	0.136	0.148
e	0.400 BSC		0.016 BSC	
L	0.300	0.500	0.012	0.020
R	0.300		0.012	