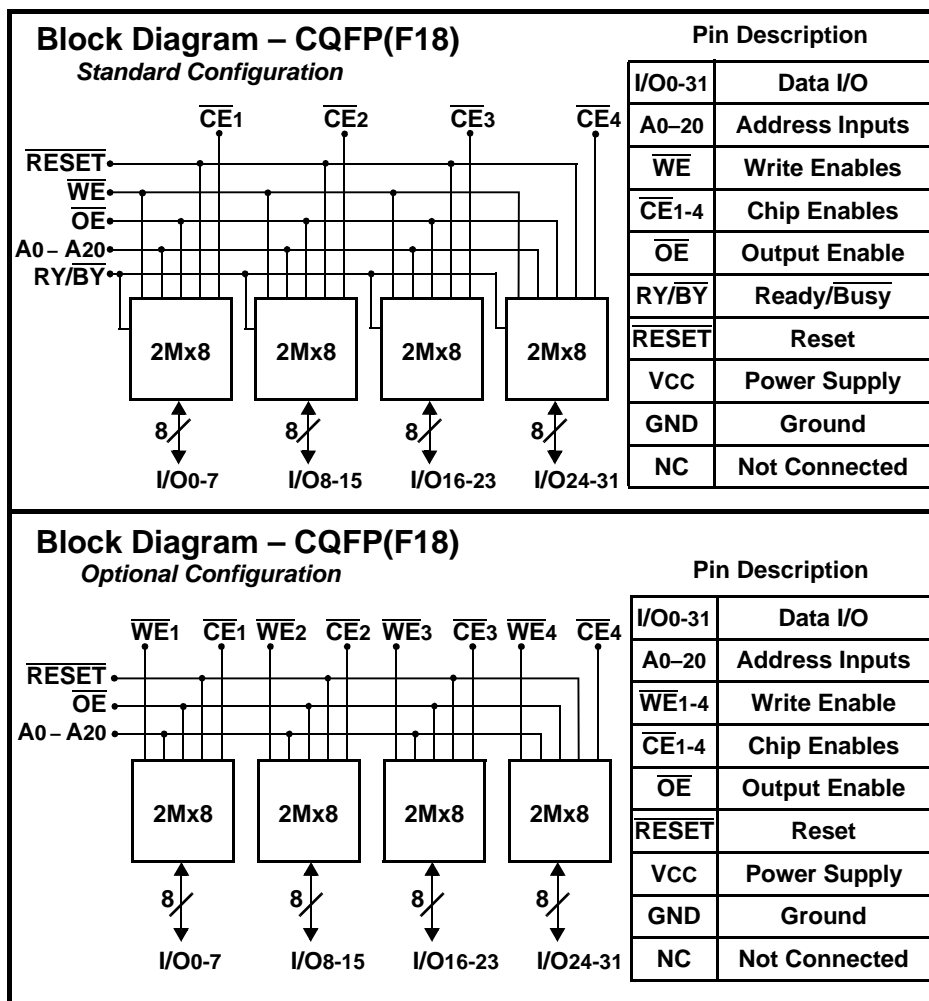


ACT-F2M32A High Speed 64 Megabit Sector Erase FLASH Multichip Module



Features

- 4 Low Voltage/Power AMD 2M x 8 FLASH Die in One MCM Package
- Overall Configuration is 2M x 32
- +5V Power Supply / +5V Programming Operation
- Access Times of 90, 120 and 150 ns
- Erase/Program Cycles – 100,000 Minimum
- Sector erase architecture (Each Die)
 - 32 uniform sectors of 64 Kbytes each
 - Any combination of sectors can be erased. Also supports full chip erase
 - Sector group protection is user definable
- Embedded Erase Algorithms – Automatically pre-programs and erases the die or any sector
- Embedded Program Algorithms – Automatically programs and verifies data at specified address
- Ready/Busy output (RY/BY) – Hardware method for detection of program or erase cycle completion
- Hardware RESET pin – Resets internal state machine to the read mode
- Erase Suspend/Resume – Supports reading or programming data to a sector not being erased
- Packaging – Hermetic Ceramic
 - 68 Lead, .94" x .94" x .140" Single-Cavity Small Outline Gull Wing, Aeroflex code# "F18" (Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)
- Internal Decoupling Capacitors for Low Noise Operation
- Commercial, Industrial and Military Temperature Ranges
- MIL-PRF-38534 Compliant MCMs Available



General Description

Utilizing AMD's Sector Erase Flash Memory Die, the ACT-F2M32A is a high speed, 64 megabit CMOS flash multichip module (MCM) designed for full temperature range, military, space, or high reliability applications.

The ACT-F2M32A consists of four high-performance AMD Am29F016 16Mbit (16,777,216 bit) memory die. Each die contains 8 separately write or erase sector groups of 256Kbytes (A sector group consists of 4 adjacent sectors of 64Kbytes each).

The command register is written by bringing WE to a logic low level (V_{IL}), while CE is low and OE is high (V_{IH}). Reading is accomplished by chip Enable (CE) and Output Enable (OE) being logically active. Access time grades of 90ns, 120ns and 150ns maximum are standard.

General Description, Cont'd

The ACT-F2M32A is packaged in a hermetically sealed co-fired ceramic 68 lead, .94" SQ Ceramic Gull Wing CQFP package. This allows operation in a military environment temperature range of -55°C to +125°C.

The ACT-F2M32A can be programmed (both read and write functions) in-system using the +5.0V VCC power supply. A 12.0V VPP is not required for programming or erase operations. The end of program or erase is detected by the RY/BY pin, Data Polling of DQ7, or by the Toggle bit (DQ6).

The ACT-F2M32A also has a hardware $\overline{\text{RESET}}$ pin. When this pin is driven low, execution of any Embedded Program Algorithm or Embedded Erase Algorithm will be terminated.

Each block can be independently erased and programmed 100,000 times at +25°C.

For Detail Information regarding the operation of the Am29F016 Sector Erase Flash Memory, see the AMD datasheet (Publication 18805).

Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Voltage with Respect to GND (All pins except A9) ⁽¹⁾	-2.0 to +7.0	V
Voltage on Pins A9, \overline{OE} , \overline{RESET} ⁽²⁾	-2.0 to +13.5	V
Vcc Supply Voltage with Respect to Ground ⁽¹⁾	-2.0 to +7.0	V
Output Short Circuit Current ⁽³⁾	200	mA

Notes:

1. Minimum DC voltage is -0.5V on input/output pins. During Transitions, inputs may undershoot GND to -2.0V for periods up to 20ns. Maximum DC voltage on input/output pins is $V_{CC} + 0.5V$, which may overshoot to $V_{CC} + 2.0V$ for periods up to 20ns.
2. Minimum DC input voltage on A9, \overline{OE} , \overline{RESET} pins is -0.5V. During Voltage transitions, A9, \overline{OE} & \overline{RESET} may overshoot GND to -2.0V for periods up to 20ns. Maximum DC input voltage on A9 is +12.5V which may overshoot to 14V for periods up to 20ns.
3. No more than one output shorted to ground for no more than 1 second.

NOTICE: Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may effect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
VCC	5V Power Supply Voltage (10%)	+4.5	+5.5	V
V _{IH}	Input High Voltage (CMOS)	0.7 x VCC	$V_{CC} + 0.3$	V
V _{IL}	Input Low Voltage	-0.5	+0.8	V
T _C	Operating Temperature (Military)	-55	+125	°C

Capacitance

(f = 1MHz, T_C = 25°C, Standard Configuration)

Symbol	Parameter	Maximum	Units
CAD	A0 – A20 Capacitance	50	pF
COE	\overline{OE} Capacitance	50	pF
CCE	\overline{CE} Capacitance	20	pF
CRESET	\overline{RESET} Capacitance	50	pF
CWE	\overline{WE} Capacitance	60	pF
CRY/ \overline{BY}	RY/ \overline{BY} Capacitance	50	pF
CI/O	I/O0 – I/O31 Capacitance	20	pF

Capacitance Guaranteed by design, but not tested.

DC Characteristics – CMOS Compatible

(T_C = -55°C to +125°C, V_{CC} = +4.5V to + 5.5V, Unless otherwise specified)

Parameter	Sym	Conditions	Min	Max	Units
Input Load Current	I _{IL}	V _{CC} = V _{CCMax.} , V _{IN} = V _{CC} or GND		10	μA
A9 Leakage Current	I _{LIT}	V _{CC} = V _{CCMax.} , A9 = +12V		50	μA
Output Leakage Current	I _{LO}	V _{CC} = V _{CCMax.} , V _{IN} = GND to V _{CC}		10	μA
Vcc Active Read Current	I _{CC1}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		160	mA
Vcc Active Program/Erase Current ⁽¹⁾	I _{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		240	mA
Vcc Standby Current	I _{CC3}	V _{CC} = V _{CCMax.} , $\overline{CE} = \overline{RESET} = V_{CC} \pm 0.3V$		4	mA
Vcc Standby Current (Reset)	I _{CC4}	V _{CC} = V _{CCMax.} , $\overline{RESET} = V_{CC} \pm 0.3V$		4	mA
Output Low Voltage	V _{OL}	V _{CC} = V _{CCMin.} , I _{OL} = 12 mA		0.45	V
Output High Voltage	V _{OH1}	V _{CC} = V _{CCMin.} , I _{OH} = -2.5 mA	0.85 x V _{CC}		V
	V _{OH2}	V _{CC} = V _{CCMin.} , I _{OH} = -100 μA	V _{CC} - 0.4V		V
Low Vcc Lock-Out Voltage	V _{LKO}		3.2	4.2	V

Notes:

1. Not 100% tested.

AC Characteristics – Write/Erase/Program Operations – \overline{WE} Controlled

(Tc = -55°C to +125°C, Vcc = +4.5V to + 5.5V, Unless otherwise specified)

Parameter	Parameter Symbol Standard	Parameter Symbol JEDEC	90ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{wc}	t _{AVAV}	90		120		150		ns
Address Setup to \overline{WE} Going Low	t _{AS}	t _{AVWL}	0		0		0		ns
Address Hold Time from \overline{CE} High	t _{AH}	t _{WLAX}	45		50		50		ns
Data Setup to \overline{WE} Going High	t _{DS}	t _{DVWH}	45		50		50		ns
Data Hold Time from \overline{WE} High	t _{DH}	t _{WHDX}	0		0		0		ns
Output Enable Hold Time	Read	toEH	0		0		0		ns
	Toggle Bit I and Data Polling		10		10		10		ns
Read Recover Time Before Write (\overline{OE} High to \overline{WE} Low)	t _{GHWL}	t _{GHWL}	0		0		0		ns
\overline{CE} Setup Time from \overline{WE} Low	t _{CS}	t _{ELWL}	0		0		0		ns
\overline{CE} Hold Time from \overline{WE} High	t _{CH}	t _{WHEH}	0		0		0		ns
\overline{WE} Pulse Width	t _{WP}	t _{WLWH}	45		50		50		ns
\overline{WE} Pulse Width High	t _{WPH}	t _{WHWL}	20		20		20		ns
Byte Programming Operation	t _{WHWH1}	t _{WHWH1}	8		8		8		μs
Sector Erase Operation	t _{WHWH2}	t _{WHWH2}		15		15		15	Sec
Vcc Set-Up Time	t _{VCS}		50		50		50		μs
Rise Time to V _{ID}	t _{VDR}		500		500		500		ns
\overline{OE} Setup Time to \overline{WE} Active	t _{OESP}		4		4		4		μs
Reset Pulse Width	t _{RP}		500		500		500		ns
Program/Erase Valid to RY/ \overline{BY} Delay	t _{BUSY}		40		50		60		ns

Notes:

1. Not 100% tested.

AC Characteristics – Read Only Operations

(Tc = -55°C to +125°C, Vcc = +4.5V to + 5.5V, Unless otherwise specified)

Parameter	Parameter Symbol Standard	Parameter Symbol JEDEC	90ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	
Read Cycle Time ⁽¹⁾	t _{RC}	t _{AVAV}	90		120		150		ns
Address to Output Delay	t _{ACC}	t _{AVQV}		90		120		150	ns
\overline{CE} to Output Delay	t _{CE}	t _{ELQV}		90		120		150	ns
\overline{OE} to Output Delay	t _{OE}	t _{GLQV}		40		50		55	ns
\overline{CE} to Output in High Z ⁽¹⁾	t _{DF}	t _{EHQZ}		20		30		35	ns
\overline{OE} to Output in High Z ⁽¹⁾	t _{DF}	t _{GHQZ}		20	0	30	0	35	ns
Output Hold from Addresses, \overline{CE} or \overline{OE} Change, Whichever Occurs First	t _{OH}	t _{AXQX}	0		0		0		ns
RESET Low to Read Mode ⁽¹⁾	t _{READY}			20		20		20	μs

Notes:

1. Not 100% tested.

AC Characteristics – Write/Erase/Program Operations – \overline{CE} Controlled

(Tc = -55°C to +125°C, Vcc = +4.5V to + 5.5V, Unless otherwise specified)

Parameter	Parameter Symbol Standard	Parameter Symbol JEDEC	90ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time ⁽¹⁾	tWC	tAVAV	90		120		150		ns
Address Setup to \overline{CE} Going Low	tAS	tAVEL	0		0		0		ns
Address Hold Time from \overline{CE} Low	tAH	tELAX	45		50		50		ns
Data Setup to \overline{CE} Going High	tDS	tDVEH	45		50		50		ns
Data Hold Time from \overline{CE} High	tDH	tEHDX	0		0		0		ns
Output Enable Setup Time ⁽¹⁾	toES		0		0		0		ns
Output Enable Hold Time ⁽¹⁾		Read	0		0		0		ns
		Toggle Bit I and Data Polling	10		10		10		ns
Read Recover Time Before Write (\overline{OE} High to \overline{WE} Low)	tGHEL	tGHEL	0		0		0		ns
\overline{CE} Setup Time from \overline{WE} Low	tWS	tWLEL	0		0		0		ns
\overline{WE} Hold Time from \overline{CE} High	tWH	tEHHW	0		0		0		ns
\overline{WE} Pulse Width	tCP	tELEH	45		50		50		ns
\overline{WE} Pulse Width High	tCPH	tELEL	20		20		20		ns
Byte Programming Operation	tWHWH1	tWHWH1	8		8		8		µs
Sector Erase Operation	tWHWH2	tWHWH2		15		15		15	Sec

Notes:

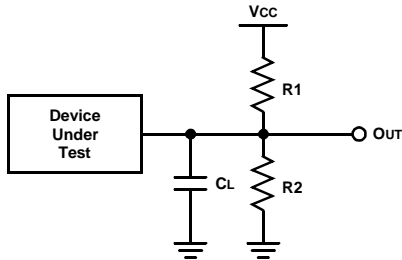
1. Not 100% tested.

AC Test Circuit

Test Configuration Component Values

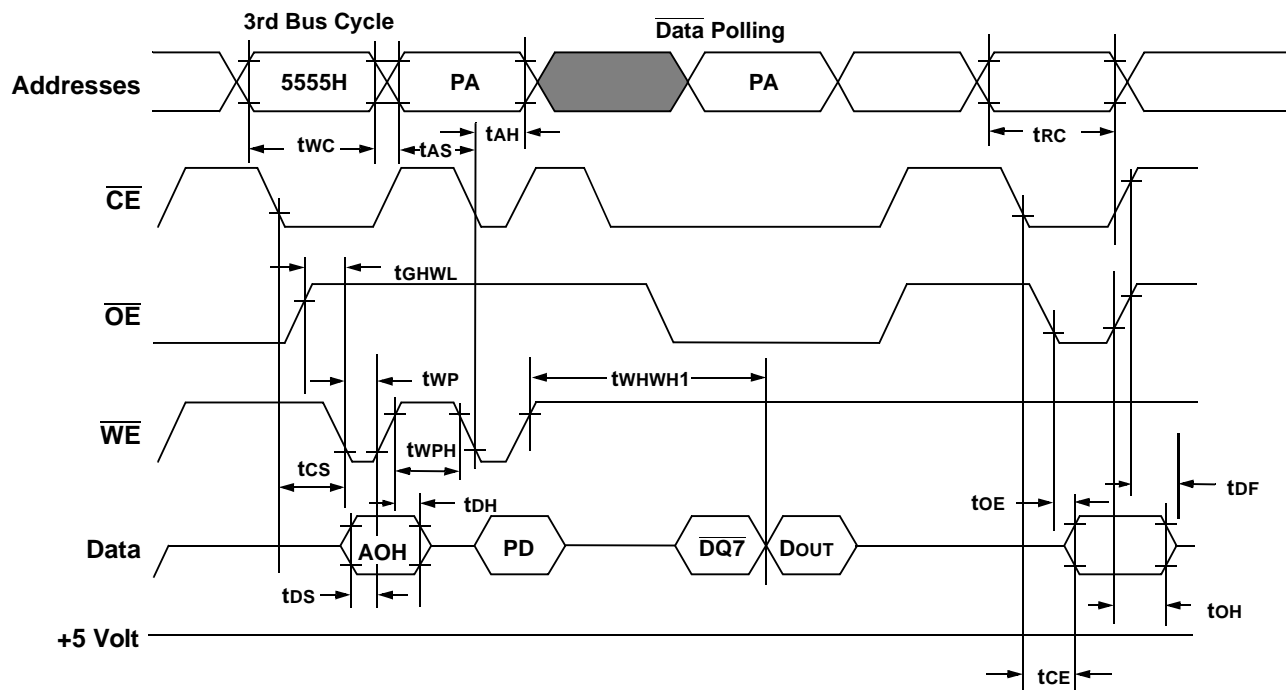
Test Configuration	CL (pF)	R1 (Ω)	R2 (Ω)
3.3V Standard Test	50	990	770
5V Standard Test	50	580	390

NOTES:
CL includes jig capacitance.

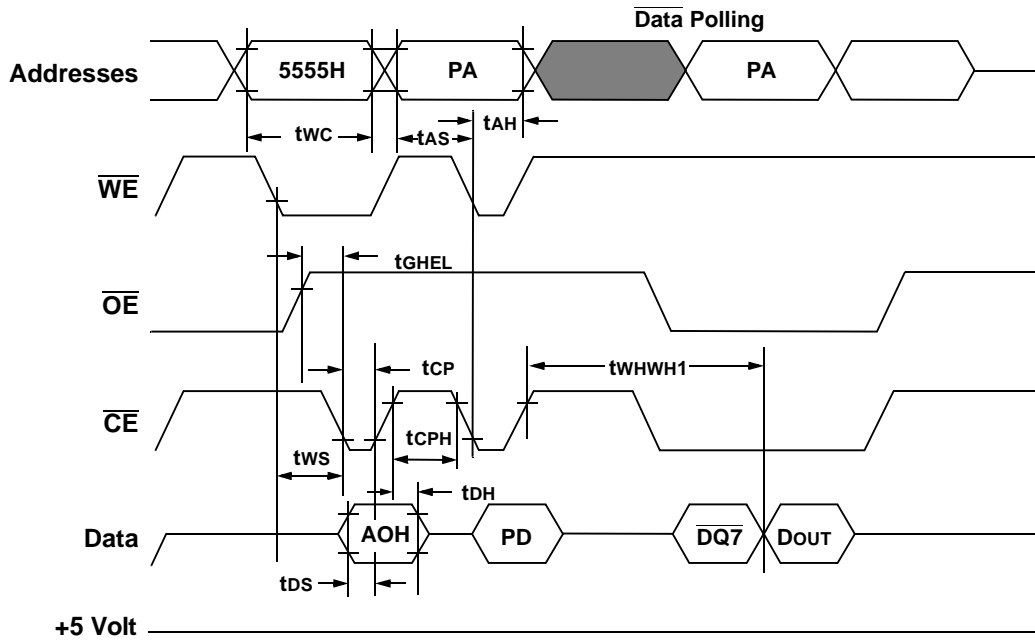


Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

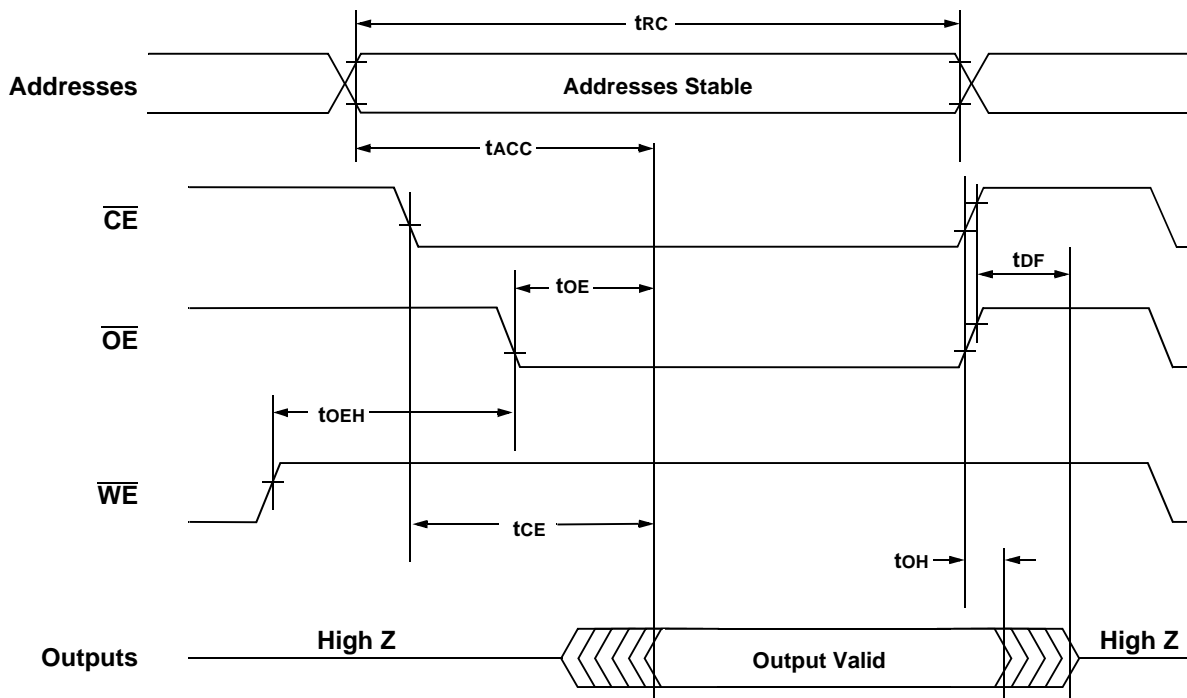
AC Waveforms for Write and Erase Operations, \overline{WE} Controlled



AC Waveforms for Write and Erase Operations, \overline{CE} Controlled



AC Waveform For Read Operations

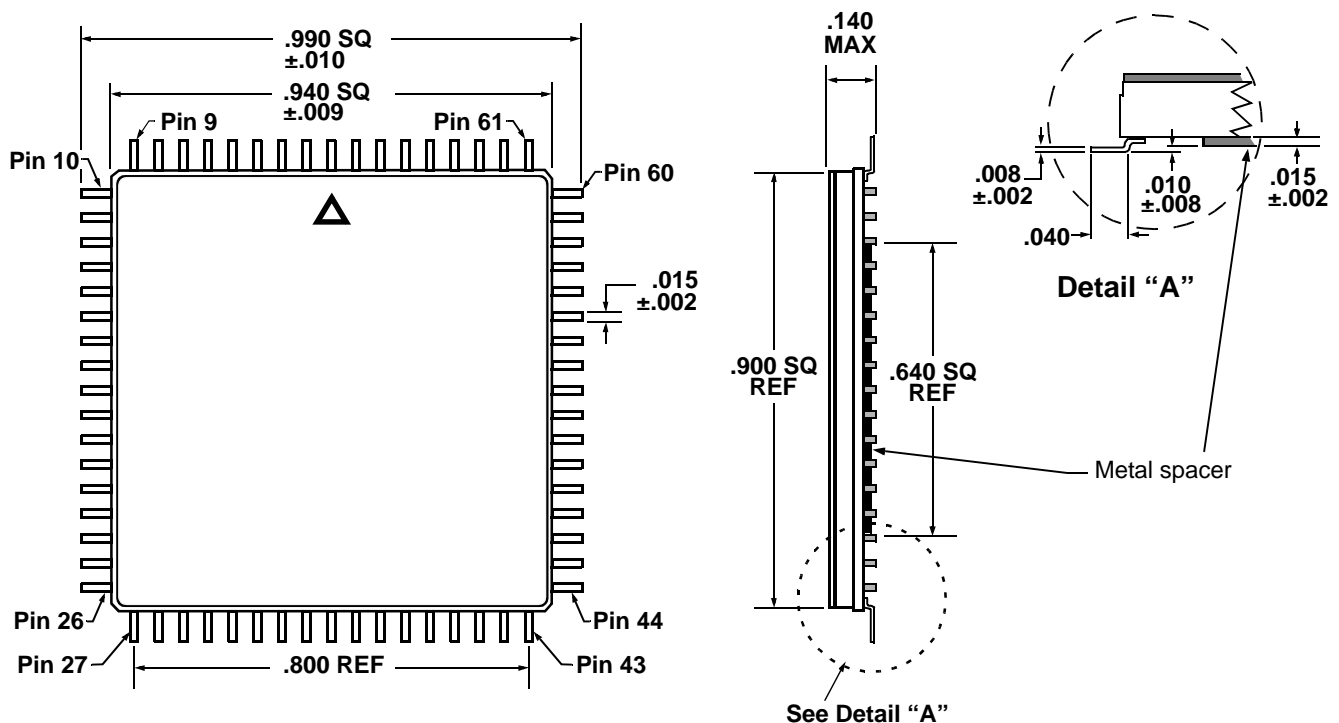


Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP (Standard Configuration)							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	\overline{OE}	52	GND
2	\overline{CE}_3	19	I/O ₈	36	\overline{CE}_2	53	I/O ₂₃
3	A ₅	20	I/O ₉	37	A ₁₇	54	I/O ₂₂
4	A ₄	21	I/O ₁₀	38	RY/ \overline{BY}	55	I/O ₂₁
5	A ₃	22	I/O ₁₁	39	NC	56	I/O ₂₀
6	A ₂	23	I/O ₁₂	40	NC	57	I/O ₁₉
7	A ₁	24	I/O ₁₃	41	A ₁₈	58	I/O ₁₈
8	A ₀	25	I/O ₁₄	42	A ₁₉	59	I/O ₁₇
9	\overline{RESET}	26	I/O ₁₅	43	A ₂₀	60	I/O ₁₆
10	I/O ₀	27	V _{CC}	44	I/O ₃₁	61	V _{CC}
11	I/O ₁	28	A ₁₁	45	I/O ₃₀	62	A ₁₀
12	I/O ₂	29	A ₁₂	46	I/O ₂₉	63	A ₉
13	I/O ₃	30	A ₁₃	47	I/O ₂₈	64	A ₈
14	I/O ₄	31	A ₁₄	48	I/O ₂₇	65	A ₇
15	I/O ₅	32	A ₁₅	49	I/O ₂₆	66	A ₆
16	I/O ₆	33	A ₁₆	50	I/O ₂₅	67	\overline{WE}
17	I/O ₇	34	\overline{CE}_1	51	I/O ₂₄	68	\overline{CE}_4

Consult Factory for Special order (Optional Configuration): Pin 38 - \overline{WE}_2 , Pin 39 - \overline{WE}_3 , Pin 40 - \overline{WE}_4 and Pin 67 - \overline{WE}_1

"F18" — CQFP Package



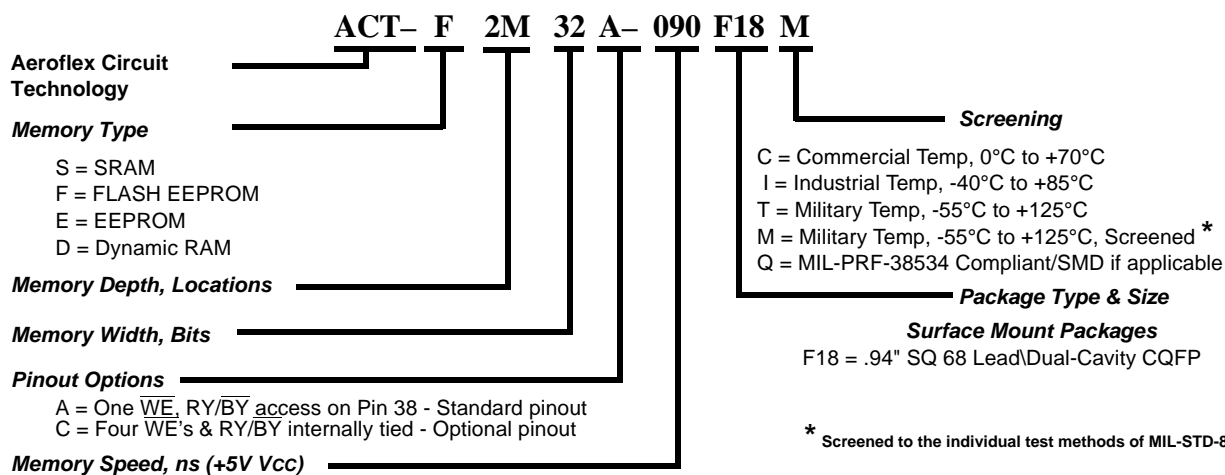
All dimensions in inches



Ordering Information

Model Number	Screening	Speed	Package
ACT-F2M32A-090F18C	Commercial (0°C to +70°C)	90 ns	CQFP
ACT-F2M32A-120F18C	Commercial (0°C to +70°C)	120 ns	CQFP
ACT-F2M32A-150F18C	Commercial (0°C to +70°C)	150 ns	CQFP
ACT-F2M32A-090F18I	Industrial (-40°C to +85°C)	90 ns	CQFP
ACT-F2M32A-120F18I	Industrial (-40°C to +85°C)	120 ns	CQFP
ACT-F2M32A-150F18I	Industrial (-40°C to +85°C)	150 ns	CQFP
ACT-F2M32A-090F18M	Military (-55°C to +125°C)	90 ns	CQFP
ACT-F2M32A-120F18M	Military (-55°C to +125°C)	120 ns	CQFP
ACT-F2M32A-150F18M	Military (-55°C to +125°C)	150 ns	CQFP
ACT-F2M32A-090F18Q	DESC Drawing Pending MIL-PRF-38534 Compliant	90 ns	CQFP
ACT-F2M32A-120F18Q	DESC Drawing Pending MIL-PRF-38534 Compliant	120 ns	CQFP
ACT-F2M32A-150F18Q	DESC Drawing Pending MIL-PRF-38534 Compliant	150 ns	CQFP

Part Number Breakdown



Specifications subject to change without notice

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