

1. General description

Planar passivated AC Thyristor Triac power switch in a SOT186A (TO-220F) "full pack" plastic package with self-protective capabilities against low and high energy transients. This "series CTN" triac will commutate the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ °C}$) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- High junction operating temperature capability ($T_{j(max)} = 150\text{ °C}$)
- High minimum I_{GT} for guaranteed immunity to gate noise
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt and IEC 61000-4-4 fast transient
- Package meets UL94V0 flammability requirement
- Package is RoHS compliant
- Package meets UL1557 isolation test requirement rated at 2500V RMS

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls
- Applications subject to high temperature ($T_{j(max)} = 150\text{ °C}$)

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|-----------------------------------|--|-----|-----|-----|------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_h \leq 85\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 12 | A |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|-----|-----|------|
| I _{TSM} | non-repetitive peak on-state current | full sine wave; T _{j(initial)} = 25 °C; t _p = 20 ms; Fig. 4 ; Fig. 5 | - | - | 120 | A |
| | | full sine wave; T _{j(initial)} = 25 °C; t _p = 16.7 ms | - | - | 132 | A |
| T _j | junction temperature | | - | - | 150 | °C |
| V _{PP} | peak pulse voltage | T _j = 25 °C; non-repetitive, off-state; Fig. 6 | - | - | 2 | kV |
| Static characteristics | | | | | | |
| I _{GT} | gate trigger current | V _D = 12 V; I _T = 100 mA; LD+ G+; T _j = 25 °C; Fig. 8 | 5 | - | 35 | mA |
| | | V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; Fig. 8 | 5 | - | 35 | mA |
| | | V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; Fig. 8 | 5 | - | 35 | mA |
| I _H | holding current | V _D = 12 V; T _j = 25 °C; Fig. 10 | - | - | 30 | mA |
| V _T | on-state voltage | I _T = 17 A; T _j = 25 °C; Fig. 11 | - | - | 1.5 | V |
| V _{CL} | clamping voltage | I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 25 °C | 850 | - | - | V |
| Dynamic characteristics | | | | | | |
| dV _D /dt | rate of rise of off-state voltage | V _{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit | 4000 | - | - | V/μs |
| | | V _{DM} = 536 V; T _j = 150 °C; exponential waveform; gate open circuit | 2000 | - | - | V/μs |
| dI _{com} /dt | rate of change of commutating current | V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 20 V/μs; gate open circuit; snubberless condition | 12 | - | - | A/ms |
| | | V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 10 V/μs; gate open circuit | 15 | - | - | A/ms |
| | | V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 1 V/μs; gate open circuit | 20 | - | - | A/ms |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------------------|--|---|
| 1 | CM | common | <p style="text-align: center;">mb</p> <p style="text-align: center;">1 2 3</p> <p style="text-align: center;">TO-220F (SOT186A)</p> | <p style="text-align: center;">LD</p> <p style="text-align: center;">G</p> <p style="text-align: center;">CM</p> <p style="text-align: center;">003aaf296</p> |
| 2 | LD | load | | |
| 3 | G | gate | | |
| mb | n.c. | mounting base; isolated | | |

6. Ordering information

Table 3. Marking codes

| Type number | Package Name | Orderable part number | Packing method | Small packing quantity | Package version | Package issue date |
|----------------|--------------|-----------------------|----------------|------------------------|-----------------|--------------------|
| ACTT12X-800CTN | TO220F | ACTT12X-800CTNQ | Tube | 50 | SOT186A | 14-Nov-2013 |

| Type number | Marking codes | |
|----------------|---------------------------------|---------------------------------|
| | Assembly factory: A | Assembly factory: d |
| ACTT12X-800CTN | ACTT12X 800CTN PJAxxxx xx | ACTT12X 800CTN PJdxxxx xx |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|--|-----|-----|------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_h \leq 85\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 12 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 120 | A |
| | | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | 132 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; sine-wave pulse | - | 72 | A ² s |
| di_T/dt | rate of rise of on-state current | $I_G = 70\text{ mA}$ | - | 100 | A/ μ s |
| I_{GM} | peak gate current | | - | 2 | A |
| P_{GM} | peak gate power | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.5 | W |
| T_{stg} | storage temperature | | -40 | 150 | °C |
| T_j | junction temperature | | - | 150 | °C |
| V_{PP} | peak pulse voltage | $T_j = 25\text{ °C}$; non-repetitive, off-state; Fig. 6 | - | 2 | kV |

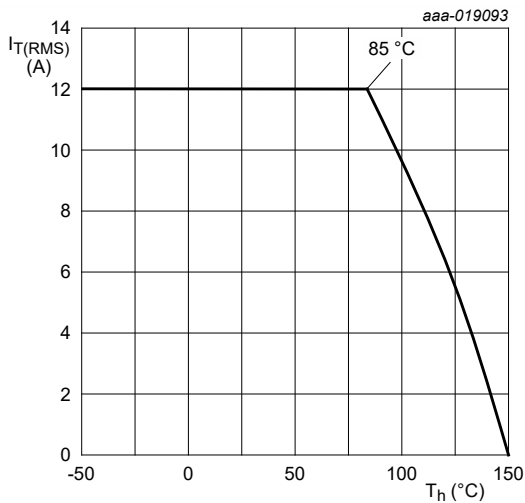


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values

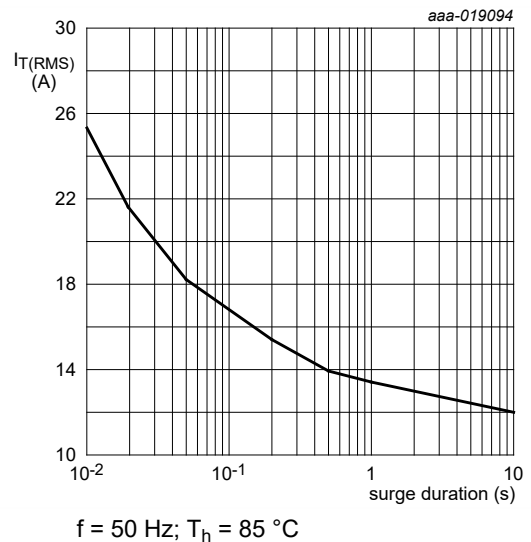


Fig. 2. RMS on-state current as a function of surge duration; maximum values

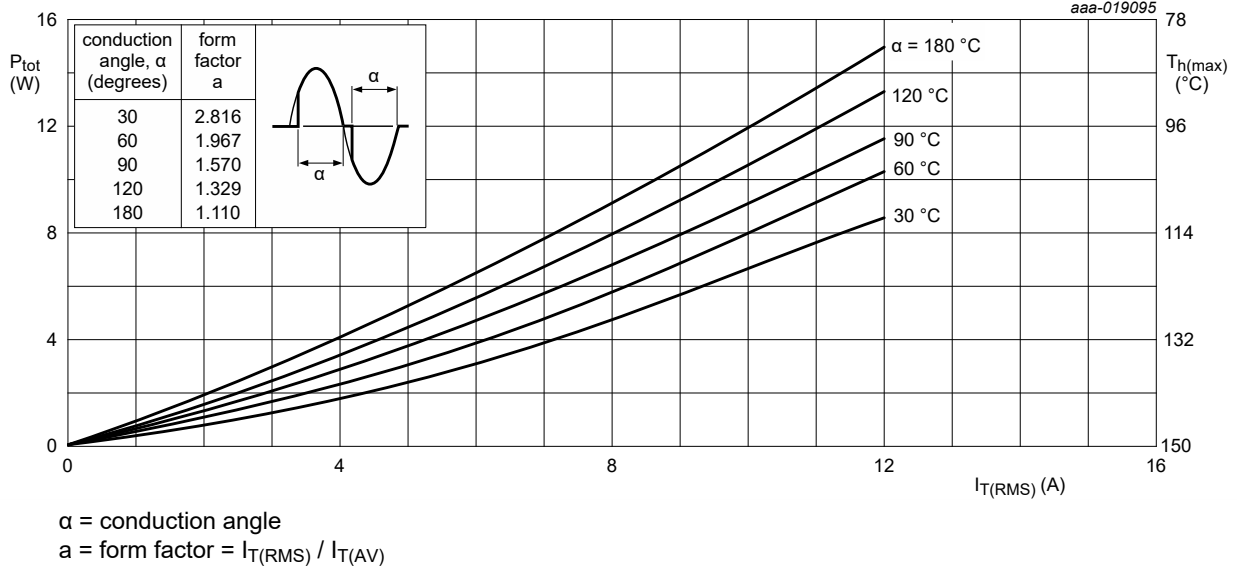


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

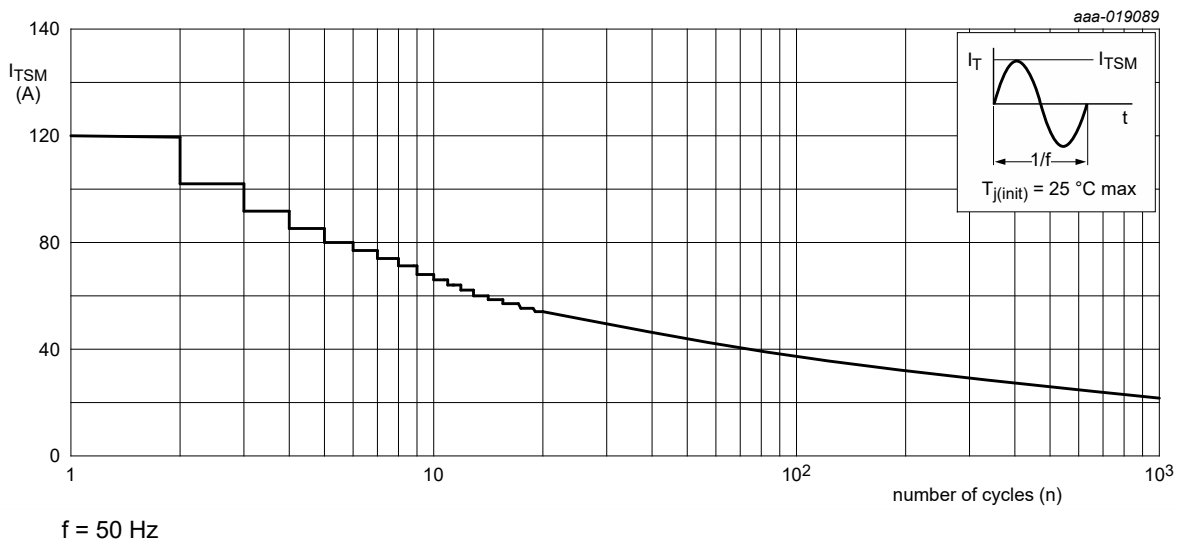


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

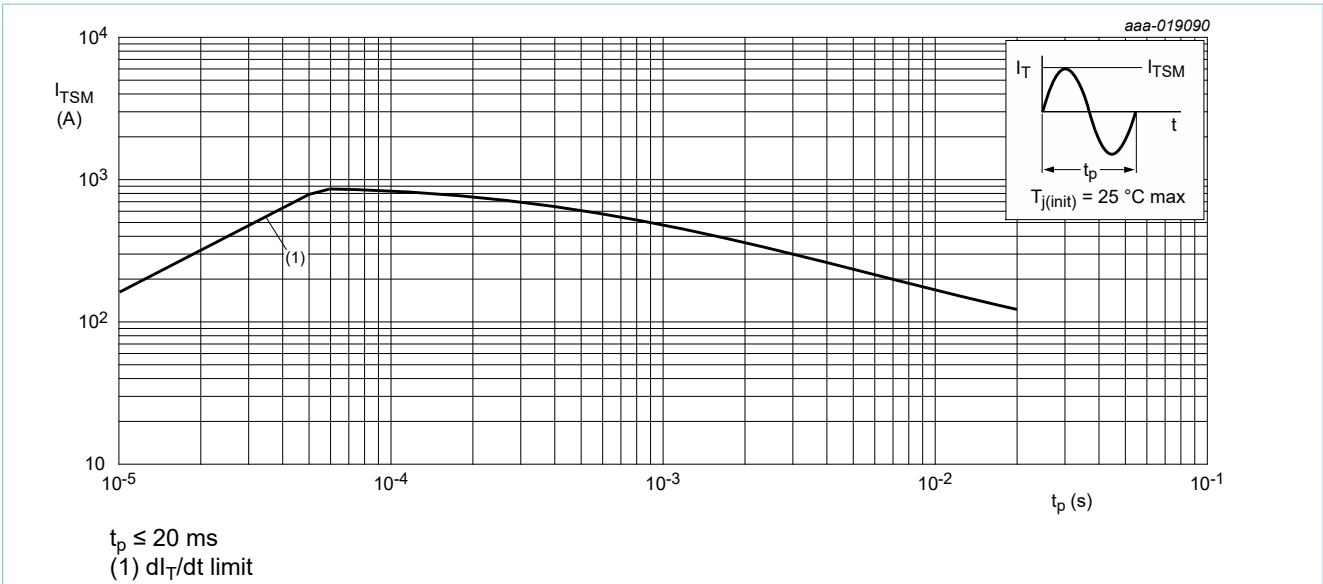


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

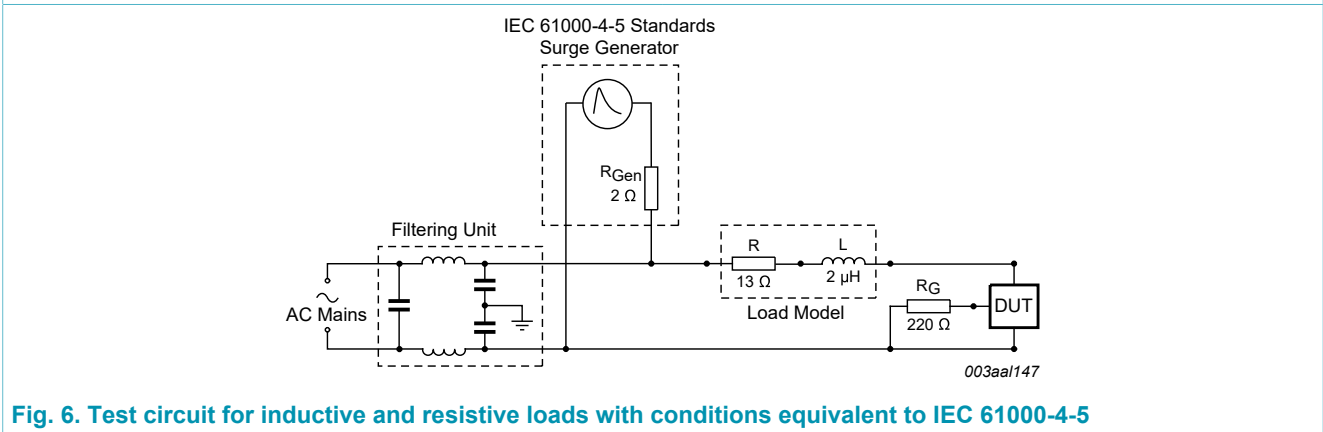


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|--|--|-----|-----|-----|------|
| $R_{th(j-h)}$ | thermal resistance from junction to heatsink | full or half cycle; with heatsink compound; Fig. 7 | - | - | 4.5 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | in free air | - | 55 | - | K/W |

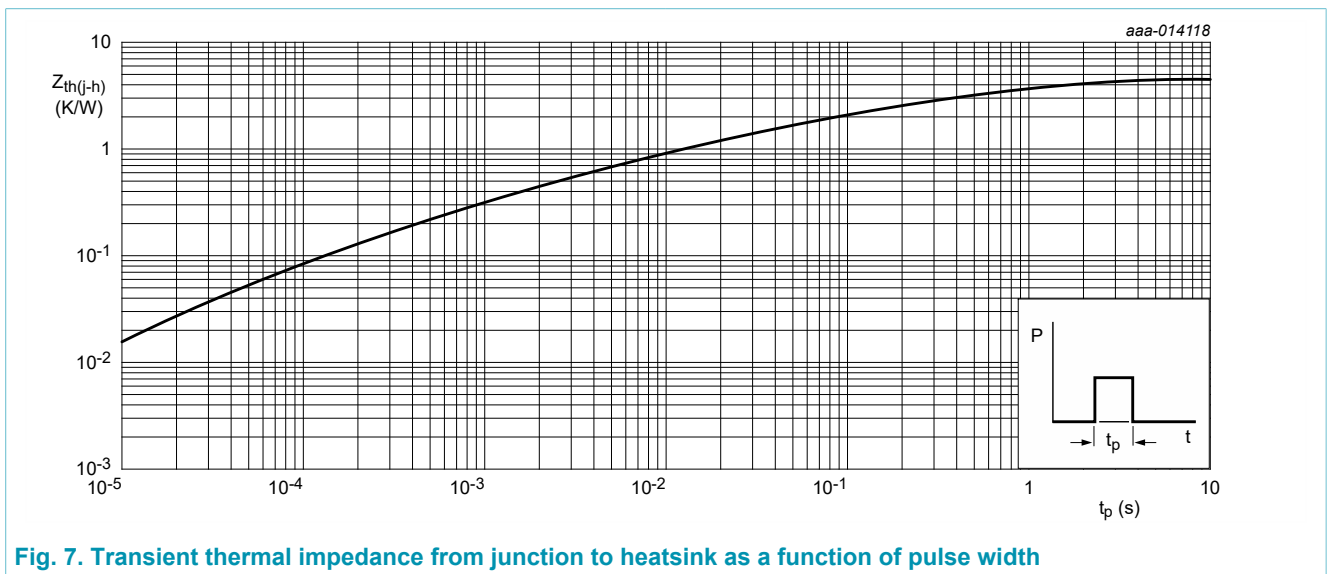


Fig. 7. Transient thermal impedance from junction to heatsink as a function of pulse width

9. Isolation characteristics

Table 6. Isolation characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|-----------------------|---|-----|-----|------|------|
| $V_{isol(RMS)}$ | RMS isolation voltage | from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $T_h = 25\text{ }^\circ\text{C}$ | - | - | 2500 | V |
| C_{isol} | isolation capacitance | from main terminal 2 to external heatsink; $f = 1\text{ MHz}$; $T_h = 25\text{ }^\circ\text{C}$ | - | 10 | - | pF |

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|------|-----|------|
| Static characteristics | | | | | | |
| I _{GT} | gate trigger current | V _D = 12 V; I _T = 100 mA; LD+ G+; T _j = 25 °C; Fig. 8 | 5 | - | 35 | mA |
| | | V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; Fig. 8 | 5 | - | 35 | mA |
| | | V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; Fig. 8 | 5 | - | 35 | mA |
| I _L | latching current | V _D = 12 V; I _G = 100 mA; LD+ G+; T _j = 25 °C; Fig. 9 | - | - | 40 | mA |
| | | V _D = 12 V; I _G = 100 mA; LD+ G-; T _j = 25 °C; Fig. 9 | - | - | 60 | mA |
| | | V _D = 12 V; I _G = 100 mA; LD- G-; T _j = 25 °C; Fig. 9 | - | - | 40 | mA |
| I _H | holding current | V _D = 12 V; T _j = 25 °C; Fig. 10 | - | - | 30 | mA |
| V _T | on-state voltage | I _T = 17 A; T _j = 25 °C; Fig. 11 | - | - | 1.5 | V |
| V _{GT} | gate trigger voltage | V _D = 12 V; I _T = 100 mA; T _j = 25 °C; Fig. 12 | - | 0.8 | 1 | V |
| | | V _D = 400 V; I _T = 100 mA; T _j = 150 °C; Fig. 12 | 0.2 | 0.45 | - | V |
| I _D | off-state current | V _D = 800 V; T _j = 25 °C | - | - | 10 | μA |
| | | V _D = 800 V; T _j = 150 °C | - | - | 2 | mA |
| V _{CL} | clamping voltage | I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 25 °C | 850 | - | - | V |
| Dynamic characteristics | | | | | | |
| dV _D /dt | rate of rise of off-state voltage | V _{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit | 4000 | - | - | V/μs |
| | | V _{DM} = 536 V; T _j = 150 °C; exponential waveform; gate open circuit | 2000 | - | - | V/μs |
| dI _{com} /dt | rate of change of commutating current | V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 20 V/μs; gate open circuit; snubberless condition | 12 | - | - | A/ms |
| | | V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 10 V/μs; gate open circuit | 15 | - | - | A/ms |
| | | V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 1 V/μs; gate open circuit | 20 | - | - | A/ms |

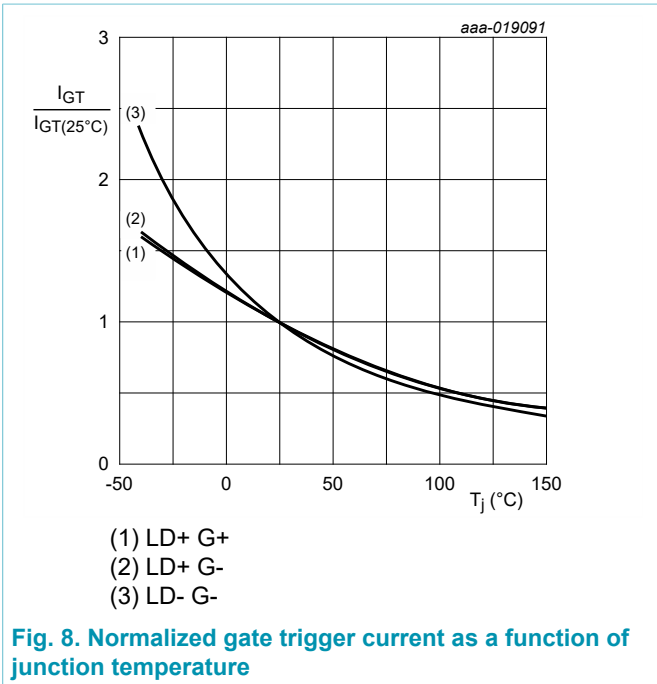


Fig. 8. Normalized gate trigger current as a function of junction temperature

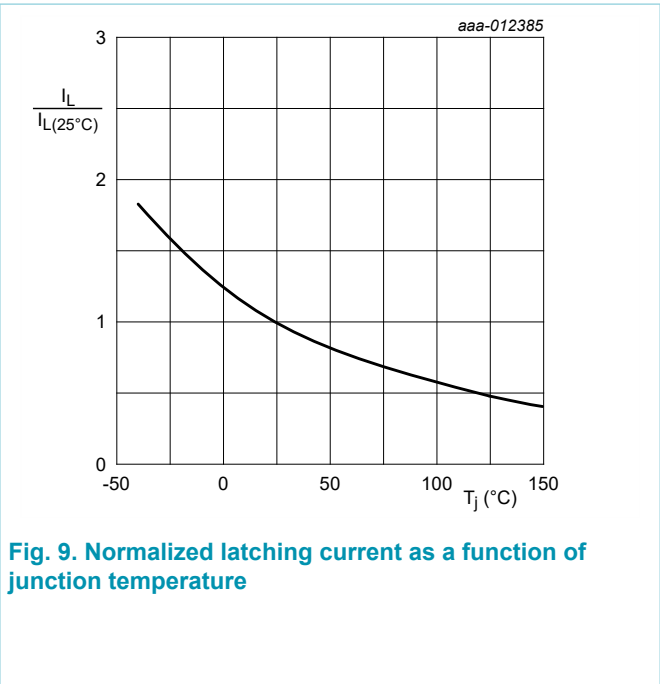


Fig. 9. Normalized latching current as a function of junction temperature

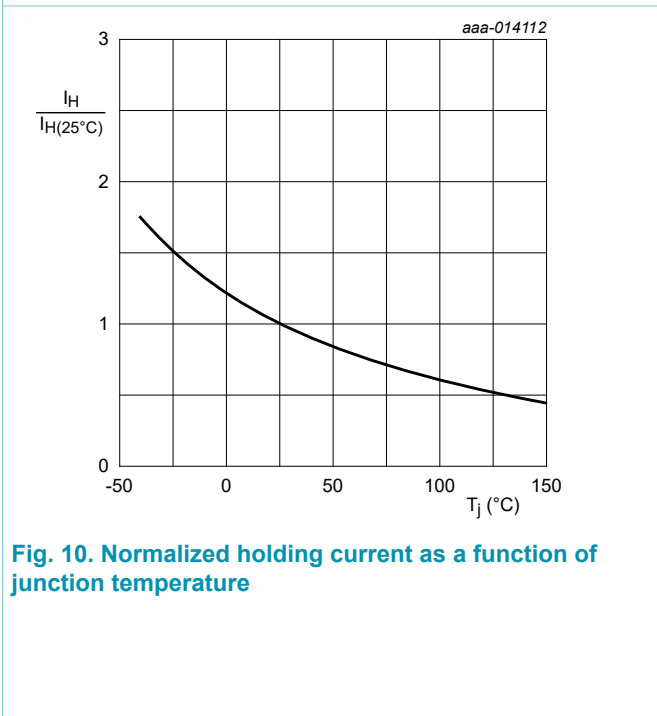


Fig. 10. Normalized holding current as a function of junction temperature

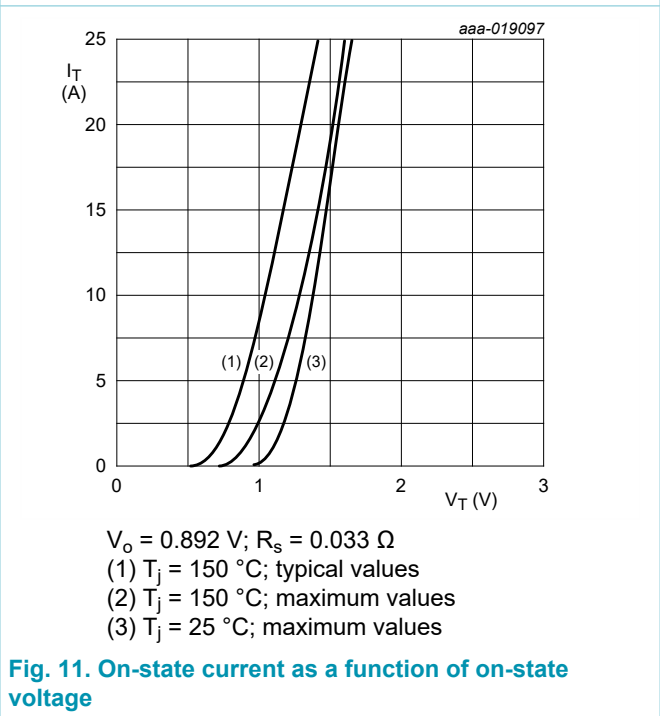


Fig. 11. On-state current as a function of on-state voltage

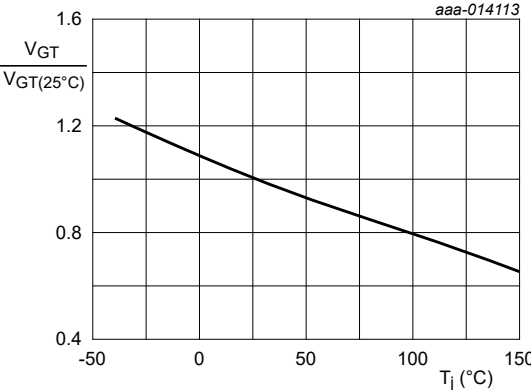


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

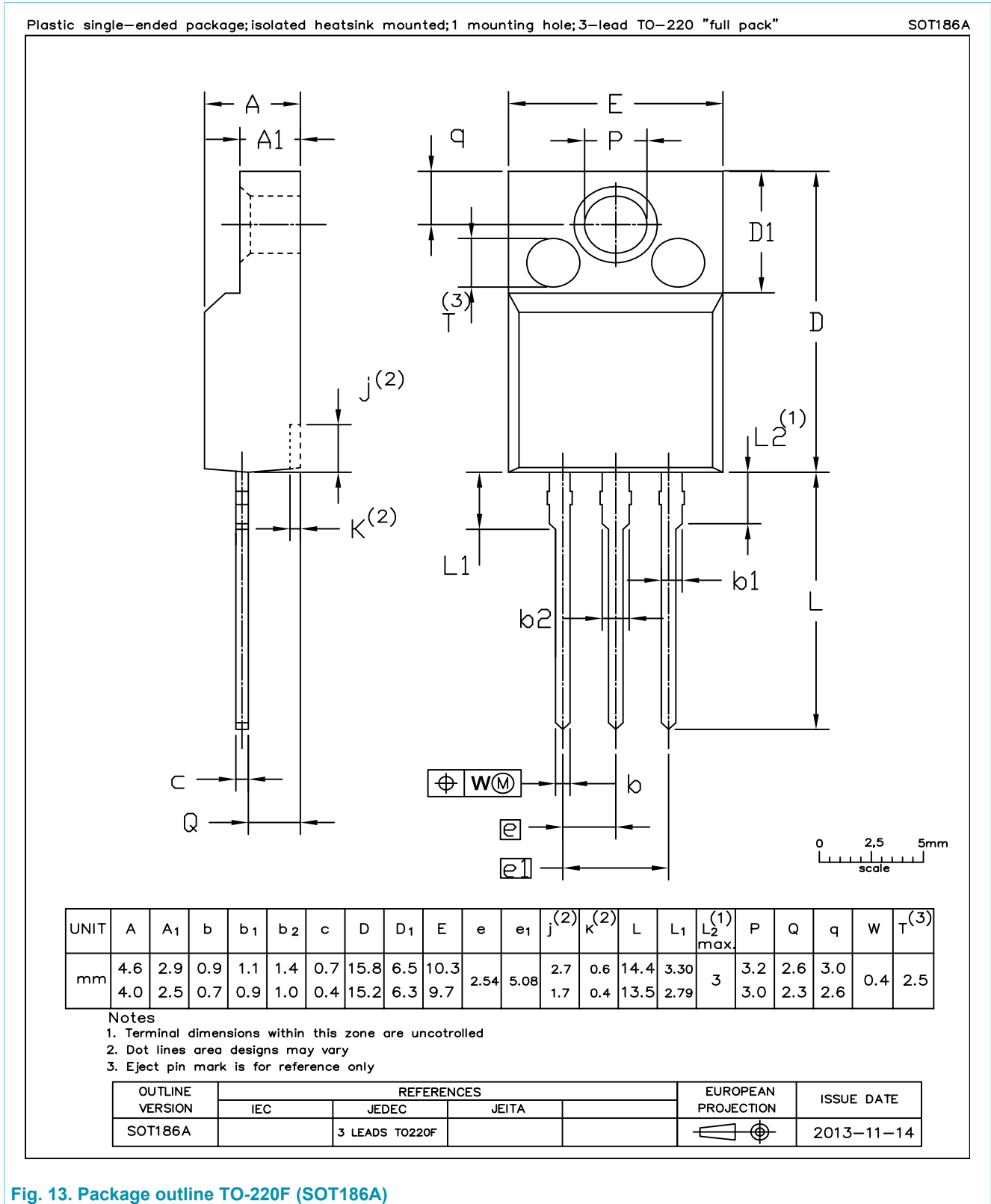


Fig. 13. Package outline TO-220F (SOT186A)

12. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

| | |
|-----------------------------------|----|
| 1. General description..... | 1 |
| 2. Features and benefits..... | 1 |
| 3. Applications..... | 1 |
| 4. Quick reference data..... | 1 |
| 5. Pinning information..... | 3 |
| 6. Ordering information..... | 3 |
| 7. Limiting values..... | 4 |
| 8. Thermal characteristics..... | 7 |
| 9. Isolation characteristics..... | 7 |
| 10. Characteristics..... | 8 |
| 11. Package outline..... | 11 |
| 12. Legal information..... | 12 |

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