

1. General description

AC Thyristor Triac power switch in a SOT186A (T0-220F) “full pack” plastic package with self-protection clamping capabilities against low and high energy transients.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Pin compatible with standard triacs
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt and IEC 61000-4-4 fast transient
- Enhanced dynamic performance
- Package is RoHS compliant
- Package meets UL94V0 flammability requirement
- Package meets UL1557 isolation test requirement rated at 2500V RMS

3. Applications

- Fan motor circuits
- Highly inductive, resistive and safety loads
- Loads such as contactors, circuit breakers, valves, dispensers and door locks
- Pump motor circuits

4. Quick reference data

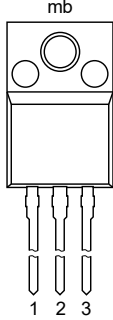
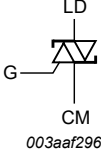
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 89\text{ }^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	6	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 16.7\text{ ms}$	-	-	66	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	60	A
T_j	junction temperature		-	-	125	$^\circ\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{PP}	peak pulse voltage	T _j = 25 °C; non-repetitive, off-state; Fig. 6	-	-	2	kV
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 100 mA; LD+ G+; T _j = 25 °C; Fig. 8	5	-	35	mA
		V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; Fig. 8	5	-	35	mA
		V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; Fig. 8	5	-	35	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 10	-	-	40	mA
V _T	on-state voltage	I _T = 8 A; T _j = 25 °C; Fig. 11	-	-	1.65	V
V _{CL}	clamping voltage	I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 25 °C	800	-	-	V
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	1500	-	-	V/μs
dI _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 6 A; dV _{com} /dt = 20 V/μs; (snubberless condition); gate open circuit	12	-	-	A/ms
		V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 6 A; dV _{com} /dt = 10 V/μs; gate open circuit	15	-	-	A/ms
		V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 6 A; dV _{com} /dt = 1 V/μs; gate open circuit	20	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 <p style="text-align: center;">mb</p> <p style="text-align: center;">1 2 3</p> <p style="text-align: center;">TO-220F (SOT186A)</p>	 <p style="text-align: center;">LD</p> <p style="text-align: center;">G</p> <p style="text-align: center;">CM</p> <p style="text-align: center;">003aaf296</p>
2	LD	load		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT6X-800CN	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Marking

Table 4. Marking codes

Type number	Marking code
ACTT6X-800CN	ACTT6X-800CN

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 89\text{ }^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	6	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 16.7\text{ ms}$	-	66	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	60	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	18	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 70\text{ mA}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current	$t = 20\text{ }\mu\text{s}$	-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_j	junction temperature		-	125	$^\circ\text{C}$
V_{PP}	peak pulse voltage	$T_j = 25\text{ }^\circ\text{C}$; non-repetitive, off-state; Fig. 6	-	2	kV

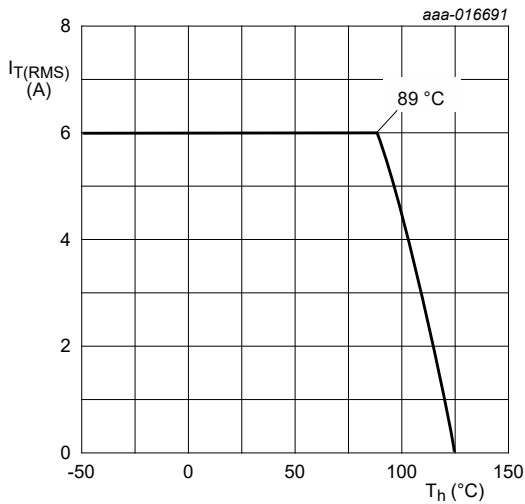


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values

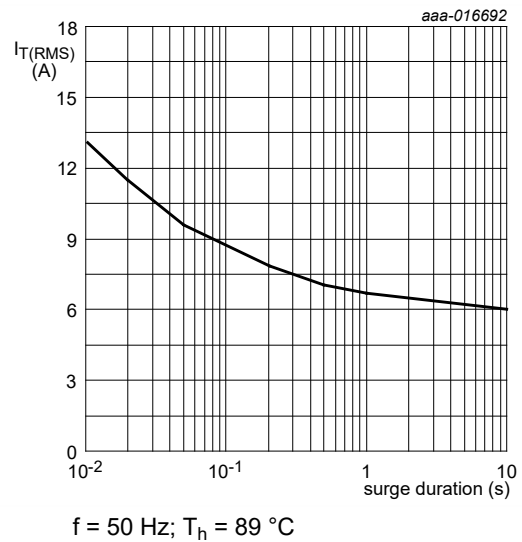


Fig. 2. RMS on-state current as a function of surge duration; maximum values

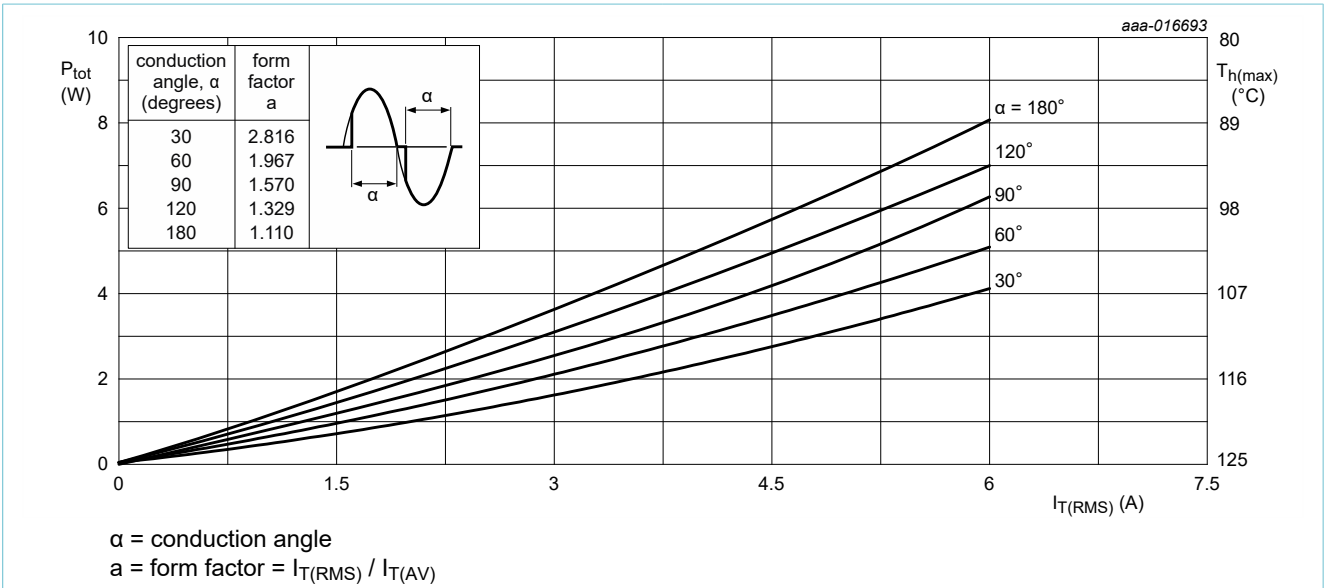


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

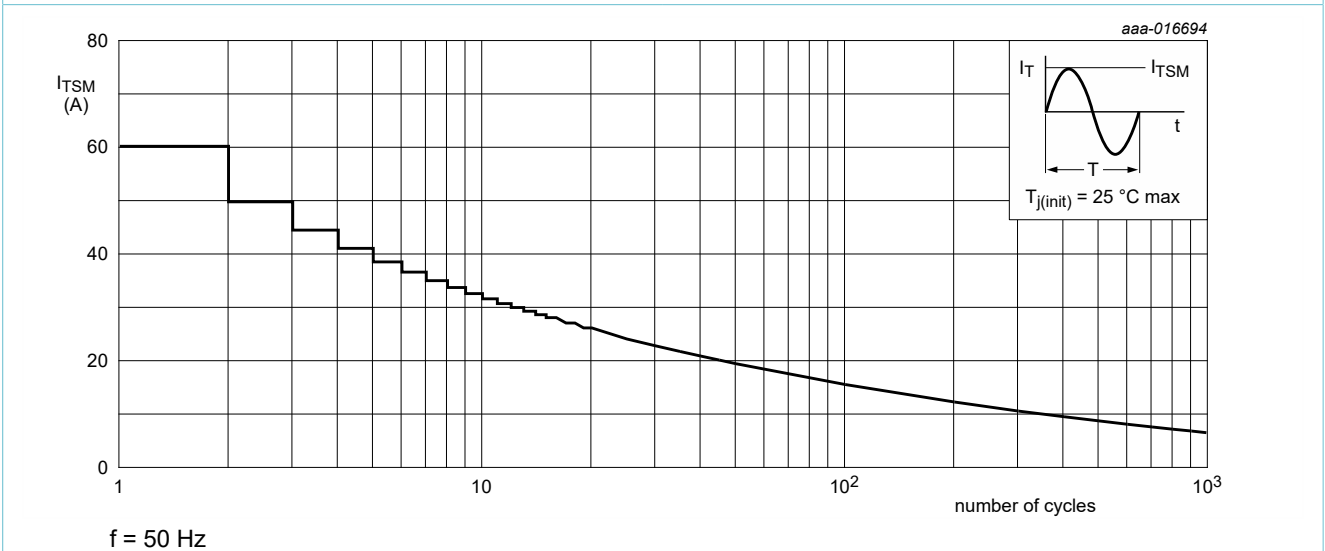


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

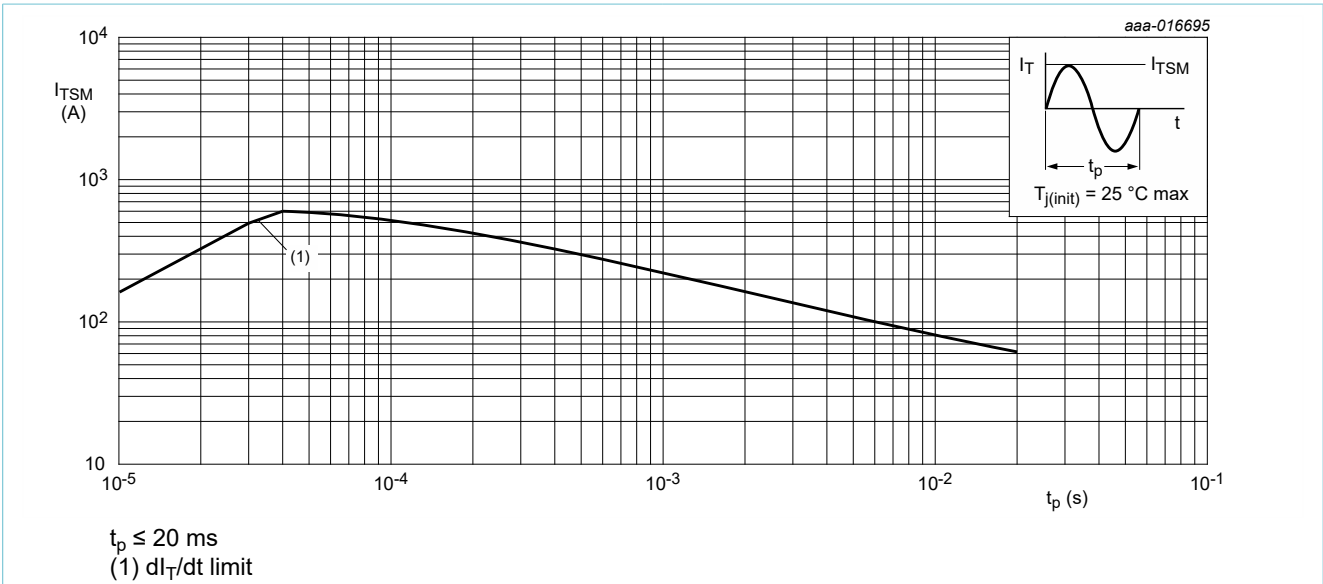


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

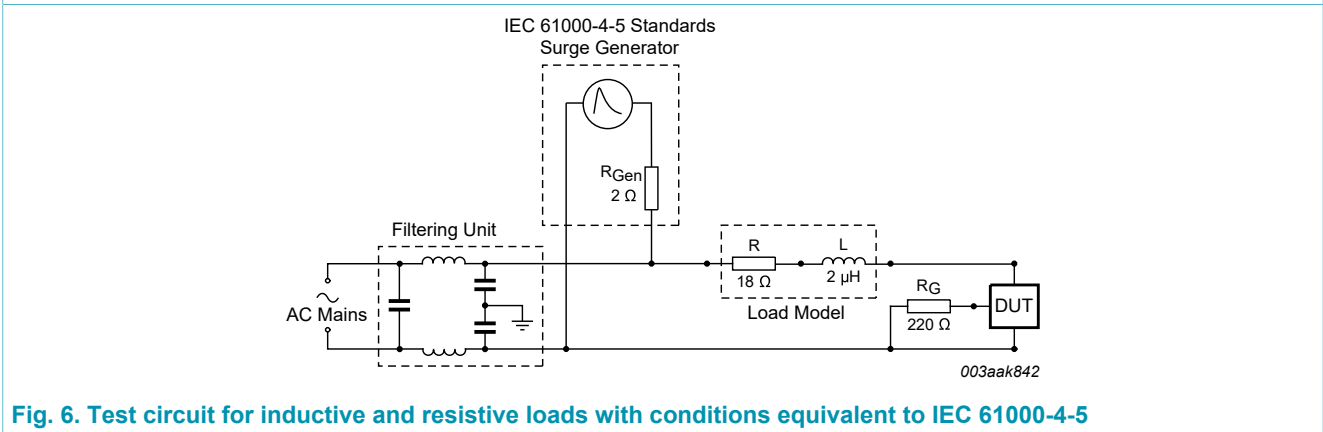


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-h)}	thermal resistance from junction to heatsink	full or half cycle; with heatsink compound; Fig. 7	-	-	4.5	K/W
		full or half cycle; without heatsink compound	-	-	6.5	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	in free air	-	60	-	K/W

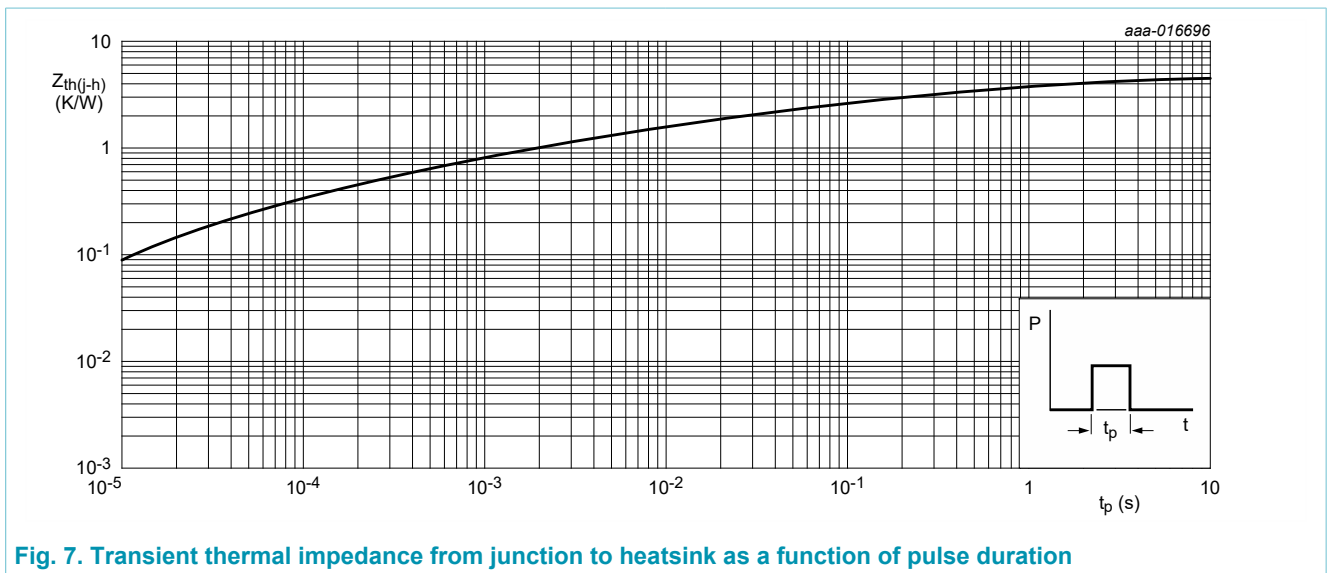


Fig. 7. Transient thermal impedance from junction to heatsink as a function of pulse duration

10. Isolation characteristics

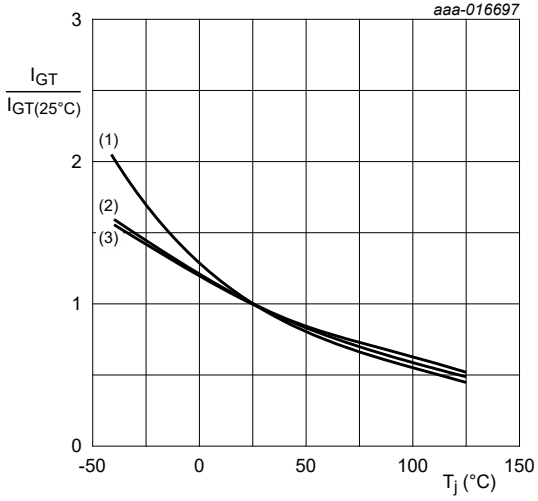
Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{isol(RMS)}	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; T _h = 25 °C	-	-	2500	V
C _{isol}	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz; T _h = 25 °C	-	10	-	pF

11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 8	5	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 8	5	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 8	5	-	35	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 9	-	-	50	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 9	-	-	75	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 9	-	-	50	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 10	-	-	40	mA
V_T	on-state voltage	$I_T = 8\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	-	1.65	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 12	-	0.8	1	V
		$V_D = 400\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 125\text{ °C}$; Fig. 12	0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 25\text{ °C}$	-	-	10	μA
		$V_D = 800\text{ V}$; $T_j = 125\text{ °C}$	-	-	0.5	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ °C}$	800	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	1500	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 6\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit	12	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 6\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit	15	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 6\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit	20	-	-	A/ms



- (1) T2- G-
- (2) T2+ G-
- (3) T2+ G+

Fig. 8. Normalized gate trigger current as a function of junction temperature

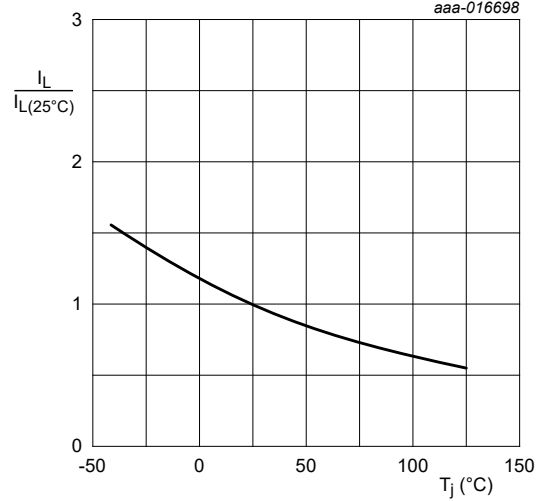


Fig. 9. Normalized latching current as a function of junction temperature

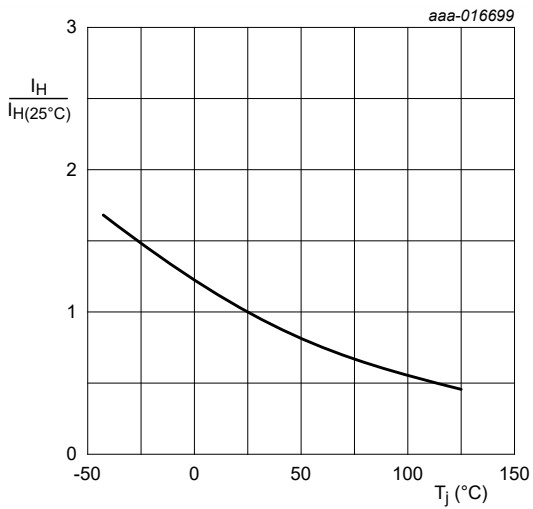
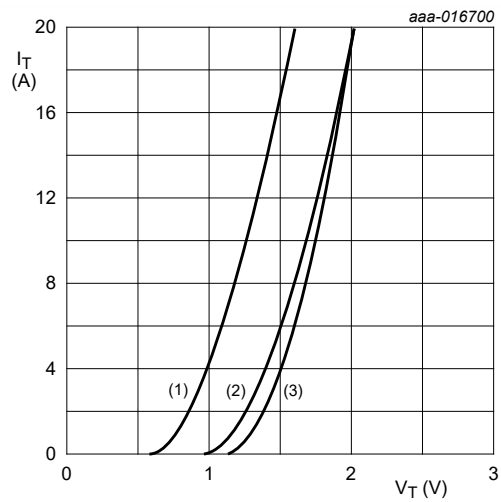


Fig. 10. Normalized holding current as a function of junction temperature



$V_o = 1.239 \text{ V}; R_s = 0.037 \Omega$

- (1) $T_j = 125^\circ\text{C}$; typical values
- (2) $T_j = 125^\circ\text{C}$; maximum values
- (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 11. On-state current as a function of on-state voltage

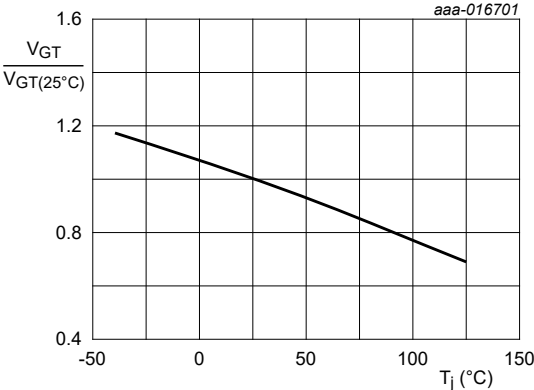
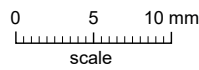
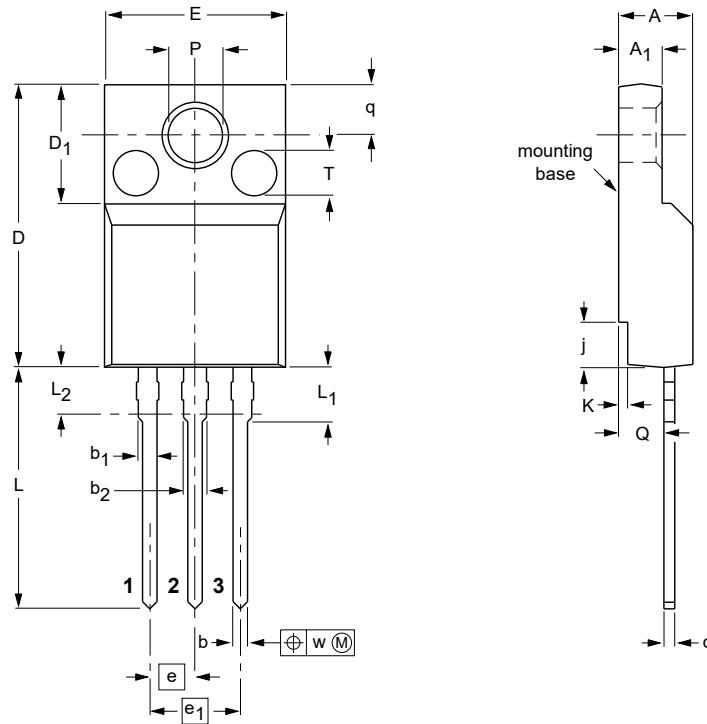


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

12. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	b ₂	c	D	D ₁	E	e	e ₁	j	K	L	L ₁	L ₂ ⁽¹⁾ max.	P	Q	q	T ⁽²⁾	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

- Terminal dimensions within this zone are uncontrolled.
- Both recesses are # 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT186A		3-lead TO-220F			02-04-09 06-02-14

Fig. 13. Package outline TO-220F (SOT186A)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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For sales office addresses, please send an email to: salesaddresses@ween-semi.com

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