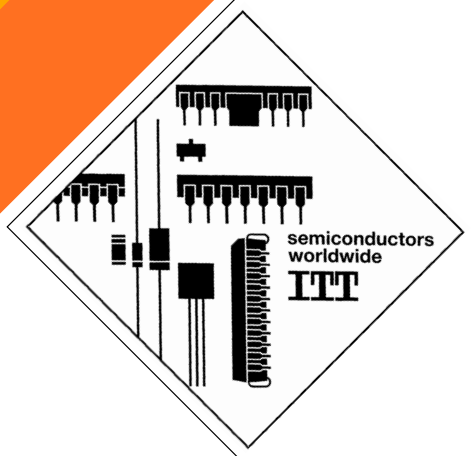

ACVP 2205
Adaptive Combfilter
Video Processor

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ITT Semiconductors

Contents

Adaptive Combfilter Video Processor

1. Introduction

The ACVP 2205 is a digital real–time signal processor for multistandard color TV sets based on the DIGIT2000 system. It handles composite video signals as well as S–VHS signals. For PAL and NTSC a 2H adaptive combfilter is implemented. It considerably improves the picture quality by a sophisticated luminance and chrominance separation. A single silicon chip contains the following functions:

– selectable 7 or 8 bit video input

– code converter and a data demultiplexer for composite and S–VHS input signals

– 2H adaptive combfilter for PAL and NTSC composite video signals

– adjustable horizontal and vertical peaking filter for luminance

– selectable luminance filter for enhanced frequency response

– black–level–expander for improving the picture contrast and the gamma correction

– contrast multiplier with limiter for the luminance signal

– adjustable chrominance filter

– all color signal processing circuits such as automatic color control (ACC), color killer, PAL identification, decoder with PAL compensation, hue correction

– color saturation multiplier with multiplexer for the color difference signals

– IM bus interface for communication with the CCU 2070 or CCU 3000 Central Control Unit

– circuitry for measuring dark current (CRT spot–cutoff), white level and photo current, and for transferring this data to the CCU.

The ACVP 2205 is pin compatible to the PVPU 2204 . It is designed in N–MOS technology and is available in a 40 pin Dil plastic package.

2. Functional Description

Supplied by one of the DIGIT2000 A/D converters (VCU 2136 or SAD 2140), the ACVP 2205 separates the video signal into luminance and chrominance. These two signals are processed in different circuits, which will be described in the following. The output signals are reconverted to analog signals in the VCU 2136 or VDU 2146. Their RGB output amplifiers are used to drive the cathodes of the CRT (see Fig. 2–4). Additionally, the ACVP 2205 performs a number of measurements and control operations (in conjunction with the VCU 2136 or VDU 2146)relating to picture tube alignment such as spot–cutoff current adjustment, white level control, beam current limiting, etc.

For a multistandard application including SECAM, the SPU 2243 SECAM Chroma Processor must be connected in parallel to the ACVP 2205 for chroma processing. The different processing delays Δt can be equalized in the DTI 2223.

2.1. Data Multiplexer and Code Converter

The data demultiplexer shown in Fig. 2–1 separates the incoming Double Data Stream DDS (composite video or S–VHS) into two data streams:

– DDS2 to luma and chroma circuits of the ACVP in case of composite video operation,

– DDS2 to luma circuits and DDS1 to chroma circuits of the ACVP in case of S–VHS operation.

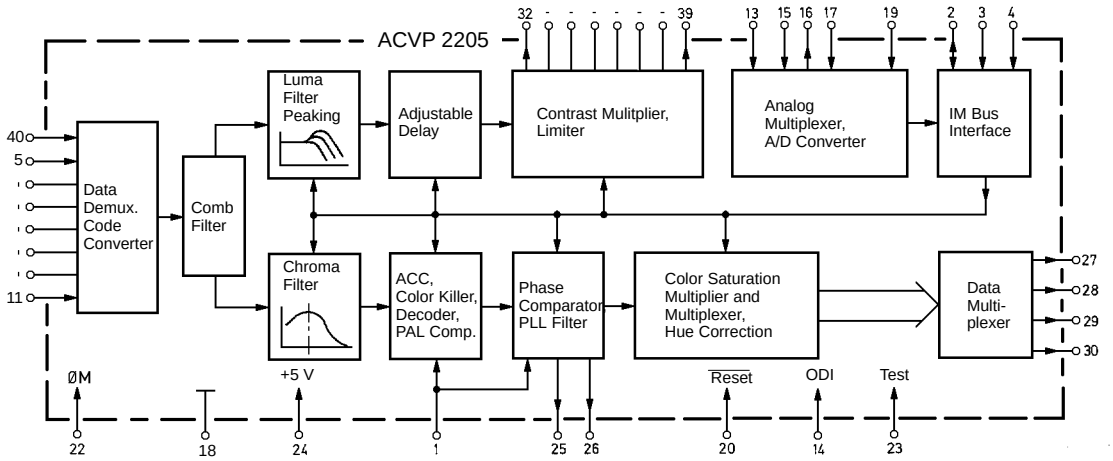


Fig. 2–1: Block diagram of the ACVP 2205 Adaptive Combfilter Video Processor

The DDS is a Gray–coded signal. The code converter converts the signal into a binary–coded signal for the composite/luminance channel and into an offset–binary–coded signal for the chrominance channel.

2.2. Luminance/Chrominance Separation

A conventional PAL/NTSC decoder decodes the composite video signal with a notch– and a bandpass filter (horizontal filtering). This way of luminance/chrominance separation reduces the maximum luminance resolution and creates crosstalk interferences called ”cross luminance” and ”cross color”. For an enhancement of the picture quality, the ACVP 2205 uses a 2H adaptive combfilter, which eliminates most of the mentioned decoding errors without introducing new artifacts like ”hanging dots”.

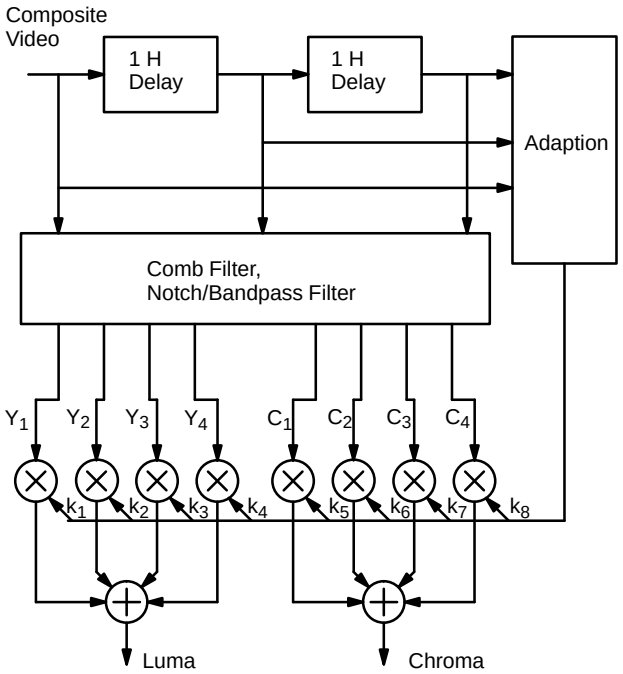


Fig. 2–2: Block diagram of the adaptive combfilter

As shown in Fig. 2–2, the input composite video signal is delayed by 0, 1H and 2H. These three signals are connected to the combfilter, which calculates up to four different processed luminance and chrominance signals for every pixel in parallel.

The adaption logic operates on the same input signals as the combfilter. Inside a 5x3 pixel matrix 12 gradients are being processed in parallel. After filtering these values in a logical filter (fuzzy logic), the output determines the most appropriate combination of the four channels for a perfectly filtered luminance and chrominance signal. The expression of the mixed luminance signal is

$$Y(n) = k_1Y_1(n) + k_2Y_2(n) + k_3Y_3(n) + k_4Y_4(n)$$

and for the chrominance it is

$$C(n) = k_5C_1(n) + k_6C_2(n) + k_7C_3(n) + k_8C_4(n)$$

The ACVP 2205 offers two selectable adaptive combfilter algorithms for both PAL and NTSC. In SECAM the luminance signal is filtered horizontally. Therefore the combfilter can be disabled.

In S–VHS mode luminance and chrominance are separate. Thus, in this mode, the combfilter is bypassed.

2.3. Luminance Channel

In the luminance channel the sync component is removed from the luminance, because it contains no information for this signal. Thus a fixed value of –0.25 (= –64 digital) is subtracted from the luminance.

The luminance frequency response is adjustable. Depending on the selected mode (combfilter on/off, S–VHS etc.) several filter are selectable. The following adjustments are implemented:

– – 6 dB reduction at the subcarrier frequency in combfilter mode

– smooth, flat or enhanced frequency response in all modes

– one or two trap filter in combfilter off mode or SECAM

Their different characteristics and the corresponding bits are shown in section 4.2. of the data sheet.

For improving the two–dimensional resolution of the picture, a horizontal and vertical peaking filter is implemented. In the horizontal direction, the sharpness is programmable in 9 steps (between –3dB and +10 dB), while in the vertical direction 16 steps are available (0dB to +6 dB). Both circuits include an adjustable coring function, which suppresses small signal amplitudes for reducing noise artifacts.

The picture enhancement of the black–level– expander is described in the next chapter.

The adjustable delay in the luminance channel has a range of ±4 clock cycles. This means ±4·56 ns with PAL or ±4·70 ns with NTSC (see Table 2–1).

Table 2–1: Variable luminance delay (Address 15)

Bits of low Byte 7	6	5	4	Number of clock cycles
0	1	1	1	+ 4
0	1	1	0	+ 3
0	1	0	1	+ 2
0	1	0	0	+ 1
1	×	×	×	0
0	0	1	1	– 1
0	0	1	0	– 2
0	0	0	1	– 3
0	0	0	0	– 4

The luminance amplitude is adjustable by the contrast multiplier. The multiplication factor is programmable between times 0 and times 2 in 64 steps via IM bus. If the output signal of the multiplier is greater then 8 bit (e.g. caused by peaking) it is limited to the maximum value of 255. The contrast setting can be adapted automatically to the room lighting by a photo sensor connected to pin 17 of the ACVP 2205. The signal of the photo sensor is digitized in the ACVP 2205 and transferred in multiplex operation to the CCU during vertical flyback. The CCU calculates the new contrast and changes the contrast multiplier value via IM bus.

A fixed value of 31 is added to the output of the contrast multiplier causing a constant DC offset of the signal. Thus the system transmits the negative undershoots caused by peaking, to the D/A converter (see Fig. 2–3).

From the contrast multiplier, the digital luminance signal is fed back to the VCU 2136. The 8 bit output signal contains the information of 10 bits by a four–step (2 bits) pulsewidth modulation of the LSB. This noise shaping reduces truncation errors caused by cutted bits of the contrast multiplier. Inside the VCU 2136 or VDU 2146, the signal is connected to the luminance D/A converter.

The converter feeds the analog luminance signal to the RGB matrix.

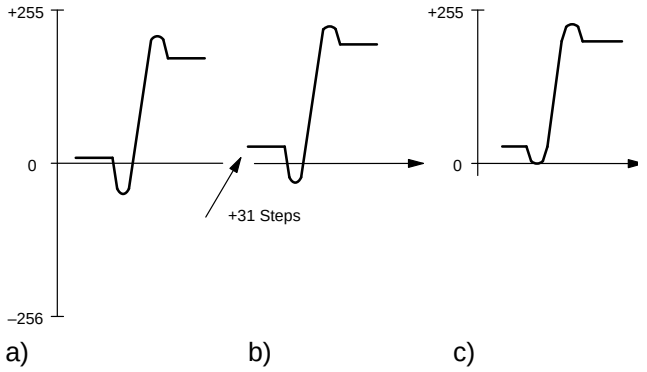


Fig. 2–3: Adding 31 steps DC signal
a) peaked signal after filter
b) the same signal with added 31 steps, this means a constant DC level or brightness
c) the signal at the output of the luminance D/A converter

2.4. Black–Level–Expander

In many reproduced TV scenes, the contrast is not optimum, and modifications of the contrast setting of the receiver may not produce an improvement. In this case a black–level–expander enhances the contrast of the picture. Therefore the luminance signal is modified with an adjustable, nonlinear function.

Criterion for the expansion is the dynamic range of the video signal. In every field, the minimum and maximum amplitudes Y_{min} and Y_{max} of the video signal are measured and stored. Based on these two values and the adjustable coefficient K1, a tilt point Y_t

$$Y_t = K1\ (Y_{max} - Y_{min}) + Y_{min}$$

is established, above which there is no expansion, while all luminance values below will be expanded (see Fig. 2–5).

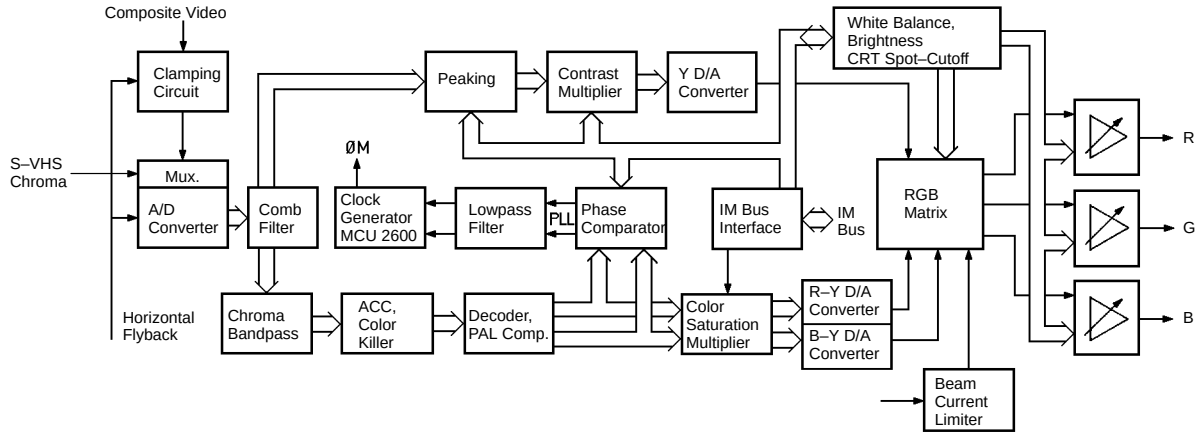


Fig. 2–4: Block diagram of the overall signal flow

The output signal of the black level expander is characterized as

$$Y_{out} = K2\ (Y_{in} - Y_t) + Y_{in}\ ,\quad Y_{in} < Y_t$$

$$Y_{out} = Y_{in}\ ,\quad Y_{in} \geq Y_t$$

The tilt point Y_t is a function of the dynamic range of the video signal. Thus the dynamic range determines the tilt point such that the larger the range, the higher the tilt-point.

The advantage of this black level expander is, that the black expansion is performed only if there is a large dynamic range in the video signal. Otherwise ($Y_{min} = Y_{max}$) the expansion to black is zero. Thus the expansion is performed only when it is most noticeable to the viewer.

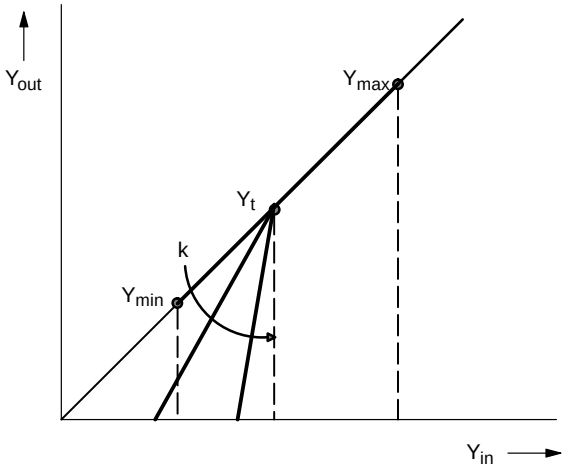


Fig. 2–5: Characteristic curve of the black–level–expander

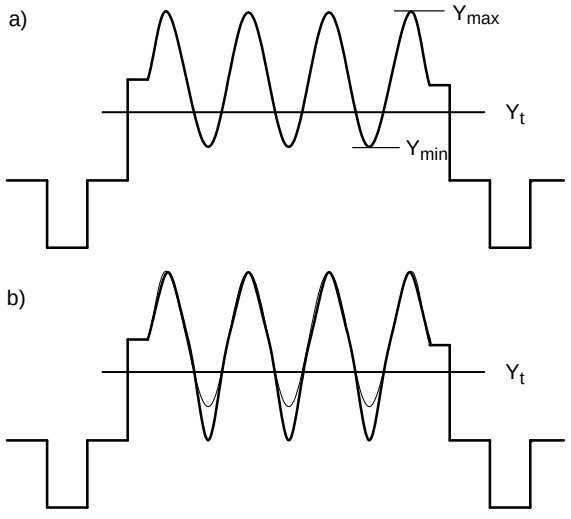


Fig. 2–6: Black–level–expansion
a) luminance input
b) luminance output

2.5. Chrominance Channel

The chrominance channel of the ACVP starts with the chroma filter. The chrominance frequency characteristic is selectable between a symmetrical or an asymmetrical response and to broad or narrow bandwidth by the CCU via IM bus. Asymmetrical response has been provided for compensation of the IF amplifier's response. In case of external video from a video tape recorder or a laser disk player, the symmetrical filter is recommended.

The automatic color control (ACC) circuit measures the burst amplitude of the chrominance signal and sets it to a constant level. The chrominance signal is switched off by the color killer in case of a weak burst amplitude or non–synchronism between color subcarrier and the demodulator. Additionally this circuit contains the PAL flip–flop, which is synchronized by the burst. The control range of the ACC is 36 dB. The reference amplitude is adjustable in 64 steps via the IM bus. The reference values for the window of the color killer are adjustable in 2 x 128 steps.

The chrominance signal is demodulated in the decoder. Outputs are the color difference signals R–Y and B–Y.

The color saturation multiplier adjusts the amplitude of the color difference signals. Caused by the small bandwidth of the color difference signals(max. 1 MHz), they are transmitted with a quarter of the luminance sampling rate to the VCU or VDU.

The hue correction is also done in the saturation multiplier by rotation of the R–Y and B–Y axles of the chroma signal.The PAL compensation of the chrominance signal is part of the combfilter.

The color saturation multiplier works according to the formula

$$(R–Y)' = (R–Y) \cdot f_S \cdot \cos\alpha - (B–Y) \cdot f_S \cdot \sin\alpha$$

$$(B–Y)' = (B–Y) \cdot f_S \cdot \cos\alpha + (R–Y) \cdot f_S \cdot \sin\alpha$$

where α is the angle of the rotation and f_S is the saturation. The resolution of α is 3° per step. The multiplication of $f_S \cdot \cos\alpha$ and $f_S \cdot \sin\alpha$ are done in the CCU.

For $\alpha = 0$, the adjustment range of the color saturation multiplier is 7 bits (128 steps) corresponding to the following scheme (two's complement code):

0 0 0 0 0 0 0 0 = × 0

0 0 0 1 0 0 0 0 = × 0.125

0 0 1 0 0 0 0 0 = × 0.25

0 1 0 0 0 0 0 0 = × 0.5

0 1 1 0 0 0 0 0 = × 0.75

0 1 1 1 1 1 1 1 = × 1

The MSB indicates the sign of the angle.

The color saturation multiplier includes a limiter. Thus the output is limited to 011111 or 10000. For a saturation greater than times 1, the reference value of the ACC can be increased.

The color difference signals are transferred in multiplex to the VCU 2136 or VDU 2146. During vertical flyblack the data for picture tube alignment is transmitted via this bus data (see section 2.6.). Here the signal is demultiplexed and reconverted to analog signals. Subsequently, they are dematrixed in the RGB matrix together with the Y signal, giving the RGB signals which drive the RGB output amplifiers of the VCU 2136.

2.6. Circuits for Spot–Cutoff Current Adjustment, White Balance Control and Automatic Contrast Setting

During vertical flyback the three spot–cutoff currents of the picture tube's cathodes, the three white currents and the current of the photo sensor are measured and fed via pins 15 to 17 to the ACVP 2205. In this unit, the measured values are sequenced as required, digitized and stored in the IM bus register. The test sequence is determined by the vertical blanking pulse and the color key pulse. The schematic diagram of this circuit is shown in Fig. 2–7.

After being processed in the CCU, the results are transferred to the IM bus register of the ACVP 2205. During vertical blanking the information is transmitted from the ACVP to the VCU 2136. The data is transferred via the C3 signal (pin 28 of ACVP 2205 to pin 20 of VCU 2136), while the clock signal ($f_{cl} = f_{sc}$) is transmitted via C0 (pin 27 of ACVP 2205 to pin 21 of VCU 2136). The data transfer is explained in detail in chapter 2.7 of the VCU 2136 data sheet.

The A/D converter shown in Fig. 2–7 has a relative resolution of 7 bits. The absolute error is below 20% and the conversion time until valid data is obtained is 12 µs.

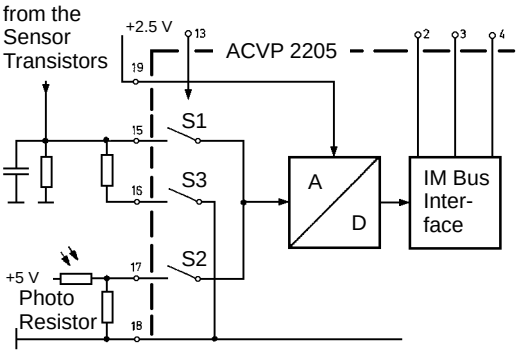


Fig. 2–7: Schematic diagram of the analog multiplexer and A/D converter for spot–cutoff current adjustment, white balance control, and measurement of the photo current.

2.7. Phase Comparator

In a subcarrier–locked system –like DIGIT2000 – the chrominance demodulator is synchronized by the burst signal of the video input. Therefore a PLL is used (see Fig. 2–1 and 2–2).The phase comparator derives the reference signal (color subcarrier burst) from the demodulated color difference signal. This reference signal is already been averaged over two lines. The phase comparators output signal (7–bit) is lowpass filtered and added to an 8–bit adjustment value of the crystal frequency.

The crystal frequency is adjustable via IM bus register. Therefore the PLL has to be disabled (CSS bit 1 reg.12). Thus the color killer is inactive and the PLL output is zero. The VCO contained in the MCU 2600 Clock Generator IC is free–running and can be aligned by varying the register value in address 14. A recommended test pattern for this operation is the color bars signal.

The PLL output signal (pin 25 and 26) is connected to the VCO of the MCU 2600 Clock Generator IC. Fig. 2–8 shows the phase comparator output signal.

Table 2–2: The "switches" S1 to S3 in Fig. 2–7 show the following positions during test sequence

	S1	S2	S3
during vertical sweep	closed	open	closed
during vertical flyback photo current sensing white current sensing spot–cutoff current sensing	 open closed closed	 closed open open	 closed closed open

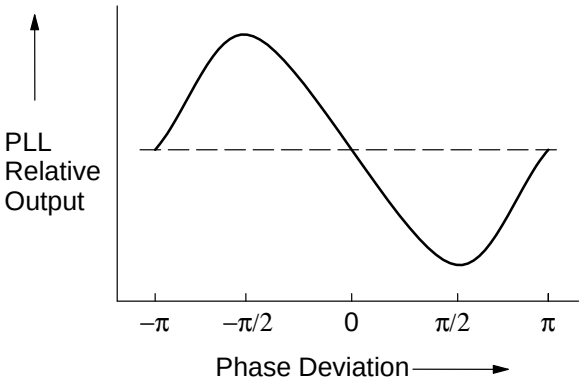


Fig. 2–8: Averaged output signal of the phase comparator

2.8. Standard Selection

Via the VCOS bits in register 14 up to three crystals connected to the MCU 2600 Clock Generator are selectable (e. g. , for PAL, NTSC, SECAM and D2–MAC processing). Table 2–3 shows the bit pattern of the high byte of address 14 and the selected VCO. The preferred standard should be designated to VCO No. 1 caused by the default mode of the MCU (see also MCU 2600 data sheet).

2.9. Dither Adjustment

The resolution of the picture can be improved by enabling the dither function. In this case, the reference voltage of the A/D and D/A inside the VCU 2136 is modified by 1/2 LSB offset every second line. If the combfilter is active, it is recommended to disable the dither. Table 2–4 shows the different settings when the video signal is delayed inside DTI by one line.

In case of 8 bit video input (SAD 2140), it is recommended to disable the described function. Here the picture resolution can be enhanced by activating an additional pulse width modulation of the luminance LSB (APWM – bit, reg. 13).

Table 2–3: Bit pattern of the high–byte of address 14

Selected Standard	Selected VCO No.	Color Subcarrier Frequency MHz	Bit. No. SEC 7	NTSC 6	OUT 3	VCOS 2	1	0
PAL	1	4.4	0	0	1	1	0	0
NTSC	1	4.4	0	1	1	1	0	0
NTSC	2	3.5	0	1	1	0	1	0
SECAM	1	4.4	1	0	1	1	0	0
D2MAC	3	20.25	1	0	0	0	0	1

Table 2–4: Dither adjustment for improved resolution

D2MAC	SEC or S–VHS	CFO	BIT8	BEN	YDAS	YDA	Function
0	0	0	0	0/1	0	0/1	dither off/on
0	0	1	0	0/1	0	0/1	dither on/off
0	1	X	X	0/1	1	0/1	dither on/off
0	X	X	1	X	0	1	dither off
1	0	0	0	0	X	0	dither off
1	0	1	0	1	X	1	dither off
1	1	X	X	1	X	1	dither off
1	X	X	1	X	X	1	dither off

Note: If the DTI is not used, YDAS has to be inverted. D2MAC = digital insertion of the D2MAC signal.

2.10. IM Bus Interface

ACVP 2205 and the CCU 2070 or CCU 3000 communicate via IM bus. The different registers of the ACVP are shown in table 2–5. The CCU has to initialize these registers with the data stored in the MDA 2062, or NVM 3060 EEPROM's (brightness, contrast, peaking etc.)

Table 2–5: IM bus registers of the ACVP 2205

Bit No. / Param. Address	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
11	PK Peaking								YBW	BAA Backlash Adjust						
	16								1	1						
12	⊠								BA Burst Amplitude						CSS Color Subcar. Switch	CMIX Comb–filter Mix
									33						0	0
13	CKL Color Killer LOW–Limit								CKH Color Killer HIGH–Limit						ICR Improved Crosscolor Reduction	APWM Additional PWM
	80								80						0	0
14	SEC Secam	NTSC NTSC/ PAL	⊠	CFR Chrom. Filter Response	OUT Outputs High–Impedan.	VCOS VCO Select 1	2	3	VCOA VCO Adjustment							
	0	0		1	1	4			0							
15	CT Luminance Contrast						CDL Chrom. D. Line Length	SCT SECAM Chrom. Trap	LD Vertical Luminance Delay				CBW Chrom. Bandw.	S–VHS	⊠	YBW2
	40						0	0	0				0	0		0
16	SCS SECM Chrom. Sync.	NIE Noise Invert. Enable	VI2 Video Input2 Select	COB Code Bits R	G	B	BCR Beam Current Reduction		BR Brightness							
	0	0	0				0		127							
17	CR Cut–off Voltage (RED)								WR White Drive (RED)							YDA Lumin. Adder
	127								127							0
18	CG Cut–off Voltage (GREEN)								WG White Drive (GREEN)							BLD Blank. Pulse Disable
	127								127							0
19	CB Cut–off Voltage (BLUE)								WB White Drive (BLUE)							YDAS Lumin. Adder Shift
	127								127							0
20	⊠								WC White Current						DME Disable Measure–ment	DLP Disable LPF
									48						0	0
21	⊠								⊠						CKI Color Killer Ident.	CKA Color Killer Ampl.
22	0	Photo Voltage							0	Leakage Current						
	0	White Current (RED)							1	Cutoff Current (RED)						
	1	White Current (GREEN)							0	Cutoff Current (GREEN)						
	1	White Current (BLUE)							1	Cutoff Current (BLUE)						
	B	Code Bits from ACVP to CCU							A							
23	HSC Hue Correction times Saturation $f_S \cos\alpha$								HSS Hue Correction times Saturation $f_S \sin\alpha$							
	80								0							
27	⊠								RGBC Ext. RGB Contrast						DGD Double Gain Disable	BEN Bit Enlarge.
									32						0	0
140	VCOR	VPK Vertical Peaking			BWIN	CFO	ACRD		BIT8	DVPK	PLLO PLL–Offset					
	1	4			0	0	0		0	0	0					
141	BTRE BLE–Threshold								BTLT BLE–Tiltpoint						BAM BLE–Amount	
	60								6						7	

⊘ = Bits are available in 72 Bit data ACVP to VCU

⊠ = Bits must be set to zero for receive registers and are don't care for transmit registers.

16 Bit register length only, except address 12 and 21 (8 Bit). Typical values are given in decimal.

Table 2–6: IM Bus of the ACVP 2205 for VCU–control

<table>
<tr><th>Parameter Address</th><th>Label</th><th>Bit No. (LSB = 0)</th><th>Default Setting</th><th>Typical Operation Value</th><th>Function</th></tr>
<tr><td>16</td><td>NIE</td><td>14</td><td>–</td><td>0</td><td>Enable S–VHS chroma input
0 = off
1 = on</td></tr>
<tr><td>16</td><td>VI2</td><td>13</td><td>–</td><td>0</td><td>Video input amplitude
0 = Video Input 2 V_{pp}
1 = Video Input 1 V_{pp}</td></tr>
<tr><td>16</td><td>COB</td><td>10–12</td><td>–</td><td>–</td><td>Code bits
Code bits are sent from ACVP to VCU/VDU in 72 bit data transfer corresponding to code bits sent from ACVP to CCU
<table>
<tr><th rowspan="2">A</th><th rowspan="2">B</th><th colspan="3">Code Bits</th></tr>
<tr><th>R</th><th>G</th><th>B</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>16</td><td>BCR</td><td>8, 9</td><td>–</td><td>0</td><td>Select of the beam current reduction
00 = 10% (–20dB)
01 = 30% (–10dB)
10 = 50% (–6dB)
11 = 70% (–3dB)</td></tr>
<tr><td>17</td><td>YDA</td><td>0</td><td>–</td><td>0</td><td>Luminance adder switch
0 = Adding of $^1/_2$ LSB to the output signal of the luminance D/A–converter every 2nd line
1 = no adding
YDA has to be disabled in the D2–MAC mode (see Table 2–4)</td></tr>
<tr><td>18</td><td>BLD</td><td>0</td><td>–</td><td>0</td><td>Blanking pulse disable
0 = Blanking pulse in the analog video output signal is switched on
1 = Blanking pulse is switched off (required for stand–alone application)</td></tr>
<tr><td>19</td><td>YDAS</td><td>0</td><td>–</td><td>1</td><td>Luminance adder shift
0 = no shift
1 = Adding of ¿ LSB to the output signal of the luminance D/A–converter (see YDA) is shifted by 180 degrees (one line, see Table 2–4)</td></tr>
<tr><td>27</td><td>DGD</td><td>1</td><td>–</td><td>0</td><td>Double gain disable of the video input amplifier
0 = double gain
1 = normal gain
In D2–MAC mode normal gain only</td></tr>
<tr><td>27</td><td>BEN</td><td>0</td><td>–</td><td>0</td><td>Bit enlargement
0 = ref.voltage of VCU's A/D–converter altered every 2nd line for $^1/_2$ bit
1 = no alternation
BEN has to be disabled in the D2–MAC mode (see Table 2–4)</td></tr>
<tr><td>140</td><td>BIT8</td><td>7</td><td>0</td><td></td><td>BIT8
0 = 7 bit composite video input (Gray coded)
1 = 8 bit composite video input (Gray coded)</td></tr>
</table>

Table 2–7: IM bus bits for general video processing

Parameter Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
14	SEC	15	0	0	SECAM mode 0 = SECAM off 1 = SECAM on, chroma outputs high–impedance
14	NTSC	14	0	0	NTSC or PAL mode 0 = PAL mode 1 = NTSC mode
14	OUT	11	0	1	Luminance and Chrominance output 0 = high–impedance 1 = outputs active
140	CFO	9	0	0	Disable adaptive combfilter 0 = adaptive combfilter enabled 1 = horizontal filtering (notch/bandpass) enabled

Table 2–8: IM bus bits for luminance processing

Parameter Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
11	PK	8–15	8	16	Horizontal peaking 00000000 = peaking curve 0 00000001 = peaking curve 1 00000010 = peaking curve 2 00000100 = peaking curve 3 00001000 = peaking curve 4 00010000 = peaking curve 5 00100000 = peaking curve 6 01000000 = peaking curve 7 10000000 = peaking curve 8
11	BAA	0–6	0	1	Adjustable coring for horizontal peaking
11	YBW	7	0	1	Luminance bandwidth (see section 4.)
15	YBW2	0	0	0	Luminance bandwidth 2 (see section 4.)
12	CMIX	0	0	0	Combfilter mix 0 = flat frequency response 1 = –6 dB reduction at fsc (see section 4.)
13	APWM	0	0	0	Additional pulsewidth modulation of the luminance LSB 0 = disabled 1 = enabled
15	CT	10–15	32	40	Set of the luminance contrast in 64 steps
15	SCT	8	0	1	Second chrominance trap 0 = on in SECAM 1 = off in SECAM 0 = off in PAL/NTSC 1 = on in PAL/NTSC
15	LD	4–7	4	0	Variable luminance delay time (see Table 2–1)
15	S–VHS	2	0	0	S–VHS switch for chroma data DDS2 or DDS 1 0 = DDS2 normal operation 1 = DDS1 S–VHS operation
16	BR	0–7	–	127	Brightness
20	DLP	0	0	1	Disable broadband LPF for S–VHS and combfilter 0 = LPF enabled 1 = LPF disabled
27	RGBC	2–7	–	32	External RGB contrast

Table 2–8 continued

Parameter Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
140	DVPK	6	0	0	Disable dyn. vertical peaking for improving vertical resolution, if adaptive combfilter is active 0 = dyn. vertical peaking enabled 1 = dyn. vertical peaking disabled
140	VPK	11–14	0	4	Vertical peaking (VPK) is adjustable in 15 steps between 0 and +6 dB. VPK — Multiplication Factor 0 — 0/16 1 — 1/16 2 — 2/16 3 — 3/16 4 — 4/16 5 — 5/16 6 — 6/16 7 — 7/16 8 — 8/16 9 — 9/16 10 — 10/16 11 — 11/16 12 — 12/16 13 — 13/16 14 — 14/16 15 — 15/16 16 — 16/16
140	VCOR	15	0	1	Adjustable coring of vertical peaking 0 = coring off 1 = coring of ”1” LSB
140	BWIN	10	0	0	Size of the active video measuring window for the BLE 0 = 4/3 measuring window 1 = 16/9 measuring window
141	BTRE	9–15	0	60	BLE–Threshold: programmable threshold of the BLE If the measured luminance value (Y_{min}) is greater than 2 · BTRE, the BLE is automatically disabled.
141	BTLT	5–8	0	6	BLE–Tiltpoint: multiplication factor to adjust the active working range and the tiltpoint of the BLE depending on the measured signal difference
141	BAM	0–4	0	7	BLE–Amount: multiplication factor to adjust the amount of BLE

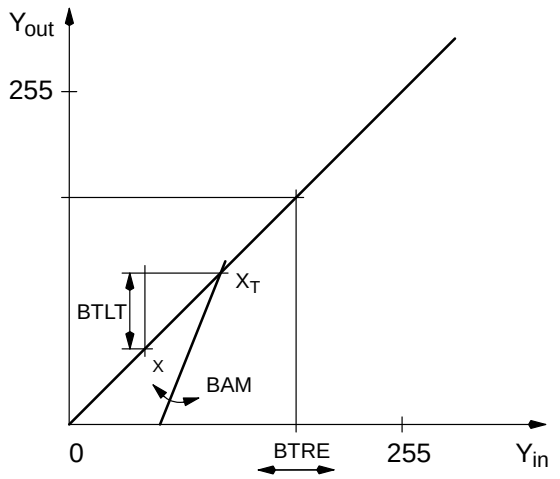


Fig. 2–9: Black–Level–Expander

Table 2–9: IM bus bits for chrominance processing

Parameter Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
12	BA	2–7	32	PAL = 33 NTSC = 22	burst–amplitude reference value
12	CSS	1	0	0	Color subcarrier switch 0 = PLL locked 1 = PLL open
13	CKL	9–15	4	80	color killer low limit
13	CKH	2–7	8	80	color killer high limit
13	ICR	1	0	0	Improved cross color reduction 0 = normal mode 1 = improved mode
14	CFR	12	1	1	Chroma filter response 0 = symmetrical response 1 = asymmetrical response
14	VCOS	8–10	4	4	Select of the MCU's VCO 001 = VCO3 selected 010 = VCO2 selected 100 = VCO1 selected
14	VCOA	0–7	0	–	VCO Adjustment
15	CDL	9	0	0	Chroma delay line length 0 = length for PAL 1 = length for NTSC
15	CBW	3	1	0	Chroma bandwidth 0 = narrow band 1 = broad band
16	SCS	15	–	0	SECAM chroma sync bit 0 = off 1 = chrominance demultiplexer is synchronized every line
21	CKI	1	–	–	Color killer ident
21	CKA	0	–	–	Color killer amplitude, color killer status (CKI,CKA): 00 = killer off 01 = killer on, burst amplitude too low 10 = killer on, no burst sync. 11 = killer on, burst low and no sync
23	HSC	8–15	+64	80	Hue correction times saturation
23	HSS	0–7	+64	0	Hue correction times saturation
140	ACRD	8	0	0	Additional chroma delay 0 = no delay 1 = additional chroma delay active and luma tristate disabled This function is necessary for SAD 2140 only, in case of VCU 21XX ACRD has to be set to 0.
140	PLLO	0–5	0	PAL = –15 NTSC = 0	PLL offset for the correction of analog phase errors in 64 steps (± 32) 0 = no offset PLLO has to be set to "0" in NTSC mode. For the improved phase correction please set 1.) PLLO = 0, CSS = 1, adjust VCOA for min. phase error 2.) Keep VCOA, CSS = 0, adjust PLLO for min. phase error

Table 2–10: IM bus bits for picture alignment

Parameter Address	Label	Bit No. (LSB = 0)	Default Setting	Typical Operation Value	Function
22	–	0–15	–	–	Measured values from A/D–converters in ACVP. The values are defined by code bits (see Table 2–6)
17	CR	8–15	–	127	cutoff voltage for the red beam
17	WR	0–7	–	127	white drive for the red beam
18	CG	8–15	–	127	cutoff voltage for the green beam
18	WG	0–7	–	127	white drive for the green beam
19	CB	8–15	–	127	cutoff voltage for the blue beam
19	WB	0–7	–	127	white drive for the blue beam
20	WC	2–7	0	48	White current sensing voltage, Attention: inverse values are written into the D/A–converter
20	DME	1	0	0	Disable cutoff and white current measurement 0 = measurement enabled 1 = measurement disabled

3. Specifications

3.1. Outline Dimensions

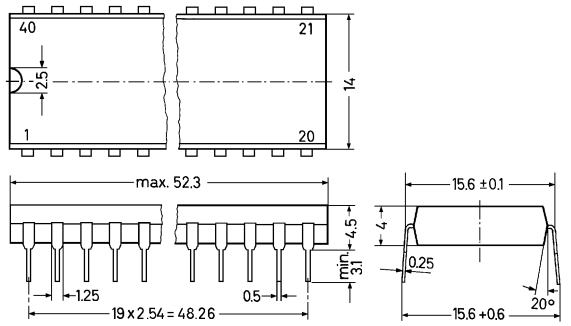


Fig. 3–1:
ACVP 2205 in 40–pin Dil Plastic Package
20 B 40 according to DIN 41 866

Weight approx. 6 g, Dimensions in mm

3.2. Pin Connections

3.2.1. 40–Pin Dil Package

1	Color Key Pulse Input
2	IM Bus Data Input/Output
3	IM Bus Ident Input
4	IM Bus Clock Input
5	V0 Video Input (LSB in case of 7 bit input)
6	V1 Video Input
7	V2 Video Input
8	V3 Video Input
9	V4 Video Input
10	V5 Video Input
11	V6 Video Input (MSB)
12	Leave Vacant
13	Vertical Blanking Pulse Input
14	Outputs Disable Input
15	Beam Current Input
16	Beam Current Switchover Output
17	Photo Sensor Input
18	Ground
19	Reference Voltage Input
20	$\overline{\text{Reset}}$ Input
21	Leave Vacant
22	ΦM Main Clock Input
23	Test Pin, connect to GND
24	V_{SUP}
25	Data Clock Output (PLL)
26	Data Output (PLL)
27	C0 Chroma and Msync Output (LSB)
28	C3 Chroma Output (MSB)
29	C2 Chroma Output
30	C1 Chroma Output
31	Leave Vacant
32	L0 Luma Output (LSB)
33	L1 Luma Output
34	L2 Luma Output
35	L3 Luma Output
36	L4 Luma Output
37	L5 Luma Output
38	L6 Luma Output
39	L7 Luma Output (MSB)
40	V_1 Video Input (LSB in case of 8 bit input)

3.3. Pin Descriptions

Pin 1 – Color Key Pulse Input
Via this pin, the ACVP 2205 gets the color key pulse from pin 19 of the DPU 2553. The signal is active at low level. The input configuration is shown in Fig. 3–2 .

Pins 2 to 4 – IM Bus Connections
By means of these pins, the ACVP 2205 is linked with the CCU 2070 or CCU 3000. Pins 3 (Ident Input) and 4 (Clock Input) are configured as shown in Fig. 3–2 Pin 2 (Data Input/Output) is shown in Fig. 3–7.

Pins 5 to 11, 40 – Video Inputs V0 to V6 and V_1
The circuit of these inputs is shown in Fig. 3–3. Via these inputs, the ACVP 2205 receives the digitized composite video signal from the VCU 2136 (7–bit) or SAD 2140 (8–bit). Input V0 is the least significant bit (LSB) and input V6 the most significant bit (MSB) in 7–bit mode, while input V_1 is the least significant bit (LSB) and input V6 the most significant bit (MSB) in 8–bit mode. In case of 7–bit mode pin 40 has to be connected to ground.

Pin 13 – Vertical Blanking Pulse Input
Fig. 3–2 shows the diagram of this input. Via this pin the ACVP 2205 receives the vertical blanking pulse from the DPU 2553. In the steady state, high level must be applied, and during pulse a low level. The vertical blanking pulse is required for controlling the tests described in section 2.6., which are carried out during vertical flyback.

Pin 14 – Outputs Disable Input
This input (Fig. 3–2) serves for fast switchover of the luma and chroma outputs (Pin 27 to 30 and 32 to 39) to the high impedance state. Pin 14 low means outputs active, and Pin 14 high means outputs disabled.

Pin 15 – Beam Current Input
By means of this pin, whose circuit is shown in Fig. 3–4, the ACVP 2205 receives the common analog signal which is supplied by three current sensing transistors inserted in the cathode lines of the picture tube. Via the internal switch S1 (Fig.2–7) the analog signal is fed to the internal A/D converter. Input voltage range is 0 V to V_{REF}.

Pin 16 – Beam Current Switchover Output
This pin serves for selecting the sensitivity of the beam current input pin 15 by connecting an additional 10 kΩ resistor parallel to pin 15 and ground, thus reducing this input's sensitivity. By this means, the current supplied by the three sensor transistors mentioned is the spot–cutoff current on the one hand (high sensitivity) and the white level current on the other (low sensitivity). The circuit of pin 16 is shown in Fig. 3–5.

Pin 17 – Photo Sensor Input
This input has the same properties as pin 15. It serves for measuring the current supplied by the photo sensor and is activated by switch S2 (Fig. 2–7). It's input voltage range is also 0 V to V_{REF}.

Pin 18 – Ground
This pin has to be connected to ground. The decoupling capacitor of the ACVP 2205 has to be connected between pin 24 and pin 18.

Pin 19 – Reference Voltage Input
This pin gets the externally–produced reference voltage of half the supply voltage, that is required by the circuitry shown in Fig. 2–7 and must be filtered by a capacitor of sufficient capacity.

Pin 20 – $\overline{\text{Reset}}$ Input
This pin's circuit is shown in Fig. 3–2. In the steady state, high level is required. A low level normalizes the ACVP 2205.

Pin 22 – ΦM Main Clock Input
Via this pin the ACVP 2205 is supplied with the required main clock signal of 17.7 MHz for PAL and SECAM, 14.3 MHz for NTSC, and 20.25 MHz for D2–MAC operation by the MCU 2600 Clock Generator IC. Fig. 3–6 shows the diagram of pin 22.

Pin 23 – Test Pin
This pin must be connected to ground.

Pin 24 – Supply Voltage, +5 V
This pin must be connected to +5 V supply voltage.

Pin 25 – Data Clock Output (PLL)
This pin whose diagram is shown in Fig. 3–5 supplies the data clock signal needed for the serial data transfer of the PLL information from the phase comparator contained in the ACVP 2205 to the voltage–controlled oscillator (VCO) contained in the MCU 2600 Clock Generator IC. The frequency of the data clock signal is one fourth of the main clock's frequency.

Pin 26 – Data Output (PLL)
This pin whose diagram is shown in Fig. 3–5 supplies the 12–bit data word explained in section 2.7. and in Fig. 2–4 (the latter contained in the description of the MCU 2600 Clock Generator IC), which serves for closing the PLL circuit which determines the main clock signal used in the DIGIT 2000 TV receiver.

Pins 27 to 30 – Chroma Outputs C3 to C0
These outputs' configuration is shown in Fig. 3–5 Via these pins, the R–Y, B–Y and picture tube alignment data is transferred in multiplex operation to the VCU 2136.

Pins 32 to 39 – Luma Outputs L0 to L7
These outputs are identical to pin 27, too. Via these pins, the ACVP 2205 delivers the digital luminance signal (Y) to the VCU 2136 where it is reconverted to an analog signal.

3.4. Pin Circuits

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter "E" means enhancement, the letter "D" depletion.

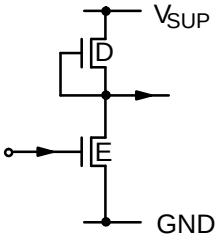


Fig. 3–2:
Input Pins 1, 3, 4, 13, 14

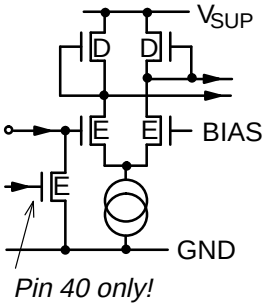


Fig. 3–3:
Input Pins 5 to 11, 40

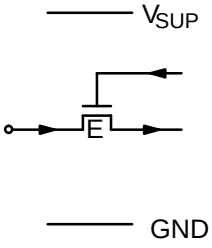


Fig. 3–4:
Input Pins 15 to 17

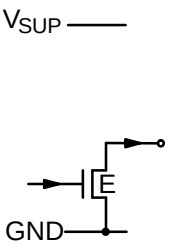


Fig. 3–5:
Output Pins 16, 25 to 30 and 32 to 39

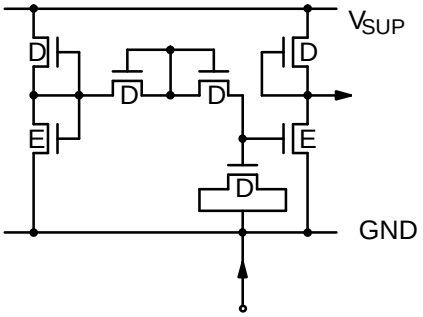


Fig. 3–6:
Input Pin 22

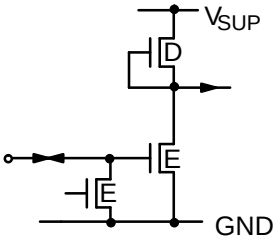


Fig. 3–7:
Input/Output Pin 2

3.5. Electrical Characteristics

All voltages are referred to pins 18 and 21.

3.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
V_{SUP}	Supply Voltage	24	0	6	V
I_O	Output Current, all Outputs	2, 16, 25 to 30, 32 to 39	0	10	mA
V_O	Output Voltage, all Outputs	2, 16, 25 to 30, 32 to 39	–0.3 V	V_{SUP}	–
V_I	Input Voltage, all Inputs	1 to 11, 13 to 15, 17, 22, 40	–0.3 V	V_{SUP}	–
T_A	Ambient Operating Temperature	–	0	+65	°C
T_S	Storage Temperature	–	–40	+125	°C

3.5.2. Recommended Operating Conditions in connection with the CCU 2070, or CCU 3000, VCU 2136, DPU 2553 and MCU 2600

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	24	4.75	5.0	5.25	V
V_{REF}	Reference Input Voltage	19	–	2.5	–	V
V_{BCI}	Beam Current Input Voltage	15	0	–	V_{REF}	–
V_{PSI}	Photo Sensor Input Voltage	17	0	–	V_{REF}	–
V_{INH}	Input Voltage High Level	1, 2, 3, 4, 13, 14, 20	2.4	–	–	V
V_{INL}	Input Voltage Low Level		–	–	0.8	V
V_{VIH}	Video Input High Voltage	5 to 11, 40	$V_{SUP}/2$ +0.3 V	–	–	V
V_{VIL}	Video Input Low Voltage		–	–	$V_{SUP}/2$ –0.3 V	V
$V_{\Phi MIAC}$	ΦM Clock Input A.C. Voltage (p–p)	22	0.8	–	2.5	V
$V_{\Phi MIDC}$	ΦM Clock Input D.C. Voltage		1.5	–	3.5	V
$f_{\Phi M}$	Clock Frequency for PAL and SECAM for NTSC for D2–MAC		 – – –	 17.734475 14.31818 20.25	 – – –	 MHz MHz MHz

3.5.3. Characteristics at V_{SUP} = 5 V, V_{REF} = 2.5 V, $f_{\Phi M}$ = 17.734 MHz, T_A = 25°C

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUP}	Current Consumption	24	–	230	290	mA	
C_i	Input Capacitance	22	–	10	–	pF	
V_O	Output Voltage Low Level	2	–	–	0.4	V	I_O = 3 mA
V_O	Output Voltages Low Level	25 to 30, 32 to 39	–	–	0.3	V	I_O = 6 mA
I_O	Output Leakage Currents	2, 16, 25 to 30, 32 to 39	–	–	10	µA	V_O = 5 mA
I_I	Input Leakage Currents	1, 3, 4, 5 to 11, 13, 14, 20, 22, 23	–	–	100	nA	
R_{on}	On Resistance of the Open–Drain Transistor	16	–	1	–	kOhm	I_O = 0.2 mA

The A/D converter for the analog signals fed to pins 15 and 17 has a 7–bit output signal which starts at 0 0 0 0 0 0 0 for V_I = 0 and ends with 1 1 1 1 1 1 1 for $V_I = V_{REF}$, whereby a certain linearity error and an offset of 5% are possible.

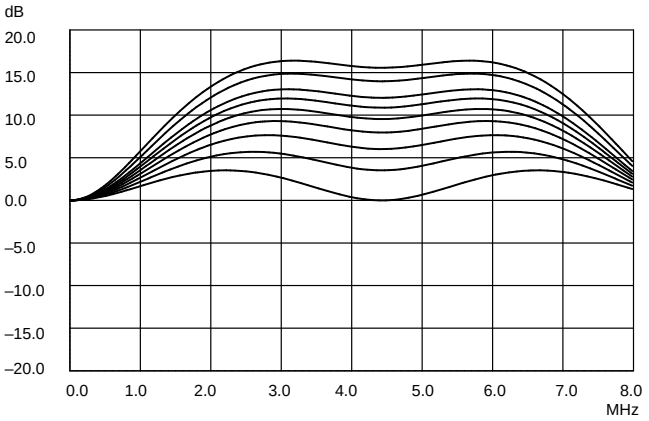
Color Killer Setting Range:
The 0 dB value corresponds to a burst amplitude of 500 mV (p–p). Via address 13, the range of the color killer can be chosen as follows

Killer Level	Value (Decimal)
0 to – 6 dB	16 to 31
– 6 to –12 dB	32 to 47
–12 to –18 dB	48 to 63
–18 to –24 dB	63 to 79
–24 to –30 dB	80 to 95

The decimal values also depend on the setting of the ACC level which is set by address 12. ACC level setting is recommended to be 34 for PAL and 22 for NTSC.

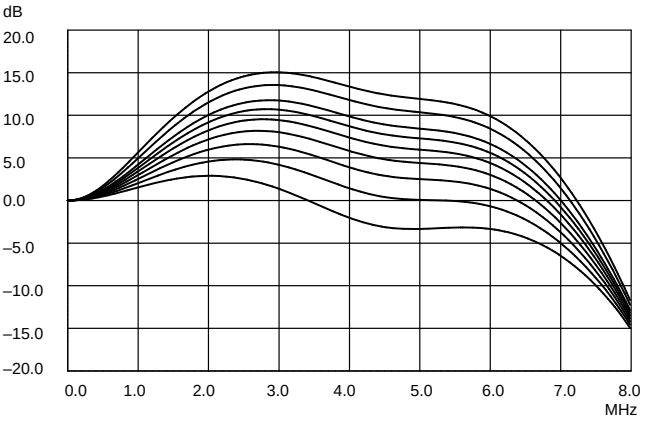
4. Luminance Frequency Responses

4.1. Frequency Responses for Combfilter–on and S–VHS



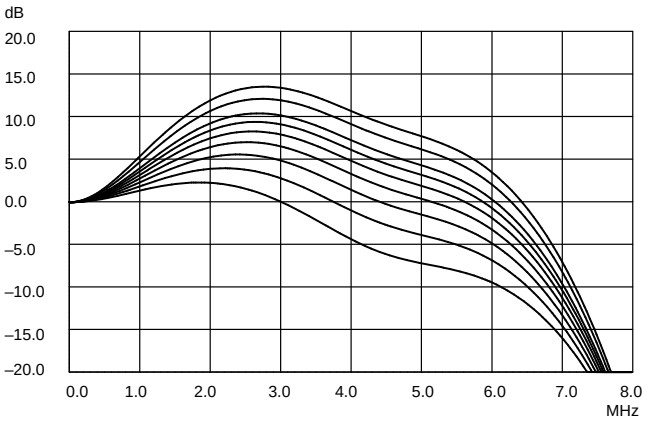
YBW2	YBW	SEC	S–VHS	CFO	DLP	CMIX	
15	11	14	15	140	20	12	ADDR.
0	7	15	2	9	0	0	BIT
							Mode
0	1	0	0	0	1	0	PAL Combfilter
1	1	0	1	X	1	X	S–VHS PAL
1	1	1	1	X	1	X	S–VHS SECAM

a)



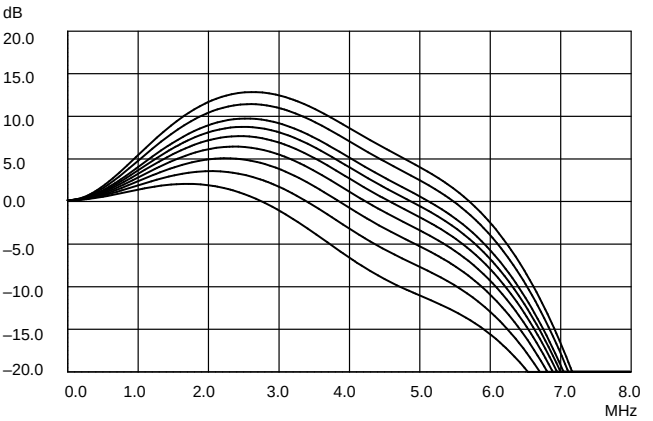
YBW2	YBW	SEC	S–VHS	CFO	DLP	CMIX	
15	11	14	15	140	20	12	ADDR.
0	7	15	2	9	0	0	BIT
							Mode
0	1	0	0	0	0	0	PAL Combfilter
1	1	0	1	X	0	X	S–VHS PAL
1	1	1	1	X	0	X	S–VHS SECAM

c)



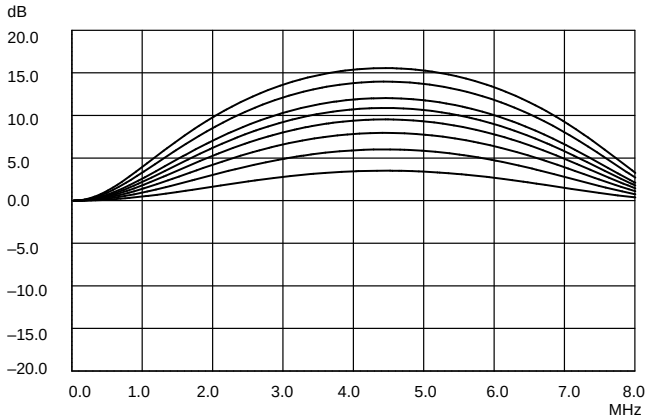
YBW2	YBW	SEC	S–VHS	CFO	DLP	CMIX	
15	11	14	15	140	20	12	ADDR.
0	7	15	2	9	0	0	BIT
							Mode
0	1	0	0	0	1	1	PAL Combfilter

b)



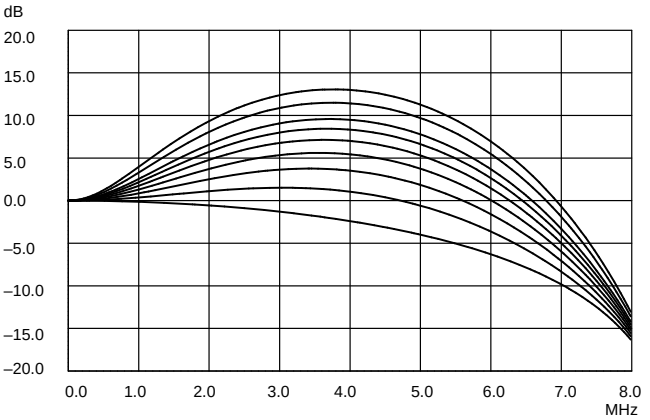
YBW2	YBW	SEC	S–VHS	CFO	DLP	CMIX	
15	11	14	15	140	20	12	ADDR.
0	7	15	2	9	0	0	BIT
							Mode
0	1	0	0	0	0	1	PAL Combfilter

d)



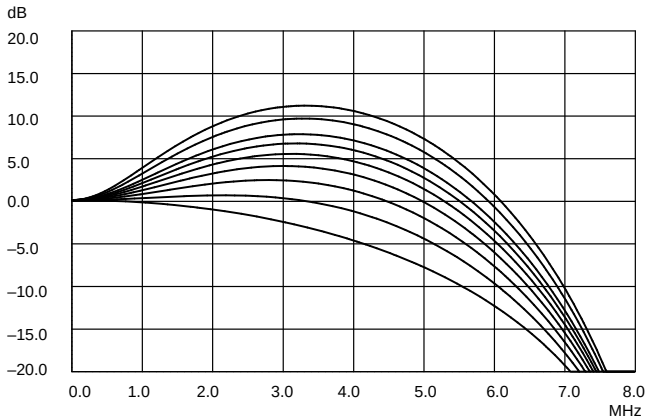
YBW2	YBW	SEC	S–VHS	CFO	DLP	CMIX	
15	11	14	15	140	20	12	ADDR.
0	7	15	2	9	0	0	BIT
							Mode
1	1	0	0	0	1	0	PAL Combfilter
0	1	0	1	X	1	X	S–VHS PAL
0	1	1	1	X	1	X	S–VHS SECAM

e)



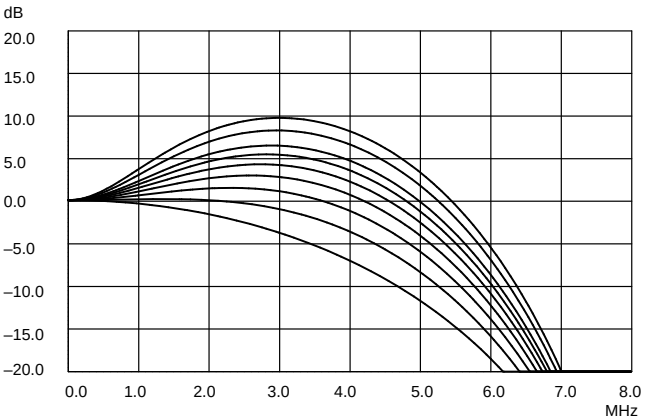
YBW2	YBW	SEC	S–VHS	CFO	DLP	CMIX	
15	11	14	15	140	20	12	ADDR.
0	7	15	2	9	0	0	BIT
							Mode
1	1	0	0	0	0	0	PAL Combfilter
0	1	0	1	X	0	X	S–VHS PAL
0	1	1	1	X	0	X	S–VHS SECAM

g)



YBW2	YBW	SEC	S–VHS	CFO	DLP	CMIX	
15	11	14	15	140	20	12	ADDR.
0	7	15	2	9	0	0	BIT
							Mode
1	1	0	0	0	1	1	PAL Combfilter

f)

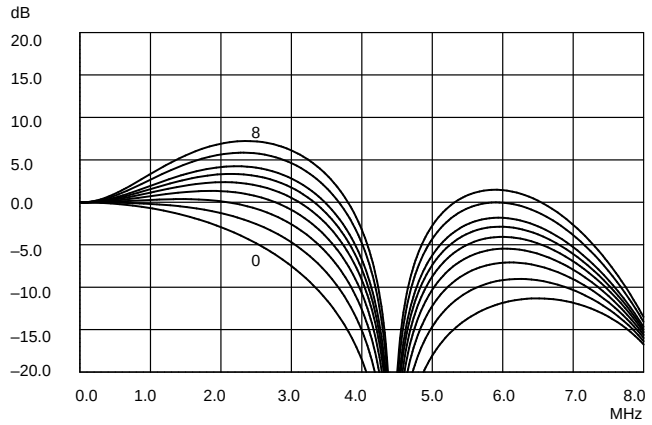


YBW2	YBW	SEC	S–VHS	CFO	DLP	CMIX	
15	11	14	15	140	20	12	ADDR.
0	7	15	2	9	0	0	BIT
							Mode
1	1	0	0	0	0	1	PAL Combfilter

h)

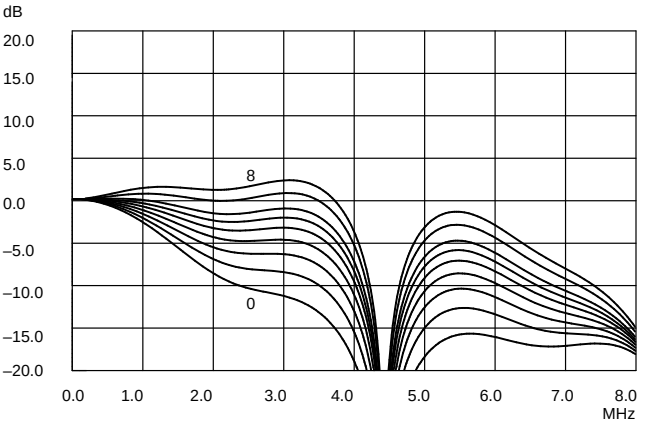
4.2. Frequency Responses for SECAM or Combfilter–off Mode

(For the following frequency responses S–VHS =0, CFO = 1, and DLP = 0.)



	YBW	YBW2	SEC	SCT		
ADDR.	11	15	14	15	No. of	TV
BIT	7	0	15	8	traps	Mode
	1	0	0	0	1	PAL
	1	0	1	1	1	SECAM

a)



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ADDR.	11	15	14	15	No. of	TV
BIT	7	0	15	8	traps	Mode
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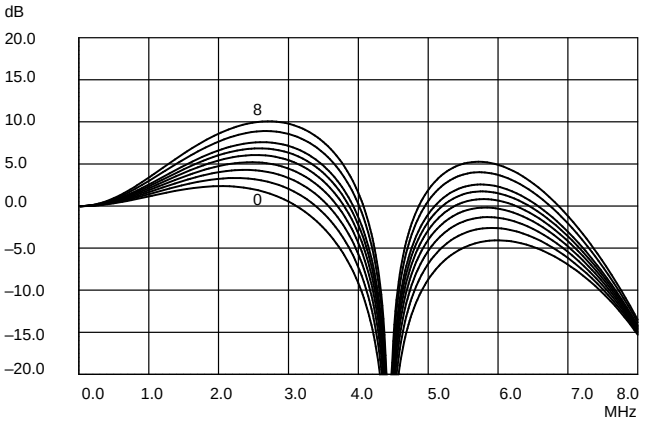
	1	1	1	1	1	SECAM

c)



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BIT	7	0	15	8	traps	Mode
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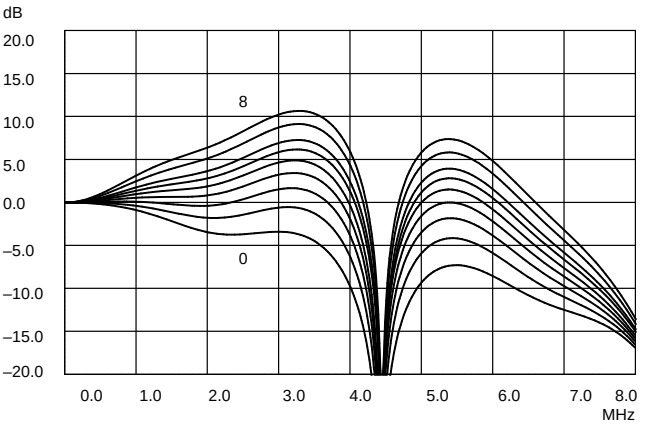
b)



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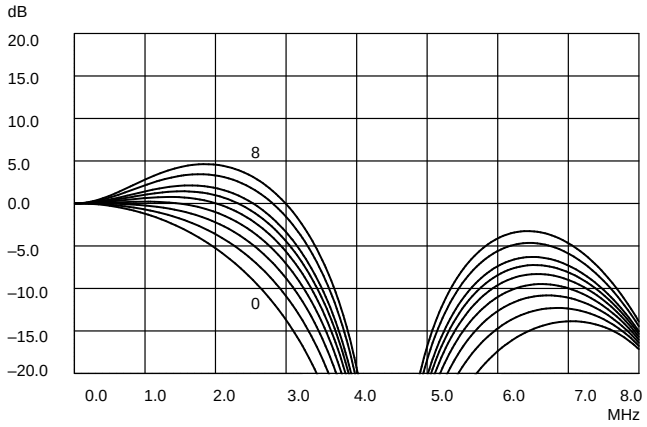
d)



	YBW	YBW2	SEC	SCT		
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BIT	7	0	15	8	traps	Mode
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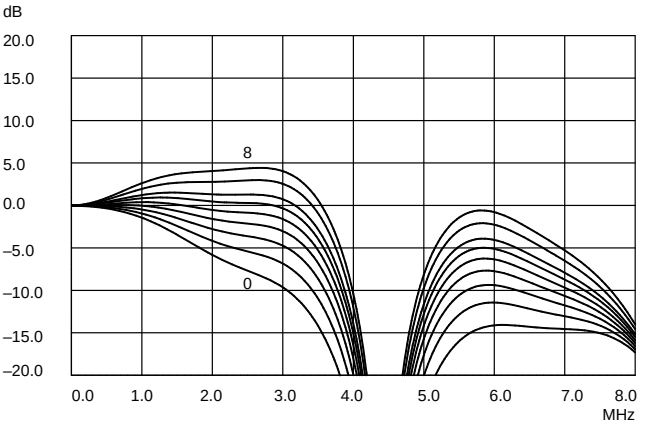
e)



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BIT	7	0	15	8	traps	Mode
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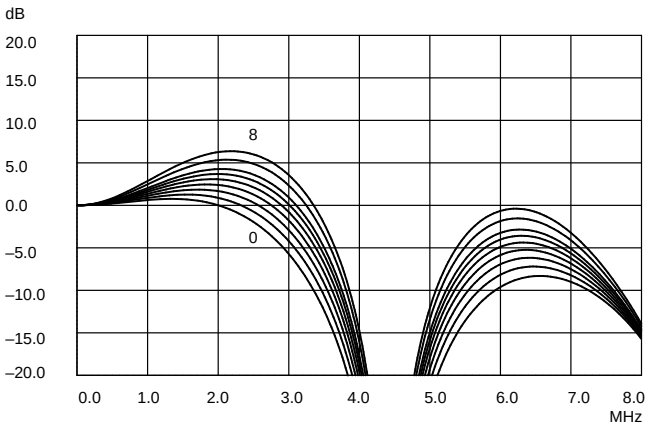
g)



	YBW	YBW2	SEC	SCT		
ADDR.	11	15	14	15	No. of	TV
BIT	7	0	15	8	traps	Mode
	0	1	1	0	2	SECAM

f)

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