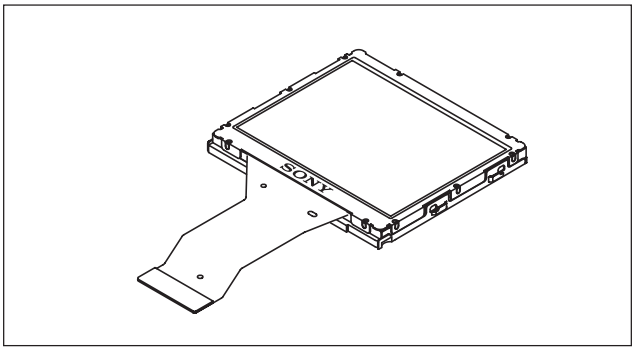
SONY

ACX306BKU

3.86cm (1.5-type) NTSC/PAL Color LCD Panel Module with LED Backlight



Description

The ACX306BKU is an LCD panel module with LED backlight developed exclusively for the ACX306BKU 3.86cm diagonal active matrix TFT-LCD panel addressed by low temperature polycrystalline silicon transistors with built-in peripheral driving circuitry.

This module provides full-color representation for NTSC and PAL systems. In addition, RGB dots are arranged in a delta pattern that provides smooth picture quality without fixed color patterns compared to vertical stripe and mosaic patterns.

Features

- Total module thickness: 3.09mm (typ.) ultra-thin type, narrow frame
- Low voltage, low power consumption: 12V drive, 43mW (panel block, typ.)
- Number of active dots: 118,000 dots, 3.86cm (1.5-type) in diagonal
- Center luminance Standard mode: 170cd/m^2 (backlight 144mW typ.)
  High luminance mode: 200cd/m^2 (backlight 185mW typ.)
- Horizontal resolution: 240 TV lines
- Optical transmittance: 7.5% (typ.)
- High contrast ratio with normally white mode: 200 (typ.)
- Built-in H and V driving circuitry (built-in input level conversion circuit, 3V drive possible)
- Smooth pictures with a RGB delta arrangement
- Supports NTSC/PAL
- Built-in picture quality improvement circuit
- Up/down and/or right/left inverse display function
- Dirt-resistant surface treatment

Element Structure

- Active matrix TFT-LCD panel with built-in peripheral driving circuitry using low temperature polycrystalline silicon transistors
- Number of pixels
  - Total number of dots: 494 (H) × 242 (V) = 119,548
  - Number of active dots: 490 (H) × 240 (V) = 117,600
- Module dimensions
  - Package dimensions: 37.0 (W) × 31.94 (D) × 3.09 (H) (mm)
  - Effective display dimensions: 31.115 (H) × 22.86 (V) (mm)

Applications

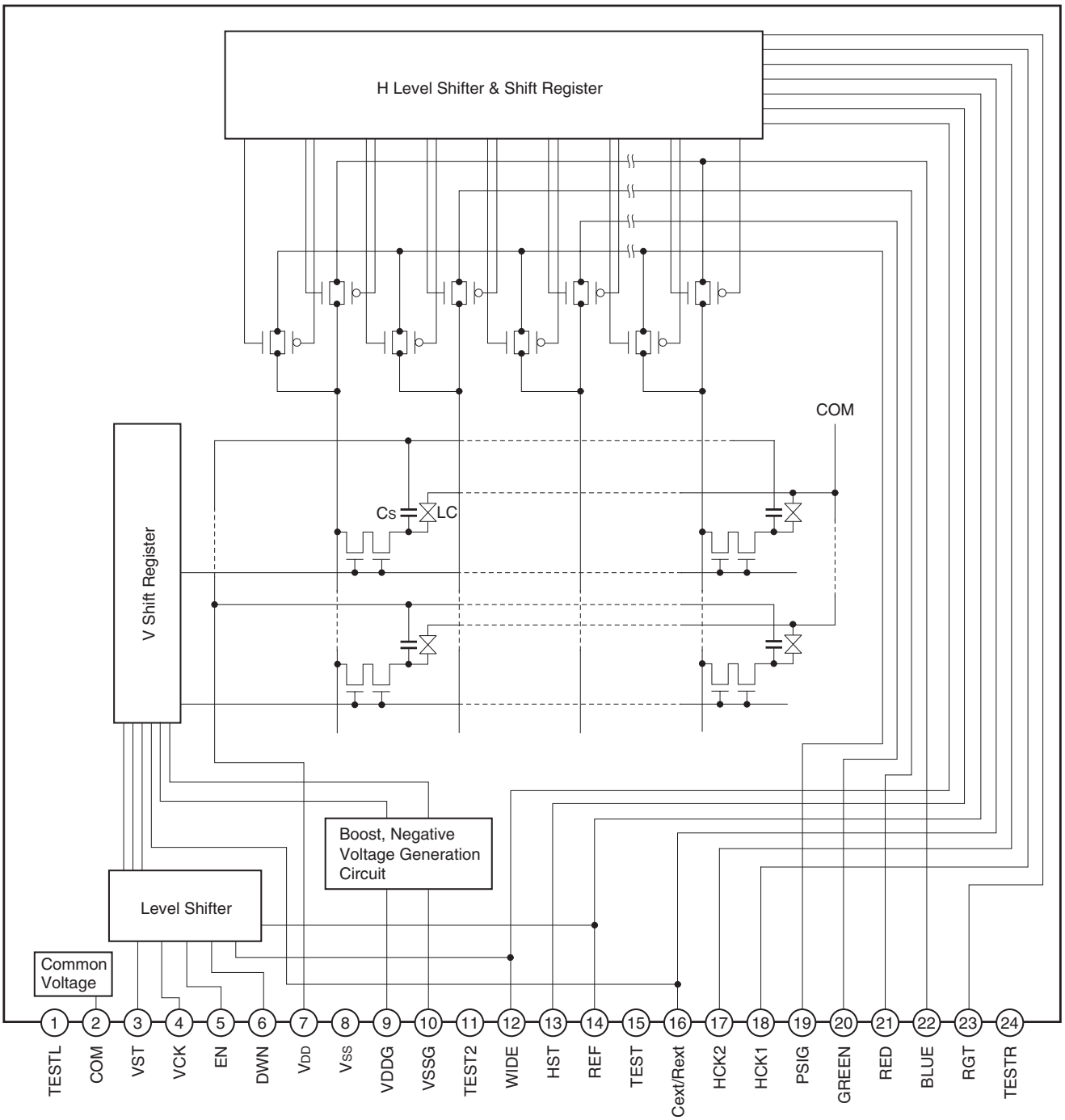
Digital still cameras

E03654-PS

Module Configuration

Panel Block Diagram

The panel block diagram is shown below.



Absolute Maximum Ratings (V_{SS} = 0V)

• H driver supply voltage	V_{DD}, Cext/Rext	–1.0 to +17	V
• V driver boost supply voltage	VDDG	V_{DD} – 1.0 to +18	V
• V driver negative supply voltage	VSSG	–3.0 to +1.0	V
• Common voltage of panel	COM	–1.0 to +17	V
• H driver input pin voltage	HST, HCK1, HCK2, RGT, WIDE	–1.0 to +17	V
• V driver input pin voltage	VST, VCK, EN, DWN, REF	–1.0 to +15	V
• Video signal, uniformity improvement signal input pin voltage	GREEN, RED, BLUE, PSIG	–1.0 to +13	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–30 to +85	°C
• LED backlight DC forward current	Ifbl	30	mA
• LED backlight reverse withstand voltage	Vrbl	0	V

Operating Conditions of Panel Block

1. Input/output supply voltage conditions*1 (V_{SS} = 0V)

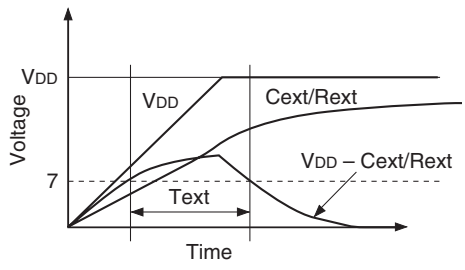
Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	11.4	12.0	12.6	V
	Cext/Rext*2	V_{DD} – 3.4	12.0	—	V
VDDG output voltage setting	VDDG	14.0	15.0	16.3	V
VSSG output voltage setting*3	VSSG	–2.3	–1.8	–1.5	V
Resistor connected to Cext/Rext pin*2	Rext	—	10	160	kΩ

*1 The V_{DD} typical voltage setting is noted as 12.0V in the above table.

*2 Connect the resistor and capacitor to the Cext/Rext pin as shown in the figure below. The Cext/Rext value differs according to the rising time of the panel supply voltage.

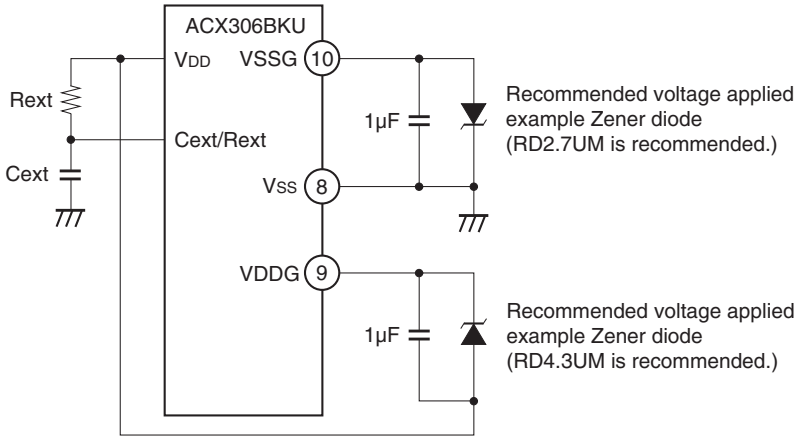
*3 For the VDDG, VSSG output setting, connect an external smoothing capacitor and a voltage stabilizing Zener diode as shown in the figure below.

Cext/Rext constant setting conditions



Set a Cext value that satisfies Text > 1ms during V_{DD} – Cext/Rext > 7V.

Recommended voltage applied example
IDD measurement circuit diagram



2. Panel input signal voltage conditions

Item		Symbol	Min.	Typ.	Max.	Unit
H/V driver input voltage	(Low)	VIL	–0.3	0.0	0.3	V
	(High)	VIH	2.6	3.0	5.5	V
REF input voltage		VREF	VIH/2 – 0.3	VIH/2	VIH/2 + 0.3	V
Video signal center voltage*4		VVC	5.8	6.0	6.2	V
Video signal input range*4		Vsig	1.5	VVC ± 4.0	VDDG – 4.0 (however, 10.5V or less)	V
Uniformity improvement signal*4		Vpsig	VVC ± 2.3	VVC ± 2.5	VVC ± 2.7	V
Common voltage of panel (Ta = 25°C)		VCOM	VVC – 0.6	VVC – 0.5	VVC – 0.4	V

*4 Input video and uniformity improvement signals should be input with the voltage amplitude symmetrical to VVC as shown in Fig. 1.

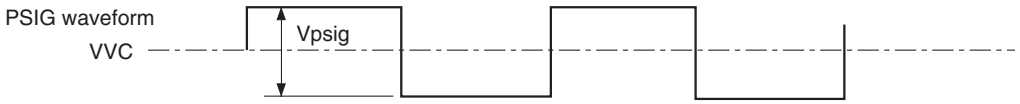


Fig. 1

Operating Conditions of Backlight Block

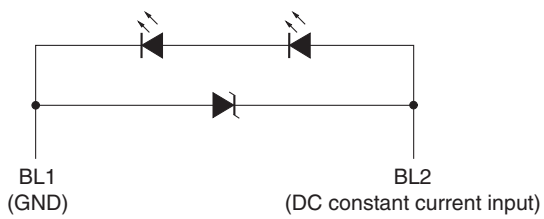
1. Input/output supply voltage conditions

Standard mode: luminance 170cd/m^2 operation

Item	Symbol	Min.	Typ.	Max.	Unit
Backlight DC forward current	IfBL	—	20	—	mA
Backlight DC forward voltage	$Vfbl_{20}$	6.4	7.2	8.0	V
Backlight power consumption	Pbl_{20}	128	144	160	mW

High luminance mode: luminance 200cd/m^2 operation

Item	Symbol	Min.	Typ.	Max.	Unit
Backlight DC forward current	IfBL	—	25	—	mA
Backlight DC forward voltage	$Vfbl_{25}$	6.6	7.4	8.2	V
Backlight power consumption	Pbl_{25}	165	185	205	mW



Backlight equivalent circuit

Pin Description of Panel Block

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	TESTL	Panel test output; no connection	13	HST	Start pulse input for H shift register drive
2	COM	Common voltage input of panel	14	REF	Level shifter circuit REF voltage input
3	VST	Start pulse input for V shift register drive	15	TEST	Panel test output; no connection
4	VCK	Clock input for V shift register drive	16	Cext/ Rext	Time constant power supply input for H shift register drive
5	EN	Gate selection pulse enable input	17	HCK2	Clock input for H shift register drive
6	DWN	V shift register drive direction signal input	18	HCK1	Clock input for H shift register drive
7	V_{DD}	Power supply input for H and V driver	19	PSIG	Uniformity improvement signal input
8	V_{SS}	H and V driver GND	20	GREEN	Video signal (G) input to panel
9	VDDG	Boost power supply setting for V driver	21	RED	Video signal (R) input to panel
10	VSSG	Negative power supply setting for V driver	22	BLUE	Video signal (B) input to panel
11	TEST2	No connection inside the panel. (with 1MΩ terminating resistor)	23	RGT	H shift register drive direction signal input
12	WIDE	Uniformity improvement signal control pulse input	24	TESTR	Panel test output; no connection

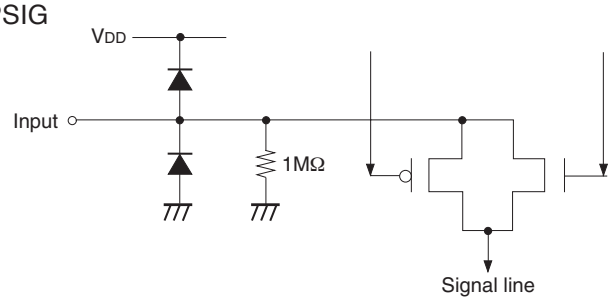
Pin Description of Backlight Block

Pin No.	Symbol	Description
1	BL1	Power supply GND for backlight lighting
2	BL2	Power supply input for backlight lighting

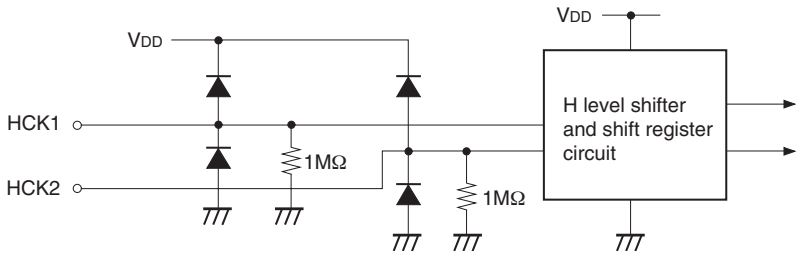
Input Equivalent Circuits of Panel Block

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal input pins. All pins are connected to VSS with a high resistance of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistor value: typ.)

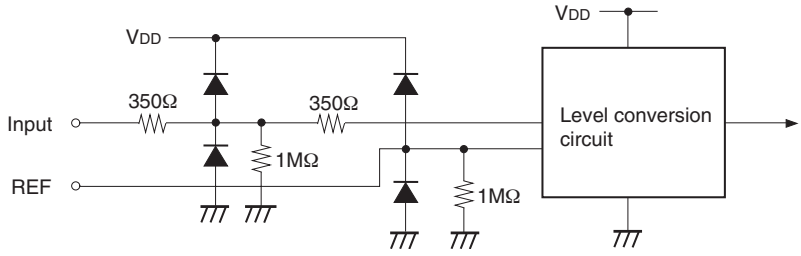
(1) RED, GREEN, BLUE, PSIG



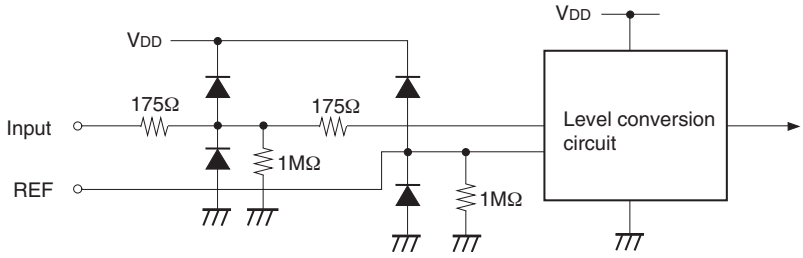
(2) HCK1, HCK2



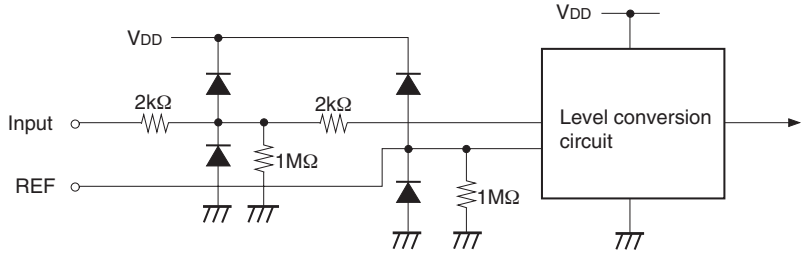
(3) WIDE, REF



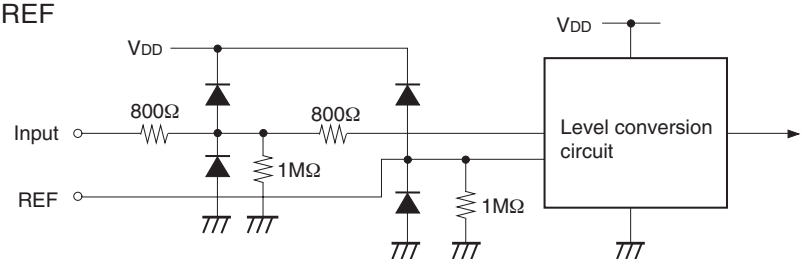
(4) HST



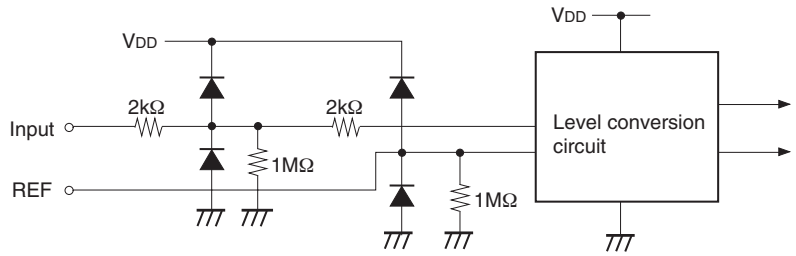
(5) RGT, REF



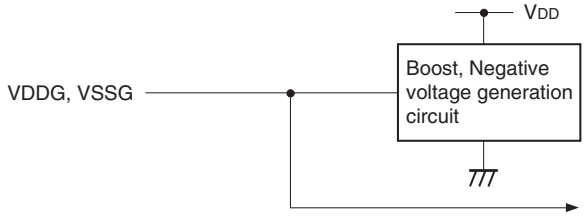
(6) VST, VCK, EN, REF



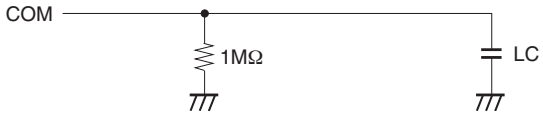
(7) DWN, REF



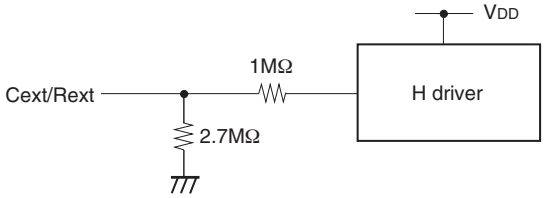
(8) VDDG, VSSG



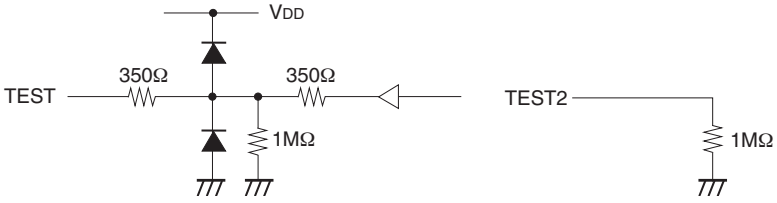
(9) COM



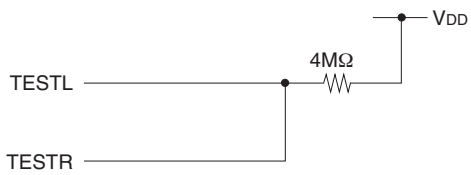
(10) Cext/Rext



(11) TEST/TEST2



(12) TESTL, TESTR

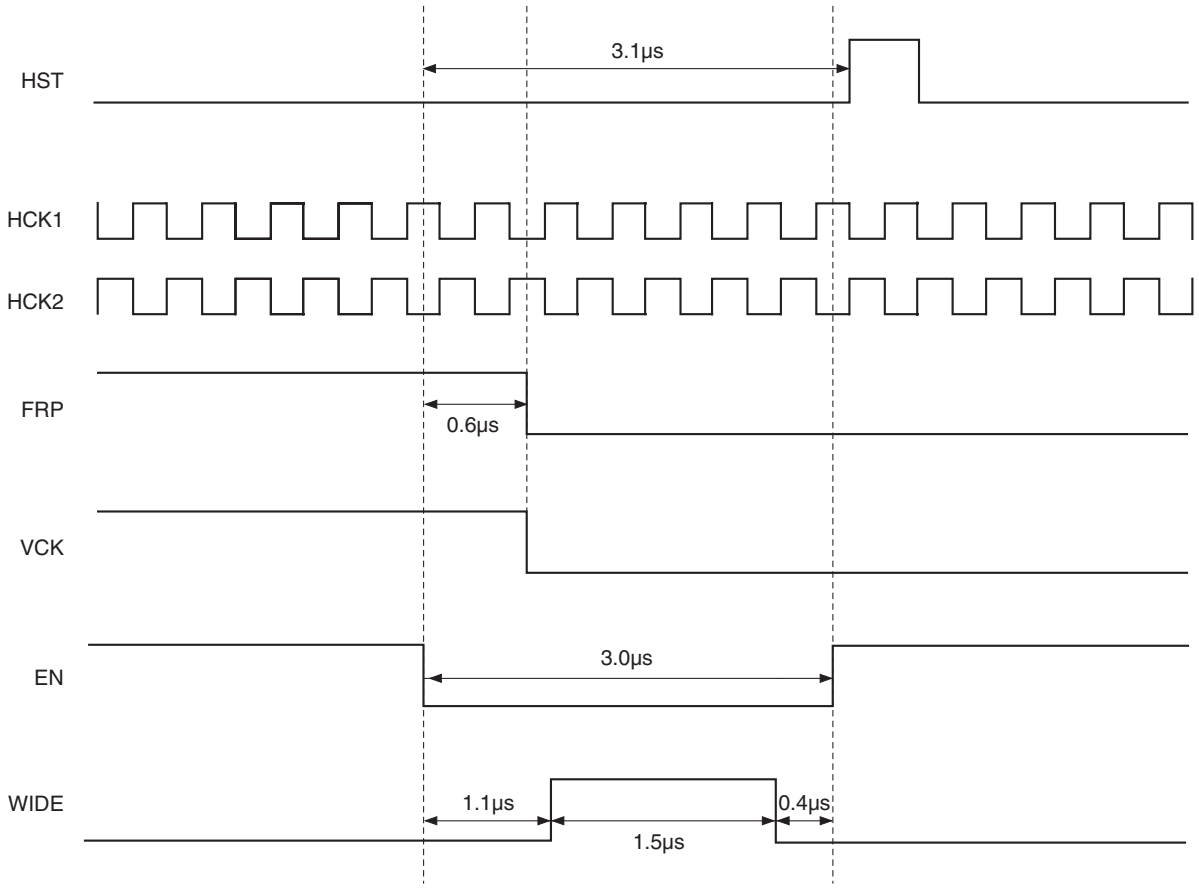


Clock Timing Conditions of Panel Block (VIH = 3.0V, V_{DD} = 12V, Ta = 25°C)

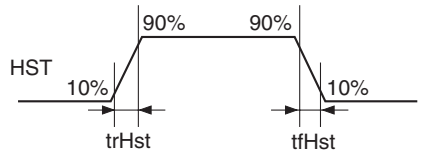
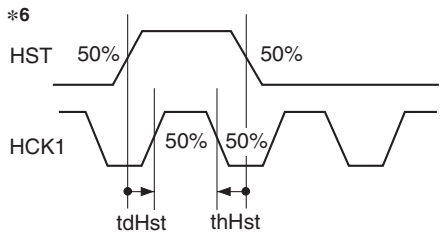
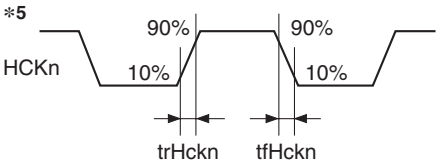
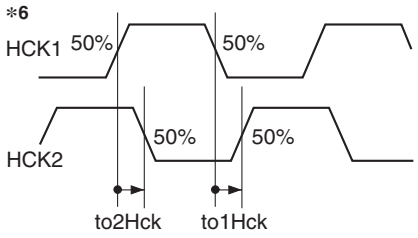
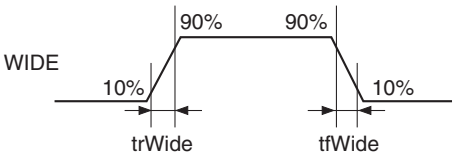
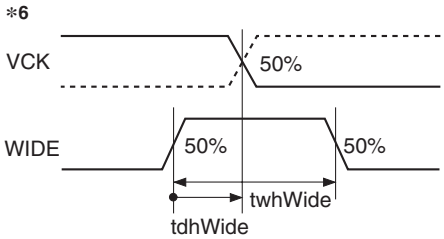
	Item	Symbol	Min.	Typ.	Max.	Unit
HST	HST rise time	trHst	—	—	30	ns
	HST fall time	tfHst	—	—	30	
	HST data setup time	tdHst	300	333	363	
	HST data hold time	thHst	–30	0	30	
HCK	HCKn*5 rise time	trHckn	—	—	30	
	HCKn*5 fall time	tfHckn	—	—	30	
	HCK1 fall to HCK2 rise time	to1Hck	–15	0	15	
	HCK1 rise to HCK2 fall time	to2Hck	–15	0	15	
VST	VST rise time	trVst	—	—	100	
	VST fall time	tfVst	—	—	100	
	VST data setup time	tdVst	30	32	34	µs
	VST data hold time	thVst	–34	–32	–30	
VCK	VCK rise time	trVck	—	—	100	ns
	VCK fall time	tfVck	—	—	100	
EN	EN rise time	trEn	—	—	100	
	EN fall time	tfEn	—	—	100	
	EN fall to VCK rise/fall time	tdEn	500	600	700	
	EN pulse width	twEn	2900	3000	3100	
WIDE	WIDE rise time	trWide	—	—	100	
	WIDE fall time	tfWide	—	—	100	
	WIDE (H) rise to VCK rise/fall time	tdhWide	–0.4	–0.5	–0.6	µs
	WIDE (H) pulse width	twhWide	1.4	1.5	1.6	

*5 HCKn means HCK1 and HCK2. (fHCKn = 1.5MHz)

Horizontal Standard Timing



<Horizontal Shift Register Driving Waveforms>

Item		Symbol	Waveform	Conditions
HST	HST rise time	trHst		• HCKn*5 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	HST fall time	tfHst		
	HST data setup time	tdHst		• HCKn*5 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	HST data hold time	thHst		
HCK	HCKn*5 rise time	trHckn		• HCKn*5 duty cycle 50% to1Hck = 0ns to2Hck = 0ns tdHst = 333ns thHst = 0ns
	HCKn*5 fall time	tfHckn		
	HCK1 fall to HCK2 rise time	to1Hck		• tdHst = 333ns thHst = 0ns
	HCK1 rise to HCK2 fall time	to2Hck		
*7 WIDE	WIDE rise time	trWide		
	WIDE fall time	tfWide		
	WIDE rise to VCK rise/fall time	tdhWide		
	WIDE pulse width	twhWide		

*6 Definitions:

The right-pointing arrow (•→) means +.

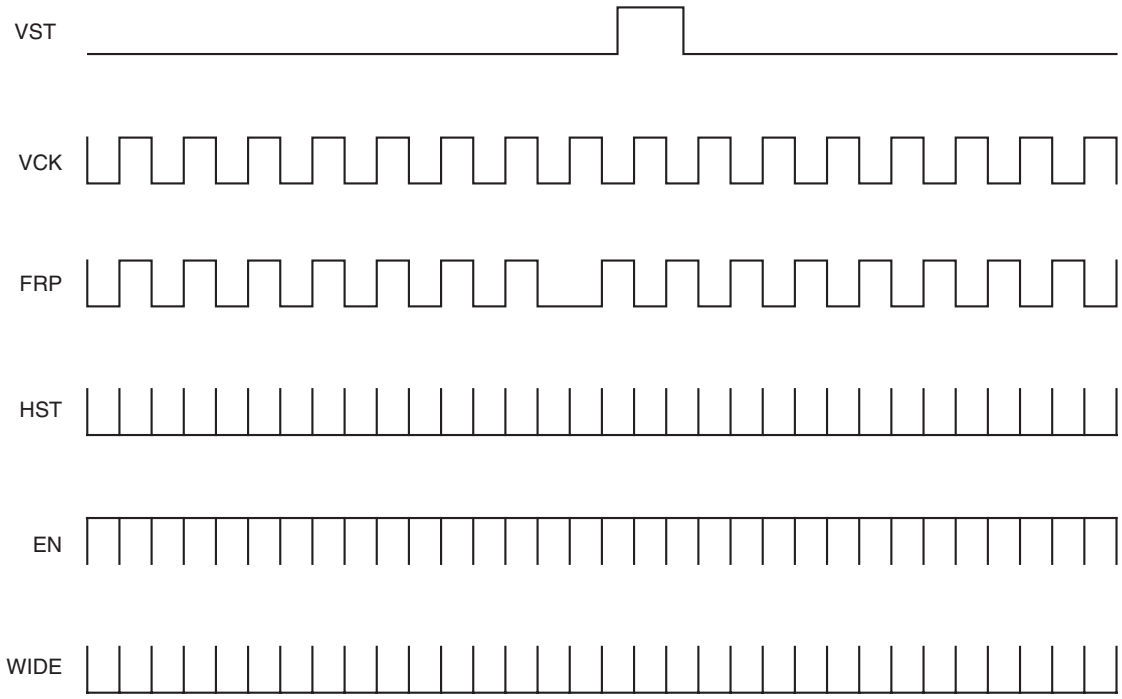
The left-pointing arrow (←•) means –.

The black dot at an arrow (•) indicates the start of measurement.

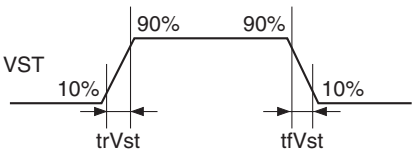
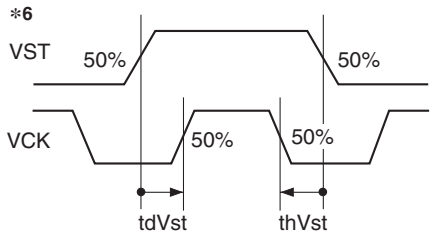
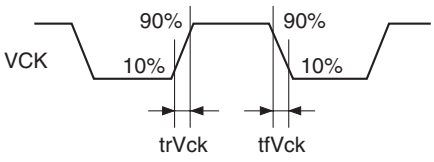
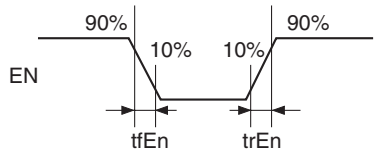
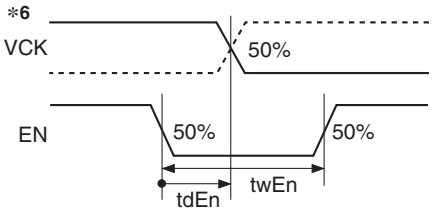
*7 WIDE represents every 1H pulse as shown in Horizontal Timing.

Vertical Standard Timing

NTSC 4:3 (in case of EVEN field)



<Vertical Shift Register Driving Waveforms>

Item		Symbol	Waveform	Conditions
VST	VST rise time	trVst		• VCK duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	VST fall time	tfVst		
	VST data setup time	tdVst		• VCK duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	VST data hold time	thVst		
VCK	VCK rise time	trVck		• VCK duty cycle 50% to1Vck = 0ns to2Vck = 0ns tdVst = 32μs thVst = –32μs
	VCK fall time	tfVck		
EN	EN rise time	trEn		• VCK duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	EN fall time	tfEn		
	EN fall to VCK rise/fall time	tdEn		
	EN pulse width	twEn		

Electrical Characteristics of Panel Block

1. Horizontal drivers

(Ta = 25°C, V_{DD} = 12.0V, VIH = 3.0V, VREF = 1.5V)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
HCKn input pin capacitance		CHckn	—	55	65	pF	
HST input pin capacitance		CHst	—	30	50	pF	
Video signal input pin capacitance		Csig	—	120	150	pF	
Psig input pin capacitance (4:3 display)		Cpsig	—	5.2	8.0	nF	
Input pin current	HCK1	IHck1	–600	–300	—	μA	HCK1: actual driving
	HCK2	IHck2	–600	–300	—	μA	HCK2: actual driving
	HST	IHst	–200	–100	—	μA	HST = GND
	RGT	IRGT	–150	–50	—	μA	RGT = GND
	REF	IREF	–900	–300	—	μA	REF = VIH/2

HCKn: HCK1, HCK2 (1.5MHz)

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
VCK input pin capacitance		CVck	—	10	15	pF	
VST input pin capacitance		CVst	—	10	15	pF	
Input pin current	VCK	IVck	–150	–50	—	μA	VCK = GND
	VST	IVst	–150	–50	—	μA	VST = GND
	EN	IEn	–150	–50	—	μA	EN = GND
	DWN	IDWN	–150	–50	—	μA	DWN = GND
	WIDE	IWIDE	–150	–50	—	μA	WIDE = GND

3. Total power consumption of the panel

Item		Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (NTSC)	(Ta = 25°C)	PWR25	—	43	67	mW

4. Pin input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
Pin – V_{SS} input resistance 1	Rin1	0.5	1	—	MΩ

Electro-optical Characteristics of Module/Panel Block (Ta = 25°C, NTSC mode)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio			CR_{25}	1	100	200	—	—
Panel block optical transmittance*8			T	2	6.5	7.5	—	%
Center luminance	Iled = 20mA		Lm_{20}	2	120	170	—	cd/m²
	Iled = 25mA		Lm_{25}		150	200	—	
Chromaticity (Iled = 20mA)	R	X	Rx	3	0.610	0.645	0.680	—
		Y	Ry		0.310	0.340	0.370	
	G	X	Gx		0.270	0.300	0.330	
		Y	Gy		0.480	0.525	0.570	
	B	X	Bx		0.120	0.150	0.180	
		Y	By		0.080	0.130	0.180	
	W	X	Wx		—	0.291	0.322	
		Y	Wy		—	0.308	0.364	
		Color temperature	Tcm	Correlated color temperature conversion (reference)	5900	8200	—	K
		Δuv	duvm		–0.016	0.004	0.022	
V-T characteristics*8	V_{90}	25°C	$V_{90\text{-}25}$	4	1.30	1.50	1.70	V
	V_{50}	25°C	$V_{50\text{-}25}$		1.70	1.90	2.10	
	V_{10}	25°C	$V_{10\text{-}25}$		2.30	2.50	2.70	
Half tone color reproduction range*8		R – G	V_{50RG}	5	–0.115	–0.080	–0.045	V
		B – G	V_{50BG}		0	0.03	0.05	
Response time*8	ON time	0°C	ton0	6	—	70	90	ms
		25°C	ton25		—	17	25	
	OFF time	0°C	toff0		—	120	180	
		25°C	toff25		—	30	75	
Viewing angle range		CR ≥ 10	θT	7	15	20	—	degree (°)
			θB		50	60	—	
			θL		35	40	—	
			θR		35	40	—	
Cross talk*8		25°C	CTK	8	—	0.9	1.5	%

Note) Optical property value includes error of ±10% brightness and ±0.01 chromaticity.

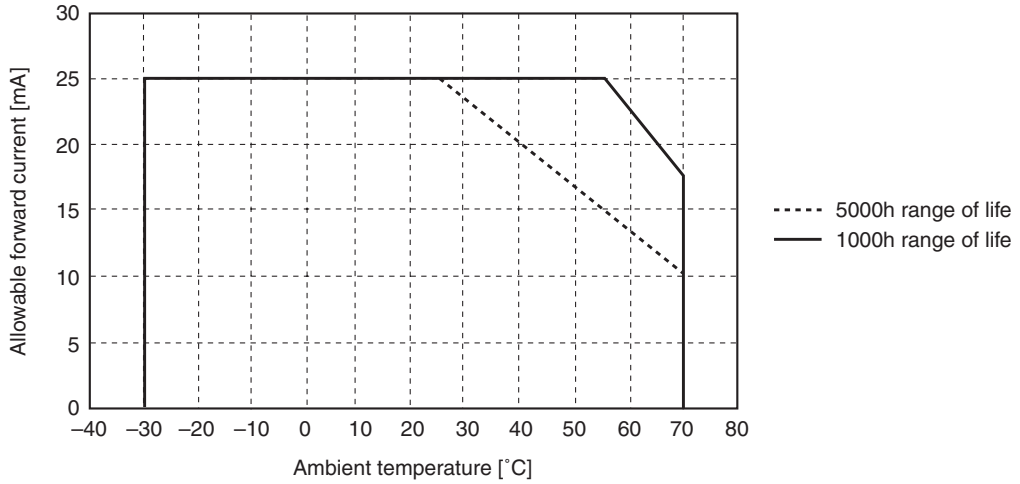
*8 Conforms to the measurement results for the discrete panel.

Electro-optical Characteristics of Backlight Block (Ta = 25°C, discrete backlight)

Item	Conditions	Symbol	Measurement method	Min.	Typ.	Max.	Unit
Backlight forward voltage	Ifbl = 20mA	$Vfbl_{20}$	9	6.4	7.2	8.0	V
	Ifbl = 25mA	Vbl_{25}		6.6	7.4	8.2	
Backlight power consumption	Ifbl = 20mA	Pbl_{20}		128	144	160	mW
	Ifbl = 25mA	Pbl_{25}		165	185	205	
Backlight center luminance	Ifbl = 20mA	Lbl_{20}		1600	2100	—	cd/m^2
	Ifbl = 25mA	Lbl_{25}		1900	2500	—	
Backlight center chromaticity	Ifbl = 20mA	x		0.281	0.303	0.321	—
		y		0.264	0.298	0.329	
		Tcbl	Correlated color temperature conversion (reference)	6000	7500	12000	K
		duvbl		0.013	–0.009	–0.013	
Backlight luminance uniformity	Ifbl = 20mA	BLunif	10	60	—	—	%
Backlight life (Luminance half-life)	Conforms to the conditions of the ambient temperature and allowable forward current shown below.						h

Note) Optical property value includes error of ±10% brightness and ±0.01% chromaticity.

LED backlight life
Ambient temperature vs. Allowable forward current characteristics



<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage
V_{DD} = 12.0V, VIH = 3.0V, VREF = 1.5V
VVC = 6.0V, VCOM = 5.5V, Vpsig = 6.0 ± 2.5V

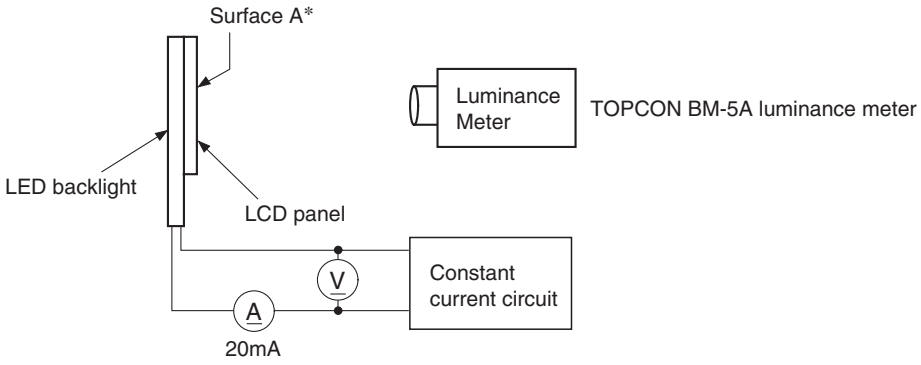
(2) Measurement temperature
25°C unless otherwise specified.

(3) Measurement point
One point in the center of the screen unless otherwise specified.

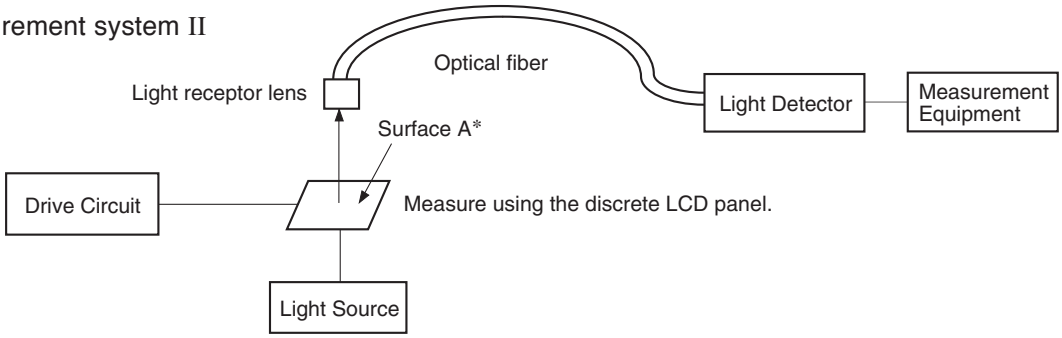
(4) Measurement systems
Three types of measurement systems are used as shown below.

(5) R, G and B input signal voltage Vsig
Vsig = VVC ± V_{AC} [V] (V_{AC}: signal amplitude)

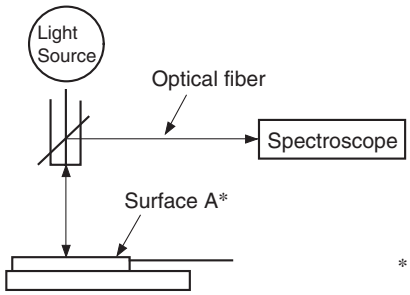
• Measurement system I



• Measurement system II



• Measurement system III



* Surface A: See the Package Outline.

1. Contrast Ratio

Contrast ratio (CR) is given by the following formula.

CR = L (White)/L (Black)

L (White): Surface luminance of the TFT-LCD panel at the input signal amplitude V_{AC} = 0.5V.
L (Black): Surface luminance of the panel at V_{AC} = 4.0V.
Both luminosities are measured by measurement system I.

2. Optical Transmittance of Panel, Center Luminance of Module, Color Temperature

Optical transmittance (T) is given by the following formula.

T = L (White)/Luminance of Backlight × 100 [%]

L (White) is the same expression as defined in "Contrast Ratio".

Lm = White luminance at the center of the panel
Tcm = Color temperature at the center of the panel

Measured by measurement system I using the TOPCON BM-5A.

3. Chromaticity

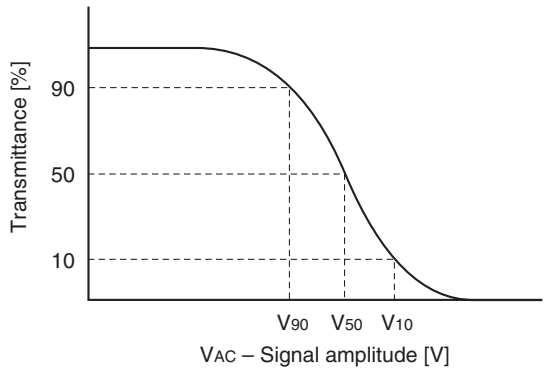
Chromaticity of the panels is measured by measurement system I. Raster modes of each color are defined by the representations at the input signal amplitude conditions shown in the table below. Measurement system I uses x and y of the CIE standards as the chromaticity here.

		Signal amplitudes (VVC ± V_{AC}) supplied to each input		
		R input	G input	B input
Raster	R	0.5	4.0	4.0
	G	4.0	0.5	4.0
	B	4.0	4.0	0.5
	W	0.0	0.0	0.0

(Unit: V)

4. V-T Characteristics

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panel, are measured by measurement system II by inputting the same signal amplitude V_{AC} to each input pin. V_{90}, V_{50}, and V_{10} correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.

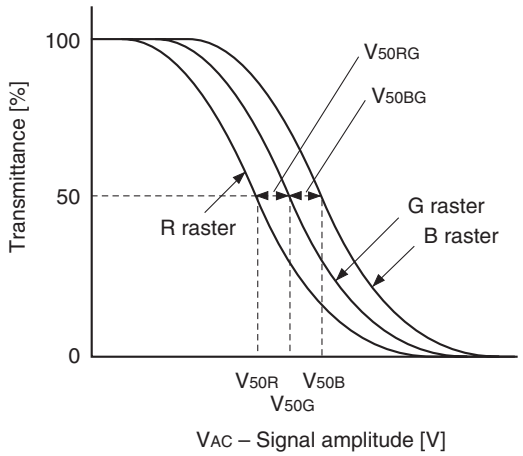


5. Half Tone Color Reproduction Range

The half tone color reproduction range of LCD panels is characterized by the differences between the V-T characteristics of R, G and B. The differences of these V-T characteristics are measured by measurement system II.

Measurement system II defines signal voltages of each R, G and B raster mode which correspond to 50% of transmittance, V_{50R}, V_{50G} and V_{50B}, respectively. V_{50RG} and V_{50BG}, that is to say the differences between V_{50R} and V_{50G} and between V_{50B} and V_{50G}, are given by the following formulas respectively.

$V_{50RG} = V_{50R} - V_{50G}$
$V_{50BG} = V_{50B} - V_{50G}$

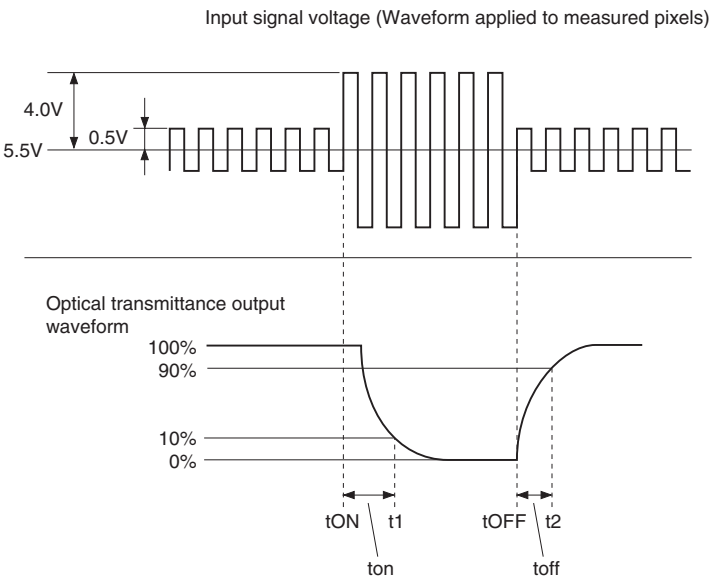


6. Response Time

Response times ton and toff are measured by measurement system II by applying the input signal voltages in the figure to the right to each input pin. These times are defined by the following formulas.

ton = t1 – tON
toff = t2 – tOFF
t1: time which gives 10% transmittance of the panel.
t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the figure to the right.

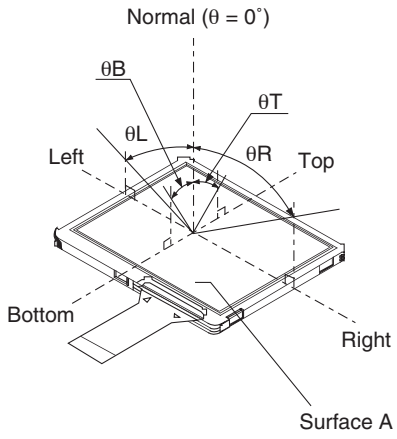


7. Definition of Viewing Angle Range

Viewing angle range is measured by measurement system I. The contrast ratio (CR) is measured at the angles defined in the figure to the right and the range where CR ≥ 10 is taken as the viewing angle range.

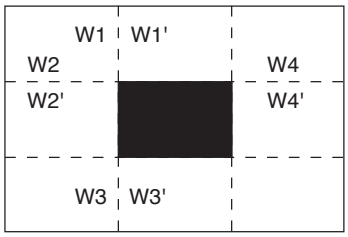
Measure with surface A* facing upwards.

* Surface A: See the Package Outline.



8. Cross Talk

Cross talk is determined by the luminance differences between adjacent areas represented by Wi' and Wi (i = 1 to 4) around the black window (Vsig = 4.0V/1V).



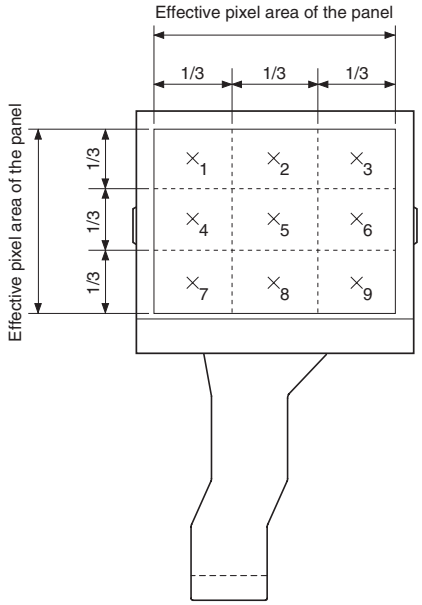
$$\text{Cross talk value CTK} = \left| \frac{Wi' - Wi}{Wi} \right| \times 100\ [\%]$$

9. Backlight Center Luminance and Chromaticity Measurement Method

1. Environmental conditions
   Temperature: 25 ± 5°C
   Humidity: 30 to 85%
   Start measurement after leaving the module in the above environment for one hour.
   Measurement should be performed in a dark room with a luminance of 10 lx or less and which is not subject to the effects of reflective or external light.
   There should be no heat insulating objects around the module unit, and measurement should be performed in a draftless condition.
2. Luminance and chromaticity measurement method
   Measurement equipment: TOPCON BM-5A, viewing angle: 0.2°, distance: 450 ± 50mm
   Measure 30s after the backlight is lit.
   Using a constant current circuit, measure the luminance under both conditions of Ifbl = 20mA and 25mA, and measure the chromaticity under only the condition of Ifbl = 20mA.

10. Backlight Luminance Uniformity Measurement Method

1. Environmental conditions
   Measure under the same conditions as "9. Backlight Center Luminance and Chromaticity Measurement Method" above.
2. Light the backlight at Ifbl = 20mA using a constant current circuit, and start measurement 30s after the backlight is lit.
   Backlight luminance uniformity is obtained by dividing the effective pixel area into 9 equal sections as shown below, measuring the luminance at each of the centers 1 to 9, and calculating Min. luminance ÷ Max. luminance × 100 [%].



11. Backlight Life Measurement Method

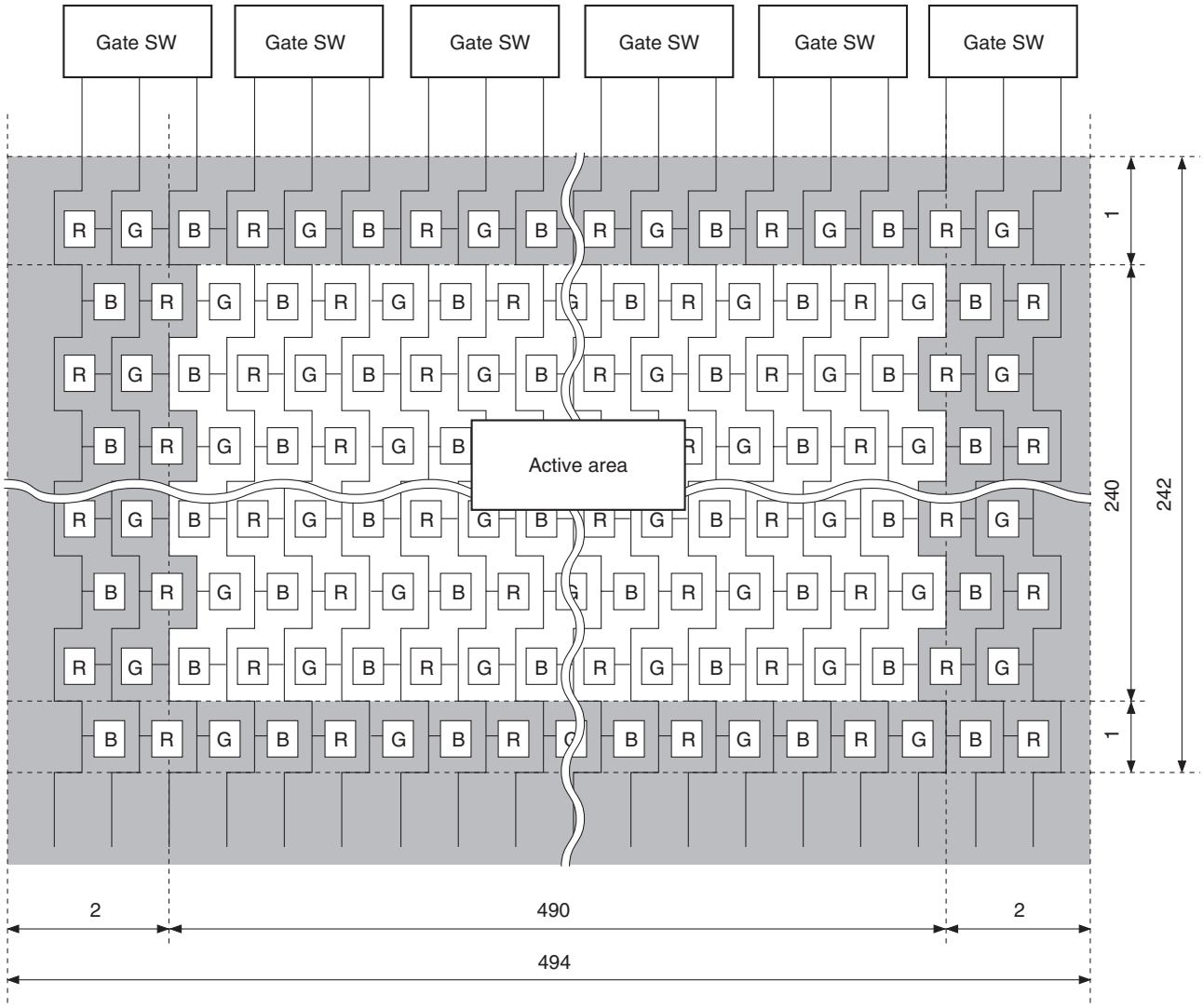
Definition of life: When the backlight center luminance drops to 50% of the initial value.
Lighting conditions: Discrete backlight under the following conditions.
Leave the module in a normal temperature (25°C) environment for one hour before performing optical measurement.

(1) Ifbl = 20mA
   1-1) Continuous lighting at an ambient temperature of 55°C. (5000h or more)
   1-2) Continuous lighting at an ambient temperature of 70°C. (1000h or more)
(2) Ifbl = 25mA
   2-1) Continuous lighting at an ambient temperature of 40°C. (5000h or more)
   2-2) Continuous lighting at an ambient temperature of 60°C. (1000h or more)

Description of Operation

1. Color Coding

The color filters are coded in a delta arrangement. The shaded area is used for the dark border around the display.



2. Description of LCD Panel Operations

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to each of 240 line electrodes sequentially one line electrode at a time in a single horizontal scanning period.

- The selected pulse is output when the enable pin goes to high level. PAL signal pulse elimination display is possible by using the enable pin and simultaneously controlling VCK.

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuitry, applies selected pulses to each of 490 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.

- The scanning direction of the horizontal shift registers can be switched with the RGT pin. The scanning direction is left to right (right scan) for RGT pin at high level (2.6 to 5.5V), and right to left (left scan) for RGT pin at low level (0V). In addition, the scanning direction of the vertical shift registers can be switched with the DWN pin. The scanning direction is top to bottom for DWN pin at high level (2.6 to 5.5V), and bottom to top for DWN pin at low level (0V). (These scanning directions are from a front view.)

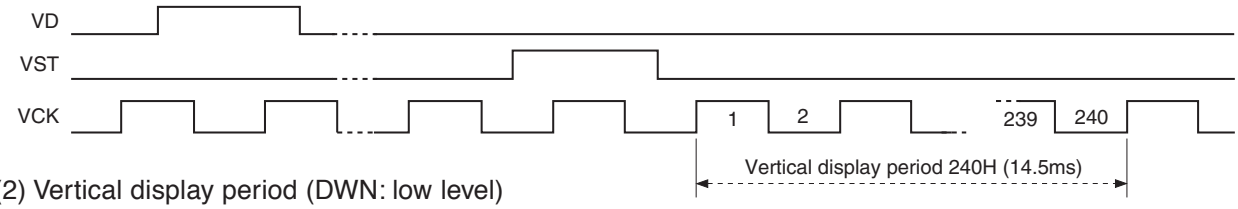
- The vertical and horizontal drivers address one pixel, and then thin film transistors (TFTs; two TFTs for one pixel) turn on to apply a video signal to the pixel. The same procedures lead to the entire 240 × 490 pixels to display a picture in a single vertical scanning period.

- Pixel dots are arranged in a delta pattern, where sets of RGB pixels are positioned shifted by 1.5 dots against adjacent horizontal lines. The horizontal driver output pulse must be shifted by 1.5 dots for each horizontal line against the horizontal sync signal to apply a video signal to each pixel properly.

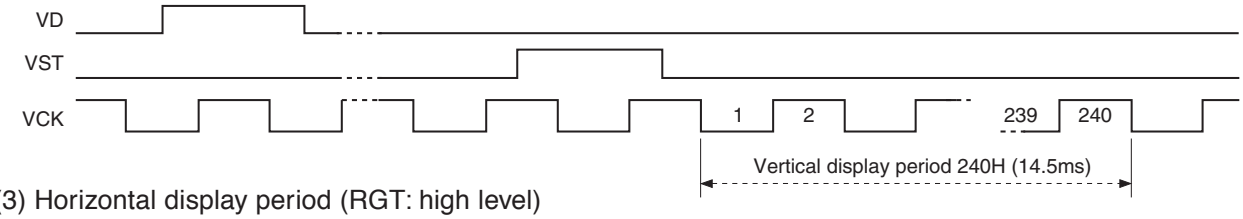
- The video signal should be input with the polarity-inverted every horizontal cycle.

- The relationships between the vertical shift register start pulse VST and the vertical display period, and between the horizontal shift register start pulse HST and the horizontal display period are shown below for top to bottom and left to right scan.

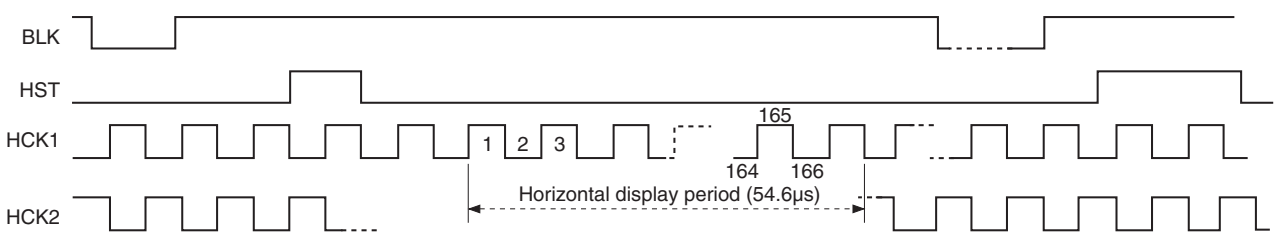
(1) Vertical display period (DWN: high level)



(2) Vertical display period (DWN: low level)



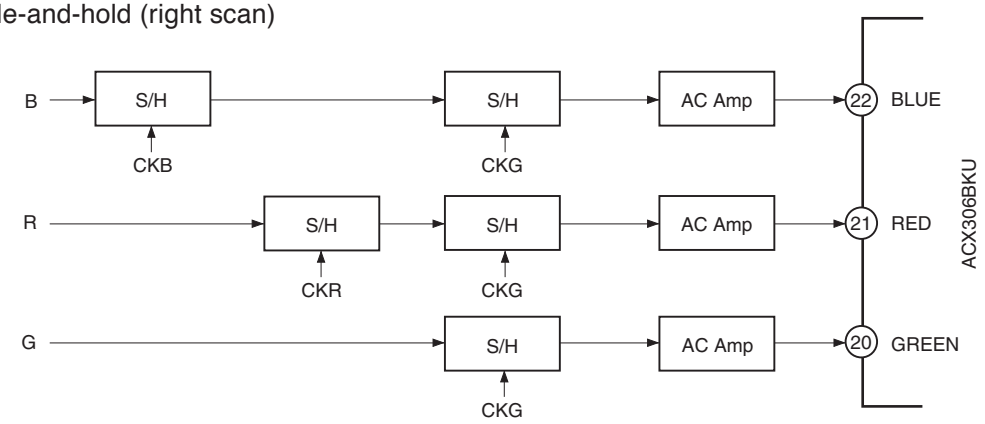
(3) Horizontal display period (RGT: high level)



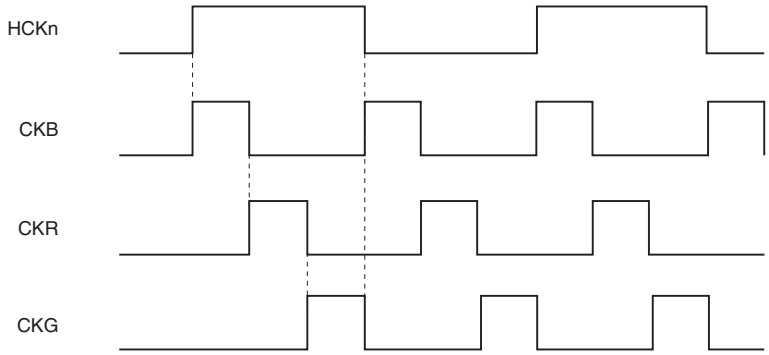
3. RGB Simultaneous Sampling

The horizontal driver samples R, G and B video signals simultaneously, which requires phase matching between the R, G and B signals to prevent the horizontal resolution from deteriorating. Thus phase matching by an external signal delay circuit is needed before applying the video signal to the LCD panel.
Two methods are applied for the delaying procedure: Sample-and-hold and Delay circuit. These two block diagrams are as follows.
The ACX306BKU has a right/left inversion function. The following phase relationship diagram indicates the phase setting for right scan (RGT = high level). For left scan (RGT = low level), the phase setting should be inverted for the B and G signals.

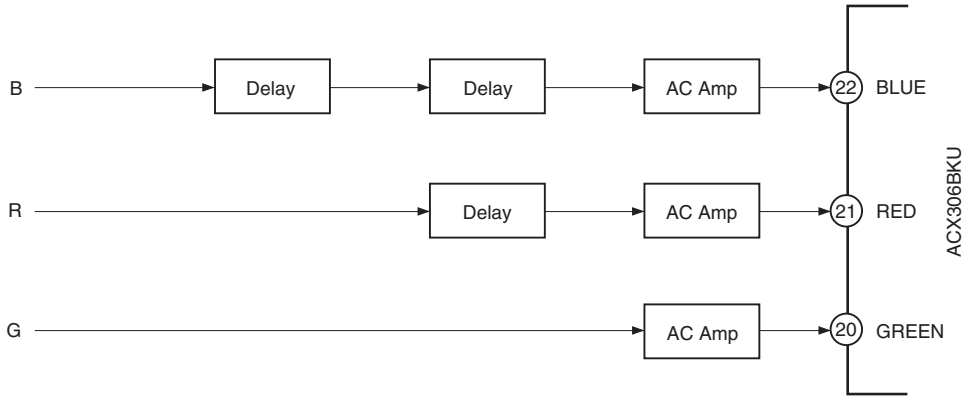
(1) Sample-and-hold (right scan)



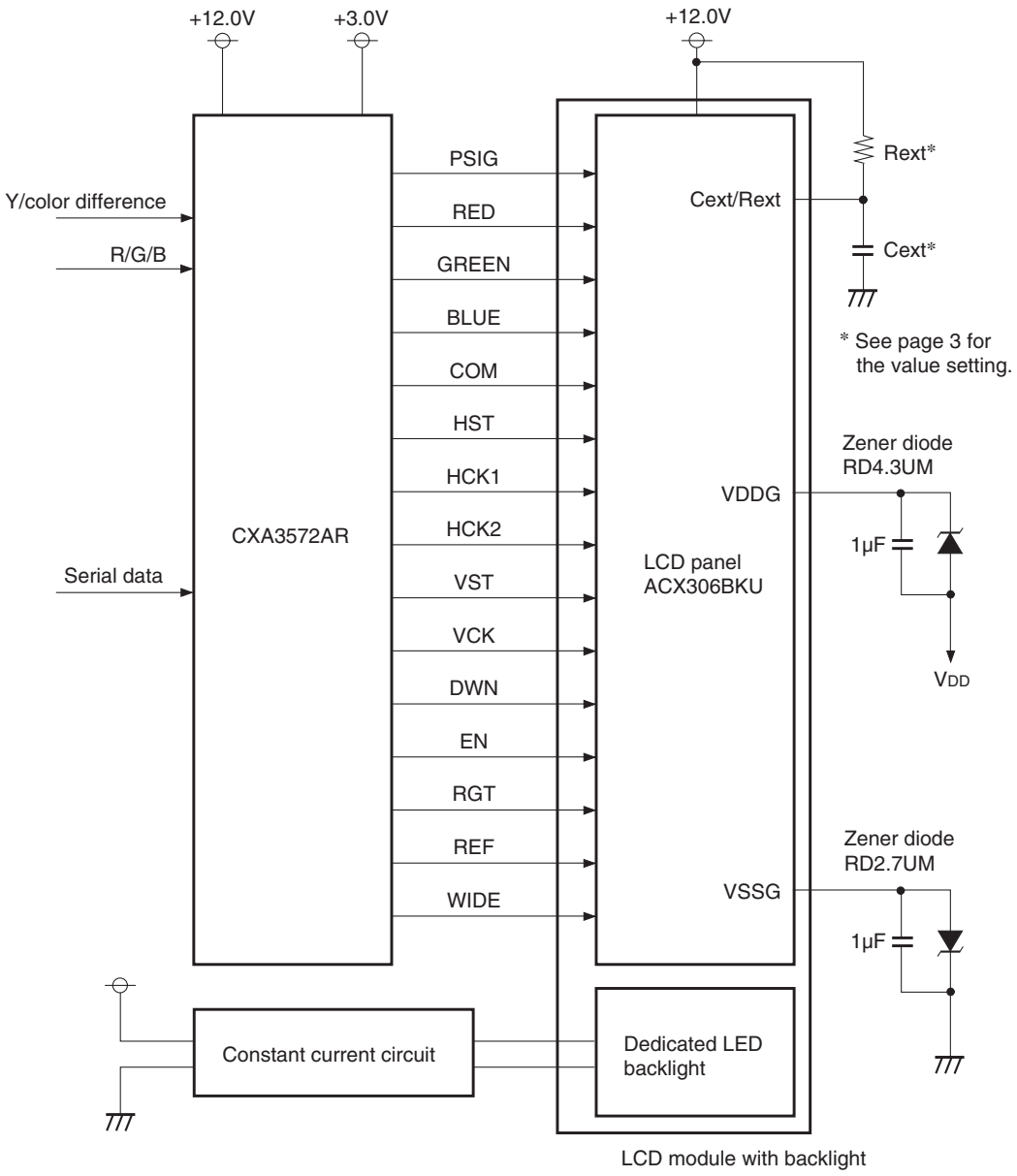
<Phase relationship of delaying sample-and-hold pulses> (right scan)



(2) Delay element (right scan)



System Configuration



Notes on Handling

(1) Static charge prevention
Be sure to take the following protective measures. TFT-LCD panels and LED backlights are easily damaged by static charges.
a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install grounded conductive mats on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

(2) Protection from dust and dirt
a) Operate in a clean environment.
b) When delivered, the panel surface (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the panel.
c) Do not touch the polarizer surface. The surface is easily scratched. When cleaning, use a clean-room wiper with ethyl alcohol. Be careful not to leave stains on the surface.
d) Use ionized air to blow dust off the panel.

(3) Module fixing method
a) The following items should be taken into account for the positioning guide design.
• The design reference edges are the upper and left edges of the panel as viewed from the front. Design the guides using the panel frame as the reference and not the backlight.
• Set the guides on the same side of the set as the monitor window frame.
• To prevent LCD image unevenness, the guides should be the maximum package tolerance or more so that a clasping load is not applied to the panel from the x and y directions.
• Make sure the guides do not block the panel FPC outlet and backlight connector outlet.
b) Guaranteed area of the polarizer appearance is within 0.5mm outer from the effective display area (Fig. 1). Design the monitor window frame of the set so that it is within this range including variance.
c) Set the holders on the rear of the backlight around the circumference as far from the center of the backlight as possible. Local pressure applied to the center of the rear of the backlight for an extended period may result in uneven luminance, so the holder pressure on the center of the backlight should be 500g/cm^2 or less.
d) Connect the panel or backlight frame to GND.
e) The intensity of the connector conforms to SUR connector specification of J.S.T. mfg.

(4) Others
a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop the panel or backlight.
c) Do not twist or bend the panel, panel frame or backlight.
d) Keep the panel and backlight away from heat sources.
e) Do not dampen the panel or backlight with water or other solvents.
f) Avoid storage or use of the panel at high temperatures or high humidity, as this may result in damage.

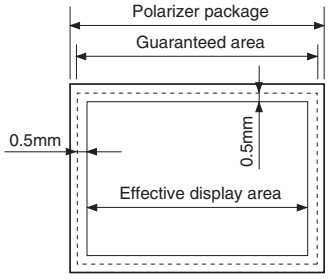
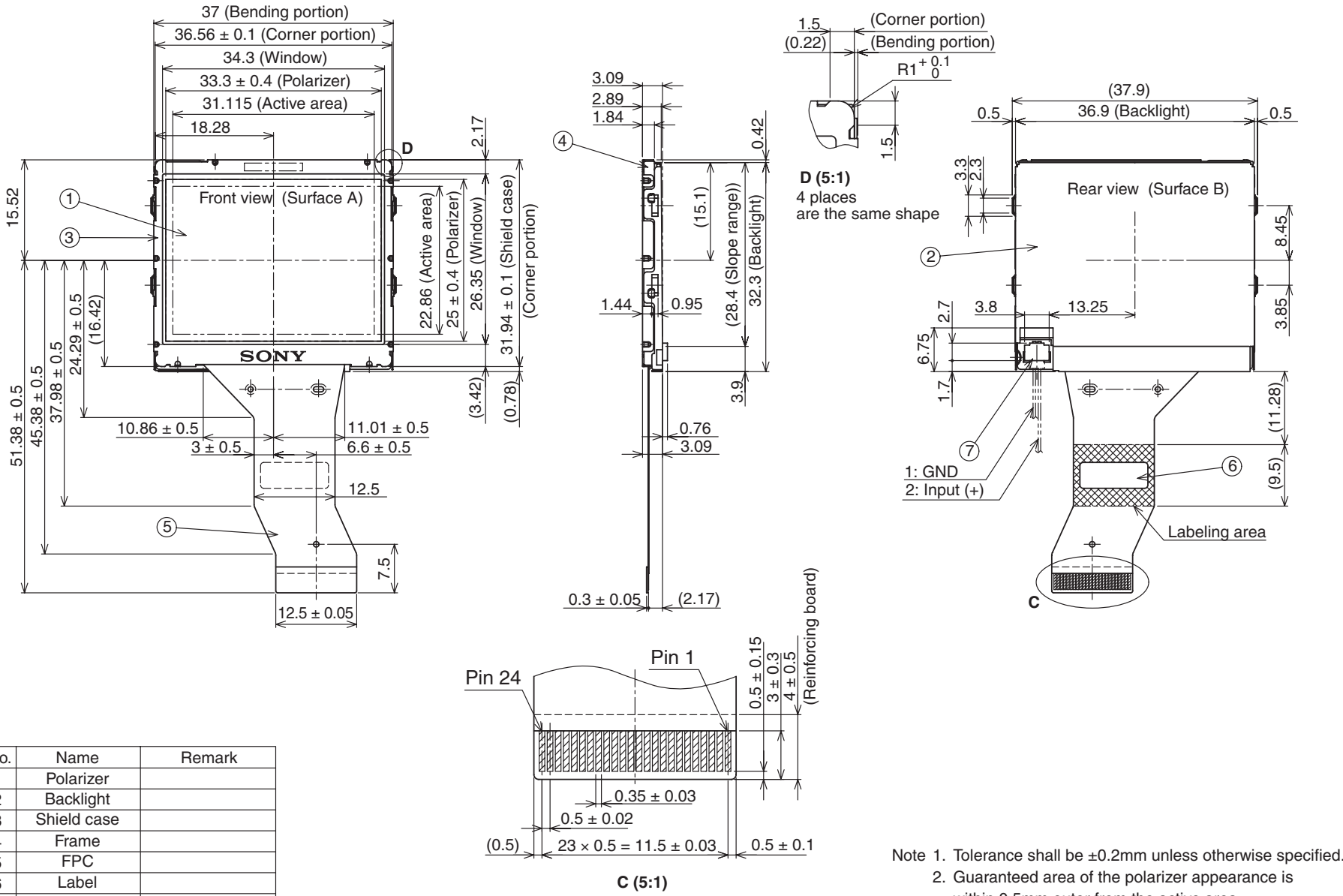


Fig. 1

Package Outline Unit: mm



No.	Name	Remark
1	Polarizer	
2	Backlight	
3	Shield case	
4	Frame	
5	FPC	
6	Label	
7	Connector	SM02B-SURS-TF

Note 1. Tolerance shall be ±0.2mm unless otherwise specified.
2. Guaranteed area of the polarizer appearance is within 0.5mm outer from the active area.