AD009-041 Remote controller

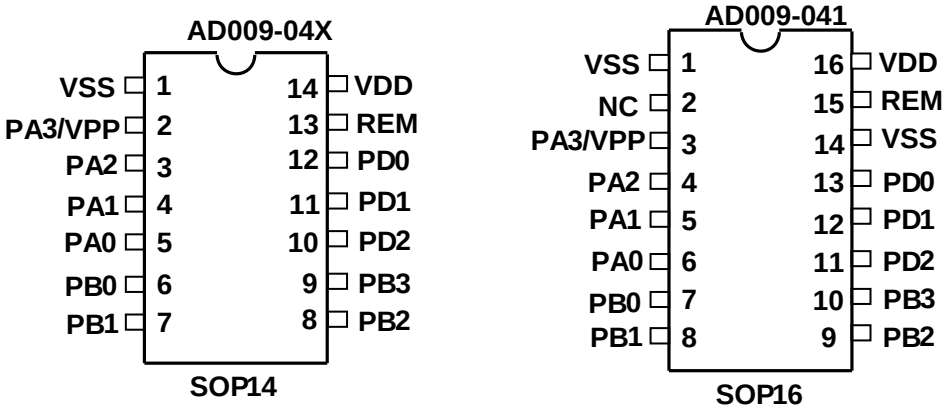
1. General Descriptions

The AD009-041 a high-performance 4-bit RISC micro-controller embedded up to 2KX12 bits OTP, 32X4 bits SRAM, 10 Input/Output pins, one input pin and built-in one IR LED drive pin. it's flexible and cost-effective solution for remote control of TV, Fans, Air conditioners ... etc.

2. Features

- MCU Operating voltage: 1.8V to 3.6V
- Operation frequency: MCU run 2 MIPS
- Memory Size
  - ☐ Program ROM size: 2K X12 bits (OTP type)
    SRAM size: 32x4 bits
- Wake up function for power-down mode
  - ☐ HALT mode wake up source: RTC timer overflow or PA0~3, PB0~3 and PD0~3 edge trigger.
- Provided 10 input /output pins: each I/O has bit programmable as input or output port, these 10 I/Os also provided edge trigger wake up function and pull up resistors configured by registers.
  (a) They are provided with high sink current 20mA @VDD=3V, VOL=0.5V.
  (b) They are provided with drive current 7mA @VDD=3V, VOH=2.5V.
  (c) Pull up 150k ohm resistor.
- Provide 1 input pin (PA3) shared with VPP pin, pull up 150k ohm resistor and edge trigger wake up function.
- Built-in one IR LED drive pin.
  (Sink current : I_{OL}=210mA at VDD=3V and V_{OL}=0.3V)
- One 8 bits timer, clock source of timer is F_{MCK} /8192(or 4096,2048,1024), the content of timer can be cleared and read by program.
- Built-in internal RC OSC 8 MHz ----
  frequency deviation within ±2%, VDD=1.8V~3.6V, temp= -20 ºC ~70 ºC
- Support 1.5 cycle length instruction (NOP15) to generate IR waveform by software.
- Four reset condition
  - ☐ Low voltage reset (LVR=1.5V)
  - ☐ Power on RC-reset
  - ☐ Watch dog timer overflow reset (WDT period is 0.26 Sec)

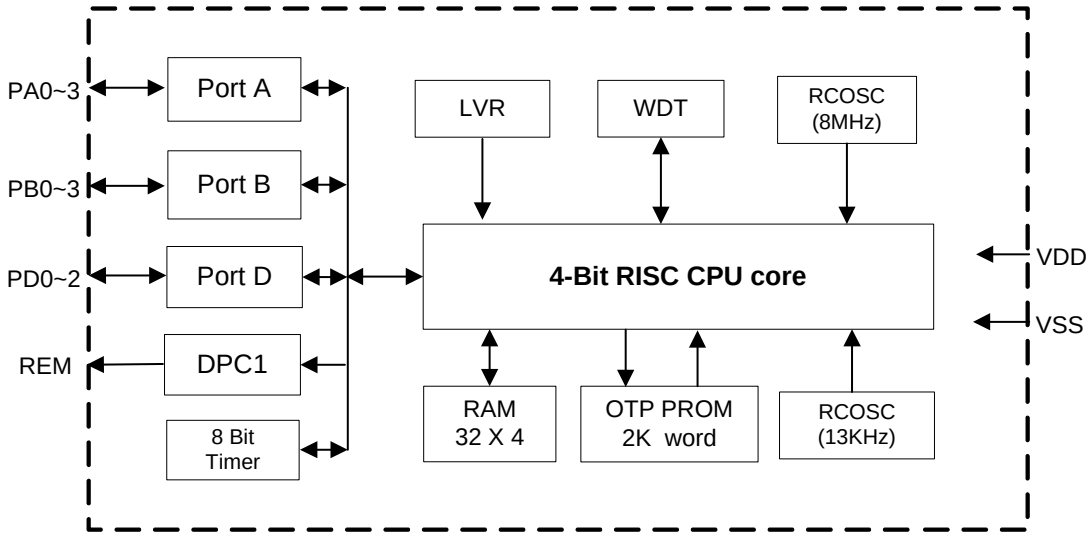
3. Package SOP14/16



4. Pads Information

PAD Name	Type	State After Reset	Description
Power Input			
VDD	I	High	Power input pin.
VSS	I	Low	Ground input pin.
General I/O ports			
PA0~PA2	I/O	XXXX	PA0~PA2 are programmable I /O ports, with pull up resistor 150K ohm. Level-change-wakeup function is provided.
PA3/VPP	I	X	PA3 is an input pin only, with pull up resistor 150K. Level-change-wakeup function is provided.
PB0~PB3	I/O	XX	PB2 and PB3 are programmable I /O ports, with pull up resistor 150K ohm. Level-change-wakeup function is provided.
REM	O	X	REM is an large sink open drain output pin, used for IR LED driving.
PD0~PD2	I/O	XXXX	PD0 ~ PD2 are programmable I /O ports, with pull up resistor 150K ohm. Level-change-wakeup function is provided.

Block Diagram



4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYSMBOL	RATING	UNIT
DC Supply Voltage	V+	< 7.0	V
Input Voltage Range	V_{IN}	-0.5 to VDD+0.5	V
Operating Temperature	T_A	-40 to 85	ºC
Storage Temperature	T_{STO}	-50 to 150	ºC

4.2 DC/AC Characteristics

DC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Operating voltage	V_{DD}	-	1.8	-	3.6	V
Operating Current	I_{OP1}	3V , MCU run 2 MIPS	-	0.7	-	mA
Standby Current 1	I_{STBY1}	MCU stop, WDT off, key scan off	-	0.1		uA
Standby Current 2	I_{STBY2}	MCU stop, WDT off, key scan on	-	0.7	3	uA
Input High Level	V_{IH}	All I/O port	0.7*V_{DD}	-	-	V
Input Low Level	V_{IL}	All I/O port	-	-	0.4*V_{DD}	V
Output Drive Current	I_{OH}	VDD=3V , V_{OH}=2.5V All I/O port, except REM	-	-7	-	mA
Output Sink Current	I_{OL1}	VDD=3V , V_{OL}=0.5V All I/O port, , except REM PIN	-	20	-	mA

Output Sink Current	I_{OL2}	VDD=3V , V_{OL}=0.3V REM PIN	-	210	-	mA
Input Resistor	R_{up}	Pull up 150K ohm	-	150	-	K ohm
LVR	V_{LVR}			1.5		V

AC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Internal HRCOSC Frequency	F_{OSC2}	VDD=1.8V~3.6V Temp.= -20 ºC ~70 ºC	7.84	8±2%	8.16	MHz
MCU Operation frequency	F_{MCK}	VDD=1.8V~3.6V Use HRCOSC		2		MHz
MCU Operation voltage	V_{OP}		1.8	3.0	3.6	V
Internal LRCOSC Frequency	F_{LOSC}	VDD=3V		13KHz±50%		KHz
Stable clock delay after power on or system reset	CKstable1	(Note 1)	-	320us + 1024 x (1/ F_{MCK}) (Note 2)		us
Stable clock delay after wake up	CKstable2	System oscillator --HRCOSC (Note 3)	-	64 x (1/ F_{MCK}) (Note 2)		us

Note1: The stable clock delay (CKstable 1) is place after first clock output of HRCOSC before user's first instruction, it means the user's program will get more stable clock after power on reset.

Note2: F_{MCK} = MCU operating clock

Note3: The stable clock delay (CKstable 2) is place after first clock output of HRCOSC before user's first instruction, it means the user's program will get more stable clock after wake up.

5. FUNCTIONAL DESCRIPTION

5.1 Program ROM (PROM)

AD009-041 support two kind of OTP ROM arrangement. The OTP ROM memory plan is shown below:

Address	AD009-041 (2 K OTP ROM)
000h ~ 0FFh	User area 2K (2016 X12)
100h ~ 1FFh	
200h ~ 2FFh	
…….	
500h ~ 5FFh	
600h ~ 7DFh	
7E0h ~ 7FFh	Reserved area

Note: 1. The content of OTP ROM address $000h~$7DFh can be read by program. Address $7E0h~$7FFh can't be read by program.

2. To read registers DMDL, DMDM and DMDH, only LD A,(n) instruction can be used. Other instructions are not allowed. (n= DMDL, DMDM or DMDH)

AD009-041 supports 2 K words OTP ROM which is located on $000h ~ $7DFh, it's used to stores user program. The reserved area is $7E0h ~ $7FFh, they can't be read by program.

To read OTP ROM valid data, use DMA2~DMA0 registers as address pointer. After these registers (DMA0~2) are specified by software, the 12bits data of ROM can be moved to A register by three instructions, they are “LD A, (DMDL)”, “LD A, (DMDM)” and “LD A, (DMDH)”. The three instructions mentioned above are two cycle instruction, all others instructions are single cycle instruction.

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~DMA2 three registers built a 11 bit addressing space (DMA2.3 not including) for read PROM data, DMA0 is lowest nibble address, DMA2 is highest nibble address. DMA2.3: It’s a register only, but for PROM address setting is useless.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	
DMDL	1CH	R	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	DMDL is used to read low nibble data of PROM by address DMA0~ DMA2.
DMDM	1DH	R/W	xxxx	DMDM.3	DMDM.2	DMDM.1	DMDM.0	DMDM is used to read middle nibble data of PROM by address DMA0 ~ DMA2. Writing this register with data 05h will clear watch dog timer (WDT)
DMDH	1EH	R	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	DMDH is used to read the high nibble data PROM by address DMA0~DMA2

For example, assume the data of address 156H is 587H.

```
LD A, #1
LD (DMA2), A
LD A, #5
LD (DMA1), A
LD A, #6
LD (DMA0), A    ; ROM address = 156H
LD A, (DMDL)    ; A register = 7H ; low nibble data of ROM address 156H
LD A, (DMDM)    ; A register = 8H;  middle nibble data of ROM address 156H
LD A, (DMDH)    ; A register = 5H;  high nibble data of ROM address 156H
```

5.2 SRAM and I/O Memory Map

AD009-041 series provided 32 nibbles SRAM on the locations $20H~$3FH, these address of SRAM is different from PROM’s address.

Direct Addressing (use MAH)		Real SRAM Address	SRAM MAP
MAH=XH (MAH no effect)	00H~1FH		Common I/O port and SFR(special function register) register
MAH=0H	20H~3FH	00H~1FH	USER SRAM (32x4)

5.2.1 I/O Memory Map

The I/O memory map consists of common I/O and extended I/O. These I/O provide some data operation instructions as the following:

5.2.2 Common I/O

The previously described common block is defined as the common I/O block. A common I/O provided LD/ADC/SBC/OR/AND/XOR/INC/DEC/RLC/RRC/CMP/ADR operation. SET, CLR (bit set/clear) can only be operated on the address range from 00H to 0FH.

Read common I/O instruction: LD/ADC/SBC/CMP/OR/AND/XOR (Ex. LD A,(n))
Write data to command I/O instruction: LD (n),A
Read and write command I/O instruction : DEC/INC/ADR/RRC/RLC (Ex. DEC (n))

U: unchanged X: unknown value R/W: readable & writeable R: readable only W: writeable only

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	0	0	CF	ZF	ZF : Zero status register CF : Carry status register
IR_DIV	01H	R/W	1000	DPC1 (REM)	X	X	X	DPC1(REM) is an output port for IR LED driving.
IOC_PA	02H	R/W	0000	USER0	IOCA2	IOCA1	IOCA0	Port A input/output direction select 1: set port A as output port individual pin 0: set port A as input port individual pin USER0: 1 bit user RAM
DATA_PA	03H	R/W	xxxx	DPA3 (Read only)	DPA2	DPA1	DPA0	Read data from PA0~PA3 PIN and write data to PA0~PA2 PIN (I/O direction is selected by IOC_PA register)
IOC_PB	05H	R/W	0000	IOCB3	IOCB2	IOCB1	IOCB0	Port B input/output direction select 1: set port B as output port individual pin 0: set port B as input port individual pin
DATA_PB	06H	R/W	xxxx	DPB3	DPB2	DPB1	DPB0	Read port B data from PB0~PB3 port and write to PB0~PB3 (I/O direction is defined by IOC_PB register)
USER1	07H	R/W	xxxx	USER1.3	USER1.2	USER1.1	USER1.0	General purpose user RAM
Reserved	08H~ 0BH	R/W	xxxx	X	X	X	X	Reserved
IOC_PD	0CH	R/W	0000	X	IOCD2	IOCD1	IOCD0	Port D input/output direction select 1: set port D as output port individual pin 0: set port D as input port individual pin
DATA_PD	0DH	R/W	xxxx	X	DPD2	DPD1	DPD0	Read Port D data from PD0~PD2 port and write to PD0~PD2 (I/O direction is define by IOC_PD register)
SCALER1	0EH	R/W	0000	TM1EN	TM1FG	T1DIV1	T1DIV0	T1DIV1~T1DIV0: The pre-scaler of TIMER1 Timer 1 clock source defined below: F_{MCK} = MCU operating clock T1DIV1 / T1DIV0 / TM1CK 0 / 0 / F_{MCK}/8192 0 / 1 / F_{MCK} /4096 1 / 0 / F_{MCK} /2048 1 / 1 / F_{MCK} /1024 TM1FG: Timer 1 overflow flag 0: no overflow occurred. 1: overflow occurred, it can be cleared by software. TM1EN: Timer 1 enabled/disabled 0:Timer 1 disabled, the content of Timer1 is cleared to all 00h. 1:Timer 1 enabled
USER2	0FH	R/W	xxxx	USER2.3	USER2.2	USER2.1	USER2.0	General purpose user RAM
TIM1_L	11H	R	0000	TIM1.3	TIM1.2	TIM1.1	TIM1.0	TIM1.3~TIM1.0: Low nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
TIM1_H	12H	R	0000	TIM1.7	TIM1.6	TIM1.5	TIM1.4	TIM1.7~TIM1.4: High nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
Reserved	13H~ 17H							Reserved
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~DMA2 three registers built a 11

DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	bits addressing space (DMA2.3 not including) for read PROM data, DMA0 is lowest nibble address, DMA2 is highest nibble address. DMA2.3: It's a register only, but for PROM address setting is useless.
DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	
Reserved	1BH	x	xxxx	X	X	X	X	Reserved
DMDL	1CH	R	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	DMDL is used to read low nibble data of PROM by address DMA0~ DMA2.
DMDM	1DH	R/W	xxxx	DMDM.3	DMDM.2	DMDM.1	DMDM.0	DMDM is used to read middle nibble data of PROM by address DMA0 ~ DMA2. Writing this register with data 05h will clear watch dog timer (WDT)
DMDH	1EH	R	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	DMDH is used to read the high nibble data PROM by address DMA0~DMA2
Reserved	1FH	R/W	xxxx	X	X	X	X	Reserved
SRAM 32 nibbles	20H~ 3FH	R/W	xxxx	SRAM.3	SRAM.2	SRAM.1	SRAM.0	

5.2.3 Extended I/O

To extend I/O memory space, AD009-041 series provided one special instructions, "LD **EXIO**(n), A", where n = 00H ~ 0FH" to obtain the 16 extra I/O registers. These registers are used for the I/O port pull up resistors control and wake up control, they can be accessed by two "LD" data transfer instruction only. For example, the pull up resistor of port A is enabled, the program as shown below.

```
LD A, #FH
LD EXIO(00H), A
```

U: unchanged X: unknown value R/W: readable & writeable R: readable only W: writeable only

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
PAPU	00H	W	0000	PAPU.3	PAPU.2	PAPU.1	PAPU.0	Port A pull up 150K ohm resistor 0: Port A pull up resistor disabled 1: Port A pull up resistor enabled
Reserved	01H	X	xxxx	X	X	X	X	Reserved
PBPU	02H	W	0000	PBPU.3	PBPU.2	PBPU.1	PBPU.0	Port B pull up 150K ohm resistor 0: Port B pull up resistor disabled 1: Port B pull up resistor enabled
Reserved	03H	X	xxxx	X	X	X	X	Reserved
PDPU	04H	W	0000	X	PDPU.2	PDPU.1	PDPU.0	Port D pull up 150K ohm resistor 0: Port D pull up resistor disabled 1: Port D pull up resistor enabled
Reserved	05H	X	xxxx	X	X	X	X	Reserved
PAWK	06H	W	0000	PAWK.3	PAWK.2	PAWK.1	PAWK.0	Port A wake up enable control 0: Port A wake up disabled 1: Port A wake up enabled
PBWK	07H	W	0000	PBWK.3	PBWK.2	PBWK.1	PBWK.0	Port B wake up enable control 0: Port B wake up disabled 1: Port B wake up enabled
PDWK	08H	W	0000	X	PDWK.2	PDWK.1	PDWK.0	Port D wake up enable control 0: Port D wake up disabled 1: Port D wake up enabled
Reserved	09H~ 0FH							Reserved

5.3 Halt Mode & Wake up

The MCU is changed into HALT mode (MCU clock and HRCOSC stop) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA0~PA3, PB0~PB3 and PD0~PD2 are provided the wake up function when rising edge or falling edge trigger occurred in halt mode. The program counter will be changed to $004H when HALT instruction executed immediately, and program counter will go to next address after stable time delay (CKstable3, see page 5) while wake up condition occurred. "system resetb" signal will release HALT state and execute reset

procedure because reset is first priority when in HALT mode, so program counter will be changed from $004h to $000h, program counter goes to next address after stable time delay (CKstable1, see page 5). Furthermore, the SRAM will keep their previous data without changed in this mode.

5.4 Watch Dog Timer Reset (WDT)

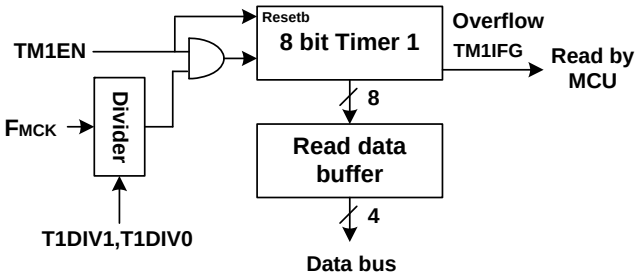
The watch dog timer (WDT) is used to reset whole chip when detect unexpected execution sequence caused by accident condition, avoiding dead lock of MCU program. This timer can be enabled or disabled by option. WDT will not have any action when WDT disabled. Software shall run an "clear watch dog timer" (write data 5h to register $1D) instruction before WDT time out if WDT is enabled. Hardware will generate a reset signal to reset whole system when WDT overflow. The watch dog timer is a simple counter. The WDT time-out period is fixed to 0.262±2% Sec.. WDT can works in NORMAL mode but disabled in HALT mode because the clock source come from internal HRCOSC oscillator.
WDT will be reset when wake up from halt, after power on reset or cleared by software. The reset watch dog timer sequence is as below :

```
LD      A, #05H
LD      (1DH), A    ; clear watch dog timer
```

Note 1. For avoiding dead lock and system stable, It's strongly recommended don't use more than one "reset watch dog" in program.

5.5 Programable 8 bits TIMER1

The Timer 1 is an 8 bit up timer. The overflow interval can be easy generated by reading the content value of timer 1 and reset values of Timer 1 to 00h by setting TIM1EN=0. The content value of Timer 1 would be readable only by programmer. The interrupt isn't provided in AD009-041 series, using polling TM1FG is only way to check out the overflow of Timer1



Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
TIM1_L	11H	R	0000	TIM1.3	TIM1.2	TIM1.1	TIM1.0	TIM1.3~TIM1.0: Low nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
TIM1_H	12H	R	0000	TIM1.7	TIM1.6	TIM1.5	TIM1.4	TIM1.7~TIM1.4: High nibble data of TIMER 1, it must be read by following sequence, low nibble first, and then read high nibble later.
SCALER1	0EH	R/W	0000	TM1EN	TM1FG	T1DIV1	T1DIV0	T1DIV1~T1DIV0: The pre-scaler of TIMER1 Timer 1 clock source defined below: F_{MCK} = MCU operating clock T1DIV1 / T1DIV0 / TM1CK 0 / 0 / F_{MCK}/8192 0 / 1 / F_{MCK} /4096 1 / 0 / F_{MCK} /2048 1 / 1 / F_{MCK} /1024 TM1FG: Timer 1 overflow flag 0: no overflow occurred. 1: overflow occurred, it can be cleared by software. TM1EN: Timer 1 enabled/disabled 0:Timer 1 disabled, the content of Timer1 is cleared to all 00h. 1:Timer 1 enabled

The clock source of Timer 1 can come from the frequency divider, there are 4 kinds of clock rate selected by register T1DIV1 and T1DIV0 in this divider, and the divider's clock source is come from MCU operation clock.

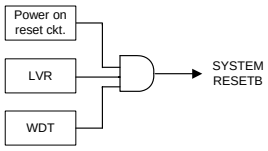
TM1CK= Timer 1 clock source (**F_{MCK}** = MCU operating clock)

T1DIV1	T1DIV0	TM1CK
0	0	F_{MCK} /8192
0	1	F_{MCK} /4096
1	0	F_{MCK} /2048
1	1	F_{MCK} /1024

The 8 bits content of Timer 1 can be reset to 00h by TMI1EN setting to 0, it will be up count while Timer 1 clock source is rising after TIM1EN setting to 1. The read operation sequence of TIM1.7~TIM1.0 must be follow low nibble (TIM1_L) first and high nibble (TIM1_H) later. The Timer 1 will issue an overflow flag (register TM1FG=1) when the content data of Timer 1 from FEh to FFh occurred, and Timer 1 will continue counting from FFh, 00h, 01h… to FFh periodical repeat automatically.

5.6 Reset

The "system resetb" signal is combine with three signals, they are power on reset, low voltage reset (LVR) and WDT overflow reset. The MCU will go back to NORMAL mode when "system resetb" occurred in HALT mode.



5.7 Low Voltage Reset

When VDD power is applied to the chip, the low voltage reset circuit default is enabled initially, it will be disabled when in halt mode. The internal "system resetb" will be generated if VDD power below about V_{LVR}(1.55V).

5.8 System Clock Oscillator

The AD009-041 is provided an internal high speed RC oscillator (HRCOSC), 8MHz ±2%. The operating frequency of AD009-041 is 2 MHz. System clock can be stopped by HALT command. Once stopped, there are three kinds of signal can re-start oscillation, they are wake-up triggering inputs (PA0~PA3, PB0~PB3 or PD0~PD2). Such oscillation will do 'stable check' before release control to software. There are some stable clock delay definition shown on table of page 5, It's arrange after first clock output of HRCOSC and before user's first instruction, it means the user's program will get more stable clock after power on reset or wake up from halt mode.

5.9 I/O Port

This chip provided total 10 I/O ports, they are bi-direction I/O port PA0~PA2, PB0~PB3 and PD0~PD2, the I/O ports provided with input and output direction controlled by IOC_PA, IOC_PB, and IOC_PD, and all I/O also provided wake up and pull up resistor function by control register.

5.9.1 Port A /Port B (input/output)

The Port A, Port B, Port D can be wake up if wake up function are enabled, if I/O port set as output mode, I/O port direction will be force to input mode automatically by hardware while in halt mode, and IOC_PA, IOC_PB, IOC_PD are unchanged.

The Port A, Port B, Port D can be wake up by following step:

(1) I/O port wake up and pull high enabled.
(2) (a) I/O port set as output port, and output data is high. (b) or I/O port set as input port.
(3) Delay more than about 200us for I/O stable.
(4) Execution HALT instruction.
(5) MCU will be wake up by I/O port falling or rising edge

Notice: In step (2)-(a) shown above, if set I/O port output low (not high) will cause auto wakeup occurred from halt mode, it seems never sleep. So it's recommend don't use set output data low for wake up condition.

Common I/O

Symbol	Addr	R/W	RSTB	D3	D2	D1	D0	Description
IOC_PA	02H	R/W	0000	USER0	IOCA2	IOCA1	IOCA0	Port A input/output direction select 1: set port A as output port individual pin 0: set port A as input port individual pin USER0: 1 bit user RAM
DATA_PA	03H	R/W	xxxx	DPA3 (Read only)	DPA2	DPA1	DPA0	Read data from PA0~PA3 PIN and write data to PA0~PA2 PIN (I/O direction is selected by IOC_PA register)
IOC_PB	05H	R/W	0000	IOCB3	IOCB2	IOCB1	IOCB0	Port B input/output direction select 1: set port B as output port individual pin 0: set port B as input port individual pin
DATA_PB	06H	R/W	xxxx	DPB3	DPB2	DPB1	DPB0	Read port B data from PB0~PB3 port and write to PB0~PB3 (I/O direction is defined by IOC_PB register)

Extended I/O

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
PAPU	00H	W	0000	PAPU.3	PAPU.2	PAPU.1	PAPU.0	Port A pull up 150K ohm resistor 0: Port A pull up resistor disabled 1: Port A pull up resistor enabled
PBPU	02H	W	0000	PBPU.3	PBPU.2	PBPU.1	PBPU.0	Port B pull up 150K ohm resistor 0: Port B pull up resistor disabled 1: Port B pull up resistor enabled
PAWK	06H	W	0000	PAWK.3	PAWK.2	PAWK.1	PAWK.0	Port A wake up enable control 0: Port A wake up disabled 1: Port A wake up enabled
PBWK	07H	W	0000	PBWK.3	PBWK.2	PBWK.1	PBWK.0	Port B wake up enable control 0: Port B wake up disabled 1: Port B wake up enabled

The Port A and Port B are 4-bit I/O port except PA3 is an input port. They can be bit programmable setting as input port or output port. In output mode, the data can be written out to external pin by DATA_PA OR DATA_PB register, and reading this output port will get data from DATA_PA or DATA_PB register. Pull-up resistor (150K ohm) will be disabled when output mode is selected.
In input mode, Port A and Port B data can be read from external pin by reading DATA_PA or DATA_PB register, and they are provided pull-up resistor 150K or not by PAPU, PBPU registers.
In addition, each pin of Port A and Port B also can be with wake up function by using register PAWK or PBWK setting to 1. In HALT mode, If Port A or Port B with wake up enabled by these registers, any edge trigger (rising or falling) occurred on Port A or Port B will wake up system and turn on HRCOSC oscillator, and the program counter of MCU will jump to the address 04H, running the wake up sub-routing program.
PA3 is an input pin only, provided with pull up 150K ohm and edge wake up function.

5.9.2 Port C (Output)

REM PIN is an open drain output port with large sink current structure, REM pin is controlled by DPC1 register.

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
IR_DIV	01H	R/W	1000	DPC1 (REM)	X	X	X	DPC1(PC1/REM) is an output port for IR LED driving.

5.9.3 Port D (input/output)

Symbol	Addr	R/W	Reset	D3	D2	D1	D0	Description
IOC_PD	0CH	R/W	0000	X	IOCD2	IOCD1	IOCD0	Port D input/output direction select 1: set port D as output port individual pin 0: set port D as input port individual pin

DATA_PD	0DH	R/W	xxxx	X	DPD2	DPD1	DPD0	Read Port D data from PD0~PD2 port and write to PD0~PD2 (I/O direction is define by IOC_PD register)

Extended I/O

PDPU	04H	W	0000	X	PDPU.2	PDPU.1	PDPU.0	Port D pull up 150K ohm resistor 0: Port D pull up resistor disabled 1: Port D pull up resistor enabled
PDWK	08H	W	0000	X	PDWK.2	PDWK.1	PDWK.0	Port D wake up enable control 0: Port D wake up disabled 1: Port D wake up enabled

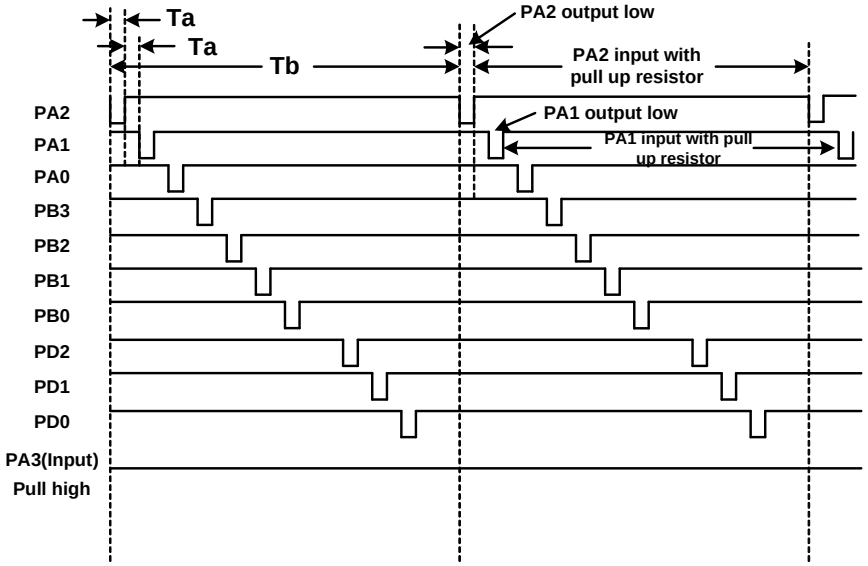
Whether all 3 bits of the Port D is input or output port depends on IOC_PD control register.
Port D also provided edge trigger (rising or falling) wake up and pull up resistor 150K, function just like Port A or Port B.

6. Wake up function for keyboard scan in halt mode

All Port A, Port B, Port D are provided a special wake up function for hardware keyboard scan in halt mode automatically.This function can be enabled by option, and individual PIN can be enabled or disabled by corresponding wake up registers.
It's built-in one low power RC oscillator 13KHz ± 50% for keyboard scan function operation.
The detail sequence of keyboard scan is described below:

1. Keyboard scan function enabled by KBSCEN option.
2. Set all scan key I/O to input mode.
3. Pull up resistor enabled by PAPU, PBPU or PDPU register.
4. Wake up function enabled by PAWK, PBWK or PDWK register. Keyboard scan function can be disabled for individual pin by corresponding wake up control registers set to 0.
5. Execute HALT instruction into power down mode.
6. When in halt mode, at the same time only one I/O port direction switch to output state and others are in input state with pull up resistor. The output port will output one low-pulse from PA2~PA0, PB3~PB0 and PD2~PD0 sequentially if all wake up registers of all I/O port are enabled. The period of keyboard scan time is fixed as shown below:
7. In halt mode, MCU will be waked up by rising or falling edge of I/O ports which key scan function is enabled.

Ta=1.2ms±50%, Tb=28ms±50%



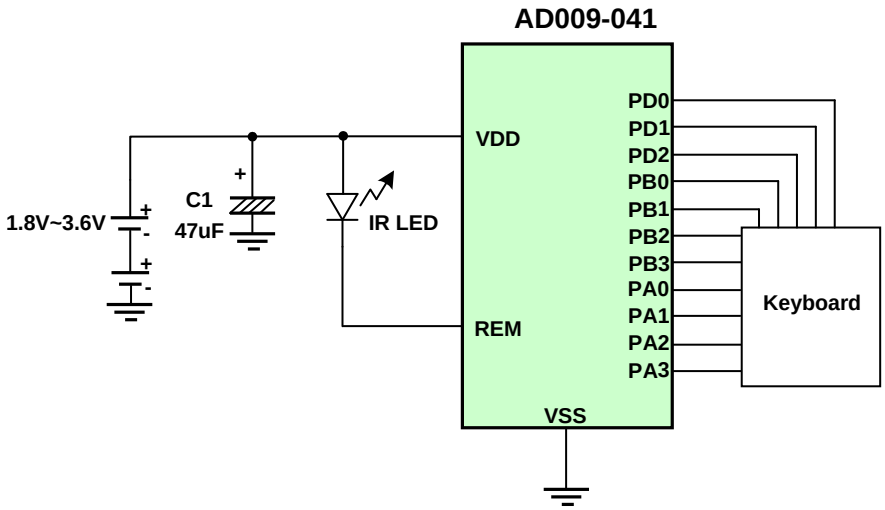
The waveform of keyboard scan function

7. Instruction table

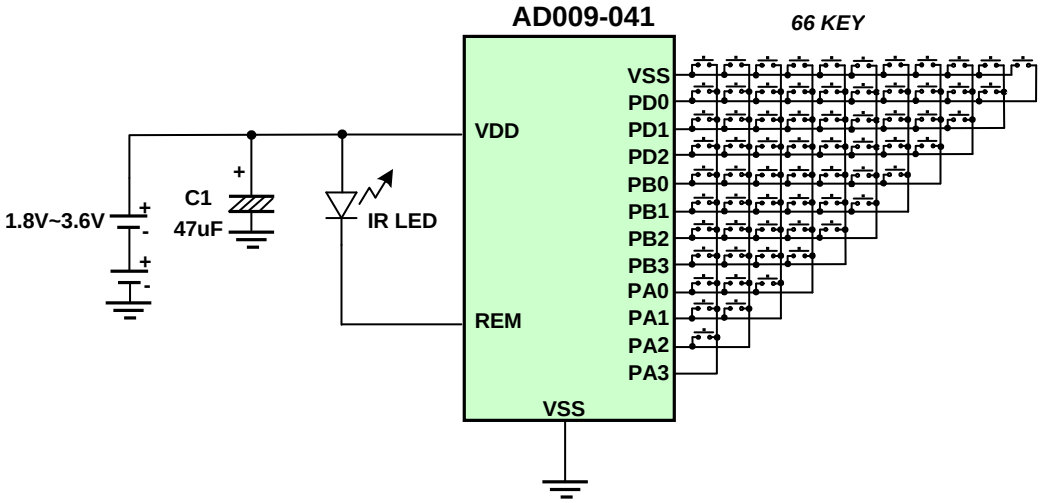
	affect Z	affect C	
JMP Adr	-	-	jump to Adr
JC Adr	-	-	if carry=1 JMP Adr
JNC Adr	-	-	if carry=0 JMP Adr
JZ Adr	-	-	if zero=1 JMP Adr
JNZ Adr	-	-	if zero=0 JMP Adr
CALL Adr	-	-	store return address and JMP Adr
RETS	-	-	return from subroutine
LDPCH Adr	-	-	load PCDH (high address)
LDMAH #D	-	-	load MAH data
LD ExIO(n),A	-	-	Store A to Extend IO
LD A,#D	Y	-	D -> A
LD (n),A	-	-	A -> (n)
LD A,(n)	Y	-	(n) -> A
ADC A,#D	Y	Y	A + D + C -> A
ADC A,(n)	Y	Y	A + (n) + C -> A
SBC A,#D	Y	Y	A - D - C -> A
SBC A,(n)	Y	Y	A - (n) - C -> A
CMP A,#D	Y	Y	A - D
CMP A,(n)	Y	Y	A - (n)
DEC (n)	Y	Y	(n) = (n) - 1
INC (n)	Y	Y	(n) = (n) + 1
ADR (n)	Y	Y	(n) = (n) + C
OR A,#D	Y	-	A = A or D
OR A,(n)	Y	-	A = A or (n)
AND A,#D	Y	-	A = A and D
AND A,(n)	Y	-	A = A and (n)
XOR A,#D	Y	-	A = A xor D
XOR A,(n)	Y	-	A = A xor (n)
RLC (n)	Y	Y	C <- (n) <- C, Z affected by result
RRC (n)	Y	Y	C -> (n) -> C, Z affected by result
SET #B,(m)	Y	-	Set (m)'s #B bit to 1, m= 0 ~ F, B = 0 ~ 3
CLR #B,(m)	Y	-	Clear (m)'s #B bit to 0, m= 0 ~ F, B = 0 ~ 3
NOP	**-**	**-**	**no operation with 1 cycle length instruction**
NOP15	**-**	**-**	**no operation with 1.5 cycle length instruction**
HALT	-	-	stop clock oscillation, reset watch dog timer(if exists)
CLR C	-	0	C = 0
SET C	-	1	C = 1
CLR Z	0	-	Z = 0
SET Z	1	-	Z = 1

Adr = address n = register address, 6 bits --- Notice 2
D = data (4 bit) A = accumulator
Notice 1: Any instruction using "n" isn't provided for register DMDL, DMDM and DMDH, but only LD A,(DMDL) , LD A,(DMDM) and LD A,(DMDH) are valid.

8. Application Circuit



Note : Substrate must be connected to VSS.



Note : Substrate must be connected to VSS.

9. Internal Option Registers

Option	Function Description
WDTEN	WDT enabled/disabled control
KBSCEN	key scan option enabled/disabled control

10. Revision History

Version	Description	Page	Date
1.0	Established		Dec,16 2013