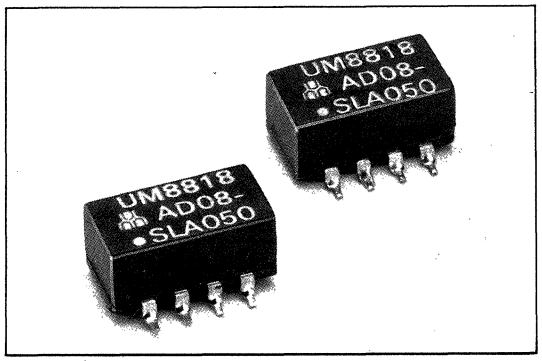
# AD08SLA SERIES: 8-PIN 5-TAP SURFACE MOUNTING, L LEAD



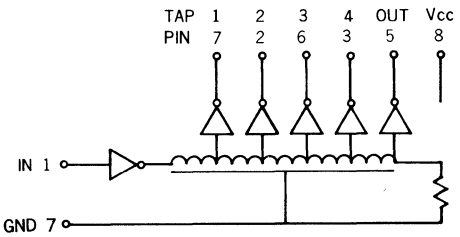

## FEATURES:

- Compatible with TTL Circuits
- 5 Equally-Spaced Delay Taps
- Surface Mount L Lead Package
- Operating Temperature Range: 0℃ to +70℃
- Custom Designs(Delays or Pin Layouts) Available upon Request

## ELECTRICAL CHARACTERISTICS

Supply Voltage Vcc: 5.0±0.25 VDC
Logic 1 Input Voltage: 2.0V min.
Input Current: 50μA max.
Logic 0 Input Voltage: 0.8V max.
Input Current: -2.0mA max.
Logic 1 Output Voltage: 2.4V min.
Logic 0 Output Voltage: 0.5V max.
All measurements made at Vcc=5.0V, 25°C

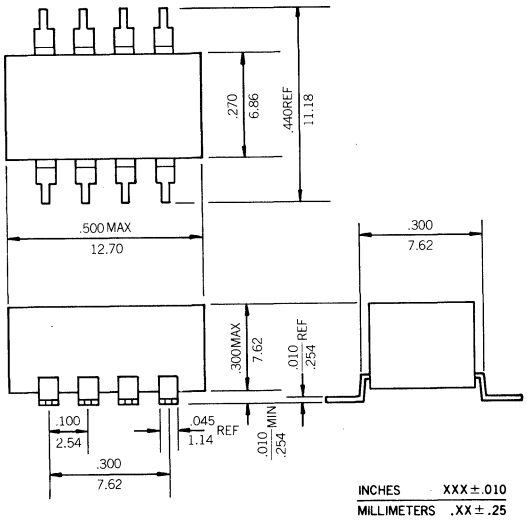
## CIRCUIT AND PIN CONNECTIONS:




## FAN OUT CAPABILITIES

Logic 0 Output: 10 TTL loads/tap max.
: 20 TTL loads/unit max.
Logic 1 Output: 20 TTL loads/unit max.

## PACKAGE DIMENSIONS:




## INPUT TEST CONDITIONS

Pulse Voltage: 3.2 V
Rise Time: 3.0 ns
Supply Current: 60 mA typical
Pulse Width: min. 100% of total delay
Duty Cycle: 33% or less

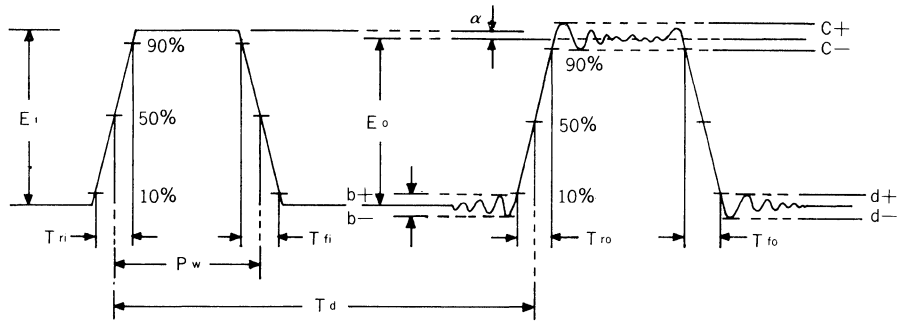
## ELECTRICAL SPECIFICATIONS:

| PART NO. | TOTAL DELAY(1) ns±5% | TAP DELAY(1) ns | RISE TIME(2) ns max. |
|---|---|---|---|
| AD08SLA025 | 25±2 | 5±2 | 4 |
| AD08SLA050 | 50 | 10±2 | 4 |
| AD08SLA075 | 75 | 15±2 | 4 |
| AD08SLA100 | 100 | 20±3 | 4 |
| AD08SLA125 | 125 | 25±3 | 4 |
| AD08SLA150 | 150 | 30±3 | 4 |
| AD08SLA175 | 175 | 35±3 | 4 |
| AD08SLA200 | 200 | 40±3 | 4 |
| AD08SLA250 | 250 | 50±3.5 | 4 |

(1) Delays measured at 1.5V level on leading edge only with no loads on taps.
(2) Rise Time measured from 0.75V to 2.4V with no loads.

# MEASURING TECHNIQUES OF PASSIVE DELAY LINE.

## ● WAVEFORM AND PARAMETER DEFINITIONS



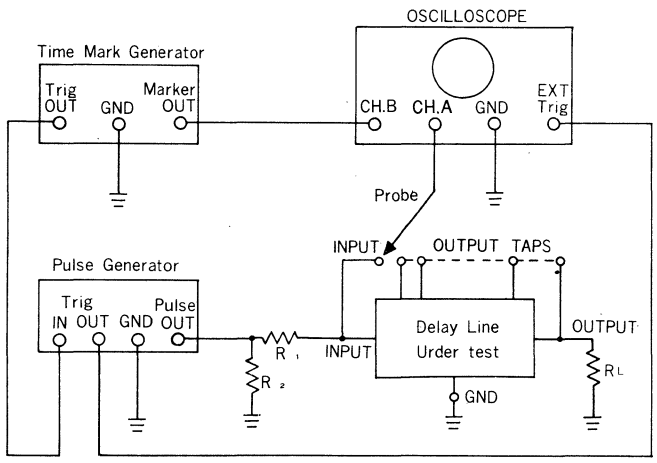

$E_i$ — Input Pulse Voltage
$E_o$ — Output Pulse Voltage
$T_d$ — Delay Time
$T_{ri}$ — Input Rise Time
$T_{ro}$ — Output Rise Time
$T_r$ — Delay Line Rise Time $T_r = \sqrt{T_{ro}^2 - T_{ri}^2}$

$Z_o$ — Characteristic Impedance
$P_w$ — Input Pulse Width
$T_{fi}$ — Input Fall Time
$T_{fo}$ — Output Fall Time
$\alpha$ — % Attenuation $= \frac{E_i - E_o}{E_i} \times 100\%$
S — % Distortion $= \frac{|b| \text{ or } |c| \text{ or } |d|}{E_o} \times 100\%$

## ● MEASUREMENT CONDITION

$E_i = 3.0V$
$P_w = 3 \times T_d$
Period $= 4 \times P_w$

## ● TEST CIRCUIT




Input Matching Resistances

$R_1 = \sqrt{Z_o (Z_o - 50)}$

$R_2 = 50\sqrt{Z_o / (Z_o - 50)}$

Terminating Resistance

$R_L = Z_o$