ANALOG DEVICES

16-Bit, 100 MSPS A/D Converter

Preliminary Technical Data

AD10680

FEATURES

100 MSPS sample rate
SNR of 85 dBFS @10 MHz
SFDR of 85 dBFS @10 MHz
VSWR of 1:1.5
AC-coupled input signal conditioning
Enhanced signal-to-noise ratio
Differential ENCODE signal
LVDS output levels
Twos complement output data

APPLICATIONS

Communications test equipment
Radar and satellite subsystems
Phased array antennas—digital beams
Multichannel, multimode receivers
Secure communications
Wireless and wired communications

GENERAL DESCRIPTION

The AD10680 is a 16-bit analog-to-digital converter (ADC) with a transformer-coupled, analog input and digital postprocessing for enhanced signal-to-noise ratio (SNR). The product operates at a 100 MSPS conversion rate with outstanding dynamic performance. Internal filters can be digitally selected for the appropriate bandwidth or externally programmed.

The AD10680 requires 5.0 V analog, 3.3 V analog, 3.3 V digital, 2.5 V digital, and a 1.2V digital supply, and a differential encode signal. No external reference is required.

Performance is rated over a 0°C to 60°C case temperature range.
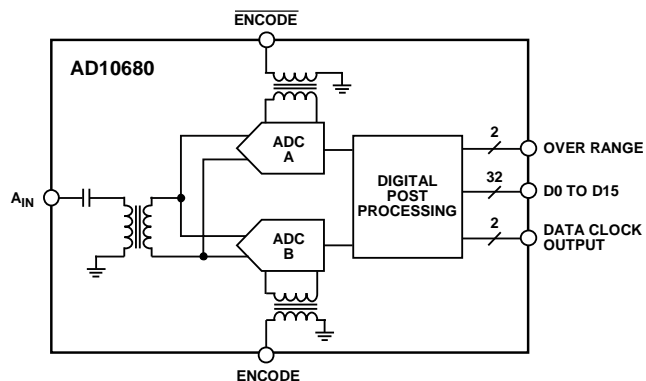
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate up to 100 MSPS.

2. Input signal conditioning with optimized dynamic performance to 40 MHz.

3. Additional performance options are available, such as increased SNR performance with digitally selectable input bandwidths, digitally selectable full-scale input ranges, and digitally selectable Nyquist zones. Contact sales for more information.

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REVISION HISTORY

6/06—Revision PrA: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD1 = 1.2 V, DRVDD2 = 2.5 V, DRVDD3 = 3.3 V, ENCODE = 100 MSPS, unless otherwise noted.

Table 1.

Parameter	Case Temp	Test Level	AD10680KWS			Unit
			Min	Typ	Max	
RESOLUTION				12		Bits
ACCURACY						
No Missing Codes		IV		Guaranteed		
Offset Error	60°C	I		±7		LSB
Gain Error @ 10 MHz	60°C	I		±0.6		%FS
Differential Nonlinearity (DNL)	60°C	V		TBD		LSB
Integral Nonlinearity (INL)	60°C	V		TBD		LSB
TEMPERATURE DRIFT						
Gain Error	60°C	V		TBD		%/°C
ANALOG INPUT (AIN)						
Full-Scale Input Voltage Range	60°C	V		2.2		V p-p
Frequency Range	Full	IV	5		45	MHz
Flatness (5 MHz to 45MHz)	Full	IV		0.5	1.5	dB
Input VSWR (50 Ω) (300 KHz to 50 MHz)	60°C	V		1.5		
Analog Input Bandwidth	60°C	V		100		MHz
POWER SUPPLY						
Supply Voltage						
AVDD1	Full	IV		3.3		V
AVDD2	Full	IV		5.0		V
DRVDD1	Full	IV		1.2		V
DRVDD2	Full	IV		2.5		V
DRVDD3	Full	IV		3.3		V
Supply Current						
I_{AVDD1} (AVDD1 = 3.3 V)	60°C	I		750		mA
I_{AVDD2} (AVDD2 = 5.0 V)	60°C	I		450		mA
I_{DRVDD1} (DRVDD1 = 1.2 V)	60°C	I		600		mA
I_{DRVDD2} (DRVDD2 = 2.5 V)	60°C	I		500		mA
I_{DRVDD3} (DRVDD3 = 3.3 V)	60°C	I		140		mA
Total Power Dissipation	60°C	I		7.15		W
ENCODE INPUTS						
Differential Inputs (ENC, $\overline{ENC}$)						
Input Voltage Range	Full	IV	0.4			V
Input Resistance	60°C	V		100		Ω
Input Capacitance	60°C	V		4		pF
Common-Mode Voltage	60°C	V		±3		V
LOGIC INPUTS ($\overline{RESET}$)						
Logic 1 Voltage	Full	IV	2.0			V
Logic 0 Voltage	Full	IV			0.8	V
Source I_{IH}	60°C	V		10		µA
Source I_{IL}	60°C	V		1		mA
LOGIC OUTPUTS (DRA, Output Bits)						
Differential Output Voltage	Full	IV	247		454	mV
Output Drive Current	Full	IV	−4		+4	mA
Output Common-Mode Voltage	Full	IV	1.125		1.375	V
Start-Up Time	Full	IV		600		ms

AC SPECIFICATIONS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD1 = 1.2 V, DRVDD2 = 2.5 V, DRVDD3 = 3.3 V, ENCODE = 100 MSPS, unless otherwise noted.

Table 2.

Parameter	Conditions	Case Temp	Test Level	AD10680KWS Min	Typ	Max	Unit
DYNAMIC PERFORMANCE							
SNR							
Analog Input	10 MHz	60°C	I	TBD	85		dBFS
@ −1.0 dBFS	30 MHz	60°C	I	TBD	84.5		dBFS
	40 MHz	Full	V		83.5		dBFS
SINAD							
Analog Input	10 MHz	60°C	I	TBD	84		dBFS
@ −1.0 dBFS	30 MHz	60°C	I	TBD	83.5		dBFS
	40 MHz	Full	V		83		dBFS
Spurious-Free Dynamic Range							
Analog Input	10 MHz	60°C	I	TBD	85		dBFS
@ −1.0 dBFS	30 MHz	60°C	I	TBD	83		dBFS
	40 MHz	Full	V		83		dBFS
Two-Tone IMD[1]							
F1, F2 @ −6 dBFS		60°C	V		−75		dBc
SWITCHING SPECIFICATIONS							
Conversion Rate		Full	IV	100			MSPS
ENCODE Pulse Width High (t_{EH})		60°C	V		5		ns
ENCODE Pulse Width Low (t_{EL})		60°C	V		5		ns
DIGITAL OUTPUT PARAMETERS							
Valid Time (t_V)		Full	IV		TBD		ns
Propagation Delay (t_{PD})		60°C	V		TBD		ns
Rise Time (t_R)	(20% to 80%)	60°C	V		TBD		ns
Fall Time (t_F)	(20% to 80%)	60°C	V		TBD		ns
DR PROPAGATION DELAY (t_{EDR})		60°C	V		TBD		ns
Data to DR Skew ($t_{EDR} − t_{PD}$)		60°C	V		TBD		ns
Pipeline Latency[2]		Full	IV		TBD		Cycles
Aperture Delay (t_A)		60°C	V		TBD		ns
Aperture Uncertainty (Jitter, t_J)		60°C	V		TBD		ps rms

[1] F1 = 10 MHz, F2 = 12 MHz.
[2] Pipeline latency is exactly TBD cycles.

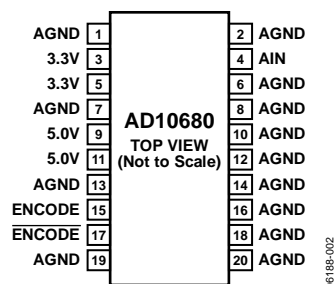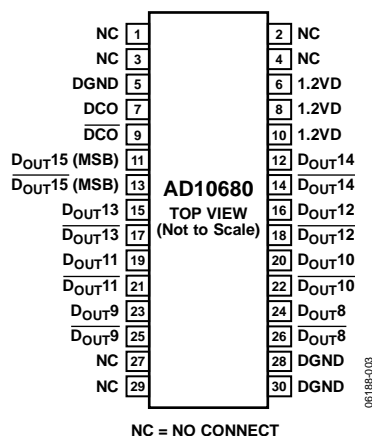# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Figure 2. Pin Configuration P1
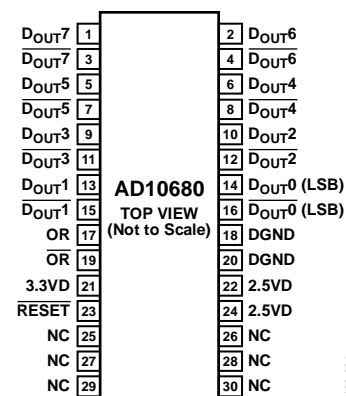

NC = NO CONNECT

Figure 3. Pin Configuration P2

Figure 4. Pin Configuration P3

Table 3. Pin Function Descriptions

P1 Pin No.[1]	P2 Pin No.[2]	P3 Pin No.[3]	Mnemonic	Description
N/A	5, 28, 30	18, 20	$\overline{DGND}$	Digital Ground
N/A	11 to 26	1 to 16	$D_{OUT}x$, $\overline{D_{OUT}x}$	Data Bit Output, Complement
N/A	N/A	17	OR	Overrange
N/A	N/A	19	$\overline{OR}$	Overrange, Complement
N/A	N/A	23	$\overline{RESET}$	Reset
N/A	6, 8, 10	N/A	1.2VD	Digital Voltage
N/A	N/A	22, 24	2.5VD	Digital Voltage
N/A	N/A	21	3.3VD	Digital Voltage (V_{DD})
N/A	1 to 4, 27, 29	25 to 30	NC	No Connection
N/A	7	N/A	DCO	Data Clock Output
N/A	9	N/A	$\overline{DCO}$	Data Clock Output, Complement
3, 5	N/A	N/A	3.3V	Encode Voltage (EV_{CC})
9, 11	N/A	N/A	5.0V	Analog Voltage (AV_{CC})
1, 2, 6, 7, 8, 10, 12, 13, 14, 16, 18, 19, 20	N/A	N/A	AGND	Analog Ground
4	N/A	N/A	AIN	Analog Input
15	N/A	N/A	ENCODE	ENCODE Input
17	N/A	N/A	$\overline{ENCODE}$	ENCODE Input, Complement

[1] Equivalent pin configuration is J1.
[2] Equivalent pin configuration is J2.
[3] Equivalent pin configuration is J3.

THEORY OF OPERATION

The AD10680 uses two, high speed 16 bit ADCs with an interleaved-averaging algorithm to improve the SNR. The AD10680 is optimized for a 40 MHz bandwidth centered in the first Nyquist zone. The AD10680 provides a single-ended, analog input pin with a full-scale input range of 2.2 V p-p. The analog input is designed for 50 Ω input impedance. The AD10680's differential ENCODE inputs are ac-coupled and internally supplied to the two16 bit ADCs. The digital outputs from the two ADCs are applied to the field-programmable gate array (FPGA) for postprocessing. The result is a 16-bit parallel LVDS word coded as twos complement.

INPUT STAGE

The user is provided with a single-to-differential, transformer-coupled input. The input impedance is 50 Ω and requires a 2.2 V p-p input level to achieve full scale.

ENCODING THE AD10680

The AD10680's differential ENCODE signal must be a high quality, low phase noise source to prevent performance degradation. The clock input must be treated as an analog input signal because aperture jitter can affect dynamic performance. For optimum performance, the AD10680 must be clocked differentially.

ANALOG AND DIGITAL POWER SUPPLIES

Care must be taken when selecting a power source. Linear supplies are recommended. Switching supplies tend to have radiated components that can be coupled into the ADCs. The AD10680 features separate analog and digital supply and ground currents, helping to minimize digital corruption of sensitive analog signals.

The 3.3 V digital supply provides power to the digital output section of the ADCs. The 1.2 V and 2.5 V digital supplies provide power for the FPGA. The digital supplies should be decoupled to digital ground (DGND).

The 5.0 V and 3.3 V analog supplies provide power to the analog sections of the ADCs. Decoupling capacitors are strategically placed throughout the circuit to provide low impedance noise shunts to ground. The analog supplies should be decoupled to analog ground (AGND).

ANALOG AND DIGITAL GROUNDING

Although the AD10680 provides separate analog and digital ground pins, the device should be treated as an analog component. Proper grounding is essential in high speed, high resolution systems. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power distribution. The use of power and ground planes provides distinct advantages. Power and ground planes minimize the loop area encompassed by a signal and its return path, minimize the impedance associated with power and ground paths, and provide a distributed capacitor formed by the power plane, printed circuit board material, and ground plane. The AD10680 unit has five metal standoffs used to fasten the AD10680 to the customer's PCB. The AD10680 pin connections mate to a connector (FSI-115-06-L-D-AD-TR for J2 and J3 and FSI-110-06-L-D-AD-TR for J1).

NOTES

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